### Design of a Rapid Prototyping Platform for Applications in Physiological Signal Processing

by

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#### Abstract

The role of technology in helping to unlock the wealth of information in physiological signals has been recognized since the invention of the stethescope in 1816. The last decade has seen tremendous growth in the development of devices designed to interact with these signals, however, the complexity of such devices has grown without sufficient consideration given to their place in real systems. This report details the design of a rapid prototyping platform for the development of low-power real-time applications in processing physiological signals. A case study is given, wherein this work was used to develop an electromyographically controlled hand prosthesis. The results of this case study are used to demonstrate that the system provides superior noise and power performance, while maintaining a high degree of customizability and still meeting the intense processing requirements of even a very sophisticated application. The rich functionality and relatively low cost of the proposed system positions it as an extremely valuable tool in creating the next generation of human interfacing devices.

Keywords: human interface devices, physiological signal processing, EMG controlled prosthesis, real-time processing, low-power processing

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# Contents

A	bstra	nct		ii
$\mathbf{A}$	ckno	wledge	ements	iii
Ta	able	of Con	tents	iv
$\mathbf{Li}$	ist of	<b>Table</b>	s	vii
Li	ist of	Figur	es	viii
N	omer	nclatur	re	ix
1	Inti	oduct	ion	1
	1.1	Purpo	se	1
	1.2	Case S	Study	3
<b>2</b>	Lite	erature	e Review	<b>5</b>
	2.1	Histor	ical Development	5
	2.2	Preser	nt Technology	6
		2.2.1	Off-line Processing	6
		2.2.2	On-board Processing	7
3	Pro	blem a	and Solution Methodology	10
	3.1	Theor	etical Background	10
		3.1.1	Nature of Physiological Signals	10

		3.1.2	Analog Signal Conditioning	12
		3.1.3	Analog to Digital Conversion	13
		3.1.4	Digital Processing	13
	3.2	Soluti	on Methodology	14
		3.2.1	Platform Overview	14
		3.2.2	Analog Acquisition Board	15
		3.2.3	Digital Processing Platform	15
		3.2.4	Environment Feedback	16
<b>4</b>	$\mathbf{Des}$	ign Pr	rocedures	18
	4.1	Acquis	sition Board	18
		4.1.1	Power	18
		4.1.2	Analog Signal Conditioning	18
		4.1.3	Analog to Digital Conversion	20
		4.1.4	Interface and Board Design	20
	4.2	Digita	l Processing Board	22
		4.2.1	Overview	22
		4.2.2	SD Card Interface	23
		4.2.3	SDRAM Interface	24
		4.2.4	VGA Interface	24
		4.2.5	ADC Interface	24
		4.2.6	Digital Potentiometer Controller	25
		4.2.7	User Buttons and Switches	25
		4.2.8	Case Study Implementation	25
	4.3	Motor	Controller Board	26
<b>5</b>	$\operatorname{Res}$	ults ar	nd Discussion	35
6	Cor	nclusio	ns and Recommendations	40
$\mathbf{A}$	Sou	rce Fil	le Tree	42
	A.1	Board	s Folder	42

### CONTENTS

A.2 DigitalOutputA.3 Datasheets FolderImage: Image: Ima	42 43
Bibliography	45
Vita	46

# List of Tables

4.1	Connections for 10-pin Header on Acquisition Board	21
4.2	Connections for 10-pin Header on Motor Controller Board	27

# List of Figures

1.1	Overview of the System	2
1.2	Overview of the Case Study	4
3.1	A Typical Digital Acquisition System	11
3.2	Diagram From [4] Demonstrating the Loss of Meaningful Signal From	
	Application of Notch Filter to Remove Line Noise	12
3.3	Block Diagram of Complete Prototyping Platform	17
4.1	Schematic for Acquisition Board	28
4.2	Routing for Top Layer of Acquisition Board	29
4.3	Routing for Bottom Layer of Acquisition Board	30
4.4	Digital System	31
4.5	EMG Controlled Prosthetic System	32
4.6	Schematic for Motor Controller Board	33
4.7	Board Layout for Motor Controller	34
5.1	Resting EMG	37
5.2	Active EMG	38
5.3	Active EMG Spectrum	39

# Nomenclature

DC	Direct Current
AC	Alternating Current
ADC	Analog to Digital Converter
ASIC	Application-Specific Integrated Circuit
FPGA	Field-Programmable Gate Array
IO	Input/Output
ESI	Electrode-Skin Interface
LPF	Low-Pass Filter
SPI	Serial Peripheral Interface
MOSI	Master Output Slave Input
MISO	Master Input Slave Output
SD	Secure Digital
FAT	File Allocation Table

## Chapter 1

### Introduction

### 1.1 Purpose

A physiological signal is defined as any measurable quantity which represents or contains information about a process occurring in a living organism [9]. Specifically, for the purpose of this project, the scope will be narrowed to considering electrical signals measured from humans with the purpose of understanding or analyzing some physiological process. The primary applications of the study of these signals are: electromyography, electrocardiography, electroencephalography, electrogastrography, electrohystography, and electrooculography. The study of these signals holds potential for tremendous advancement in medicine in applications from wear-at-home health monitoring technology to the development of prosthetics which respond to a user's intentions and provide meaningful feedback to the user in response from the environment. It is clear even from these two examples of applications, and many more such examples exist, that these technologies are primarily embedded, that is, they must function for long periods of time in a stand-alone, form-factor constrained environment. This presents a particularly interesting design challenge. To further complicate the matter, often the compute requirements from these applications is quite intense.

The purpose of this project is to address the need for a design platform which

abstracts the designer from these complications. The platform should include a means of acquiring data from the environment, processing the data, and returning the results of the processing to the environment, as per Figure 1.1. Exactly such a system has been designed. A complete low-power acquisition system was developed and a processing platform has been proposed. Furthermore, two means of providing a response to the environment from the results of the calculations have been created: a multi-channel motor controller system and a logging system which allows storage of huge amounts of data.



Figure 1.1: Overview of the System

Due to the tightly constrained nature of this project, it was necessary to establish some design requirements as well as some optimization criteria. The design requirements were the non-negotiable components of the design, while the optimization criteria were the parameters within the design requirements, which were always pushed as close to their optimal boundary as possible. Following are the requirements which were established:

- easy scalability to multiple channels
- ability to process any possible physiological signal

- sufficient compute power to permit real-time performance on even very sophisticated algorithms
- stand-alone (i.e. anything necessary for the system to function should be carriable)

while the following were taken as the optimization criteria for everything which was designed:

- low power consumption (i.e. the device should run for an extended period from batteries)
- low cost
- ease of development for the platform
- large amount of designer feedback (i.e. transparent operation)

### 1.2 Case Study

In order to demonstrate the functioning of the system, a case study was undertaken with Shameem Bhatti and Philip Chrapka. The nature of the case study is an electromyographically controlled prosthetic hand. Figure 1.2 shows how this maps into the system overview established in Figure 1.1.

Phil Chrapka was responsible for implementing the algorithm for classifying the signals, while Shameem designed the robotic hand. This case study is very appropriate for a number of reasons:

- requires long wearability
- heavy computing requirements
- natural scalability to multiple channel processing
- practical applicability



Figure 1.2: Overview of the Case Study

. Furthermore, this is a field in which a significant amount of prior knowledge exists but in which the vast majority of work is done without consideration given to the highly form-factor constrained nature of the application (this is discussed further in Chapter 2).

Over the course of this case study, many things were learned about the requirements of such a rapid prototyping platform and an excellent demonstration of the quality of the developed system was attained.

## Chapter 2

# Literature Review

The analysis of electrophysical signals can be divided into two main stages: acquisition and processing. Ideally, these two functions would be implemented in a single generic framework that could be used for experimentation with any biological signal. However, due to the diverse nature of electrophysical signals and the different processing requirements of each application, actually realizing this framework is a significant challenge. This chapter outlines the sum of the present work in this area and motivates the need for this project.

### 2.1 Historical Development

The idea of a generic platform for biomedical instrumentation is far from new. More than 30 years ago, Arnett published a laboratory setup for rapid implementation of various signal conditioning and processing designs [1]. The work consisted of 20 instrument modules including amplifiers, filters, comparators, multipliers, etc. which could be connected in various configurations on a breadboard to measure a certain feature of a signal. Although the work done by Arnett represents an impressive achievement, it was done during a significant migration - especially in experimental and pedagogical environments - to performing such signal manipulation digitally [5]. Digital signal processing offers noise immunity with the added benefit of rapid and inexpensive prototyping and so it became desirable to do as much of the processing as possible in the digital domain.

In order for digital signal processing to have a significant impact in biomedical instrumentation, a certain compute threshold needed to be crossed. As early as 1962, computers began to be used in interpretation of electrocardiograms [10]. However, this processing was performed on remote mainframes and was therefore exceptionally costly and inconvenient. As the cost of microprocessors decreased and their compute power increased, such processing was migrated to microcomputers within the hospitals themselves and was finally integrated into bedside carts [5].

In the last two decades, the rapid scaling and ubiquitous availability of compute power has enabled the development of more sophisticated processing techniques for electrophysical signals. This has opened interest in expanding the application domain of such processing from the hospital to end-user applications. Section 2.2 describes the present state of the technology in this field and discusses some of its limitations.

### 2.2 Present Technology

The technology which is presently applied to analysis of physiological signals can be divided into two main categories: on-board and off-line. For the purposes of this report, on-board processing will be considered to be processing which occurs within a given system, while off-line processing is defined as processing which is delegated to a computer, processing grid, or other external entity.

#### 2.2.1 Off-line Processing

This section will detail the present technologies which use off-line processing to analyze electrophysical systems. Essentially, signals are acquired and imported to a computer where some kind of user-friendly software development kit is used to perform processing. Possibly two of the most widely available examples of these systems are National Instrument's LabView and CleveMed's CleveLab system. LabView is a graphical programming environment where developers can drag-and-drop math processing functions as well as control functions to create a virtual instrumentation sys-

tem [8]. It is typically used in conjunction with one of NI's acquisition boards. This is in contrast to CleveLab, where the acquisition and processing are much more tightly integrated. In CleveLab, the development environment is similar, where a graphical user interface is used to create processing functionality, however, the development environment is less open in the sense that it is specifically created to interface the CleveMed BioRadio - an 8 channel programmable gain wireless acquisition system [3]. These two systems represent the standard approaches to off-line processing platforms but it is worth noting that other systems do exist, such as BioMOBIUS and Flow-Stone DSP. These systems provide an effective means of rapidly prototyping a desired behaviour, however, they suffer some limitations as well. The biggest limitation with off-line processing is form-factor. Many end applications which would be developed in these systems are only practical if they can be completely self-contained and embedded and often the effort required to migrate a design from a computer to an embedded system can be of the same scale as the effort of simply redesigning the system. Furthermore, even the compute power offered by a workstation may be insufficient to prototype applications where very strict real-time constraints are in place. Because of their tremendous ease of use, these off-line systems can often provide good insight into algorithms during initial development stages but are severely limited in their ability to design most real systems.

#### 2.2.2 On-board Processing

This section forms the focal point of the literature survey because it is directly in the application domain of this project. The first platform that will be discussed in this section is a fetal heart-rate recorder [7]. This platform has integrated a programmable signal conditioning block with an analog digital converter (ADC) on a single application specific integrated circuit (ASIC). This level of integration gives good noise performance with very low power consumption. This ASIC interfaces directly with a Toshiba TMS320C50 digital signal processor (DSP) and 4 Megabytes of Static Random Access Memory (SRAM). This provides the capability for collection of data alongside reconfigurable computing. The C50 line of DSPs has 64Kbytes of program memory and has an instruction time of only 50ns so it provides significant compute performance at a modest 2.4mA per mega-instruction per second (MIPS). The ADC is programmable in the sense that it can trade sampling rate against sampling precision, scaling from 75Hz at 16-bits to 9600Hz at 9-bits. This platform is impressive considering it was published more than a decade ago. Obvious deficiencies (such as the relatively slow sampling rate of the ADC at 16-bits) could easily be improved solely with the improved knowledge in these fields. However, the platform lacks some things which are extremely valuable in such an application. For example, there is no non-volatile storage, which is highly valuable if large amounts of data are to be collected, especially remotely. Furthermore, the power consumption scales quite quickly with the amount of computation to be performed. Also, the system does not provide a way to integrate multiple channels of data.

The second platform that will be discussed is FPGA based reconfigurable platform [2]. This platform has two acquisition boards connected to an FPGA which is integrated with a bank of SDRAM as well as a number of debug interfaces (LCD, LEDs, Pushbuttons, switches). This FPGA also provides an interface to a personal computer. This platform has many strengths. The computer interface opens a huge number of possibilities for rapidly testing new algorithms, as well as long term data collection. The acquisition boards provide for triggered inputs, which gives the possibility for more complex data acquisition patterns. However, the acquisition boards are also fixed-range, that is, they provide static signal conditioning blocks which are appropriate for most applications. Because of this, though, the acquisition chain is highly over-designed for physiological applications (the ADCs provide 20-125 megasamples per second (MSPS)). Also, there is no scalability in terms of number of channels. Probably the biggest problem with this platform, though, is its form-factor. It would be very difficult to do, for example, a collection over an entire day with this system because it is not battery-operable and the system was not built with "wearability" in mind.

Finally, a reconfigurable platform developed by Grana and Perez [6] will be discussed. This platform has a programmable analog front end connected to a Cyclone II FPGA which implements a high-speed USB interface to a PC. It benefits greatly from the PC interface in terms of speed of development and does provide reconfigurable digital logic for very intense compute application but again, the platform lacks non-volatile storage, necessary for long-term collection applications, and the analog signal condition was not build with electrophysiological signals in mind. The system is limited to two input channels and there is only very modest reconfigurability on the input gain. The ADC runs at 200MSPS, which is much more than is necessary for physiological applications. Finally, the computer interface is integral to the operation of this system, so it is virtually impossible to operate this system in a portable way, which severely limits its functionality in many physiological applications.

## Chapter 3

# Problem and Solution Methodology

### 3.1 Theoretical Background

This section will attempt to give an understanding of the nature of the signals dealt with in this project. Furthermore, it will outline some of the standard approaches taken to addressing each of the key stages in the project.

#### 3.1.1 Nature of Physiological Signals

Electrophysical signals typically have bandwidths from the high tens to low hundreds of Hertz and skin-surface amplitudes of high hundreds of microVolts [9]. This makes their measurement a significant challenge. Futhermore, there is tremendous variation in the spectrum of useful information from different signals. For example, we can aquire useful monitoring information in the 1Hz-40Hz band for ECG, whereas a research application, such as EMG controlled prosthetics, should require acquisition from 0Hz-500Hz. This presents a few very unique challenges discussed in this section.

A typical acquisition system is depicted in Figure 3.1. The purpose of the measurement block is to bring the electrophysical signals from the point of measurement (eg, skin surface) into a wire and the purpose of the signal conditioning block is to amplify and filter this signal so that it can be converted into a digital signal by the analog to digital converter (ADC). When dealing with electrophysical signals, there



Figure 3.1: A Typical Digital Acquisition System

are a few unique challenges. Firstly, although some valuable information can be carried in the 0-1Hz band, this band also contains a number of artifacts which can cause problems for acquisition. For example, this is the band in which motion artifacts occur and it is also common to observe DC drift in an electrophysical signal. This can cause saturation problems of all later conditioning stages. Furthermore, there are many inherent sources of noise for physiological signals:

- instrumentation noise
- line noise (60Hz hum)
- motion artefacts
- fluctuation in electrode-skin interface
- etc

A decision needs to be made about where these sources of noise will be compensated. Naturally the best way to avoid noise is by preventing its causes but this cannot always completely remove the noise. A traditional approach is to filter out the noise, for example, by placing a sharp notch filter at 60Hz to remove the line noise. Unfortunately, however, this noise occurs directly inside the meaningful portion of the power spectrum [4] as per Figure 3.2. The tradeoff, though, is that if that noise is not filtered in the analog domain, one risks it overpowering the meaningful signal and even saturating the amplifier stages. A comprehensive approach that addresses all of these issues is discussed in chapter 4.



Figure 3.2: Diagram From [4] Demonstrating the Loss of Meaningful Signal From Application of Notch Filter to Remove Line Noise

### 3.1.2 Analog Signal Conditioning

The first step of the conditioning block is typically a differential instrumentation amplifier. This takes positive and negative signals from the two bars of the electrodes and amplifies them and converts them to a single signal relative to ground. Important characteristics for the instrumentation amplifier are that it have a very high commonmode rejection ratio, that is, a very small representation of the common components of the +/- signals is present in the output, a very wide gain range, and very small input voltage and current offsets.

After the instrumentation amplifier, typically some filtering is performed with the objective of further amplifying and band-limiting the signal. The importance of this is discussed in Section 3.1.3.

#### 3.1.3 Analog to Digital Conversion

One of the greatest challenges in acquiring an analog signal for digital processing is in the analog to digital conversion. There are many texts addressing how this can be performed but the major design decisions are resolution and rate. Obviously a higher resolution and sampling rate will lead to a greater power consumption which is undesirable, however, especially when dealing with very small signals which may have a significant noise component, high resolution is important. Furthermore, it is necessary to sample at a sufficient rate that no aliassing occurs (i.e. at least twice the rate of the maximum frequency component in the signal) and also at a rate sufficiently high that the entire bandwidth of the signal is captured (however, this should be guaranteed by the former condition). Another complication that arises out of analog to digital conversion is the range problem. Most analog to digital converters convert signals from 0 to the DC-level of the digital circuitry (i.e. 3 or 5V). The obvious advantage to this is that only one set of supplies need be provided to the chip but that means that an offset must be provided to the input signal, since the output of the previous stages is symmetric about 0V.

#### 3.1.4 Digital Processing

There are many different techniques for digital processing. These range from microprocessor solutions to application-specific integrated circuits (ASICs). The primary advantages of using microprocessors are ease and speed of development and low cost. However, they have a significant drawback in that they are very limited in the processing they can perform. Even very powerful microprocessors can have only a couple hundred kilobytes of storage and operate in the low hundreds of Megahertz. When applications demand significant compute power, their needs often can't be met by microprocessors. Furthermore, microprocessors tend to have no more than low tens of General Purpose IOs which would limit the number of acquisition channels which could be connected to the device. On the other end of the scale are ASICs. These are custom-fabricated microchips that have the obvious advantage of incredible performance at much lower power than a microprocessor solution but each design iteration represents a huge fabrication cost and the design effort is tremendous. In the middle of microprocessors and ASICs are field-programmable gate arrays (FPGAs). These are devices with a tremendous amount of reconfigurable logic. That is, one can program the device to have virtually any configuration of registers, memories, signalprocessing blocks, and combination circuits imaginable. This gives the flexibility to have many design iterations with no fabrication costs, while offering performance which approaches that of ASICs.

### 3.2 Solution Methodology

This section will address the methodology for solving the problems outlined in the previous section. It will give a block diagram of the final solution, with the specific design details being deferred to Chapter 4.

#### 3.2.1 Platform Overview

A block diagram of the complete platform with all relevant parts labelled is in Figure 3.3. In order to have a successful system for processing physiological signals, there are number of necessary components. Firstly, there must be a reconfigurable analog acquisition board that can acquire signals of various amplitudes and at various offsets to accomodate the wide variety of characteristics in physiological signals. The number of channels must be scalable, since, for example, an ECG application would need many fewer channels than an EEG application. The platform must provide a large amount of non-volatile memory since in many cases it is desirable to collect large amounts of data over extended periods of regular use. This necessity for extended use also means that it is very desirable for the platform to have very low power consumption and to be completely "wearable". Also, it must provide a substantial amount of processing power, since, as applications become more complex there is an ever increasing demand for compute power. Along with this increased compute power, it is very desirable for the platform to have a large bank of high-speed memory since some compute applications require substantial memory bandwidth. Furthermore, it should provide some means of bidirection developer interaction (i.e. screens, buttons, switches, etc). Finally, it is desirable that the various interfaces in the system be handled in a developer-friendly way to allow as much time as possible to be focussed on algorithm development. The way in which all these requirements were achieved by this platform is detailed in the following sections.

#### 3.2.2 Analog Acquisition Board

In order to provide for very easy multi-channel acquisition, a board was designed which incorporates all of the necessary circuitry for acquiring an analog signal, conditioning it, and converting it to digital. This board was designed to be very small and of reasonable cost so that it could be replicated very easily for as many channels as necessary. Its extremely small footprint allows it to be worn directly on top of (and clipped directly to) the electrode. This helps to dramatically reduce line noise, since the only signals leaving the point of measurement are digital signals. The interface to the boards is serial and they provide adjustable gain and offset to combat the problems discussed in section 3.1.1.

#### 3.2.3 Digital Processing Platform

An Altera FPGA is used to do all the digital processing. Because of the timelimitations of the project and the huge complexity of building a board capable of housing an FPGA, the Terasic DE2-70 was chosen as a processing platform. It has a number of unnecessary peripherals and slightly violates the power and form-factor criteria outlined for the project but it provides very good proof-of-concept. A small board was built to interface this board to the acquisition boards. In order to enhance the functionality of the digital processing platform, an interface was built to the 64MBytes of SDRAM available on the DE2-70. This provides a huge memory-space for a digital designer to use in prototyping a system for processing electrophysical signals. Also, the 18 switches on the board were connected to the design for use in configuring the oscilloscope as well as for providing some general inputs to aid in system development.

### 3.2.4 Environment Feedback

An interface between the FPGA and an SD Card was built for storage of design data or for logging of, for example, long-term at-home health monitoring data. Also, oscilloscope-like functionality was added through the VGA interface present on the DE2-70 board. This allows immediate display for a designer of the data acquired from the analog boards. Furthermore, a motor controller board was designed which allows for immediate integration of a robotic application to the processing platform.



Figure 3.3: Block Diagram of Complete Prototyping Platform

## Chapter 4

# **Design Procedures**

This chapter details the specific design decisions that were made throughout the course of the project and provides plans for constructing each of the components of the project.

### 4.1 Acquisition Board

#### 4.1.1 Power

The analog signal conditioning board operates on two separate power supplies: the analog supply from -4.5V to +4.5V and the digital supply from 0V to 3V. Tremendous care was taken to ensure clean delivery of the source to each device. Every chip is bypassed to ground as close as possible to the package with tanalum capacitors. The digital potentiometer (particularly susceptible to noisy operation) was bypassed with a parallel tantalum ceramic pair. Care was taken at the design of each stage to use low-power devices and ensure power-efficiency (examples given later).

### 4.1.2 Analog Signal Conditioning

The signal conditioning occurs in two stages: headstage amplification and low-pass filtering. The headstage amplification is performed by the AD620 instrumentation

amplifier. This amplifier provides a number of features which make it an ideal choice for this application. It has very high input impedance with low input offset voltage and current and superior noise characteristics at a very low cost. In this case, a slight compromise was made with respect to power. There are certainly instrumentation amplifiers which operate at lower power than the AD620, however, because of the sensitivity of the headstage signal to noise, it was better to opt for better signal quality than lower power in this case. The headstage is the where the true flexibility of this system becomes apparent. The AD620 provides single-resistor gain setting and an input offset pin. Therefore, a two-channel digitally controllable potentiometer (Analog Devices AD5262) was placed on board with one channel acting in the feedback path to set the gain of the instrumentation amp and the other acting as a voltage divider to provide a reference voltage for the input offset of the instrumentation amplifier. This provides dynamic adjustment of the gain and offset of the signal allowing run-time compensation for any number of environmental factors that can compromise signal integrity on long-term acquisition, such as:

- signal degredation over time of electrode-skin interface
- signal drift due to extreme movement or degredation of ESI
- range saturation/underutilization due to changing environmental noise parameters
- etc.

Overall through feedback from the digital controller, this configuration ensures that the signal passed from the headstage to the LPF is centered in and fills the range from 0V to 1.3V.

In the following stage, an eigh-order Butterworth low-pass filter with  $f_c = 10kHz$ in Sallen-Key topology is implemented with an additional gain of 2.2 (note that this brings the range up to 0V-3V, the full range of the ADC). An eigh-order filter was used to provide very sharp cutoff characteristics. This helps prevent aliassing even when very little head-room is given above the Nyquist criterium by the ADC. This is a good design decision because the ADC's power consumption scales with the sampling rate, so it is desirable to be able to sample as close to 20kHz as possible.

#### 4.1.3 Analog to Digital Conversion

The board is fitted with a 250ksps 16-bit Linear Technologies LTC1864 ADC. It may be observed by the keen reader that there seems to be a wasteful amount of headroom in the frequency-space considering most of the meaningful information is in the 0-1kHz band so it seems ridiculous to have a 250ksps sampling rate. The main tradeoff here is that a higher sampling rate results in higher power consumption. However the ADCs have an adjustable sampling rate with an automatic shutdown feature which means that they consume virtually no power outside of a conversion cycle, therefore the headroom in the ADC doesn't really waste any power. Naturally, the 10kHz analog cutoff frequency means that the sampling rate must be at least 20kHz but the device has superior power performance even up to 20kHz and this leaves some room for future applications that would like to study more of the spectrum. Another brilliant feature of these ADCs is that the digital interface provides one bit per clock cycle from MSB to LSB. This means that the designer can exploit the power vs. precision tradeoff. For example, if an application requires very low power but only requires quantization into 16 bins, each conversion cycle can be aborted after the first four bits are clocked out of the ADC, saving the power of the rest of the cycle.

#### 4.1.4 Interface and Board Design

A 10-pin header is provided on the board for connecting it through ribbon cable to the interface board (refer to Figure 3.3). In retrospect, it may have been better to implement a lower-profile connector but in general this setup ensures signal integrity from the acquisition board all the way to the FPGA and gives a very tidy connection scheme. The pin connections for the 10-pin header on the acquisition board are given in Table 4.1. Note that in order to reduce the number of pins required, the Serial Peripheral Interface (SPI) bus is shared between the ADC and the digital potentiometer - i.e. it is not possible to adjust gain or offset during a conversion. However, this does not typically present a problem since there is a relatively large amount of dead-time on the SPI bus due to the pauses between conversions.

Header Pin	Function
1	Digital V+
2	Analog Ground
3	Analog V- (-4.5V -5.5V)
4	Digital Ground
5	Potentiometer Chipselect#
6	MOSI Line (SPI Shared)
7	SCLK Line (SPI Shared)
8	MISO Line (SPI Shared)
9	ADC Convert Signal
10	Analog V+ $(4.5V 5.5V)$

Table 4.1: Connections for 10-pin Header on Acquisition Board

The board was designed with small foot-print in mind (final layout was 2.4 square inches). Nearly all of the components are surface-mount. This provides a two-fold benefit: firstly, it permits the inexpensive use of higher-tolerance components and secondly it ensures that the board has the lowest possible inertial mass. This has huge implications because the board is designed to sit directly on top of the electrode (so that only digital signals leave the site of measurement providing excellent noise immunity) but that immediately introduces risk for damaging the signal with motion artefacts. Therefore, the lightweight design carries major benefits for signal integrity. The digital and analog components were isolated: the entire analog chain resides on the bottom of the board, while the digital components are on the top of the board. The boards were milled using the equipment in the IEEE laboratory. The schematic and actual board layouts are shown in Figures 4.1, 4.2, and 4.3, and Eagle CAD files for the design are provided in the source package (see Appendix A).

In Figure 4.3 we can see the two large pads at either end of the board. These

are the inputs to the instrumentation amplifier. The idea is that the two poles of the electrode should be clipped directly to these pads. Because of time constraints, we used standard wet electrodes with little tabs that we were able to alligator-clip to these pads but ideally dry electrodes would be used because they have better long-term performance. in any event, the electrode mounting system provides a very modular way to connect electrodes to the acquisition board giving it flexibility for a wide range of applications.

### 4.2 Digital Processing Board

The elegance of the digital component of this system is its reconfigurability. Hence, a number of stock cores were provided that create a shell in which a designer can work completely abstracted from the low-level details of all the available interfaces. A block diagram of the entire digital system is given in Figure 4.4 and explained in subsequent subsections.

#### 4.2.1 Overview

At the top level, the digital system is split into two components: hardware and software. The hardware component represents most of the FPGA and is a group of peripheral interface cores attached to a large area of reconfigurable "user hardware". It is inside this user hardware space that the designer can create a large digital system for processing electrophysical signals. The ability to run custom software is provided by the NIOS Microprocessor core. This is a microprocessor built from reconfigurable logic units and includes a library for interpreting the data on the SD Card as a FAT filesystem as well as a large space where a designer can implement their own program. There is another major benefit to architecting the system in this mixed hardware/software way. For applications where relatively few compute resources are required, the rapid prototyping offered by microcontroller solutions is still offered by this system with the added benefit that no microcontroller cycles are wasted with system functions such as acquiring data. Note that there are some parts of the system not shown here (i.e. the Flash chip interface and software boot-loader used for auto-booting a program on board power-up).

#### 4.2.2 SD Card Interface

This is a custom hardware core developed from scratch by me that boots an SD high-capacity card and has the ability to read and write blocks. Keeping in mind the target for very low power consumption, the interface block utilizes less than 250 logic elements and only one on-chip memory. It consists of a command controller that has built-in CRC error checking and a data buffer that is one block large. Notice that this makes the interface to the SD card somewhat slow (especially when file-system intensive operations are being performed because these often require almost randomaccess to the card and cause many cache refreshes), however, this is not a serious problem because all the data from the SD card comes through NIOS anyways, so it is not possible to achieve very high data rates. As Section 4.2.3 shows, this is really not a big issue because any data that needs to be accessed with very high bandwidth can be pre-cached to the SDRAM. The source distribution also contains a more sophisticated controller that can be substituted for this one that has multiple data buffers to cache FAT information and to perform separate read/write caching but (at least for the case study) the performance gains are negligible since the card is rarely pushed to its maximum speed. The interface to the SD card operates at roughly 2MBytes/second in raw streaming mode. Depending on the file system fragmentation, the controller can write a file while allocating on-the-fly at a little over 1MByte/second. Notice that this is still well over the maximum data rate that can be acquired from the ADC so it is possible to stream data directly from the ADC to the SD card without getting buffer overflows. This is very useful if a designer wants to capture very long sequences of data for post-analysis on a computer and the fact that FAT32 is implemented in the system makes this transition so much easier.

#### 4.2.3 SDRAM Interface

This hardware interface was adapted from a random-access controller provided by Altera for the DE2. It was modified to act in streaming mode (i.e. a start point is set and the controller will read or write from that point in preset burst-lengths). This makes sense because this memory is primarily used for two things: capturing large datasets for processing or precaching information that must be used at highbandwidth on chip. In the former case, the data naturally comes in "streaming" mode and in the second case you have the option of what order to precache in. Having established, then, that this makes sense for this application, it was implemented in that way to allow huge data rates across the interface. The physical layer of the interface operates at 133MHz with a 16-bit data bus to each of two physical memory chips, each with a 24-bit address space. The controller virtualizes this for the user hardware space as a 64-bit data bus operating at 50MHz (i.e. 8 bytes \* 50MHz = 380MBytes/second!). A practical example of the need for this kind of bandwidth appears in Section 4.2.8. Notice that the user software space has direct access to the SDRAM controller as well to allow caching into this memory from the SD card, or storing this memory's contents into the SD Card.

#### 4.2.4 VGA Interface

This is a standard 800x600 VGA controller that was used almost without modification from the COE3DQ4 laboratory material. It is used to display, for example, an oscilliscope view of the acquired data. A multiplexer is in place for the inputs so the developer can switch between seeing scope data and seeing some data generated within their design.

#### 4.2.5 ADC Interface

This module manages the serial interface to the ADC on the acquisition board. This module can be replicated as many times as necessary (i.e. once per acquisition board). It performs all the clock division in module and drives the ADC with a 3.125MHz

clock (note this clock signal is shared with the digital potentiometer). It takes as an input the number of clock cycles to wait between conversions and returns as an output a 16-bit data bus representing the data in from the ADC and a one bit data\_valid signal that is asserted for one clock cycle when a new sample is captured. It is at this point why it becomes clear that it was necessary to fabricate a well-planned out acquisition board and to run all the lines with ribbon cable because at 3MHz signal integrity becomes a huge concern. The ADC input data is fanned out to the scope module and as well to the user hardware space.

#### 4.2.6 Digital Potentiometer Controller

This is the controller for the digital potentiometer. Both channels (for gain and offset) are controlled out of this one module. It takes as inputs the desired values of the wiper positions for each of these potentiometers and keeps track of current position and when it doesn't match desired position it reprograms the potentiometer chip. Typically, this would be part of a feedback loop created in the user hardware area from the ADC.

#### 4.2.7 User Buttons and Switches

Nine of the switches are connected to the scope to control the trigger point and mode, while the other 8 and the four pushbuttons are connected to the user hardware space.

#### 4.2.8 Case Study Implementation

This section describes how the system was created for the EMG controlled prosthetic device. The block diagram of the system is given in Figure 4.5.

In this system, the SVM training occurs offline, i.e. feature vectors are captured onto the SD card and the training is performed on a computer. This was a good design decision because the training need only occur once and the extra resources that it would have required to port it to the embedded processing platform would have simply consumed unnecessary power during regular operation. After the training occurs, the model files are placed back on the SD Card and loaded into the design. They are buffered into the SDRAM and then the system can begin running. The system performs ten classifications per second. The digital filtering block was implemented by me and is simply a FIR filter with a notch at 60Hz. The feature extraction and SVM classification were implemented by Phil Chrapka. The motor control was implemented by me. Everything in the main path is implemented in the user hardware block. This was necessary because it was nearly impossible to do within the real-time constraint in software. The SVM requires access to the entire model file on each classification. This presented a difficult design challenge because the model file was in excess of 100kB. It would have consumed a huge amount of resources to store the entire file on-chip so the model was stored on the SDRAM and streamed on chip for each classification. This represents about 1MB per second data transfer, which, although possible from the SD card for one SVM classifier, does not scale to the multiple classifiers which would be necessary to adapt the design to multiple gestures.

### 4.3 Motor Controller Board

The motor controller board is not particularly complex. Its schematic is shown in Figure 4.6 and the board layout is shown in Figure 4.7 (final board footprint is 1.7 square inches). The Eagle CAD files are included in the distribution (see Appendix A). The board employs a two channel H-bridge with PWM to provide the drive for the motors. The driver chip chosen was the Toshiba TB6552FN. Again the interface is through the 10-pin header with pin assignments listed in Table 4.2.

Header Pin	Function
1	Digital Ground
2	Motor Ground
3	Motor V+
4	Channel B PWM
5	Channel A PWM
6	B Control Input 2
7	A Control Input 2
8	B Control Input 1
9	A Control Input 1
10	Digital V+

 Table 4.2: Connections for 10-pin Header on Motor Controller Board



Figure 4.1: Schematic for Acquisition Board



Figure 4.2: Routing for Top Layer of Acquisition Board



Figure 4.3: Routing for Bottom Layer of Acquisition Board



Figure 4.4: Digital System



Figure 4.5: EMG Controlled Prosthetic System



Figure 4.6: Schematic for Motor Controller Board



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Figure 4.7: Board Layout for Motor Controller

## Chapter 5

## **Results and Discussion**

Some samples of raw EMG data captured from the acquisition board are shown in Figures 5.1 and 5.2. The frequency magnitude spectrum is shown in Figure 5.3.

Observe the superior noise performance of the system even before digital filtering. Again, I reiterate that the only modifications done to this data were to attach range and time information. The 60Hz line noise component after amplification is under 10mV Pk-Pk and the active signal in Figure 5.2 fills nearly the full 3V range. The power spectrum in Figure 5.3 is textbook for an EMG signal. This superior performance is attributable to the careful setup of the system to avoid all possible sources of noise. This signals were collected from the palm, with the electrode laid along the thumb. This was to demonstrate the best possible functioning of the system, as this is where the best signal was observed.

The average power consumption of the acquisition board was under 10mA. The acquisition board was powered from 6 AA batteries and under worst-case scenario (250ksps sampling rate and gain/offset adjustment in between each sample) the battery life was 2.3 hours. This is obviously much harder than the system would ever be pushed in a typical application and the power consumption is still quite impressive.

It is difficult to give results for the entire digital platform that was implemented, since this is an enabling development, and there are no specific measurements to be made from it, however, the success of the system speaks for itself in that the SVM was able to be implemented successfully in such a way as to perform 10 classifications per second.

It is also worth noting that the entire system was able to function as a whole and during the demonstration, we were able to observe the robotic hand following the motions made by the demonstrator for one gesture (open/close).



Figure 5.1: Resting EMG



Figure 5.2: Active EMG



Figure 5.3: Active EMG Spectrum

## Chapter 6

# **Conclusions and Recommendations**

In conclusion, the system functions well. There are a few changes I would like to make to the analog acquisition boards so that their performance is a little more stable and there is plenty of room for building other external interfaces into the platform (i.e. wireless or some kind of cell phone interface) but overall the project added significant value and hopefully it can be used by other people planning to build an application that depends on the ability to acquire clean data from a physiological source and perform complex processing on that data. Appendices

# Appendix A

# Source File Tree

The distribution includes sources for the entire digital design, as well as the Eagle CAD files for all the boards that were fabricated. The file structure is as follows:

### A.1 Boards Folder

- motor.sch: EAGLE schematic for the motor controller board
- motor.brd: EAGLE board file for the acquisition board
- acq.sch: EAGLE schematic for the acquisition board
- acq.brd: EAGLE board file for the acquisition board
- phil.lbr: Parts library
- Sparkful.lbr: Parts library

### A.2 Digital

Note that this folder contains the entire case study including SVM classifier, however, the filetree is well structured so that it is easy to remove the unneeded portions. The main folder contains sources for the NIOS system as well as the following subfolders:

- emg\_capture: folder containing interfaces to all peripherals except SD Card as well as scope module and SVM
  - emg\_classifier: folder containing SVM sources
  - sdram\_70\_controller: sources for controller for SDRAM
- sdhc\_if: folder containing sources for hardware interface to SD Card
- software: folder containing software sources for control application

### A.3 Datasheets Folder

This folder contains the datasheets for many relevant parts used in the design

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