Design of Sleep Detection Device

For

Application towards Sleep Disorder

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Abstract

Sleep disorder is an irregular pattern of sleep cycles in a person. Some can be very serious and the symptoms can be unpredictable. Due to the irregular sleep patterns, a person with narcolepsy can put him/herself in unwanted or dangerous situations that could yield serious physical and mental damages along with financial losses through accidents by falling asleep irregularly. The Sleep Detection Device is a wearable device that alerts the user of sleep attacks. By measuring the frequency change of the EEG signal, the Sleep Detection Device can notify the user of their state of sleep through buzzers. Detailed guidelines provide, Introduction to the topic, Relevant Theory, Theoretical Development of the Device, Design Procedures, Detailed Design Specifications, Results, Conclusion and Recommendation.

Keywords: EEG, Sleep, Sleep Detection,

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1. INTRODUCTION

Sleep disorder is an irregular pattern of sleep cycles in a person. Some can be very serious and the symptoms can be unpredictable. One of the most serious cases of this disorder is narcolepsy**.** Narcolepsy is a chronic sleep disorder, which is categorized under Excessive Daytime Sleepiness. Patient symptoms include extreme fatigue and the possibility of falling asleep regardless of the time or place. **[1]** Due to the irregular sleep patterns, a person with narcolepsy can put him/herself in unwanted or dangerous situations that could yield serious physical and mental damages along with financial losses through accidents by falling asleep irregularly. By alerting the users of these sleep attacks and awake them through out the day can aid them to stay awake during important tasks, such as driving.

1.1 Objective

The goal of this project is to develop a device that will aid users with possible sleep disorders. By alerting them of irregular sleeping patterns as well as of any sudden sleep attacks, after time, the user can begin to find an optimal balance between certain activities that cause unfavorable effects on sleep to their sleeping habits, which could improve their daily lives. **[2]**

The final device will be in the form of an eyewear, which will monitor the user's brainwaves and Rapid Eye Movement. When the eyewear detects of any sleep characteristics it will alert the user through a buzzer. The eyewear will also accompany a device that will store data gathered for physicians to be analyzed in depth for further improvements of the patient's symptoms.

1.2 Methodology

In order to detect sleep, I have decided to monitor the brainwaves and the amount of rapid eye movement, which occurs during when a person is asleep. Both will be measured through EEG and EOG, respectively. It is imperative that both of the signals obtained from EEG and EOG are to be amplified to 1V range so that it can be properly analyzed. Once the signals are amplified then it will be processed through a frequency analysis algorithm to detect any frequency changes

in the signal in real time. Depending on the frequency changes in the algorithm the device will output proper alarms to alert the user of his/her state of awareness.

1.3 Scope

The project is divided into several different modules, which in the end will merge to complete the full expectations of the device.

1.3.1 Electroencephalogram

There are different types of brain waves that need to be considered for the project: alpha, beta, delta, and theta. The brain waves will be collected through an EEG, which will monitor the frequency of the brainwaves. By monitoring the decrease in frequency we can recognize whether the user has fallen asleep or decrease in an awareness. **[4]**

The EEG electrodes will be placed on the end tip part of the eyewear, where the input electrodes will be placed behind the user's ear to extract the signal. The signal gain from this area will be very weak so further signal amplification and filtering is critical. **[3]** The module for the EEG must be able to amplify the weak signal to amplitude of between 1V to 10V peak to peak. Additionally, since the brain signal received is presumably be very disorganized, the module need to eliminate any DC bias and noise to obtain a signal more recognizable to the physicians and myself for signal analysis.

1.3.2. Electroculargram

For the measurement of rapid eye movement, an EOG will be used. It will measure the biopotential produced by changes in the eye position, which is different from the measure of muscular activity occurred in the shift. Since the EOG measures the electric dipole between the cornea and the retina, when the eye moves to the right from its stationary point (middle), the output signal will be more positive, compared to when the eye moves to the left. **[6]** The sign of

the signal is completely up to the convention, meaning since the output from EOG is considered to be “Right – Left”, eyes moving to the right will be more positive.

As for the placement of the electrodes, they will be placed on the inside leg part of the frame, where the electrodes will be attached to the outside left/right of the eyes. The reference electrode will be attached on the middle of the forehead. Similarly to EEG, the signal gained from the EOG input electrodes need to be amplified. Since the output signal will be approximately under 1.0mV, significant increase in gain is desired. A design of a filter is also needed, since the frequency of the signal will be very small.

1.3.3. Analog Signal Circuit

For the analog amplifying circuit, the EEG and EOG signals needs to be amplified to the 1V ~ 10V range. Failing to properly amplifying the signals can lead to complication since the rest of the modules require the amplitude to be in the range specified. Also it is more convenient to have the amplification done properly for the signal analysis.

The proper filtering of the signal is also essential. The sufficient filtering frequency range is between 2.2 to 30 Hz. It is critical to eliminate any noticeable noise in the system for more accurate results for the signal-processing module. Hence, and acceptable SNR ratio needs to be maintained through out the circuit.

Currently the filters, necessary algorithms and additional circuitry are still being looked at being designed at this stage. Some of the filters have been considered but more correct data through experiment is needed before any of the filters are decided.

For the signal-processing module, PIC and DSP is being considered. But PIC is likely to be the choice because of its cost and its ability is sufficient enough for the application.

1.3.4. Signal Processing Module

The main function of the signal-processing module is to determine the frequency of the EEG signal in real time. Since the frequency of the EEG signal can determine the state of awareness for the user, this module will determine the frequency and will assign appropriate awareness level and give specific level of output accordingly. The output for the signal-processing module consists of Buzzer_0, Buzzer_1, and User_Sleep. Buzzer_0 and Buzzer_1 will be the main output for the module, where these data bits will determine the buzzer output level of the device.

User_Sleep data bit will be used as an indicator of whether the user has changed his/her state of the awareness or not. This bit is important to accurate indicate the threshold frequency of the system. The threshold frequency chosen was at 4Hz, 8Hz, and 13Hz, which indicate the changes in the state of user awareness.

1.3.5. Buzzer Circuit

The buzzer circuit serves the purpose of properly alerting the user of the awareness level. This is achieved by two bits from the signal processing modules; Buzzer_0 and Buzzer_1. The output level or volume of the buzzer circuit will be determined through data logic. For example, ‘00’ will indicate the lowest volume or silence and ‘11’ producing the loudest volume of the device. The buzzers will not be silent but progress to the next level of intensity every 2 seconds until the user is awaken

2. LITERATURE REVIEW

In the past, there has been few devices that record and alert people with sleep disorders, but none successfully commercial device. The main design flaw with such application is the method of gathering the necessary data. With the available technology, only real way of measuring or detecting whether a person is going to fall asleep or not is through the analysis of brainwaves. Since extracting such information requires us to place electrodes on the person’s scalp, it makes it tougher to make the device portable and user friendly. **[3]** The process is very tedious and

placing the electrodes in the correct position with gel also contributes to the discomforting feeling a user might get from the procedure. For this project, I will try to eliminate as much as discomfort as I can by placing all of the electrodes on an eyewear, so that the user wont have to guess where the electrodes will be placed. If time permits, sending the signals from the electrode eyewear to the processing unit wirelessly will be considered as well.

3. STATEMENT OF PROBLEM AND METHODOLOGY OF SOLUTION

3.1 Relevant Theory: Brain Waves

The human brain goes through several cycles of sleep while a person is sleeping. These stages can be categorized into 4 different stages, each highlighting its own type of brain waves. Shown in Table 3.1.1, brain waves can be categorized into 4 different sections, which are Alpha, Beta, Theta and Delta waves. These waves are sectioned according to its signal amplitude but mainly through its frequency. With these different waves highlighting different stages of sleep, REM sleep can be found, which can be common to be shown around 10~15 minuets into a deep stage of sleep. For someone with a sleep disorder these stages sleep can be disoriented resulting in patients to feel constant fatigue.

Stages of Sleep:

Stage 1: Alpha wave is shown strongly in stage 1 sleep. Alpha wave, which ranges from frequencies 8 to 11 Hz, is an indication of onset sleep. (Awake-like sleep) It is very common to notice cases where alpha wave is transition into theta waves, which ranges from 4 to 7 Hz. Theta wave is recognized as light sleep and can be easily skipped.

Stage 2: The main characteristics of this stage are the sleep spindles and K-complexes. Although these special patterns are found occasionally, they tend to appear only for a short period of time of 0.5 to 1.5. This is also the stage where relaxation of muscular activity and consciousness to the environment are loss.

Stage 3 + 4: These stage is known as a transition stage between 2 to 4, facilitating at 1 to 4 Hz. These ranges of frequency can be categorized in as delta waves and for the application of this device the loudest alarm will be applied for this wave. This is due to delta wave being considered as a state of 'deep sleep'.

3.2 Relevant Theory: Frequency Analysis

The frequency analysis for the signal-processing module is essential for the detection of sleep. Since the device is using a 24-pin PIC the frequency-determining algorithm needs to be cheap in processing power. There were number of devices or methods that can complete the task of measuring frequency of a wave but implementing these method into the sleep detection device is a challenge.

Counting

In theory, by counting is the most common method used for measuring the frequency of a wave. If the occurrences of an event can be counted within a specific time interval, then frequency of the wave can be determined. (Equation 3.2.1)

$$f = N_0/T \tag{3.2.1}$$

Where, N_o is the number of times an event has occurred

T is the specific time interval

f is the frequency of the wave

Frequency Counter

Frequency counter is an electronic device that is capable of measuring the frequency of an electronic signal. This device uses the idea of counting the number of cycles during a specific time interval. In the device there is a counter, which accumulate a value for the counting process and transfers the value onto a display. A clock oscillator is used with this device to greatly improve on the accuracy and resolution of the measurement. The clock oscillator is usually considerably larger than the expected frequency. On the market, most of the frequency counters already include some sort of amplifier, filtering, and wave shaping module at the input. This

device is very accurate and the core principles can be implemented in a way that can fit the specifications of the sleep detection device.

Zero Crossings

Zero crossings are a point in a wave that crosses the zero amplitude. At this instantaneous point, there is no voltage present. The fundamental principle of zero crossing in a signal is applied in many different field of signal processing. Counting zero crossing can be seen in speech processing and digital audio players. Using the counting method specified above, zero crossings method shows great promise in determining the frequency of a signal. Further development of the frequency determinant algorithm using zero crossing will be discussed further in the design procedure section.

4. DESIGN PROCEDURES

4.1 Analog Signal Circuit

There are two core parts to the analog signal circuit, signal amplification and signal filtering. It is essential to provide enough amplification of the EEG & EOG signals successfully so that the signal-processing module can receive sufficient inputs. Filtering process is also essential so that the signal is not disrupted greatly due to noise. The analog signal circuitry is an important pre-step for the frequency analysis, and can be considered to be essential as the EEG and EOG 'information' needs to be properly delivered to the signal processing module for proper analysis. Incorporated with this circuitry is the actually electrodes for extracting the signals needed, which will be in the form of disposable Ag/AgCl electrodes. The placements of the EEG electrodes will be on the forehead of the user, which are the FP1 and FP2 of the 10-20-system electrode placement grid. Figure 4.1.1. The reference electrode for the EEG leads will be located at the mastoid process of the user. The EOG electrodes will be placed on the side of the user beside the eye. So that a voltage difference can be measured with reference to the reference electrode located on the forehead. A resistor network was present in the circuit before the pre-amplification stage so that the user is protected from any circuitry in the device when wearing the electrodes.

For the initial amplification of the circuit, a low cost low power bioinstrumentation amplifier was used. Some of the main features of an instrumentation amplifier were the easy to use gain setter, excellent DC performances, and low noise of 0.28 uV p-p noise. With these specific features of the AD620 amplifier designed by Analog Devices, the amplification result was rated to be far greater than using 3 op-amps.

For the filtering portion of the circuit, both high pass and low pass filters were used. The main purpose for the filter process is the elimination of the noise in the signal. Two main type of the noise that could be attenuated in this module would be the 60 Hz and DC offsets. In the EEG part of the circuit, a 4^{th} order Tchebyscheff filter with 1dB pass band ripple using a Sallen and Key topology was used to implement the low pass filter. This low pass filter was present to eliminate the 60 Hz noise presented by the power lines. The OP491, micropower Single-Supply Op Amps, designed by Analog Devices were used to implement the Tchebyscheff low pass filter. As for the DC offsets created from the electrode shifts was eliminated through both active and passive high pass filters. Active high pass filters were designed; again, with op amps from the OP491 and passive high pass filters were designed using a simple capacitor and resistor network. Additionally a secondary amplification is presented in the active high pass filter. Some of the key features of the OP491 were the low offset voltage of 700 uV, a wide input voltage range and sharp cut-offs, which is very important in filter design. For the EOG part of the circuit, the very same low pass filter was used but the only different filtering process was the elimination of the high pass filters. In an EOG circuit the DC offsets are an important part of the analysis, since the dipole present in the eye is the key principle of EOG readings. Since high pass filters eliminate the DC offsets created from the dipole presented in the eye, high pass filter presence would eliminate the very purpose of EOG circuit.

4.2 Signal Processing Module

The determining signal process of the device is essential, as this is the process that will determine whether the user is sleeping or not. Additionally, this process needs to have the ability to alert the user before he/she falls into a deep state of sleep. The signal-processing module serves the core purpose of the device by using the EEG signals obtained from the analog EEG circuit from the previous section. This module will determine the frequency of the EEG signal in

real time and will assign appropriate awareness level and output bits accordingly. Upon reaching the signal-processing module, the analog EEG circuit will have amplified the signal to be between 0 and 5V with zero DC offsets. In terms of frequency, the signal-processing module will only receive signals between 1 and 30 Hz from the analog EEG circuit. The main output of the signal-processing module will be in total of 3 bits; User_Sleeping, Buzzer_0 and Buzzer_1. These bits are the output that will essentially control the buzzer circuit, which will be discussed in detail in the next section. A 16-bit microcontroller, PIC24HJ32GP designed by Microchip, was chosen for its high-performance CPU, 10-bit ADC capability, and C compiler optimized feature. A microcontroller PIC was chosen over DSP mainly because of its low-complexity and low price. Using a PIC, a C language program can be written to properly determine the frequency of the signal.

The discussion of the different brain wave ranges was discussed in 3.1 Relevant Theory: Brain waves section. The four frequency ranges given are alpha (8 – 13 Hz), beta (13 – 22 Hz), delta (0.5 – 4 Hz), and theta (4 – 8 Hz). The awareness level of the user will be fitted according to these ranges of frequency. In the signal-processing module, beta wave with 13 – 22 Hz will be given the highest level of alertness of the user. For the alpha wave with 8 – 13 Hz will be given awake-like sleep, which will be the 2nd highest level of alertness. The theta wave with 4 – 8 Hz is the light sleep level with the 3rd highest level of alertness and lastly, the delta wave with 0.5 – 4 Hz is the lowest level of alertness, which is the level of deep sleep.

There are 2 main complications to the signal-processing module. While determining the frequency of the user is very important, the module needs to do so in real-time with little or ideally with no delay. Secondly, the module needs to be able to consistently compare the user's frequency level with his/hers' previous state and update. This is important because the signal-processing module needs to alert the user of the 4 different level of alertness but also needs to alert the user of the changes in the level of alertness, and again in real-time.

To discuss in detail the method of properly determining the frequency of the signal, the fundamentals of zero crossing need to be introduced again. Using the PIC24HJ32GP, the frequency-determining algorithm was written in C language. The basis of the algorithm is the

idea of zero crossing. There were alternative methods but with a low cost CPU, there were limitations with the processing power. But by using a low cost PIC with a C written code, an algorithm using the zero crossing was the best suited for the device.

At the beginning of the project a simple equation,

$$f = N_0/T \tag{4.2.1}$$

N_o being the number of zero crossing counted and T being the amount of time counting. The average time value chosen was at 250 ms and the zero crossings were represented in the code as when the amplitude would make a transition between positive to negative. This method is a very easy effective method if and only if good zero crossing points are obtainable, which with an ADC is not always the case. To improve the method edge detection of the signal was considered. By measuring the number of counts in a specific time period by measuring the number of counts between the last edge and the end of the time period could enhance the algorithm. The above equation would be modified slightly into,

$$f = N_0 \Big/ (T + t_{n-1} - t_n) \tag{4.2.2}$$

Where, No is the number of zero crossings

T is the specific time interval (250 ms)

t_n is the time interval between the last edge and the end of the time interval 'n'.

With this algorithm, complications arose with the frequency lower than 1/T. Additionally, with the EEG signal where specifying the edges of the time interval surfaced as another source of error. The zero crossing is also harder to be determined through this method due to some of the overlap counts that could potentially occur. From this algorithm, it was noted that as long as the sample frequency is not much higher than the expected frequency than counts of the sign – change might be a better way of approaching the problem. Instead of focusing on when the signal becomes instantaneously 'zero', defining the zero crossing of the signal to be a sign

change between positive to negative was another option that could give more accurate result; essentially, counting of the number of maximas and minima's of the signal. Resulting,

$$f = {}^{2N_0}/_{T} \tag{4.2.3}$$

Where, N_o is the count of positive to negative transition

T is the specific time interval (250 ms)

f is the resulting frequency

When the counts of positive to negative transition were measured over a specific time interval a fairly accurate result would be given. Additionally, it is less computationally expensive compared to the second algorithm presented, but more accurate than the first.

C code program was written according to the algorithm, and the PIC outputs 3 different bits. The User_Sleep bit is an indicator bit that shows if the user is ultimately sleeping or not, where the Buzzer_0 and Buzzer_1 bits are used in the buzzer circuit. Buzzer_0 and Buzzer_1 bits are given either '0' or '1' and with digital logic an appropriate level of response is given.

4.3 Buzzer Circuit

To output a proper response is very import to the device. When the signal process algorithm outputs proper alerting levels it is very important to alert the user using the device. For the project buzzers were used to notify the user of his/her awareness levels and ultimately waking them up. The buzzer circuit is composed of two different piezeo buzzers and a 4:1 multiplexer. Using the combinations of the two buzzers three different buzzer levels will be outputted in 2-second intervals determined by the output logic combinations from the signal-processing unit.

The output logic will be '00' for fully awake where no buzzer sound will be outputted. The logic bits '01' will be for the slight loss of awareness with the lowest volume. Once the user has reached this stage of awareness the signal-processing algorithm from the signal-processing unit will check the awareness level after 2 seconds. If the user has fallen down a level of awareness, indicating that the user has fallen deeper into a sleep mode, than the bits inputted to the buzzer

circuit multiplexer will be '10' outputting medium level of volume. After another frequency analysis and if the user has fallen into the deepest state of sleep than the bits '11' will indicate the buzzer circuit to produce the highest level of volume through both buzzers. Of course, in between the stages of user's awareness level indicates that the user is waking up; the buzzer volume level will simply decrease accordingly.

The design specification of the buzzer circuit will include a voltage divider, which will be used to produce different volume levels using the buzzers. The voltage divider will be connected before the multiplexer and it will range between 0 to 5 V where the voltage dividers will assign no volume to the loudest volume through assigning different voltage levels to its appropriate response.

5 EXPERIMENTAL PROCEDURES

5.1 Analog Signal Circuit

5.1.1 EEG Circuit

The first part of the analog signal circuit unit is the EEG circuit. The main specification of this circuit is to amplify the brain waves in to the range of 1 to 10 Vpp. The brainwaves collected from the electrodes were 10 to 100 uV, and for this reason it was imperative that the amplifier circuit portion of this unit would have a gain of at least 10,000. The overall design schematic for the EEG circuit is shown in Figure 5.1.2.1.

The first head stage amplification was set at the gain of 10, using Analog Devices AD620. Using equation 5.1.1 converting to Equation 5.1.2 to find the resistor for the gain of 10. So, R_G=5.49k ohms, G_1=10, where the gain resister R_G will be placed across pin 1 and 8 for AD620.

$$G_1 = \frac{49.4k\Omega}{R_G} + 1 \tag{5.1.1}$$

$$R_G = \frac{49.4k\Omega}{G - 1} \tag{5.1.2}$$

The second part of is the combination of 1st order high-pass filter and the second amplification stage. Using Analog Device ¼ OP491, second gain would have to be higher than G_2=1000 and the filter will have to have a cutoff frequency of 1Hz.

$$G_2 = \frac{R_1}{R_2} + 1 \tag{5.1.3}$$

$$f_{c\,HP} = \frac{1}{2\pi R_1 C} \tag{5.1.4}$$

Equation 5.1.3 will provide proper gain, and having G_2=1000, R_1 and R_2 were chosen to be 1M ohms and 1k ohms respectively. R_1 and R_2 are resistors placed on the negative feedback of the filter. (Figure 5.1.1.2) Equation 5.1.4 is the equation used to calculate the cutoff frequency of the 1st order high-pass filter. C=2.2nF was chosen, and knowing that f_c would have to equal 1Hz, R_1 was calculated to be 73.1k ohms.

$$G_{Final} = G_1 \times G_2 \tag{5.1.5}$$

To calculate the final gain of the EEG circuit, first gain and second gain is cascaded to give G_{final} of 10000. (Equation 5.1.5)

$$A(s)_{HP} = \frac{1}{1 + \frac{2}{w_c R_1 C s} + \frac{1}{(w_c)^2 R_1 R_2 C^2 s^2}} \tag{5.1.6}$$

The second high-pass filter was chosen to be 2nd order. This active filter serves to have cutoff frequency of 1Hz, hence w_c = 1Hz. The transfer function is shown in equation 5.1.6. The resistor and capacitor values were chosen according to the correct parameter for the Sallen-Key second order Tchebyscheff high pass filter, where a_1 = 1.302 and b_1 = 1.551. Using a_1 and b_1 parameters to compute R_1, R_2 and C, equation 5.1.7 shows that R_1 = 111.1k Ohms, R_2 =30.3k Ohms and C = 2.2uF.

$$a_1 = \frac{2}{w_c R_1 C}, \; b_1 = \frac{1}{w_c^{\,2} R_1 R_2 C^2}$$

(5.1.7)

The final filtering portion of the unit is the 4th order low-pass filter to get rid of the 60Hz noise. The transfer function of the low-pass filter is shown in equation 5.1.8, where w_c = 30Hz. This means that any frequency above 30Hz will be cut off.

$$A(s)_{LP} = \frac{1}{1 + w_c(R_1 + R_2)C_1 s + (w_c)^2 R_1 R_2 C_1 C_2 s^2}$$

(5.1.8)

Again, using the appropriate fourth order Tchebyscheff filter with 1dB pass band ripple parameters resistor and capacitor values were properly calculated, where the parameters are a_1=2.5904, b_1 = 4.1301, a_2 = 0.3039 and b_2 = 1.1697. Since it is a 4th order low-pass filter, two ¼ OP491 were used in cascade. (Figure 5.1.1.2) To compute the resistor values capacitors chosen ahead of time, where C_1=33nF, C_2=330nF, C_3=4.7nF and C_4=330nF. However, it is important to ensure that the capacitor values are satisfying equation 5.1.9.

$$c_2 \geq c_1 \frac{4b_1}{a_1^{\,2}}$$

(5.1.9)

The capacitor values chosen above all satisfy the condition above, which ensures that saturation does not occur. Using Equation 5.1.10, resistor values were calculated, where f_c=30Hz, R_1=22 k Ohms, R_2 = 330 k Ohms, R_3 = 56k Ohms and R_4 = 275k Ohms.

$$R_{1,2} = \frac{a_1 c_2 \mp \sqrt{a_1^{\,2} c_2^{\,2} - 4 b_1 c_1 c_2}}{4\pi f_c c_2 c_2}$$

(5.1.10)

All of the above units allow the frequency range to be between 1 to 30Hz with the gain of 10,000. With the above components is able to satisfy enough amplification for the signal-processing unit.

5.1.2 EOG Circuit

The second part of the analog signal circuit unit is the EOG circuit. The main specification of the EOG circuit is very similar to the EEG circuit in terms of the gain. Instead of the EEG having a microvolt range, EOG is concerned with millivolt range. The major difference in the frequency range is that the frequency range of the EOG circuit is DC to 30 Hz, where the EEG circuit needs the DC frequency completely eliminated. The overall design schematics are shown in Figure (5.1.2.1).

The head stage is identical to the EEG circuit head stage. Using Equation 5.1.1 converting to Equation 5.1.2 to find the resistor for the gain of 10. Again, R_G=5.49k ohms, is needed to have G_1=10. The second amplification stage is similar to the EEG second amplification stage where the passive high-pass filter before the second amplification stage has been eliminated so that the DC frequency components are needed. Using Analog Device ¼ OP491, second gain would have to be approximately G_2=100. (Equation 5.1.3) From Equation 5.1.5 the final gain of EOG circuit is to be 1000.

The 4th order low pass filter is identical to the EEG circuit. (Please refer to low pass filter section of 5.1.1) One of the major differences in EEG and EOG circuit is the voltage regulator. This is needed so that the voltage reference can be adjusted. The voltage regulator consists of an op-amp and a voltage regulated resistor. (Figure 5.1.2.2) With this in consideration, the V_{ref} needs to be in the range of 0 to 200mV. The voltage regulating resistor, R_2, ranges from 0 to 5k Ohms, where the voltage regulating resistor, R_2, is connected in series with R_3. (Equation 5.1.11)

$$R_2' = R_2 + R_3 \tag{5.1.11}$$

The important equation used to find R_1 and R_3 of the voltage regulator a current circuit analysis was performed on Figure 5.1.2.2. The resulting equation is as shown in 5.1.12.

$$V_{ref} = 5\frac{R_2' - R_1}{R_2' + R_1}$$

(5.1.12)

Since V_{ref} is ranging from 0 to 200mV, when the voltage-regulating resistor, R_2, is 0 Ohms resulting V_{ref} should be 0V and when R_2 is 5k Ohms, V_{ref} is equal to 200mV. This is outlined in equation 5.1.13, and with these two condition R_1 and R_3 was calculated to be 6.8k Ohms and 5.2k Ohms, respectively.

$$200mV = 5\frac{(5k\Omega + R_3) - R_1}{(5k\Omega + R_3) + R_1} \quad 0V = 5\frac{(0\Omega + R_3) - R_1}{(0\Omega + R_3) + R_1}$$

(5.1.13)

The V_{ref} is inputted into the first amplification stage so that there is a voltage difference between the two electrodes placed on outer side of the eye.

5.2 Signal Processing Unit

The main core of the signal-processing unit is a 28-pin PIC24HJ32GP from Microchip. The full schematic of the PIC design is shown in Figure 5.2.1. There are other components that support the microcontroller such as, a AAA 20 MHz oscillator to continually feed an oscillating signal for the clocks, IN5820 Schottky diodes and resistors to protect the microcontroller from instantaneous current spikes and negative voltage. The inputs are the amplified and filtered 1 Vpp range EEG signal from the EEG analog signal circuit unit and ultimately outputting logic bits to the buzzer circuit.

In detail, the microcontroller is supplied with +5Vs at VDD, pin 13 and 28. It is protected with the IN5820 Schottky diodes. All of the VSS, at pin 8 and 19 are set to ground. The EEG signal is inputted into A1, pin 3, which is also protected with IN5820 Schottky diodes and 1k Ohms resistor. At the clock input A2, pin 9, is connected with 20 Mhz oscillator, which is fed with +5V. The output B0 (Buzzer_0) and B1 (Buzzer_1), or pins 4 and 5 respectively, are set for the buzzer circuit. Current limiting resistors, at 240 Ohms, are also placed to protect the

microcontroller and also to prevent any memory reset due to instantaneous voltage spikes. The resistor values were chosen so that the microcontroller is limited with the current being used.

$$V_{max} = I_{max} \times R_{ci}$$

(5.2.1)

Another important aspects of the signal-processing unit are the sampling rate. The microcontroller's internal A/D converter is used to digitize the EEG signal, which is necessary for the signal analysis. The provided internal A/D converter is a 10-bit digital sampler, and for the purpose of this project a sampling rate of 250 samples per second was chosen. The equation 5.2.2 shows the Nyquist rate, which states that the minimum sampling rate is required to be greater than the band-pass sampling frequency to avoid aliasing.

$$fs \geq f_N = 2B$$

(5.2.2)

Since the maximum frequency being considered for the project is 30Hz, the sampling rate should be higher or equal to 60 Hz. For these reason 250 samples is more than adequate and satisfies the Nyquist rate. As it was stated from Section 4.2, equation 4.2.3, the frequency analysis equation is rewritten in C.

The microcontroller will count the transition from a positive peak to negative peak using the digitized samples and will divide the number of transition by the sampling rate, which is 250 ms. This frequency is the calculate frequency which will be used to assign awake level of the user. The following is a short segment of the alert level assigning code of the signal-processing unit.

The calculated frequency and alert level of the user is compared in real time every 2 seconds, which is sufficient enough to find out if the user has changed his/her state of sleep and produce outputs accordingly. The full C program is provided in the Appendix.

5.3 Buzzer Circuit

The buzzer circuit unit is the main source of output that directly alerts the user of the device of his/her alert level. Through the use of two 6 VDC buzzers the user is notified of their sleep stages through the level depending on the frequency analysis completed in the signal processing unit. The entire application is composed of 1k Ohms resistors, 3/5V ADG609BNZ 4:1 Multiplexer designed by Analog Devices, and two 6VDC Buzzers. The 4:1 Multiplexer is supplied with +5V voltage source, which is divided up through voltage dividers to supply different level of voltage into switch inputs, SA0 ~ SA3 addresses. The multiplexer switches one of the 4 inputs to a common output determined by 2-bit binary address lines; A0 and A1. The address line A0 and A1 are the outputs received from the signal-processing module, where address A0 receives the bit Buzzer_0 and A1 receives the bit from Buzzer_1. An EN input is used to enable the device, which is connected to the bit User_Sleep, meaning when the User_Sleep bit is ON then the Multiplexer will be enabled to supply its outputs to the buzzers.

The SA0 ~ SA3 addresses, as specified before, is connected to a voltage divider that is able to supply different level of voltage so that the appropriate level of volume can be controlled with the buzzers.

$$\frac{V_{Total}}{V_{Supply}} = \frac{R_{Total}}{R_i} \tag{5.3.1}$$

Where V_{Total} is the +5 V voltage supply and V_{Supply} is the voltage level supplied to SA0 ~ SA3. R_i is the resistors connected between each multiplexer input, and between each input 1k Ohm resistor is connected and input SA3 is the closest to the +5V. This allows SA3 to be unaffected by the voltage divider to receive full +5V, hence both buzzers being at their loudest state. The resister network is designed so that SA2 would receive the affect of have one 1k resister with 3.33V. SA1 have the affect of two 1k resisters with 1.5V and lastly, SA0 with 0V. The buzzer will respond the voltage level and simply produce the highest volume when supplied with the highest voltage level.

The truth table is shown in Table 5.3.1, which indicates that when the input A0 and A1 are “11” than SA3 will be producing +5V. When the input A0 and A1 are “10” is associated with SA2,

"01" will associate with SA1 and "00" will be no volume, which are all directly related to the truth table discussed with Buzzer_0 and Buzzer_1 bits from the signal-processing unit.

6. RESULTS AND DISCUSSION

There were several tests performed specifically on each subunit of the device for its functionality and performances. Its level of performance and functionality can be affected by lot of different areas, such as signal-to-noise ratio, common-mode rejection ratio, power consumption, output level and etc. Each of the subunits was tested using the oscilloscope and the function generator provided in the lab, as well a voltage supply. This is for the sole reason of idealizing the initial conditions of all of the 'inputs' for each subunit device so that an accurate result can be derived from the tests. If not done so, some of the errors, noise and other complications could carry over to the other units not portraying its real performance. However, the complete form of the device was also tested to address those complications and to discuss how the lack of performance on one device is affecting the other units.

6.1 Analog Signal Circuit

There are two critical portions of the analog signal circuit; amplification and filtering of the signal. To test the amplification the actual gain was calculated and compared with the theoretical results. Theoretical gain, as discussed section 5.1.2, was 10,000. Using the function generator, 10mVpp sine wave was used to replace the brain waves. Since the function generator was not capable of producing sine waves in the order of 100 uV, a voltage divider was used to divide the voltage so that smaller input peak-to-peak voltage was supplied.

$$G_{Actual} = \frac{V_{out}}{V_{in}}$$

(6.1.1)

For the sake of testing out each of the components, the two stages of amplifications were tested separately and together at different times. In theory, the first gain of the AD620NZ amplifier was 10V. From the lab, the actual voltage received on the oscilloscope was at 117mV. (Figure 6.1.2) (due to the reading setting on oscilloscope, this 234mV is the doubled reading of the actual

voltage reading, meaning it is actually at 117mV.) This is slightly larger than the 100mV theoretical reading. The second amplification readings were at 2.44V. (Figure 6.1.3) Which is perfectly acceptable for the application since the device input should be in the order of 1Vpp. Additionally, calculating the Total Actual Gain of the device is recognized to be 24,400 through equation 6.1.1.

The signal-to-noise ratio tested for the analog amplifier circuit was important to ensure that the signal being amplified and filtered were in an acceptable range of SNR. The equation for the signal-to-noise ratio is provided by equation 6.1.2, where the power of the signal divided by the power of the noise signal would give the SNR of the system. Since the analog circuit is composed of passive components, and the amplifier, equation 6.1.2 were broken down into equation 6.1.3, where the noise components of the analog circuit are taken into consideration in detail. To test out the values needed for this calculation, each resister/capacitor network noise power was measured separately, as well as the amplifiers by grounding the inputs. The equation 6.1.4 shows the noise of the components broken down individually, where v_{source} is equal to the RMS of 10uV according to the amplifier datasheet. The final SNR_0 was calculated to be 88.2, which is an acceptable range. To decrease the noise, shorter wires, and better combination of resisters were used.

$$SNR = \frac{P_{Signal}}{P_{Noise}} \tag{6.1.2}$$

$$SNR_0 = \frac{\tilde{v}_{source}^{\,2}}{(4KTR_f + e_{ni}^{\,2})B} \tag{6.1.3}$$

$$SNR_0 = \frac{\tilde{v}_{Source}^{\,2}}{\{4KTR_f + (e_{n_1}^{\,2}) + (e_{n_2}^{\,2}/Kv_1^{\,2}) + (e_{n_3}^{\,2}/Kv_1^{\,2}Kv_2^{\,2})\}B} \tag{6.1.4}$$

Common-mode rejection ratio was also calculated to evaluate the performance of the device. A high CMRR shows that the performance of the instrumentation amplifier is working effectively, especially under small voltage differentials. Similar to calculating the SNR of the circuit, the

amplifier's inputs were short circuited to measure the output gain. The common-mode gains of each amplifier were measured to be 0.143 and 1e-4 respectively. This shows that the CMRR of the first amplifier was calculated to be 36.89dB and 147.74dB. Taking in consideration that the gain difference between the actual gain and the common-mode gain is very large, these numbers are acceptable for the application.

$$CMRR = 10\log_{10}\left(\frac{A_d}{A_{cm}}\right)^2 \tag{6.1.5}$$

$$CMRR = 20\log_{10}\left(\frac{A_d}{|A_{cm}|}\right) \tag{6.1.6}$$

For the second portion of the analog amplifier circuit unit, the frequency response of the amplifiers was taken into consideration. The frequency range of the device is to be 1 to 30Hz. Passive high pass filter, active high pass filter and the 4th order low pass filters were simulated in PSpice so that the proper frequency response could be analyzed correctly.

The Figures 6.1.4 and 6.1.5 show the frequency response of the passive high pass filter with the cutoff frequency of 1Hz. Both the actual and simulated frequency response graphs show that the cutoff frequency of 1Hz is very closely followed, additionally, that the DC offset noise is being eliminated correctly for the application. The passive and active high pass filters only exist in the EEG circuit and not in the EOG circuit.

The Figures 6.1.6 and 6.1.7 show the frequency response of the active 4th order low pass filter with the cutoff frequency of 30Hz. Again from the plots it is noticeable that the low pass filter is eliminating any of the frequencies above 30Hz, which is very important for eliminating any 60Hz noise. The actual and simulated is very similar for the low pass filter as well.

As a final test, the entire analog circuit was tested all together, which shows that the EEG signal was properly amplified to 984mVpp with approximately 1.4Hz to 32.3Hz frequency range. The Figure 6.1.8 is the output of the final EEG signal. The Figure 1.6.9 shows the output of the final

EOG signal, which was taken using CleveLab Bio Radio. It is noticeable that as the eye movement changes from left to right the voltage level is varying from positive to negative.

6.2 Signal-Processing Module

Main test generated for the signal-processing module was to determine if the correct bit combinations were outputted for its specific range of frequency. Table 6.2.1 shows the range of frequency and the awake level specified and Table 6.2.1 shows the binary bit combination of the awake levels. Three output bits were monitored, User_Sleep, Buzzer_0 and Buzzer_1, where the User_Sleep will be on so that the buzzer circuit is powered and Buzzer_0 and Buzzer_1 will be the core bit combination produced for the frequency analysis.

For the sake of testing the module, a 1Vpp sine wave was used from function generator. With the function generator it is very easy to change the range of frequencies. The output was monitored through using the LED lights provided on the PIC itself, since the PIC was manufactured and modified by IEEE McMaster University Chapter, it was very easy to assign bits to the 4 different LED lights on the circuit board.

First, the frequency range of the beta wave was monitored. When the frequency was slowly decreased from 30 to 15Hz the output response was at bits ‘00’. This is very close to the frequency range specified from Table. The minor error in the frequency range is acceptable for the beta wave. The alpha wave of frequency range 13 to 8Hz was monitored next. When the frequency transitioned from 15 Hz into the 13Hz range the appropriate response of a second light activation was monitored, meaning ‘01’ bits were activated. However, when the frequency at approximately 12Hz, the response changed. This results in some of the programming error in the frequency analysis, where the ‘10’ bit response should not be shown until the frequency is much lower at 8Hz. When the theta wave, 8 to 4Hz, were monitored, similar complications arose. The measured theta wave range was outputted as 12 to 6Hz. This means that the user will be getting the 2^{nd} loudest volume before the theoretical awake level. Lastly, the delta wave, specified to range from 0.5 to 4Hz, was shown to be at approximately 6 to 1Hz. . As it is recognizable in Figure 6.2.1, the frequency analysis algorithm has created a margin of frequency error, where the result is acceptable but can be more accurate.

When the entire module was tested with EEG signal, the result was very similar to the ones from the function generator. However due to the random characteristics of the EEG signal the error in the frequency analysis produced greater error in the frequency ranges. This could be avoided by having more complex frequency analysis algorithm and by having a more powerful microcontroller. Because of the cost consideration, a cheap microcontroller was used for the device but with a more powerful microcontroller, a more complex frequency analysis algorithm can be incorporated reducing the errors that are present. Additionally, more complex analog circuit that is able to reduce the noise in the system would also aid in reducing the error margin of the signal-processing module.

6.3 Buzzer Circuit

The main functionality of the buzzer circuit is to provide correct volume level for the buzzer according to its awake level. This circuit was tested providing different voltage into the Switch Input of the multiplexer, since the bits assigning test was already been successful in signal-processing module. When the buzzer circuit was provided with '00' in its input, a 0V was shown with silence. When A0 and A1 were set at '01', the buzzer shows approximately 1.4V with the lowest volume from the buzzers. When A0 and A1 were inputted with '10' bits, the buzzer was shown to have approximately 3.11V with a medium level of volume. Lastly, when the inputs were set at '11', the multiplexer showed to be provided with 4.89V producing the highest level of volume. The buzzer circuit shows to be working properly.

6.4 Overall Device

Overall device was tested overnight with the EEG leads to the buzzer circuit. The initial design showed that the device was working at an acceptable level with margin of error created in the signal-processing module. However, at an attempt to decrease the margin of error in the frequency analysis algorithm resulted in the signal-processing module to be dysfunctional. There are some problems with the current code and debugging the program to get the signal-processing module to work functionally was unsuccessful. However, the previous recorded results show that the device was working at an acceptable level.

7. CONCLUSIONS AND RECOMMENDATION

The Sleep Detection Device performance was acceptable. Most of the objectives stated before the project was completed, however, there were few portions of the device that was found to be less applicable. The EEG & EOG signal amplifier and filter circuitry unit was able to amplify the signal to its appropriate amount. The frequency response of the overall system was also very impressive as all of the variables that could greatly affect noise have been reduced. The EEG frequency was varying and very random during the experimental stage but the device was performing at an acceptable level where it took some of the random nature of the brain waves into consideration. Some of the source of problem that surfaced was noise and error due to noise. Smaller wires to rearrangement of resistors were performed in the analog circuitry to ensure that the signal to noise ratio was high.

Signal-processing unit was lacking because of the complications with the program. At one point the device was working with a margin of error in the frequency range, however, the current program still needs to be debugged for more accurate results. The microcontroller could also be upgraded so that a more complex frequency analysis would be performed for the device. This was one of the biggest challenges of the project, due to the random nature of the brain waves; it is very difficult to analyze the exact frequency in real time.

Another major discovery in the process of the project was that the EOG is not a very applicable source of input to determine a user's sleep state. Stronger results were shown with the EEG signal rather than EOG, because the REM patterns from EOG were not always consistent. Later EOG circuit was added just for the purpose of user's REM recording, but nothing more.

The cost of the project was at a medium level. More portions such as a portable battery source, or different methods of alerting the user could make this device more user friendly. This project proved that using EEG signals to detect sleep patterns and to alert the user of his/her state could very well be applied to commercial use. More improvements with the frequency analysis as well as the user-comfort level needs to be enhanced but as for the idea and the fundamental theory of device were proven to be successful.

APPENDIX A: Overall Design Block Diagram

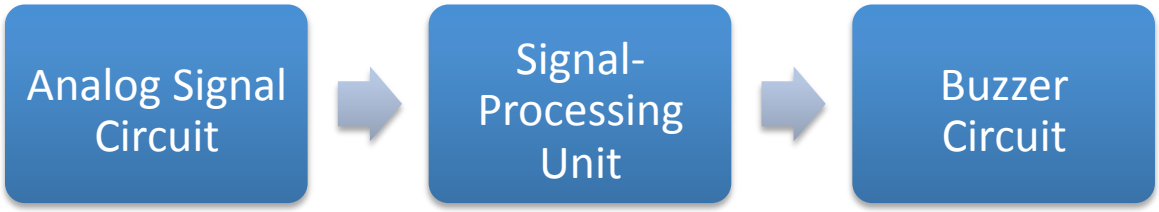


Figure 1.3 Scope of the Device

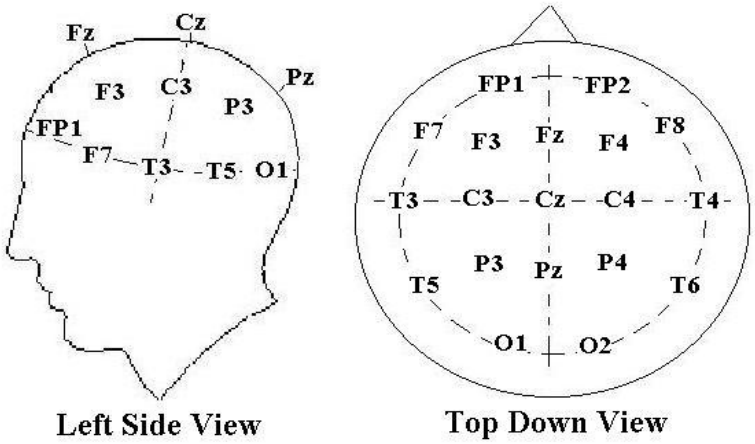


Figure 4.1.1 10-20 system of electrode placement

APPENDIX B: Block Diagrams and Circuit Designs

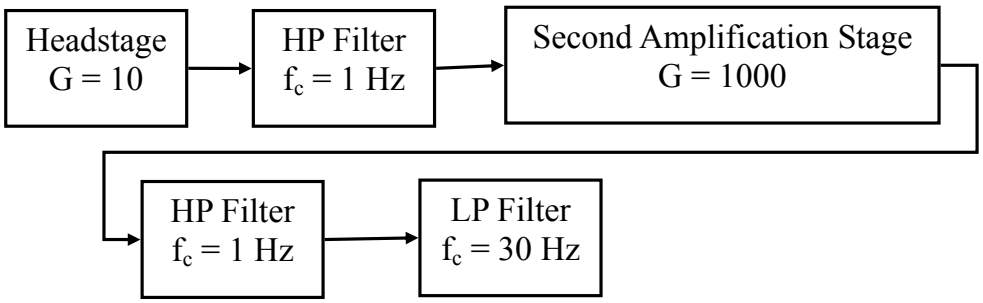


Figure 5.1.1.1 Design Schematic for EEG Circuit

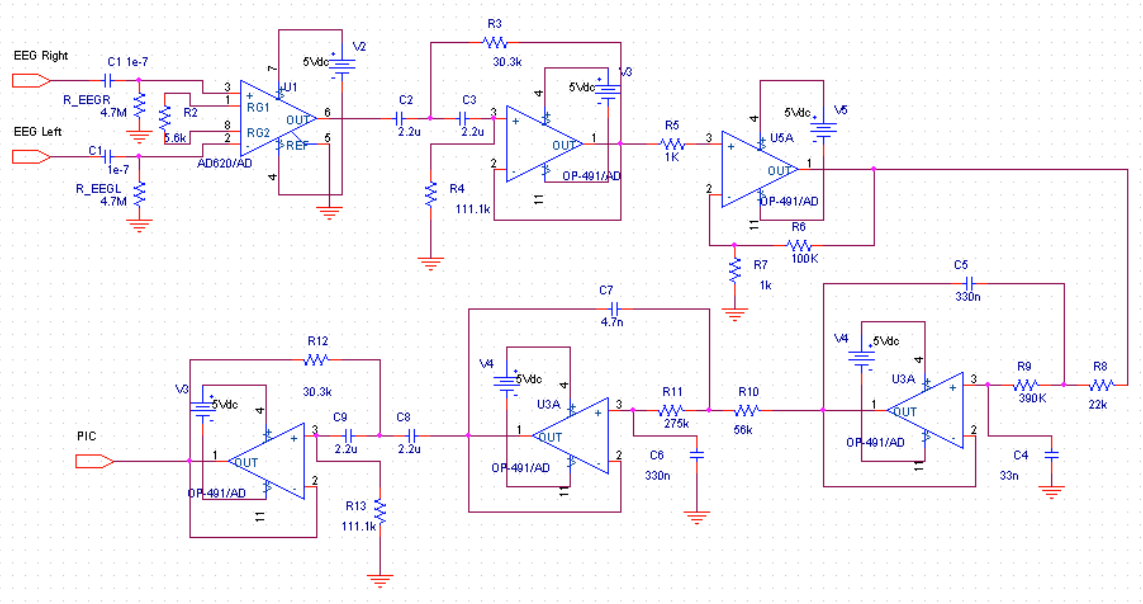


Figure 5.1.1.2 Detailed Schematic for EEG Circuit

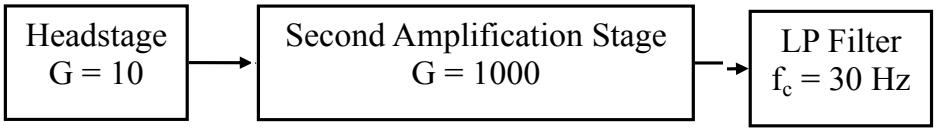


Figure 5.1.2.1 Design Schematic for EEG Circuit

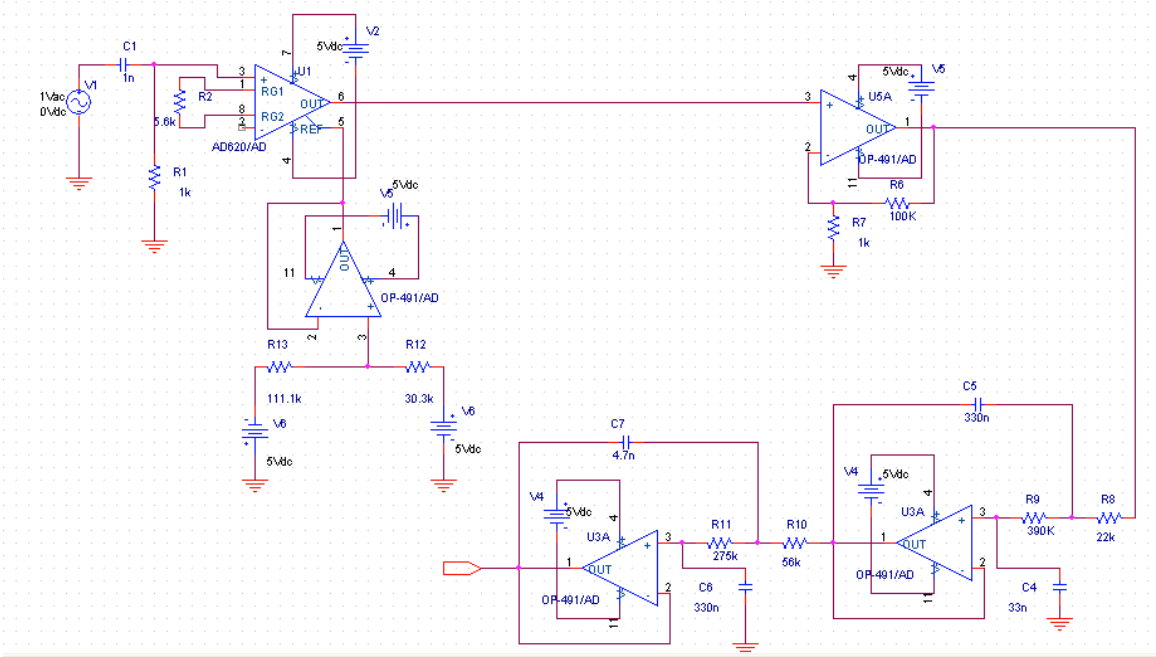


Figure 5.1.2.2 Detailed Schematic for EEG Circuit

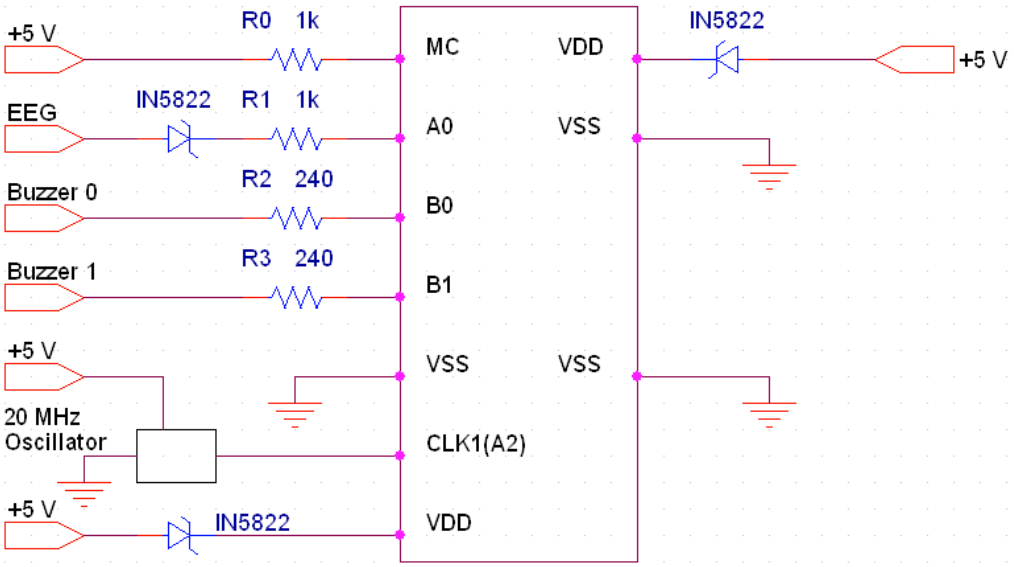


Figure 5.2.1 Detailed Schematic for the PIC

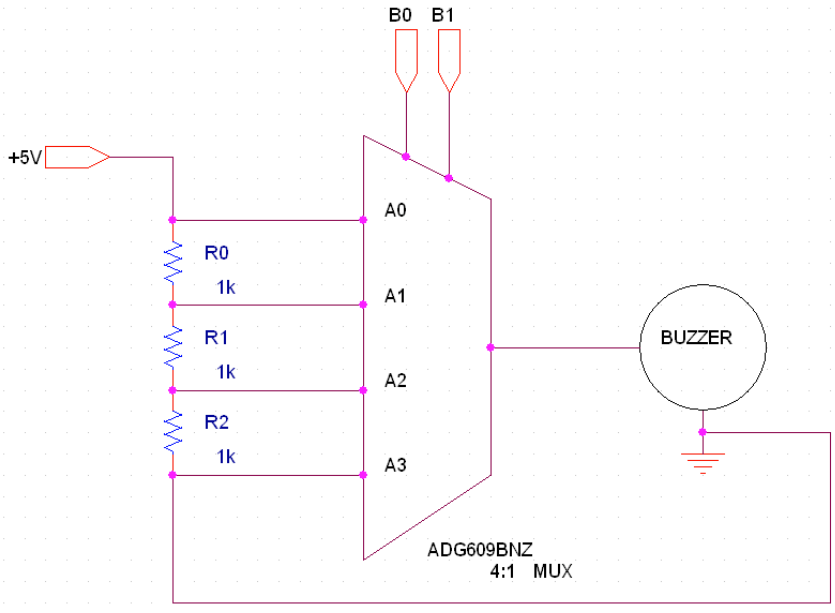
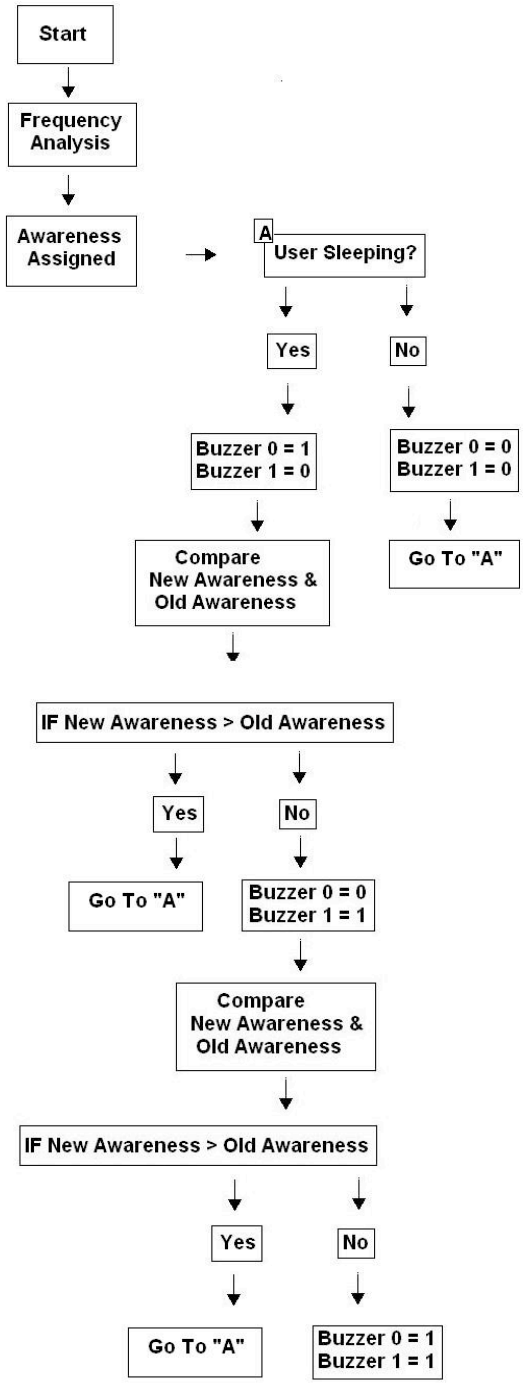


Figure 5.3.1 Detailed Schematic of Buzzer Circuit

APPENDIX C: Flow Chart



APPENDIX D: Results

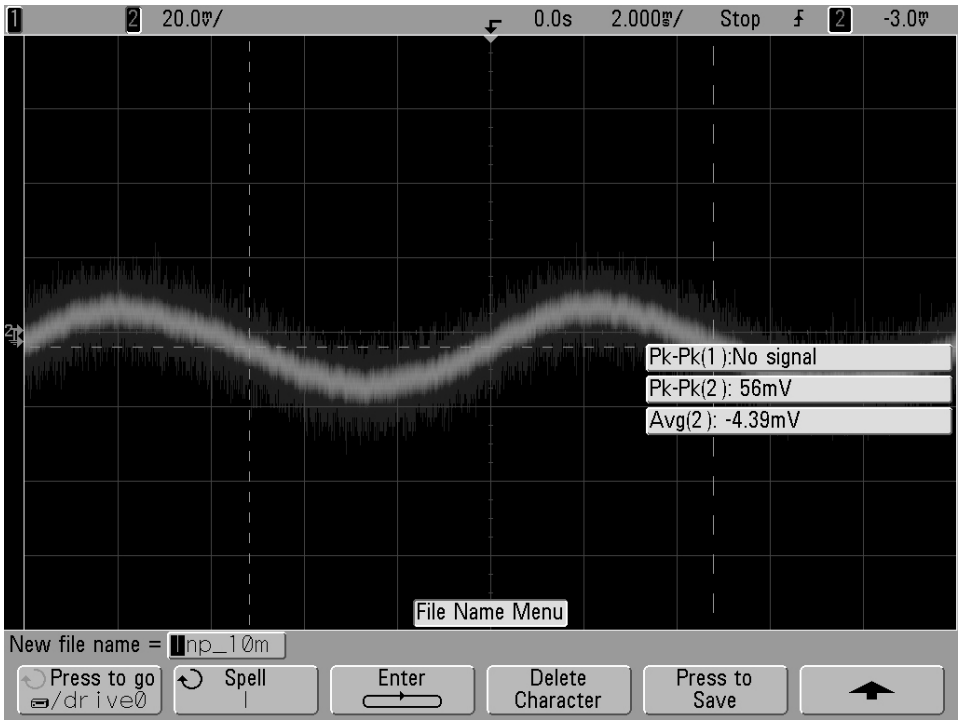


Figure 6.1.1 Input Signal (Function Generator)

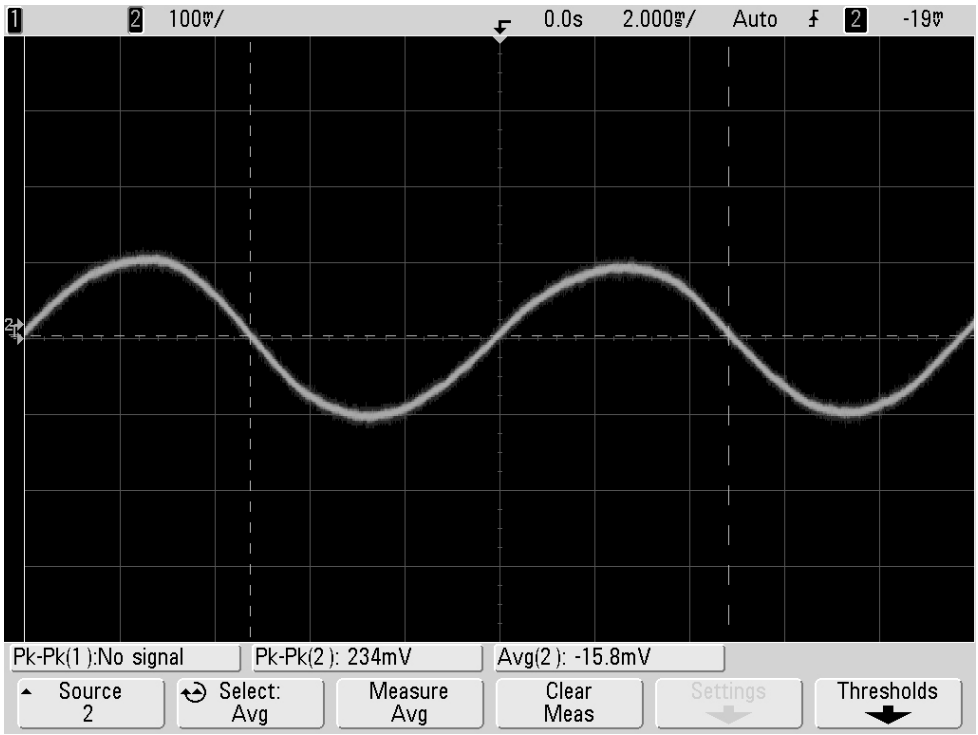


Figure 6.1.2 1st Amplification Stage Gain

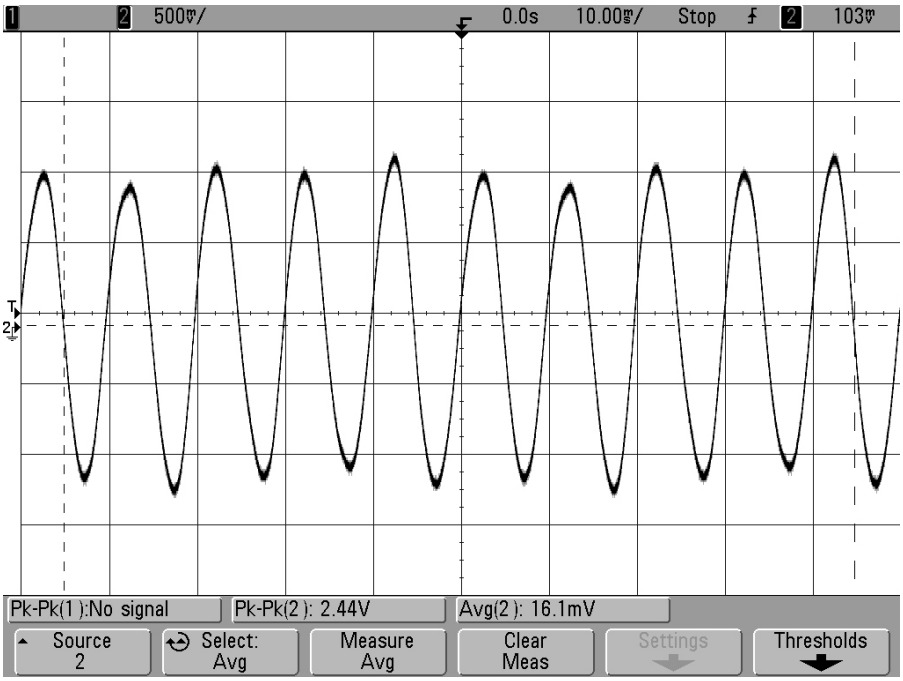


Figure 6.1.3 2nd Amplification Stage Gain

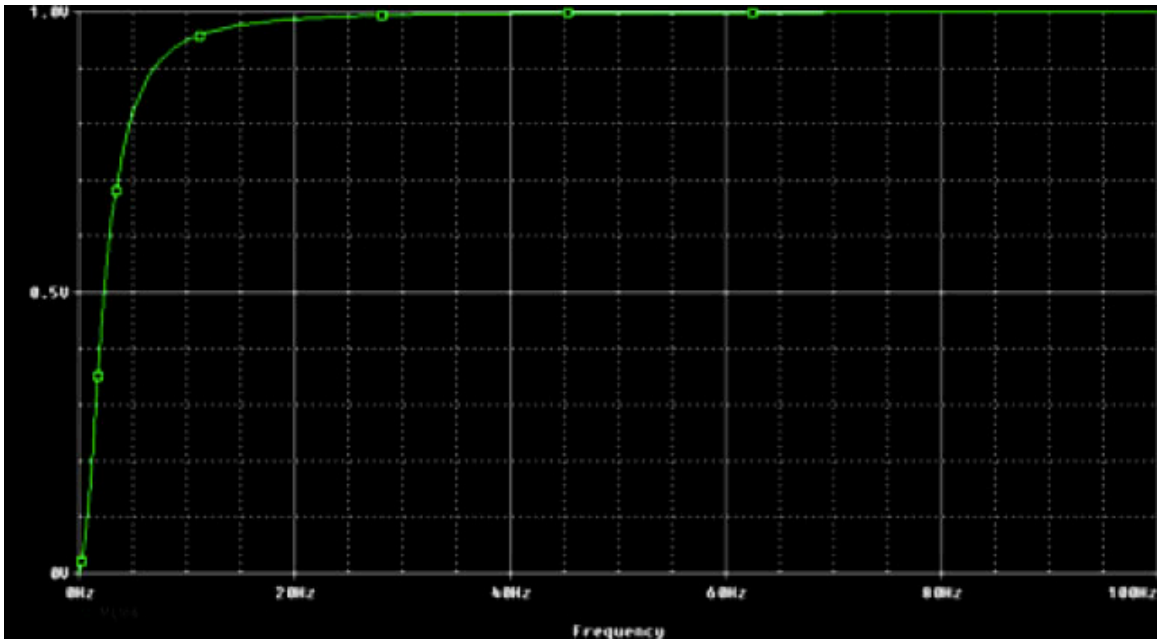


Figure 6.1.4 PSpice Simulation of High Pass Filter, fc=1Hz

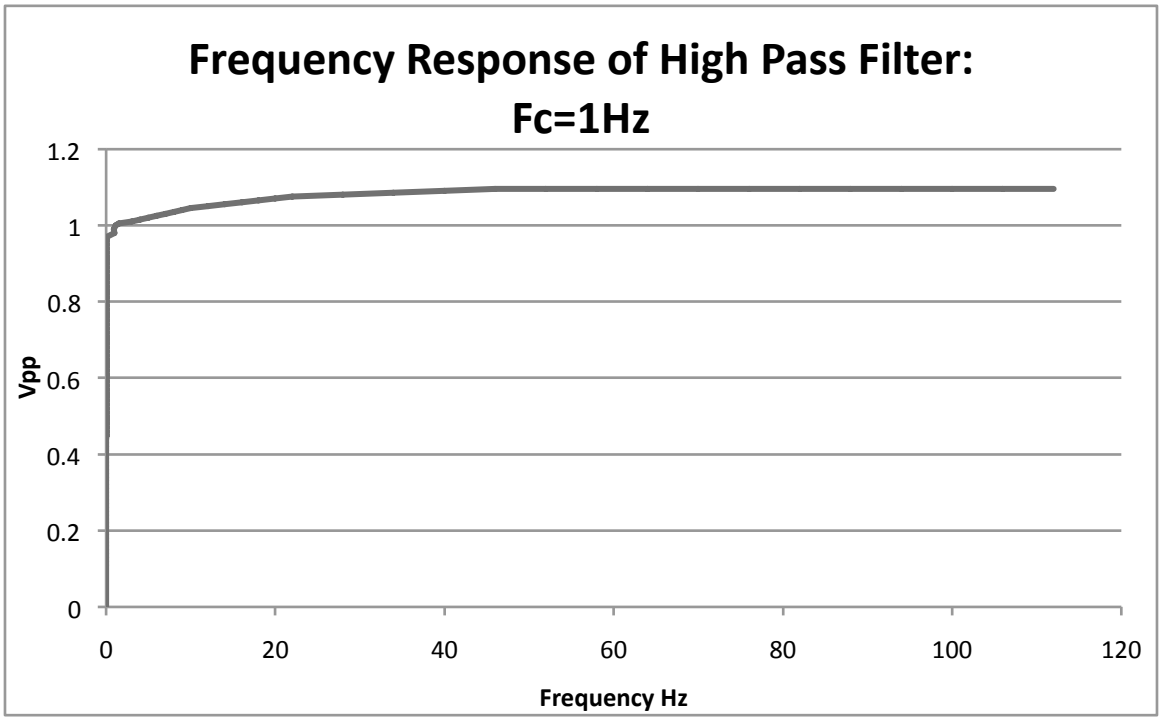


Figure 6.1.5 Frequency Response of High Pass Filter, fc=1Hz

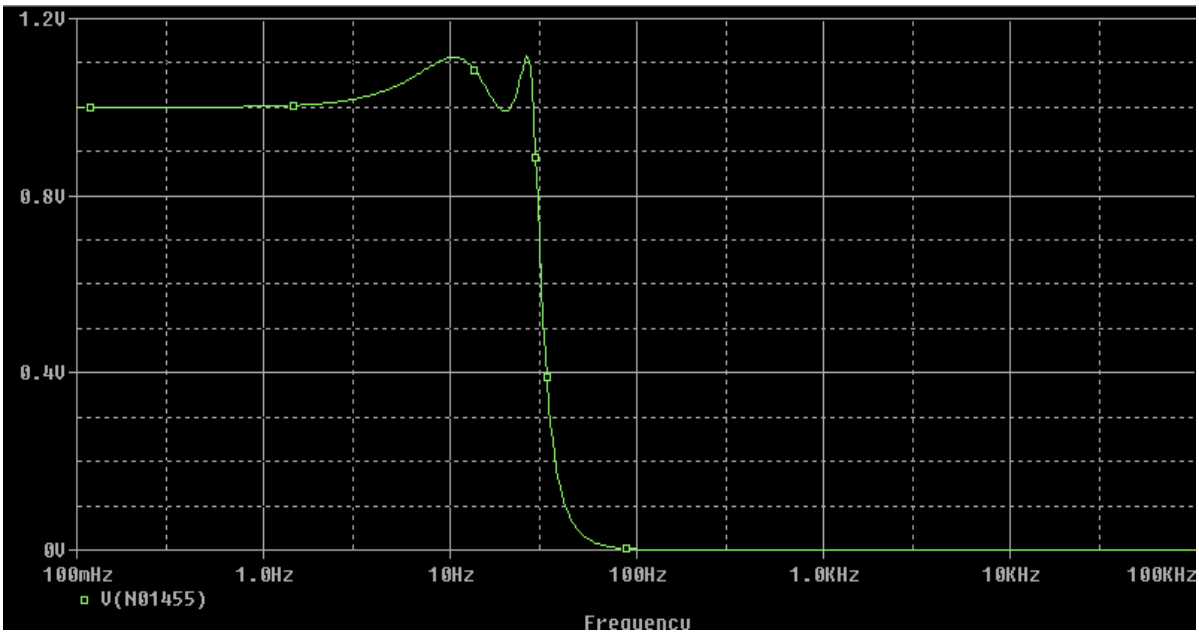


Figure 6.1.6 PSpice Simulation of Low Pass Filter, fc=30Hz

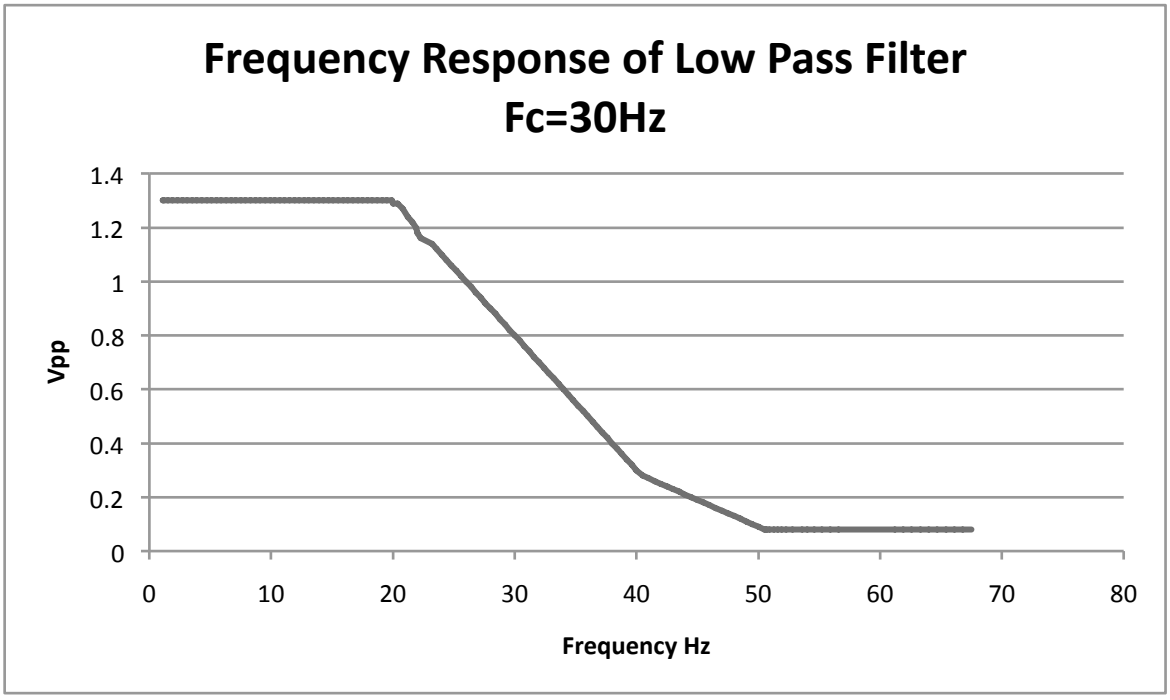


Figure 6.1.7 Frequency Response of Low Pass Filter, fc=30Hz

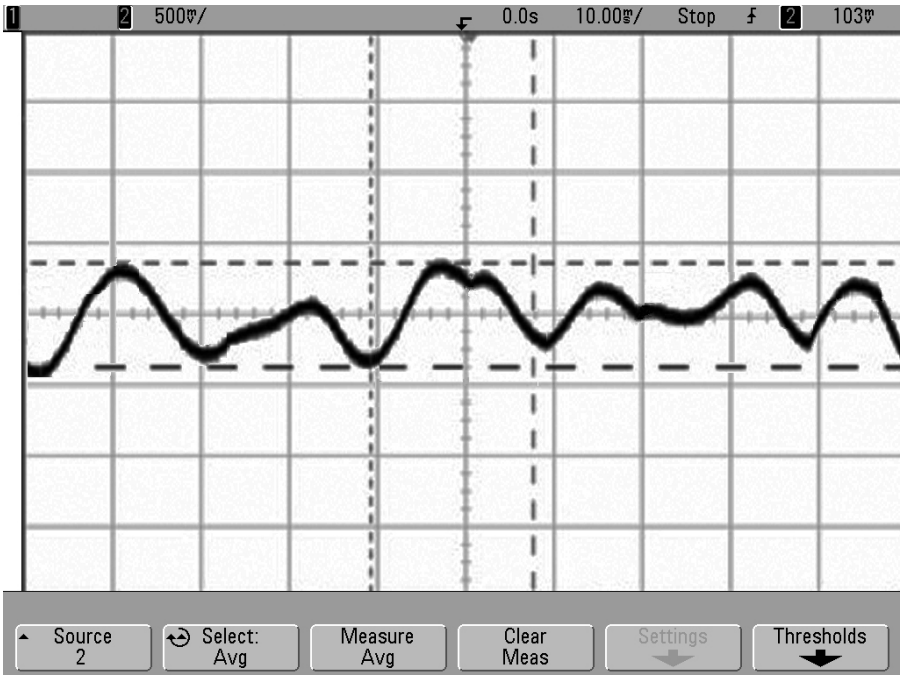


Figure 6.1.8 Output EEG Signal

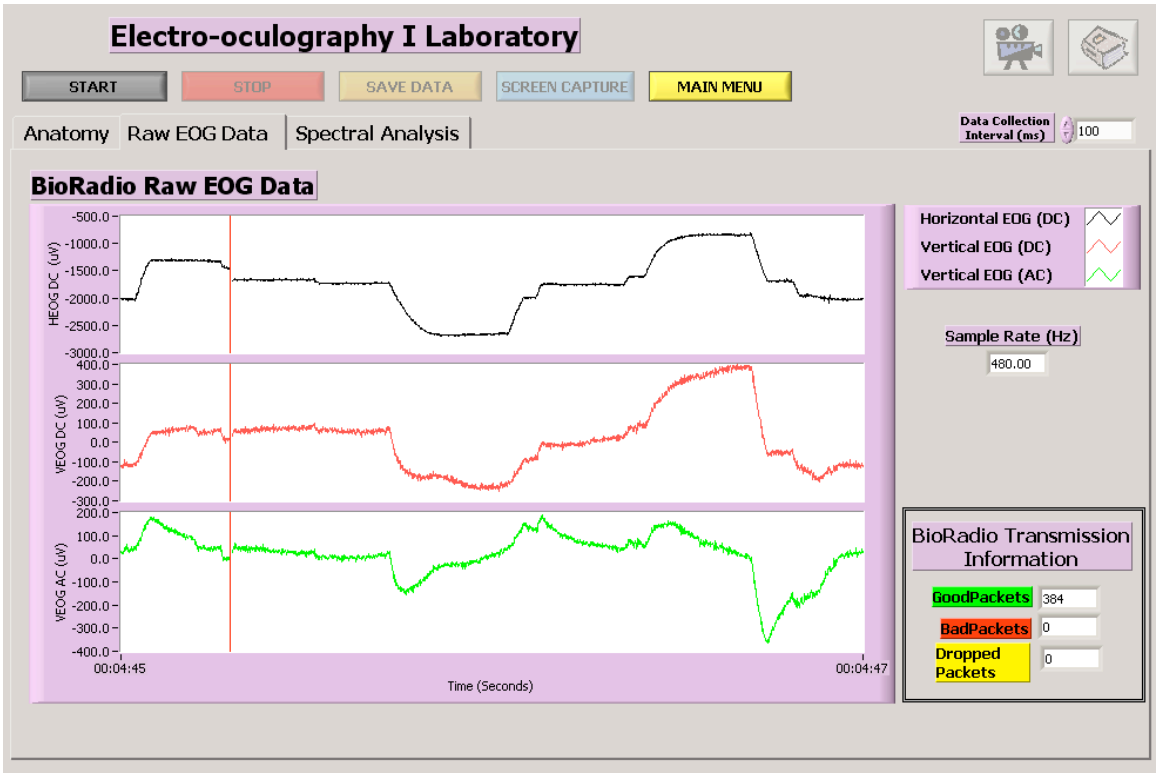


Figure 6.1.9 Output EOG Signal (Left to Right Movement)

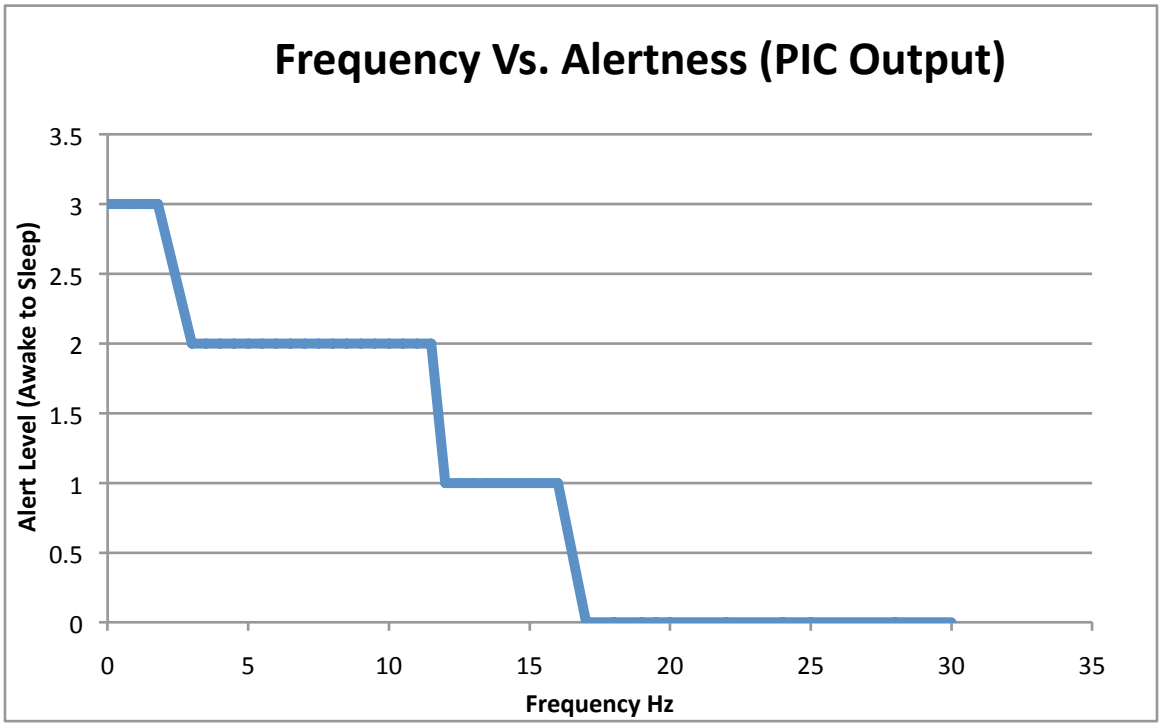


Figure 6.2.1 Frequency Vs. Alert Level

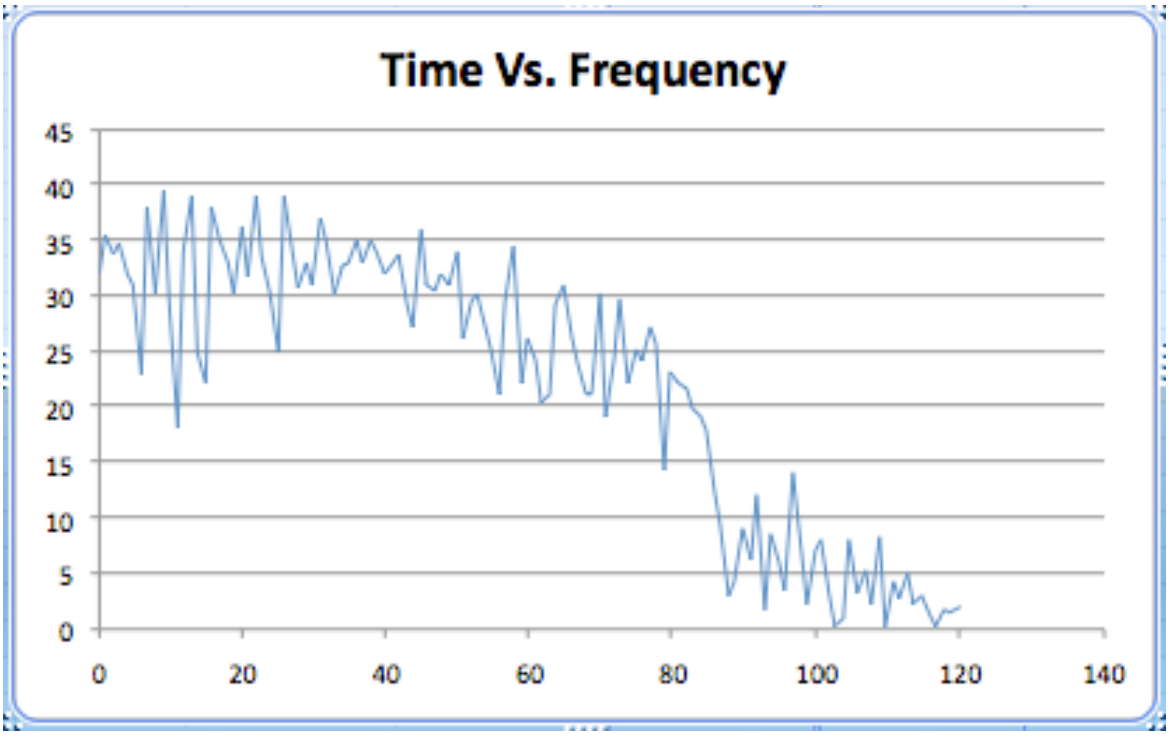


Figure .6.2.2 A Study of Frequency Decrease in the User over Time

APPENDIX E: Pictures

Figure E.1 Electrode Placement with Sleep Detection Glasses

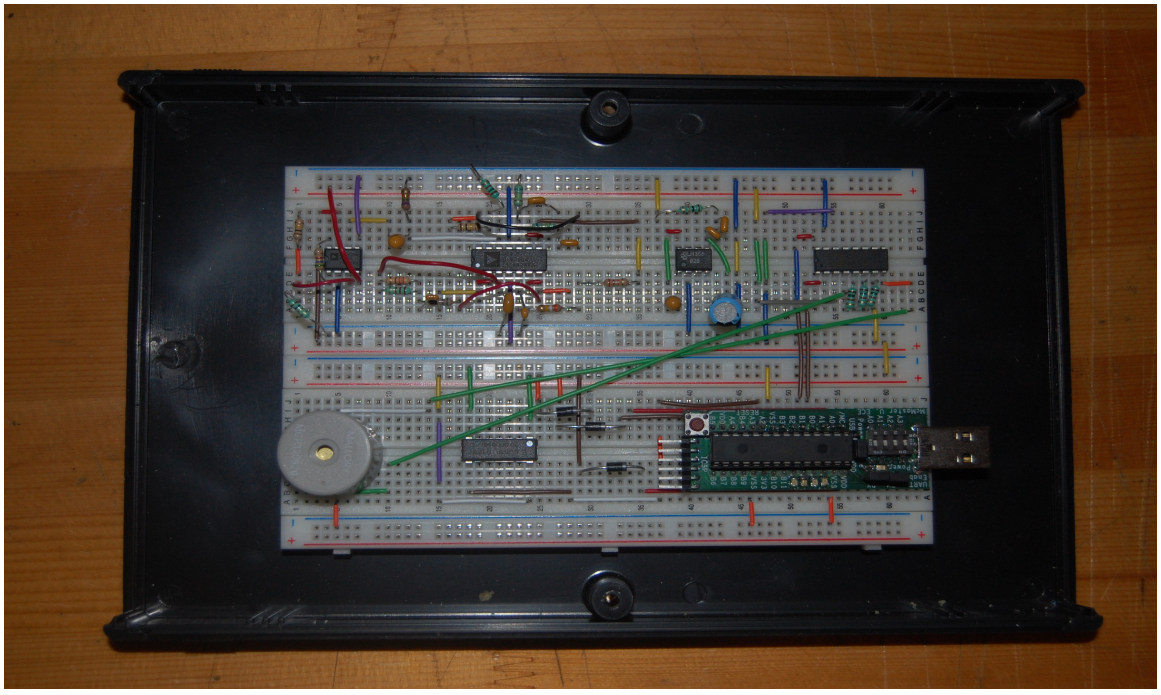


Figure E.2 Overall Circuit Board

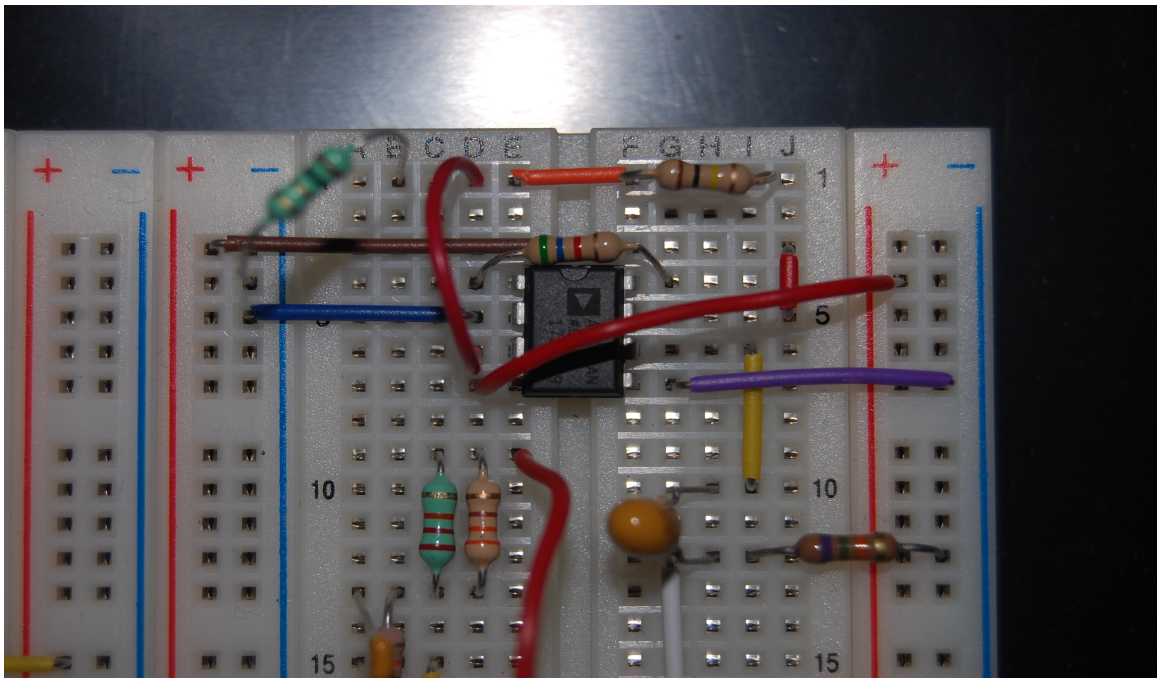


Figure E.3 First Amplification Stage

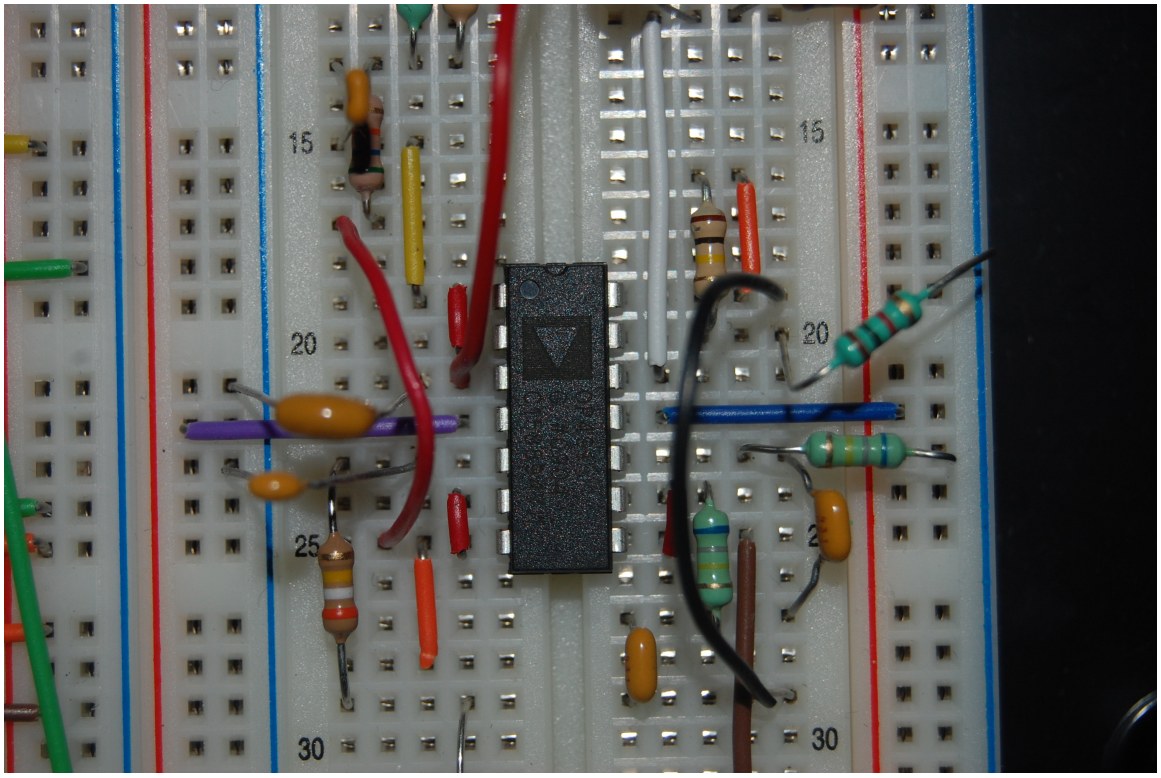


Figure E4. Second Amplification Stage with HP & LP Filters

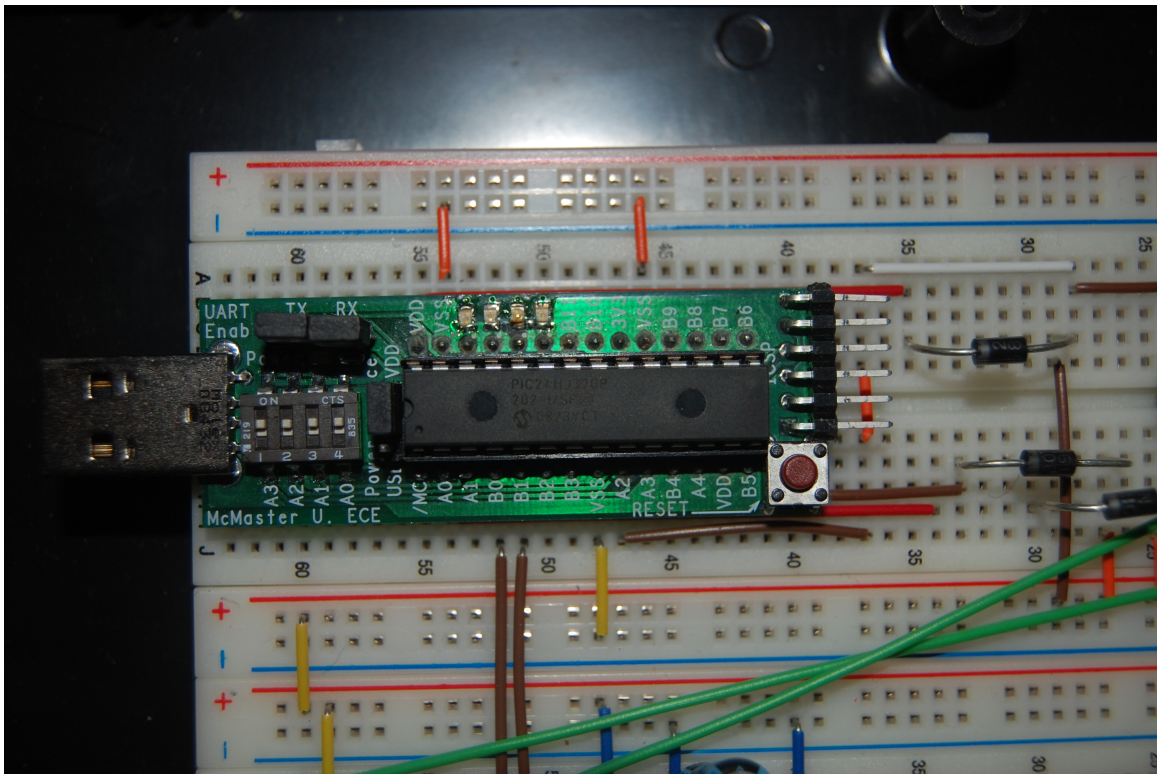


Figure E.6 Microcontroller for Signal Processing Unit

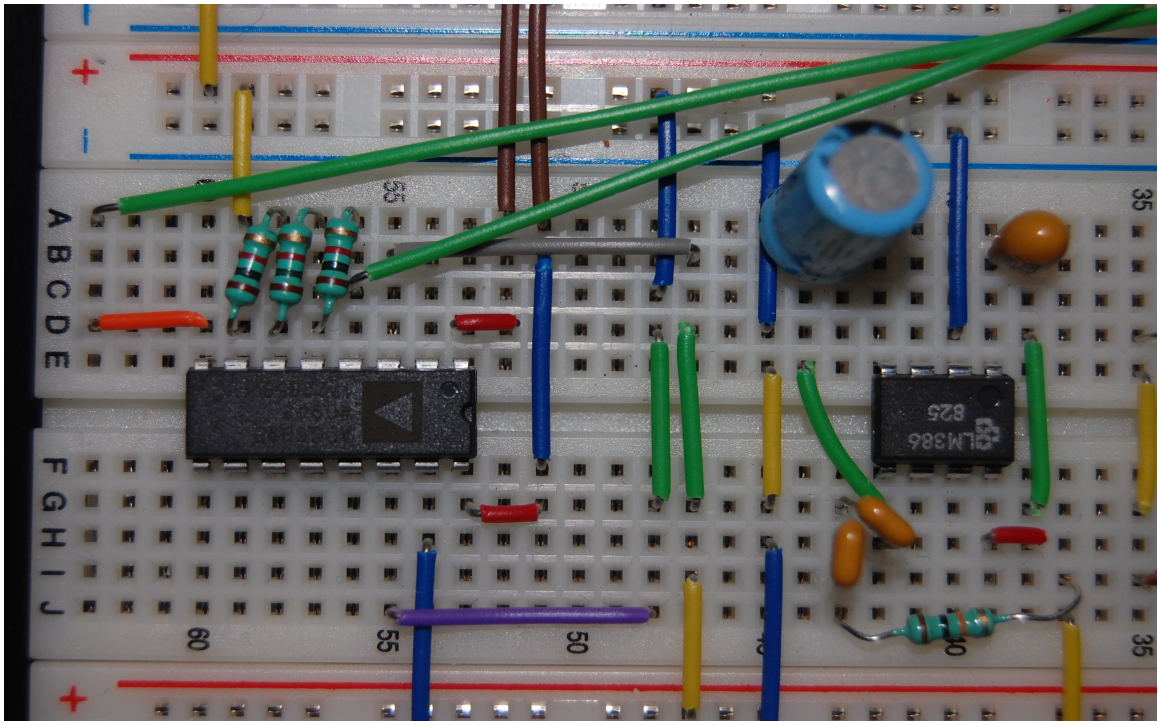


Figure E.7 4:1 Multiplexer for Buzzer Circuit

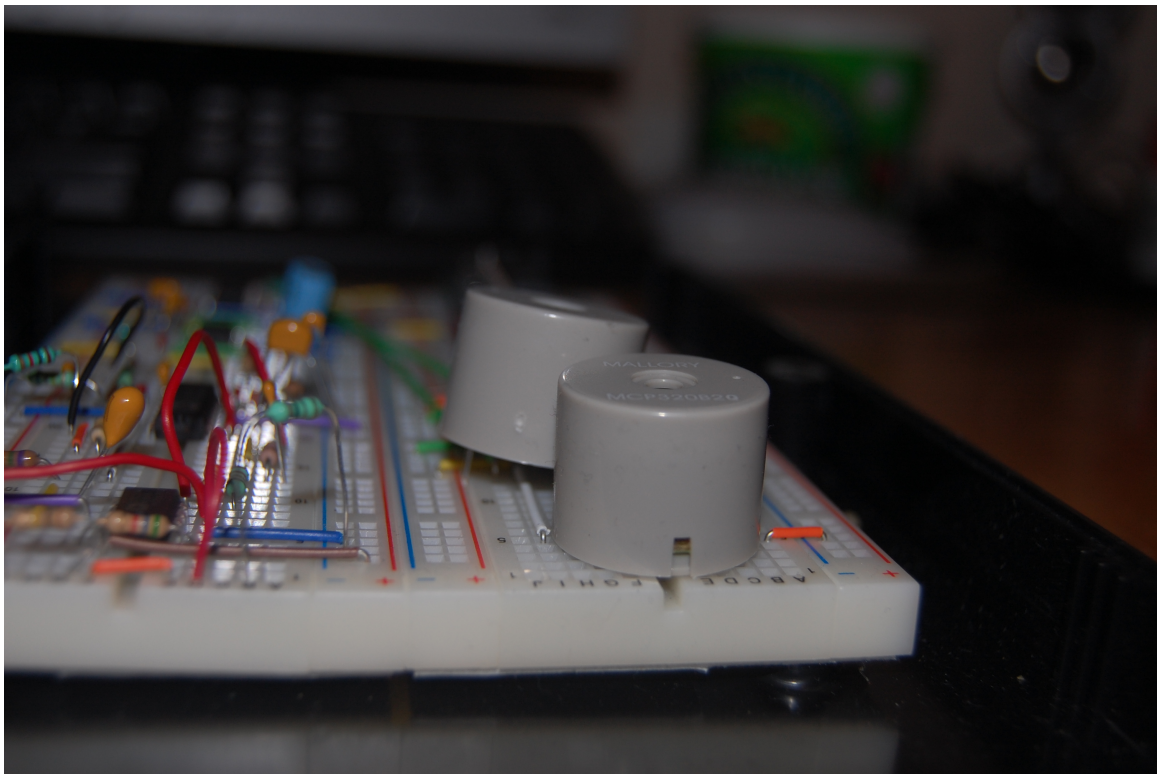


Figure E.8 Buzzers

APPENDIX F: Tables

Rhythm	Typical Frequencies (Hz)	Typical Amplitude (uV)
α	8 - 13	2-100
β	13 - 22	5-10
Δ	0.5 - 4	20-100
θ	4 - 8	10

Table 3.1.1 Different Types of Waves and its Frequency Range

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

Table 5.3.1 Truth Table of AD609 Multiplexer

Frequency	Awake Level	Signal Processing Unit: Output Bit			
		User_Sleep	Buzzer_0	Buzzer_1	Outcome
Greater than 13Hz	Awake (0)	0	0	0	00
8Hz to 13Hz	Less Awake (1)	1	0	1	01
4Hz to 8Hz	Falling Unconscious (2)	1	1	0	10
Less than 4H	Sleep (3)	1	1	1	11

Table 6.2.1. Frequency and Awake Level with Truth Table of SPU

APPENDIX G: Parts & Cost

Part Number	Manufacturer	Description	Unit	Price	Qty	Total
GS26150	BMI	Pre-gelled Disposable EEG Sensor	EEG	$40.00	1	$40.00
AD620BNZ	Analog Devices	Instrumentation Amplifier	Analog Circuit	$2.15	1	$2.15
OP491	Analog Devices	Op-Amp	Analog Circuit	$1.20	2	$2.40
PIC24HJ32GP	Microchip (Mod by IEEE)	Microcontroller	SPU	$35.00	1	$35.00
IN5820	FCI	3.09 Amp Diode	SPU	$1.00	5	$5.00
SG-651	SOJ	Crystal Oscillator	SPU	$3.00	1	$3.00
MCP310	Mallory Sonalert	6VDC Buzzer	Buzzer Circuit	$1.00	2	$2.00
ADG609	Analog Devices	4:1 Multiplexer	Buzzer Circuit	$2.00	1	$2.00
N/A	Shoppers Drug Mart	Glasses	Head Unit	$1.00	1	$1.00
N/A	Sayal Electronics	Breadboard	Circuit	$10.00	2	$20.00
N/A	Sayal Electronics	Project Case	Overall	$40.00	1	$40.00

(Critical Parts Only, resistors and capacitors not included)

APPENDIX H: Signal Processing Unit Program

```
/*
                    FrequencyAnalysis.C

        Frequency of the EEG signal received from the amplifiersvare to be analyzed in this
        section of the program. The core idea is to receive and digitize the EEG signal. When the
        signal is digitized then the freqeuncy analysis algorithm will count the number of times
        the voltage changes from positive to negative. This counting process will occur for
        250ms, and the counter will be divided by 250ms to determine the frequency of the
        signal.Once the frequency has been determined, than an awake level will be
        assigned.This process is repeated continually every 2 seconds. The determined frequency
        will be compared with the previous frequency every 2 seconds to determine whether the
        user's awake level has changed.

        Inputs:

                A1      EEG Signal

        Outputs:

                B0      Buzzer_0

                B1      Buzzer_1

                B2      User_sleep


                                */
include basic header definition
#include "p24HJ32GP202.h"


_CONFIG2 (0xFBFD);
_CONFIG1 (0x377F);
int main(void)
{
        OSCCON      =       0x11C0;
        while(1)
        {
```

```
        }

long value;

#device *=16 ADC=10      // Use 16-bit pointers, use 10-bit ADC
#include "Include\FrequencyAnalysis.h"
// function declarations
void inittimers(void);
void initADC(void);

void main( void)
{
        disable_interrupts(GLOBAL);
        // Variables
        OSCCON = 0x33C0;
        CLKDIV = 0x0000;
        signed int16 NewADC;
        signed int16 OldADC;
        ADCInit ();
        AD1CON1 = 0x80E4;
        AD1CON2 = 0x6000;
        AD1CHS = OldADC;
        AD1PCFGbits.PCFG4=0;
        int16 begin;
        int16 sleep;
        int8 sleepmode_fresh;
        int8 sleepmode_old;
```

```
int16 postoneg;
int16 eeg_f;

// Initialize variable
sleepmode_fresh = zeroposition;
sleepmode_old = zeroposition;
begin = 1;
sleep = 0;
NewADC = 0;
OldADC = 0;
eeg_f = 0;
delay_ms(250);
initADC();

// begining Value of Outputs
output_low(User_sleep);
output_low(Buzzer_1);
output_low(Buzzer_0);

while(FOREVER)
{
        oldADC = read_adc();
        // Analyzing Frequency
        while(time < 250*time_Interval)
        {
                newADC = read_adc();
                if((oldADC == 0) && (newADC>0))
```

```
                Freq_Count++;
                OldADC = NewADC;
                time++;
        }
        eeg_f = (Freq_Count + Freq_Count)/time;
        sleepmode_old = sleepmode_fresh;
        Freq_Count = 0;
        time = 0;

        if (begin == 1)
                sleepmode_fresh = awake;
        else if((eeg_f > Theta_Low || eeg_f <= Theta_Low)&&(eeg_f < theta || eeg_f >=
theta))
                sleepmode_fresh = sleeping;
        else if((eeg_f > delta || eeg_f == delta)&&(eeg_f < alpha || eeg_f >= alpha))
                sleepmode_fresh = loss_cons;
        else if (eeg_f > beta || eeg_f >= beta)
                sleepmode_fresh = awake;
        else
                sleepmode_fresh = zeroposition;
        // final output
        if(begin == 1
                output_low(Buzzer_1);
                output_low(Buzzer_0);
                begin = 0;
                delay_ms(20);
                output_low(User_sleep);
        }
```

```
else if((sleepmode_old == loss_cons)&&(sleepmode_fresh == awake))
        {
                output_low(Buzzer_1);
                output_low(Buzzer_0);
                output_high(User_sleep);
                delay_ms(20);
        }
else if((sleepmode_fresh == sleeping) && (sleepmode_old == loss_cons))
        {
                output_high(User_sleep);
                output_low(Buzzer_1);
                output_high(Buzzer_0);
                delay_ms(1500);
        }
else if((sleepmode_old == sleeping)&&(sleepmode_fresh == sleeping))
                output_high(User_sleep);

                if(sleep == 1)
                        {
                                output_low(Buzzer_0);

                                output_high(Buzzer_1);
                                sleep = 0;
                                delay_ms(1500);
                        }
                else
                        {
                                output_high(Buzzer_1);
```

```
                                output_high(Buzzer_0);
                                delay_ms(1500);
                        }
                output_low(User_sleep);
        }

else if((sleepmode_fresh == awake))
        {
                delay_ms(75);
                output_high(User_sleep);
                output_low(Buzzer_1);
                output_low(Buzzer_0);
                sleep = 1;
                delay_ms(25);
                output_low(User_sleep);
        }
else if((sleepmode_fresh == awake) && (sleepmode_old == awake))
        {
                output_low(User_sleep);
                delay_ms(75);
                output_high(User_sleep);
                output_low(Buzzer_0);
                output_low(Buzzer_1);
                delay_ms(25);
                output_low(User_sleep);
        }
else if((sleepmode_fresh == loss_cons) && (sleepmode_old == sleeping))
```

```
                {
                        output_low(User_sleep);
                        output_low(Buzzer_0);
                        output_high(User_sleep);
                        output_low(Buzzer_1);
                        sleep = 1;
                        delay_ms(25); }
        else
                {
                        output_low(User_sleep);
                        output_low(Buzzer_1);
                        output_low(Buzzer_0);
}
    }
 }
```

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