Evaluation of Active Balancing Algorithms and an Improved Method for a Deployed Active Battery Balancer as Well as Physical Implementation

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By

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A THESIS

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Evaluation of active balancing algorithms and an improved method for a deployed active battery balancer using MATLAB Simulation as well as physical implementation

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Abstract

Lithium-ion cells have been the workhorse for customer products including laptop computers, cell phones and battery energy storage systems that can store energy from renewable energy sources. The internal resistance of them is very low, resulting in a low amount of wasted energy. Performance of Li-Ion cells is wonderful if they treated well. For this reason, an efficient battery management system (BMS) is essential in order to maximize the battery's capacity, battery means a collection of cells wired in series providing a higher voltage. So by using a BMS, SOC (State Of Charge) levels of cells get closer to each other resulting increased life and capacity of a battery. There are active and passive battery balancers. The energy which is extracted from those cells with higher SOC using passive balancer is wasted in heat, so it is not so efficient in terms of wasted energy in comparison with active balancing algorithms. There are different types of active balancing techniques. Cell to cell technique, cell to battery and battery to cell. Among the above mentioned, cell to battery performs well. However, when push-pull converters (which have high performance) are used, flux imbalance phenomenon (which is resulted in a asymmetric hysteresis loop of a magnetic core) is unavoidable. In order to prevent this phenomenon, current mode topology is used. Hence, the transistors won't burn out due to this effect. In this thesis I simulated current mode algorithms with push-pull converters with MATLAB SIMULINK. I also physically designed push-pull converters and built it with help of chips (current mode controllers, optocouplers, transistors, fast recovery diodes, linear and shunt regulators). I did simulate two active balancing methods (Cell to cell and cell to battery) and compared the results. The results that came from cell to battery indicated a better performance in terms of balancing speed. For three cells balancing time reduced from 3570 seconds in cell to cell method to 518 seconds in cell to battery method.

To my mother, who sacrificed for well-being, and to my wife and daughter.

Acknowledgments

I would like to express my sincere gratitude to my supervisor, Dr.T. Kirubarajan, for giving me an opportunity to work on an interesting topic, and for providing continuous guidance, advice, as well as ongoing support. Further, my thanks are due to ECE Department staff, especially Cheryl Gies. I also appreciate Dr Nabavi, my ex-supervisor, and Beiki for their support.

Finally, I would like to thank my family for supporting and encouraging me to pursue this degree.

Abbreviations

HSOC	Highest State Of Charge
LSOC	Lowest State Of Charge
BMS	Battery Management System
ZVS	Zero Voltage Switching
PWM	Pulse Width Modulation
CM	Circular Mills
PFT	Primary Flatted-Topped
R_{On}	ON-Resistance of transistors
T_{On}	ON-Time of transistors
$V_{ce(on)}$	Collector-Emitter ON-Voltage of transistors
L_{pm}	Inductance of primary winding
V_{dc}	Cell voltage

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CHAPTER 1

INTRODUCTION AND PROBLEM STATEMENT

BMS CONCEPTS AND NEED FOR A LI-ION BMS

In industry electric car manufacturers and solar plant manufacturers using storage systems choose more advanced, active balancing systems to shrink every drop of energy from the battery pack.
The Battery pack is one of the high-priced and least trustworthy components of the electric vehicles and solar systems. Eminently performed Battery Management System (BMS) is a solution to cover the vulnerability and proneness of battery packs which are being used in EV and solar systems.

In a battery containing series cells, there is much chance that overall voltage of battery is not equally divided between its cells. The best manufactured cells with equal initial capacity have inherently different parameters when released from manufacturing line. Hence, the cells will be unbalanced, and one of them will be the first fully charged cell and then overcharged. Different in amount of charge is known as capacity mismatch. Lithium Ion cells when charged, they are not able to take more current and instead, their voltage increases dramatically to dangerous levels, danger of thermal runway. Unequal aging of cells is major reason of temperature gradients in a battery pack. Thermal management is expensive and highly important.

Total voltage of whole battery pack will be kept at desired while one cell is overcharged; other cells are not fully charged. Hence, charger system will rely on total battery voltage giving a false sense of safety [1]. Battery pack manufacturers put their effort to screen and choose the cells for best match before putting them in a battery pack. Excess cost is applied due to the time required for testing. After a long term due to cells aging, they lose much more capacity and their parameters differ.
A BMS (Battery Management System) monitor such a battery and balance its cells to maximize whole capacity of battery and prevents any cell of being overcharged.

A BMS takes care of a battery and do the followings [1]:

1. Monitor the battery
2. Protect the battery
3. Estimate SOC of the battery
4. Improve the performance

Imbalance resulted from variations during battery manufacturing, variation in internal impedance, and difference in self-discharge rate.

Due to internal leakage and different capacity of cells, a battery is more likely to become unbalanced [1]. Imagine that all cells start at 100% SOC, over time and due to internal leakage, SOC of cells will change finally. Practically, when a battery is manufactured, cells start more unbalanced over time due to capacity and internal leakage [1].

With cells in series, charging ability is restricted to the first cell which is fully charged and while discharging, current drawing ability is restricted to the first cell that is fully discharged. These two points are about to determine a battery capacity including series cells [1]. To clarify more there are two variables defining capacity of a battery SOC% and DOD%.

SOC% is present battery capacity as percentage of maximum capacity and DOD% is percentage of a battery capacity which has been discharged.

A cell to battery balancer can transfer excess charge from a cell or multiple cells with highest state of charge to the whole battery pack (all cells in series). So the cells with lowest state of charge get charged and all cells get balanced, same level of state of charge.

In order to transfer charge from cell to battery, boost converters are required. As number of cells increases, output power of boost converters should increase in order to provide a proper charge for the whole pack. For example if we have 20 cells with voltage of 3.7 volts and capacity of 2200 mAh and whole pack wants to be charged with charge rate 2.2 Ah, the required output power for each step-up converter is calculated as below formula:

$$P_{Output} = (20 cells).(3.7 Volts).(2.2 Ampere) = 162.8 Watts$$

For powers more than 100 watts, especially for a solar plant, and hybrid cars, push-pull topology should be used inevitably [4]. The problem associated with this topology is flux imbalance. Difference in resistance of primary windings even for low amount, difference

in Ron (On-Resistance) of transistors and finally unequal volt-second product on both halves of transformer primary, as well as storage time are causes of flux imbalance. Longer storage time will result in longer volt-second. Hence, thermal runway condition happens [4] that brings about a core to be driven into deep saturation and finally destroying power transistors.

Current mode topology rather and voltage mode topology should be used to prevent this phenomenon. A PWM voltage mode controller changes the pulse width to keep the output voltage at desired level and has no control in peak current of transistors for each cycle. In a PWM current mode controller, the peak currents of two transistors on each cycle are measured and based on that, desired pulse width for gate of transistors is provided. So, regardless of differences in resistance of half primary windings, and Ron of transistors, the circuit smoothly works without any flux imbalance by having the equal peak currents drawn of transistors. Cell to battery balancer is very efficient topology because the rectifiers are at high voltage side and switches are at low voltage side bringing about low switching loss, so there is no need using ZVS. Low voltage transistors will be used. Circuit can be simple and trusted especially for distributed BMSs.

MOTIVATION AND THESIS OUTLINES

DC-DC converters are utilized in cell to battery balancer (boost), and battery to cell balancer (buck).

Opposite to battery to cell balancer, cell to battery balancers have best performance [1]. Rectifiers are more efficient, because they are at high voltage side. Low voltage transistors are utilized because they are at cell side. Hence, switching loss is low. There is no need using ZVS (Zero voltage Switching) opposite to battery to cell balancers. The issue associated with boost converters using push-pull topology is magnetic flux imbalance problem [3] so transformer core operates asymmetrically about the hysteresis loop. The consequence is the core moves up toward saturation and one transistor draws more current during on time than does the opposite transistor [4].

Difference resistance of windings in same side (primary or secondary) of multi winding transformer or difference resistance between the on-time resistances of transistors causes this phenomenon.

This phenomenon brings about to destroy the transistor with higher current over time.

A push pull converter continues to operate for a short while with certain amount of flux imbalance without quickly saturating its core. But finally it destroys the transistors.

A current mode topology is used to control peak current in each transistor on pulse by pulse basis and makes equal current peak amplitudes. Consequently, current amplitudes of transistors become equal and prevent them from burning out [4]. This method is a valuable contribution to the possible topologies.

In this thesis a cell to battery balancer (boost converter) with current mode topology has been simulated using MATLAB SIMULINK and physical implementation for three cells has been implemented and tested. Also, cell to cell balancer using single inductance has been simulated. Response time of these two techniques will be compared to each other.

CHAPTER 2

OVERVIEW OF ACTIVE BALANCING METHODS

2.0 Cell Balancing Methods

Balancing can be [1] [2] [3].

- Passive
- Active

In passive balancing, excess energy is removed from cells which have been charged more than others and wasted in heat. Disadvantage is costly wasted energy [1].

In active balancing, energy is transferred from cells with higher SOC to cells with lower SOC. Advantage of using this method is to prevent energy from wasting in form of heat. Disadvantage is more elements are required in the structure.

Active balancing techniques are categorized to four groups [1]:

1. Cell to cell: energy is transferred between neighboring cells.
2. Cell to battery: energy is removed from cells with highest SOC and dumped to the whole battery.
3. Battery to cell: Energy is removed from the battery pack and transferred to the cells with least SOC.
4. Bidirectional: Based on needs, energy is transferred from cell to battery or vice versa.

Cell to cell is appropriate for little scaled batteries [1].

Cell to battery has the most eminent efficiency [1].

2.1 Cell to cell balancing

2.1.1 Capacitor Base

Single Switched Capacitor

Capacitive cell balancing is intuitive. In this method just one capacitor and 2 n switches are utilized [2] [5] [6]. The controller finds the cells with highest and lowest SOC, and their corresponding switches [3] [2]. Figure 1 depicts the operation of the method.

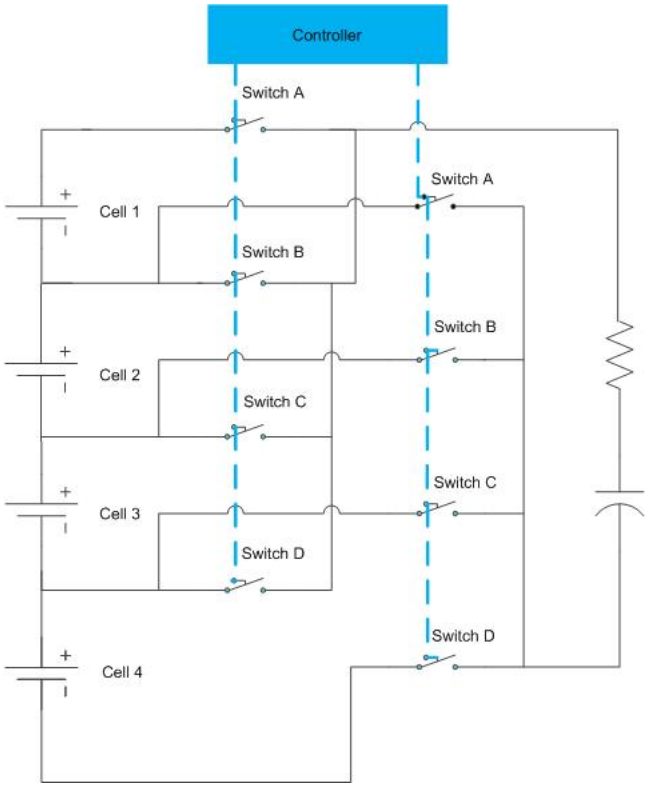

Figure 1. Single Switched Capacitor

Energy is shuttled from higher SOC cell to the capacitor with a constant RC. And then energy is transferred from capacitor to the lower SOC cell. This operation keeps carrying on until all cells are balanced. Disadvantages are that a smart controller for fast equalization is required [2] [3] and modular design capability is poor [2].

Equation can be shown as below:

$V_b(t) = RI_c(t) + Vc(t)$, where V_b is battery voltage at time step t, and V_c is capacitor voltage at time step t. Initial value of capacitor voltage and capacitor current history defines the final value of capacitor after the capacitor charging current stopped.

Thermistors are distributed equally among the cells to monitor cell temperature.

$$V_b(t) = RI_c(t) + \frac{1}{C}\int_{t0}^{t} I_c(\tau)d\tau + V_c(t_{0^-}) \quad (1).$$

Lap lace transform is used to derive the induced current.

$$\frac{V_b(s)C}{S} = RCI_C(s) + \frac{1}{S}I_C(s) + \frac{V_C(s_{0^-})C}{S} \quad (2).$$

$$V_b(s)C = RCI_C(s) + I_C(s) + V_c(s_{0^-})C$$

$$I_c(s) = \frac{C[V_b(s) - V_c(s_{0^-})]}{1 + RC}$$

$$I_C(t) = \frac{[V_b(t) - V_C(t_{0^-})]}{R}e^{\frac{-t}{RC}}, so\ V_C(t) = \frac{1}{C}\int I_C + V_C(t_0)$$

Balancing theory described as below:

1- Circuit should be in no load condition
2- Switching frequency is calculated based on RC time constant
3- Two cells with max and min voltage are selected
4- If $SOC_{\max.} - SOC_{\min.} > 0.01$, balancing circuit is activated
5- Switches associated with $V_{\max.}$ are selected if $V_{\max.} > V_C$ (Capacitor gets charged), otherwise switches associated with $V_{\min.}$ are selected ($V_{\min.}$ gets charged by capacitor)
6- If battery temperature or voltage is outside of safe operating area, balancing circuit gets deactivated
7- Balancing continuous until cells are balanced

Switched Capacitors

As it is shown in figure 2, in order to balance n cells, 2n switches and n-1 capacitors are used [7] [8] [2] [3]. When capacitor connected to the higher voltage cell, energy flows from the cell to the capacitor. When connected to the lower voltage cell, energy moves from capacitor to the cell. Either zero resistance relays (for energy efficiency) or MOSFETS can be used [1]. However if zero-resistance relays are used, inrush current when first connects, is high. Furthermore energy efficiency will never be over %50 [1]. Hence, none zero resistances are part in cell, switch, and capacitor which are in series [1]. Initial inrush current is obtained by voltage difference between cell and capacitor divided by these resistances [1].

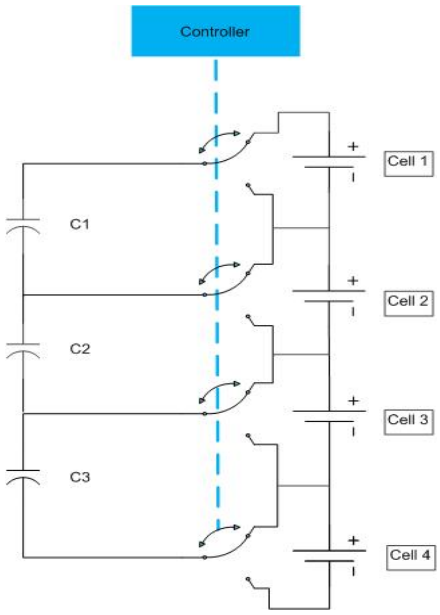

Figure 2. Switched Capacitors

Modular design capability is easy [2] and equalization rate is low [3].

2.1.2 Inductor Base

Single Inductor / Multi Inductors

This method is simple. Just one inductor takes care of balancing whole pack including all cells [2]. Figure 3 shows the topology [2] [9] [10] [11]. Switching duty cycle is 50% [1]. Controller

selects the most charged and least charged cells. [1] [2] [3].Then, energy is shuttled from higher SOC cell to the inductance in half cycle, and then next half cycle, energy is transferred from inductor to the lower SOC cell [1] [2] [3]. 50% duty cycle brings about an equalization of two cells voltage [1]. For example if cell1 has highest SOC and cell3 has the lowest SOC, SW1 and SW2 will be on at first half cycle, then second half cycle SW4 and SW7 will be on. Opposite to the capacitive base method, this topology doesn't have inrush current due to presence of inductor [1]. Another problem arises that is adjacent transistors will possibly be burned out due to voltage spike that happens when connection between adjacent cells is open or loose [1]. That means this tremendous amount of current caused by huge voltage will pass through the transistor, Figure 4.

As an illustration, if there are 100 cells with voltages of 3.6v and there is a loose connection between adjacent cells, 360v will drop across the switch and if on-resistance of switch is 0.2 Ω and resistance of inductor is 0.3 Ω, when the switch is on, 720 A will pass through it, causing it to be destroyed, Fig 4.

In multi inductors, n-1 inductors are used to balance n cells [3]. A pulse width controller is utilized. This topology takes long time to balance all cells compared to single-based inductor technique [3]. In both techniques, capacitive filters are required for high switching frequency [3].

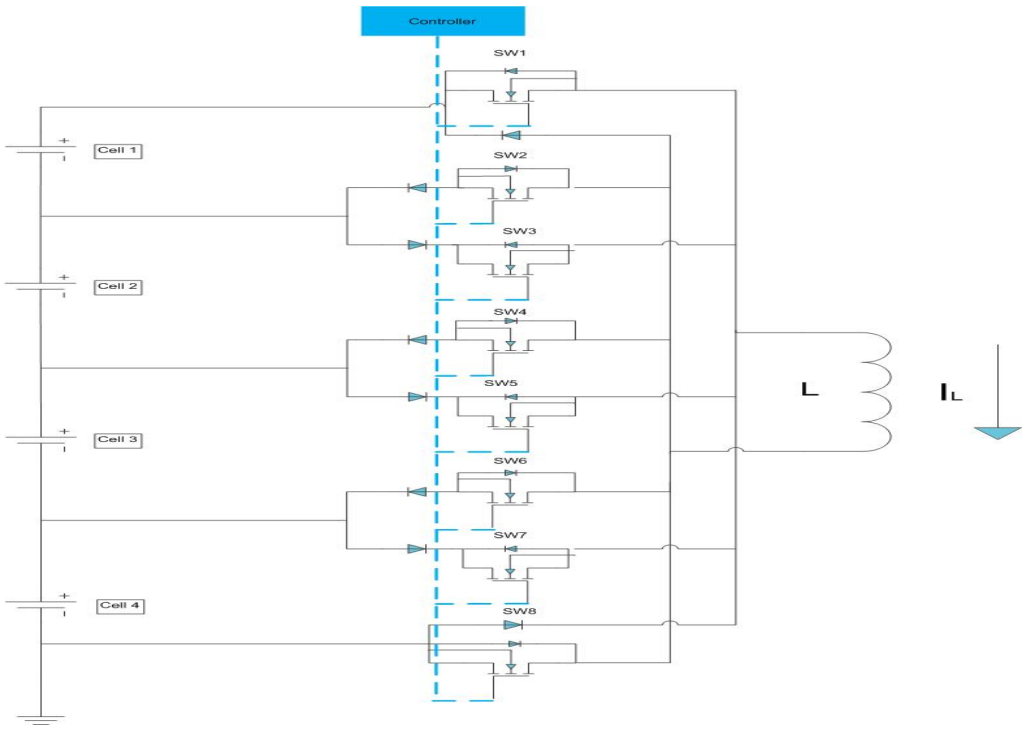

Figure 3. Single Inductor

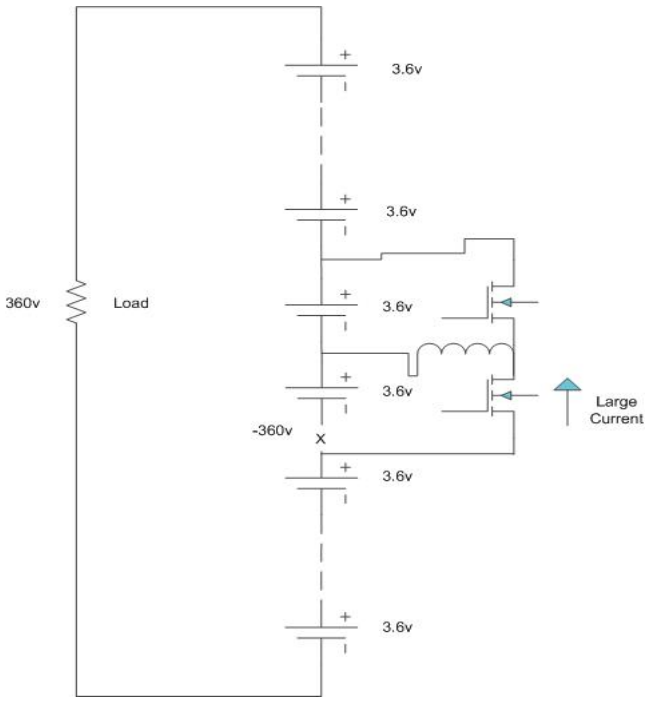

Figure 4. Open Connection in Single Inductor

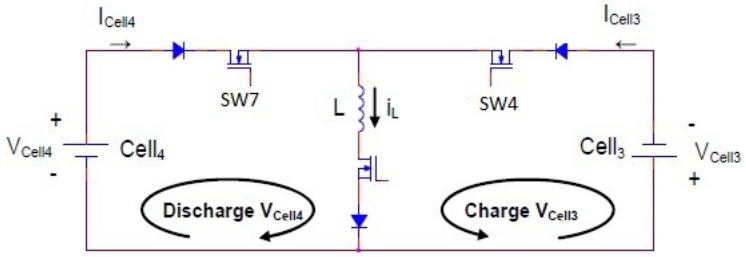

Figure 5. Equivalent circuit indicating
energy transfers between Cell4 and Cell3 [21].

As an illustration with two adjacent cells, if cell 4 has the highest SOC and cell 3 has the lowest SOC, during the charge, current directions are shown in figure 5.

Amount of the energy which is transferred from cell 4 to the L is:

$$V_L = V_{Cell4} = L\frac{dI_L}{dt}, so, I_L = \frac{1}{L}\int_0^{t_{on}} V_{Cell4}\,dt = \frac{V_{Cell4}}{L}t_{on} \quad (3).$$

$$Q_{cell4} = \frac{1}{2}LI_L^{\,2} = \frac{1}{2}\frac{t_{on}^{\,2}V_{Cell4}^{\,2}}{L} \quad (4).$$

During $t_{off} = 1 - t_{on}$, energy is transferred from L to cell 3, causing the cell 3 to be charged.

This amount of energy is $Q_{Cell3} = Q_{cell4} = \frac{1}{2}\frac{V_{Cell4}^{\ 2}}{L}\ t_{on}^{\ 2}$ (5).

2.1.3 Transformer Base

Figure 6 indicates a multiple transformer topology [2] [5] [12] [13] [14]. In normal condition, point A and B are connected.

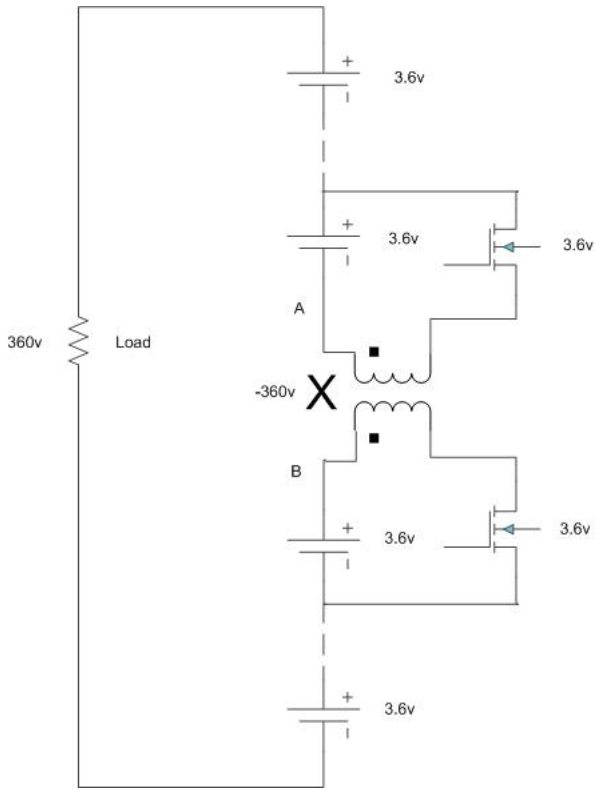

Figure 6. Multi Transformer Topology

A transformer-based cell to cell balancer is complicated and is not as efficient as an inductive balancer [1]. However, in case of loose or open connection between neighboring cells, there won't be a tremendous amount of current caused due to huge voltage across the switches [1]. Just cell voltage (3.6v) will drop across the switch, not 360v for 100 cells, Fig 6. Figure 7 shows a charge equalization converter with reduced

number of windings causing loss reduction [22]. Charge equalization has three operation cases. First case, current is transferred by buck-boost operation between odd-numbered cells and their next cells; fig 8 indicates the flow path.

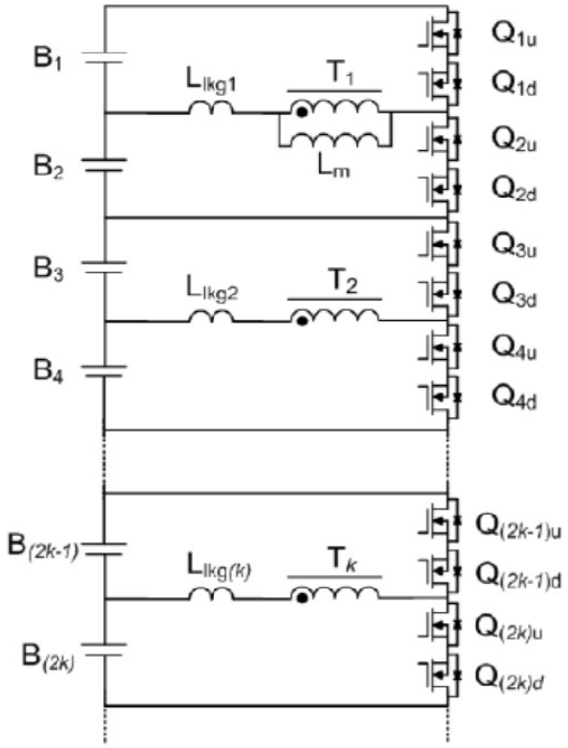

Figure 7. Charge equalization converter [22]

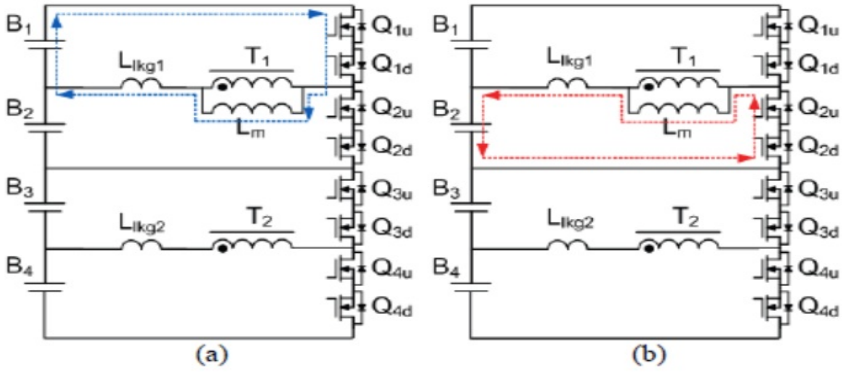

Figure 8. Case1- Current path of case 1. (a) Mode 1: discharging B1. (b) Mode 2:Charging B2. [22]

In mode1 (a), B1 is discharged during on time, when Q_{1u} is turned off, mode 2 (b), starts and the energy stored in L_m Lm and L_{lkg} is transferred to B2.

$$E_{B2,charge} = E_{B1,discharge} = \frac{1}{2}\frac{V_{B1}}{L_m + L_{lkg1}}(t_{on})^2 [22] \quad (6).$$

In case2, the current is transferred by fly back operation between odd-numbered cells and even-numbered cells which are not adjacent [22]. Figure 9 shows case2.

Current is transformed by fly back operation and T1 and T2 are operated as fly back transformer. In mode1 (a), energy is stored in L_m from B1, and in mode 2(b), Q_{1u} is off and energy stored in L_m is transferred to B4 through T1:T2 [22].

In case3 charge is transferred by buck-boost and fly back operation [22].

In mode1 (a), figure10, B1 is discharged and energy is stored in L_m by buck-boost operation. In mode2 (b), B2 is charged and energy from L_m is transferred to B2. In mode3 (c), B2 is discharged through fly back transformer T1, and in mode4 (d), energy is stored in B3 through fly back transformer T1:T2 [22].

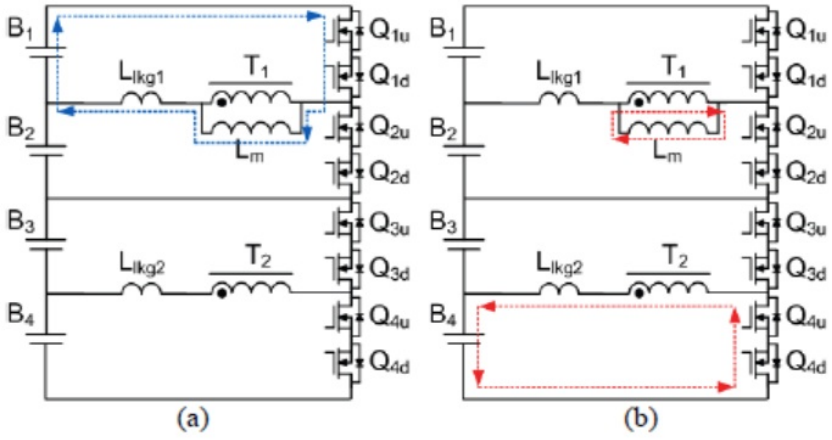

Figure 9. Current path of case 2. (a) Mode 1: discharging B1. (b) Mode 2: Charging B4 [22].

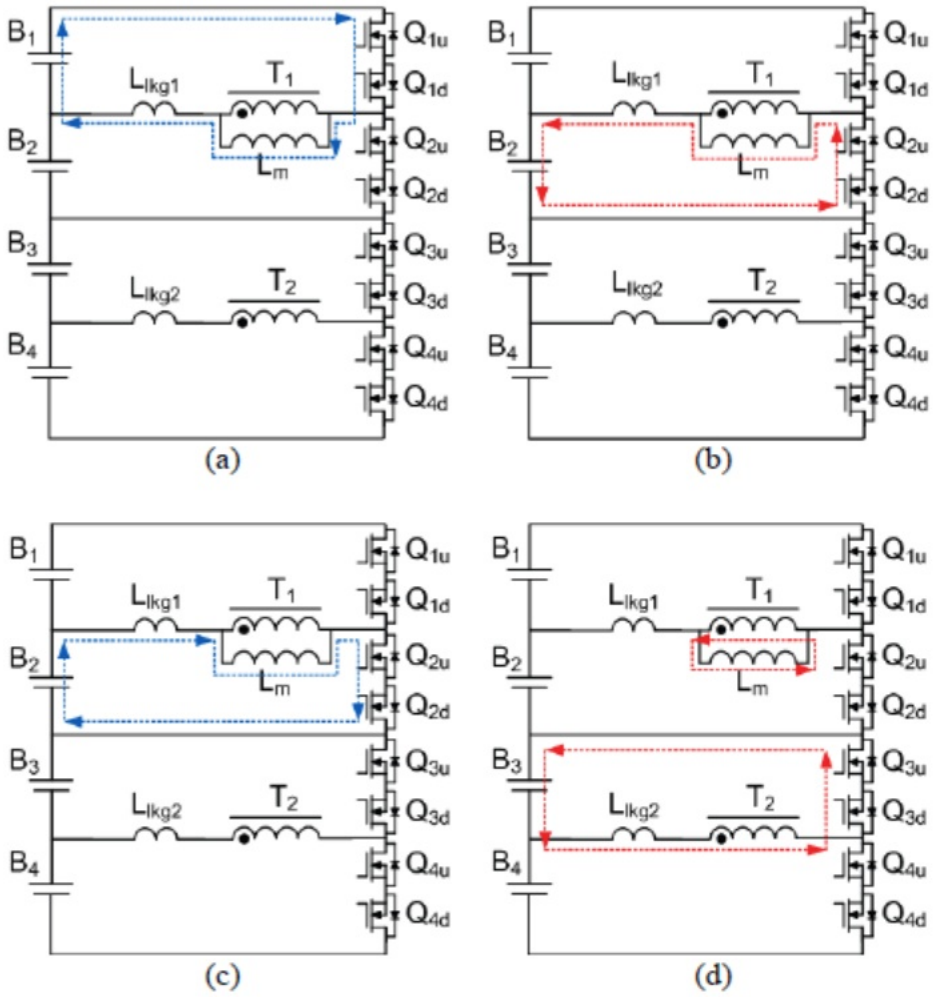

Figure 10. Current path of case 3. (a) Mode 1: discharging B1. (b) Mode 2: Charging B2. (c) Mode 3: discharging B2. (d) Mode 4: charging B3. [22].

2.2 Cell to battery balancing

2.2.1 Converter Base

Figure 11 shows a boost converter [1-3] [15-17]. Isolated DC-DC step-up converters are used [2]. This is very efficient topology because the rectifiers are at high voltage side and switches are at low voltage side bringing about low switching loss [1], so there is no need using ZVS. Low voltage transistors will be used [1]. Circuit can be simple and trusted especially for distributed BMSs [1]. This topology is used in most low cost DC-DC converters [1]. Each cell is equipped with a boost converter. Outputs are connected together which go to the whole battery pack. Controller selects a cell with highest SOC and corresponding converter will be on [1] [2] [3]. Hence, the excess energy will be transferred from cell to the entire battery. This process will keep going until all cells are balanced (Same state of charge).

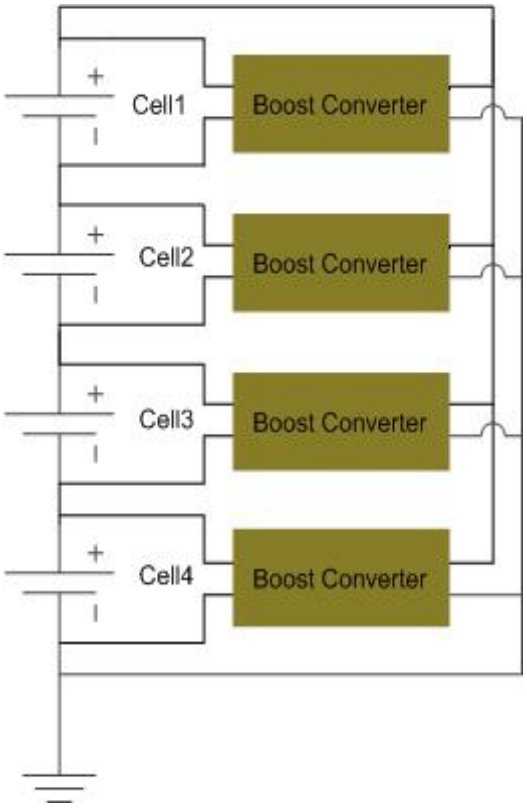

Figure 11. Cell to battery Topology

In figure 12, a boost converter is shown. Voltage and current stress is very low [3]. Equalization speed is good [3] and approximate efficiency is good [3].

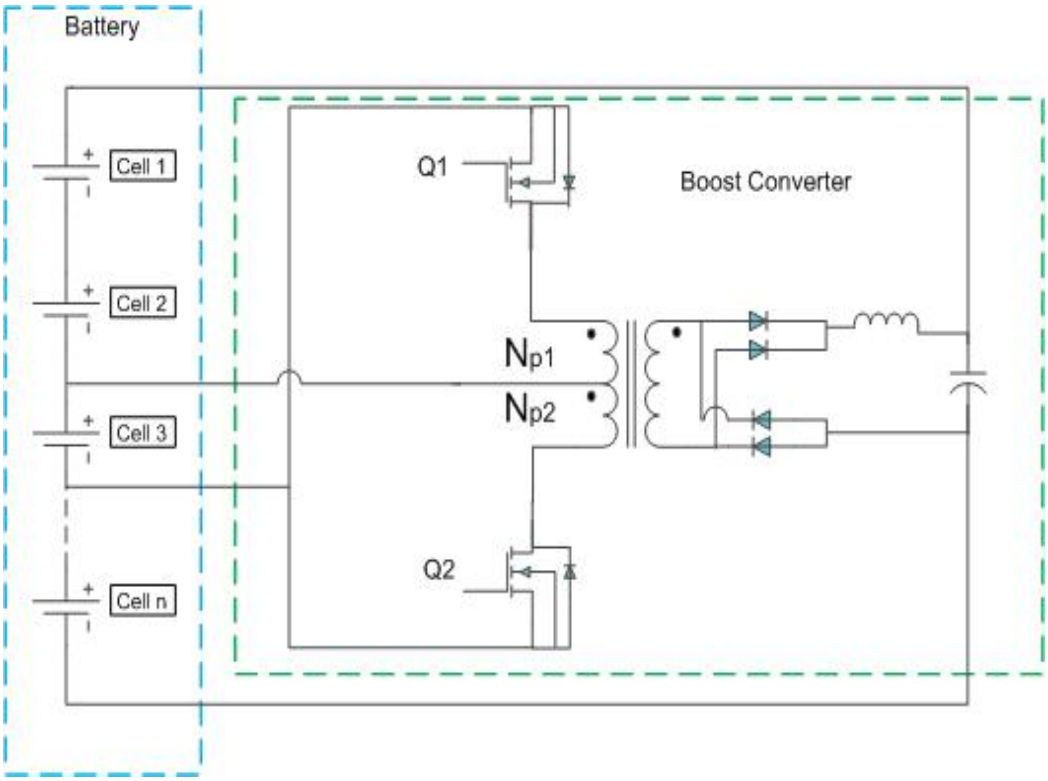

Figure 12. Boost converter

Multi-winding transformer with magnetic core is components of dc-dc converter. The problem associated with the above topology is flux imbalance, phenomenon of magnetic core saturation in multi-winding transformers [18]. Either difference in winding resistance or difference in on time resistance of transistors causes the phenomenon. Consequently transformer core operates asymmetrically [4] and core drifts further off center of the origin, it goes into deep saturation [4] and destroy power transistors after a while.

CHAPTER 3

HYSTERSIS LOOP AND FLUX IMBALANCE

Figure 13.a shows an AC current passes through a winding on a magnetic core. At the beginning, we assume that flux is zero in a core. When the current increases, flux moves on ab curve in figure 13b. This is called magnetization curve. When the current decreases, flux moves on another way, on BCD curve. When the current again increases, flux moves on deb curve. Flux in a core not only depends on passing current through winding but also depends on residual flux, φ_{res}, in a core.

bcdeb route in figure 8b is called hysteresis loop.

In figure 13, if volt-second across Np1 when Q1 is turned on equals to volt-second across Np2 when Q2 is turned on, then after one entire period, the core will shift up from d to b and return to b in Figure 13.

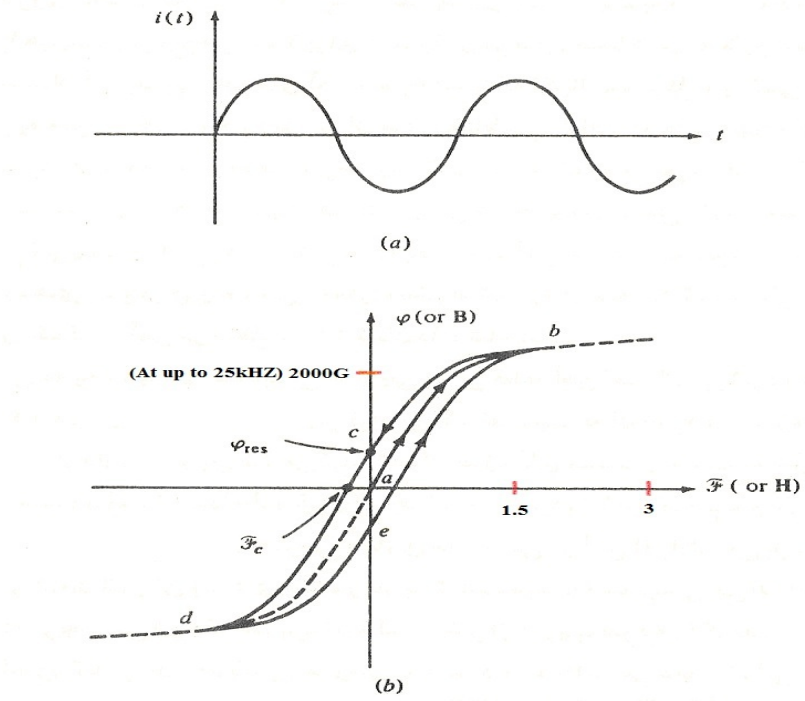

Figure 13. Hysteresis loop of a typical ferrite core [4]

If volt-second differs by a little percent, the core will return to beginning point within one cycle. After a number of cycles the core will drift off the center into saturation [4]. Obviously, in saturation condition, the core cannot keep the voltage and next time when transistor is on, the transistor will be prone to high current and voltage, resulting in being destroyed [4].
Number of reasons cause to difference in volt-second. In bipolar transistors, storage times cause to keep the collector on longer than the time that base of transistors is on. Range of storage time is between 0.3 to 6 μs [4]. This storage time is dependent on temperature [4]. When temperature increases, storage time of bipolar transistors increases [4].

If one transistor has more volt-second than another one, that transistor will draw more current.
Core magnetizing current becomes a significant part of load current. The transistor that draws more current gets warmer resulting in storage time increase. Longer storage time will result in longer volt-second. Hence, thermal runway condition happens that brings about a core to be driven into deep saturation and finally destroying power transistors.

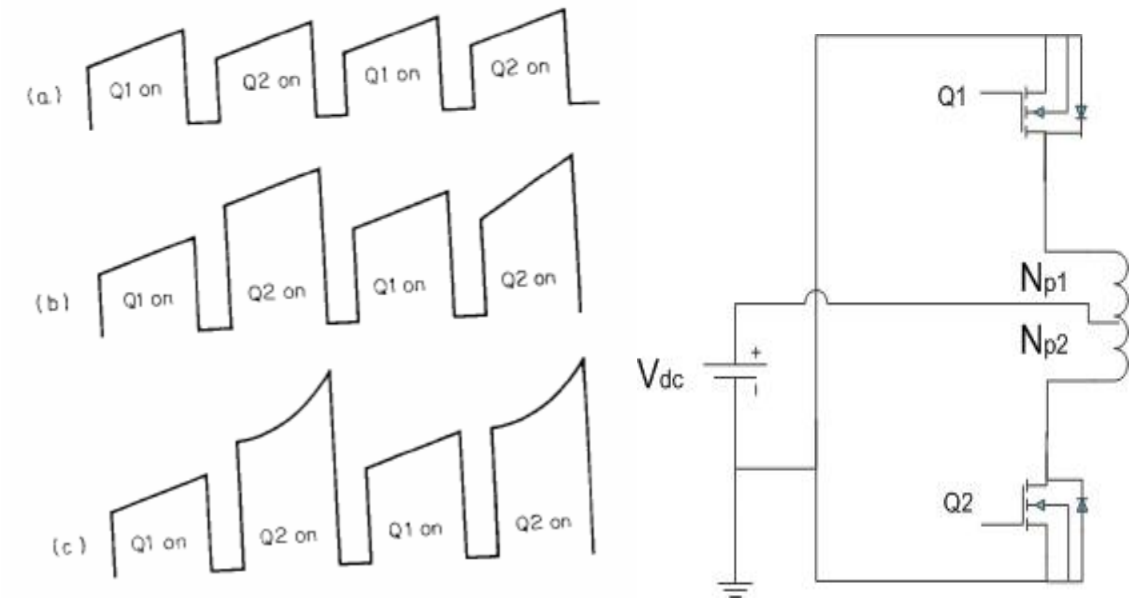

Figure 14. Current at transformer center tap. Equal volt-second product on both halves of transformer primary. (b) Transformer center tap current. Unequal volt-second product on both halves of transformer primary. Core is not yet on curved part of hysteresis loop. (c) Transformer center tap current. Unequal volt-second product. Upward concavity indicates dangerous situation. Core is far up on curved part of hysteresis loop [4] .

Magnetizing current ramps up linearly at a rate $\frac{dI}{dt} = \frac{[V_{dc} - V_{ce(on)}]T_{on}}{L_{pm}}$ (7).

$$I_{pm} = \frac{[V_{dc} - V_{ce(on)}]}{L_{pm}}$$

Figure 14 indicates where core is on hysteresis loop. In Figure 14.a, current peaks are equal, because volt-seconds are equal. In figure 14.b volt-second products are not equal and core operation is not centered. As long as the DC bias does not drive the core up the hysteresis loop, slop of ramp still remains linear and operation is in safe area. In Fig14.c, volt-seconds on half cycles are largely unequal and the core is biased toward saturation and entered the curved part of hysteresis loop. Now magnetizing current increases largely. In this condition, any small amount of increase in temperature, results in thermal runway.

In MOSFET transistors, this problem is less serious. They have no storage time [4]. With increase of temperature, on voltage (Vds) of transistors increases. The transistor which draws more current gets warmer, increasing its on voltage. So decreasing its current due to robbing voltage from its half primary. Hence there is a tendency to correct flux imbalance. However, it can not be sorely relied on quantitatively to solve flux-imbalance problem in all power levels and with worst case combination of two transistors in push-pull topology [4].

Matching power transistors is another way to combat flux imbalance. But it is costly to have on voltage and storage time of two transistors matched to each other [4].

CHAPTER 4

CURRENT MODE TOPOLOGY

4.1 Current-mode control circuitry

Current mode is the best solution to combat the flux-imbalance problem that occurs in push-pull topology. By monitoring the current in each of push-pull transistors based on pulse by pulse and makes them oblige to have same amount of amplitude [4].

Current mode topology has two different feedback loops: outer and inner [4]. Figure 15 shows a current mode topology. Outer (EA) measures the output DC voltage and compares with reference voltage and then provides the inner loop with V_{eao} (Output error amplifier). Inner loop containing current sensing resistor R_i (converting ramp current of transistors to ramp voltage), and peak current sensing voltage comparator (PWM) [4]. In order to have the output voltage constant based reference voltage, on time of transistors alternate. As the line voltage changes, on time of transistors change. Current-mode topology corrects this change without delay in error amplifier. In figure 15 a current mode controller is shown. In this figure, fundamental components controlling a push-pull converter are depicted. On time of transistors is defined by voltage sensing error amplifier output V_{eao} and PWM voltage comparator, comparing V_{eao} to ramp voltage V_i [4]. Current passing through primary of transformer has a ramp shape and this current exist at R_i, current at common emitter or source of transistors. Transistor on time is calculated as follow. There is an internal oscillator that its frequency is set by R_t, C_t.

Oscillator period is $0.9 R_t C_t$ [4]. Each rising edge of oscillator reset the feed forward (FF1) consequently resetting the output Q_{pw} (T). So, off time of Q_{pw} is same as duration of on time of either Q1 or Q2 transistor. When point of A is on, the transistor Q2 is on, and Q2 transistor related current starts increasing linearly resulting linear increase of V_i. When V_i, wants to be equal or more than V_{eao}, FF1 (T flip flop input) sets to high, bringing A point to low so turning off the Q2. As long as the clock has not set to high,

Q_{pw}(T) is on, and in this on time duration, both output gates of A and B are off. When the clock sets to high, Q_{pw}(T) sets to low, then sets point B to high resulting in turning Q1 on. Q and Q! are outputs of T flip flop. In figure 16 current mode controller signals are shown. Figure 17 indicates current mode system in MATLAB SIMULINK.

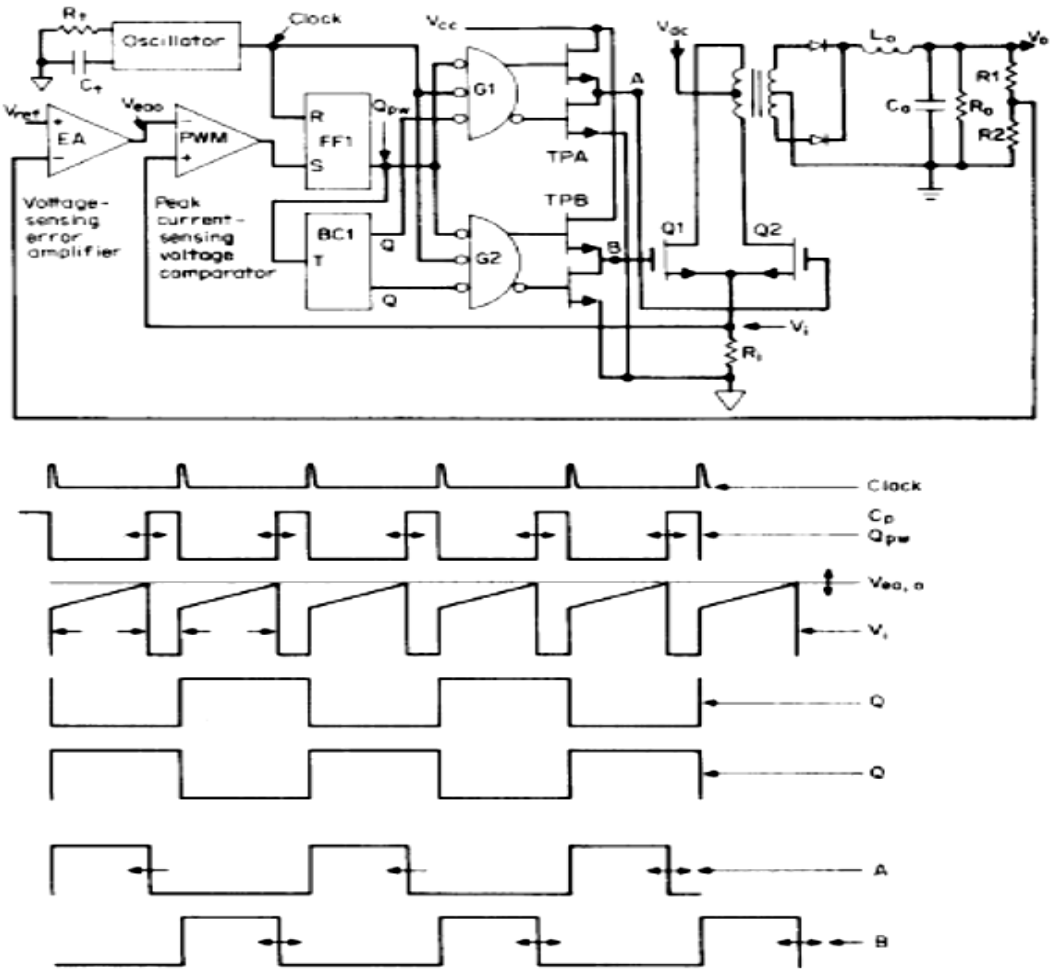

Figure 15. "Current-mode controller drives a push-pull converter. At each clock pulse the transistors turn on sequentially and they turn off when the peak voltage across the common current sensing resistor gets equal to output voltage of an error amplifier. PWM obliges power transistors of Q1 and Q2 to have equal amplitude of current" [4].

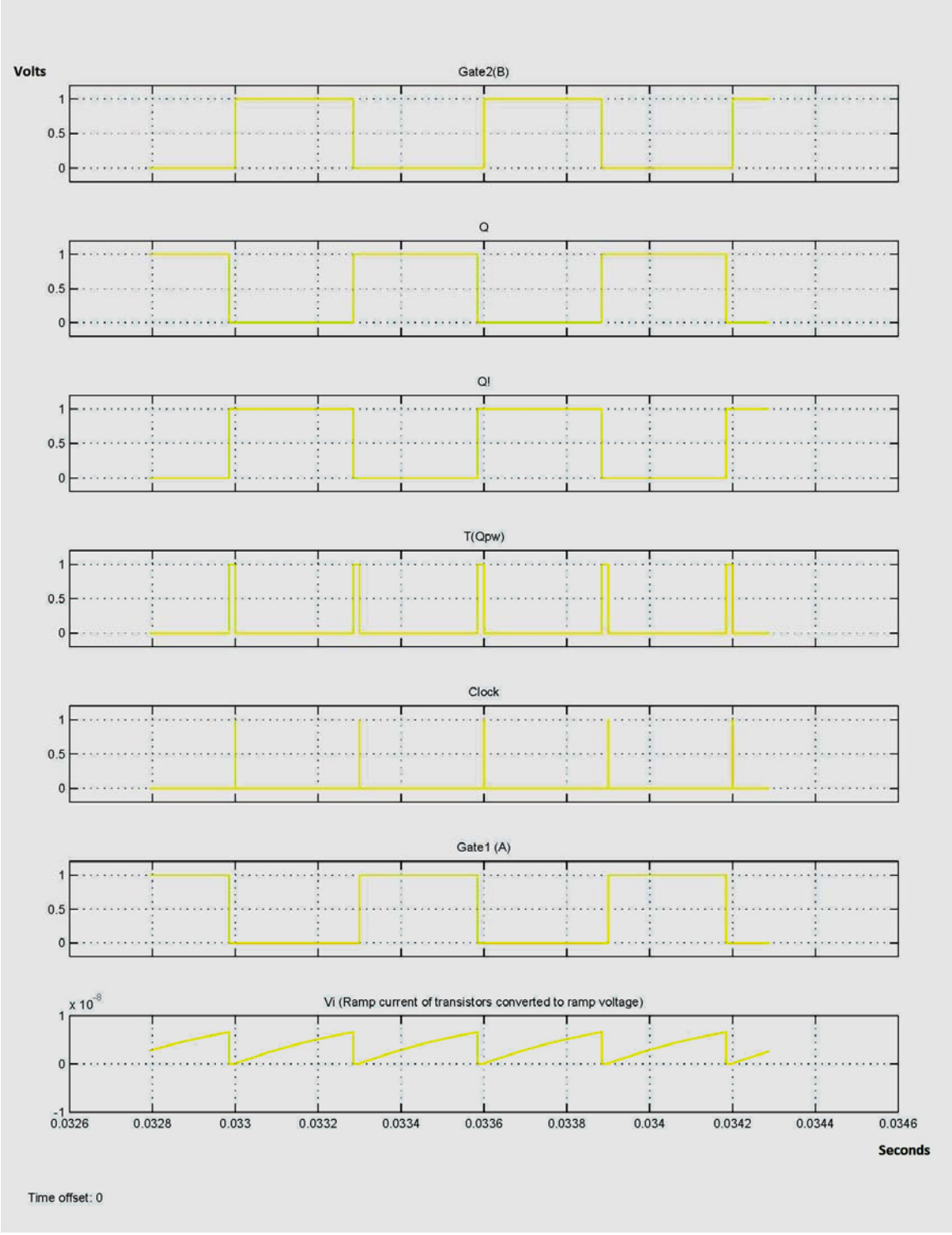

Figure 16. Signals of a current mode controller

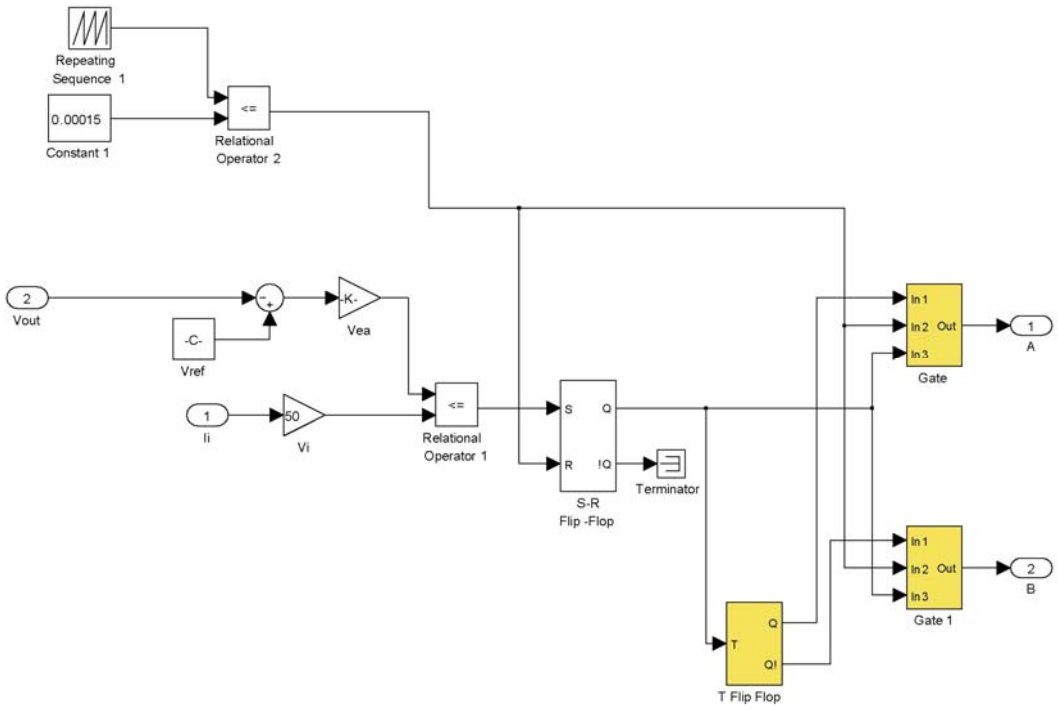

Figure 17. Current mode system

4.2 Current mode advantages

A PWM-Current mode controller has below advantages:

4.2.1 Line Voltage Regulation [4]

This section clarifies how controller regulates line voltage against variation.
If line voltage increases, which has been resulted in increased on-time of transistors, output voltage of error amplifier (V_{eao}) decreases in order to keep voltage same as V_{ref}. Then, output pulse width of RS flip flop (Q_{pw}) increases resulting in decrease of output pulse width of gates (G1and G2) and the transistors are turned on for the shorter time. So this results in decreased peak current of transistors and consequently decreasing output voltage. Voltage is basically proportional to secondary winding peak voltages and power transistor on time. Consequently, when on time and peak currents decrease, secondary voltage peak current and on time will decrease resulting in decreased V_{dc} of output. Figure 15 shows the signals and current mode circuit.

4.2.2 Elimination of flux imbalance [4]

If transformer core gets oF center and goes into saturation, V_i gets close to the end of on time, that means equal to V_{eao}, earlier in time resulting to terminate on time sooner. Hence, flux increase that happened in that cycle stops. So the core will be back down in flux. Since the peak currents are equal on both cycles, flux which is proportional to current will be balanced.

CHAPTER 5

ACTIVE CELL BALANCING CONTROL MODELS IN MATLAB SIMULINK

5.1 Cell to cell balancing

5.1.1 Single Inductor model

Duty cycle for this topology is approximately 50%. Because the transistors have delay on time and delay off time [19]. Delay on time is the time required to charge C_{gs} (Capacitor between gate and source of a MOSFET) until voltage V_{gs} reaches to threshold voltage V_T. Cell balancing algorithm removes excess energy from cell with highest SOC in half cycle and transfers energy to cell with the lowest SOC in next half cycle. Table below describes the functionality of the method.

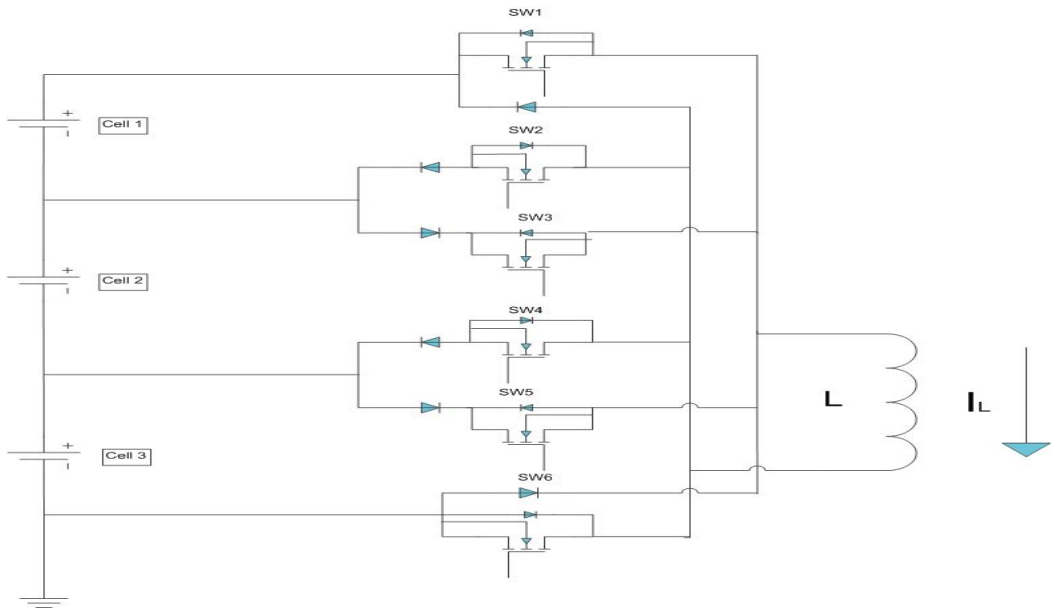

Figure 18. Single inductor model

HSOC	Cell1	Cell2	Cell1	Cell3	Cell2	Cell3
LSOC	Cell2	Cell1	Cell3	Cell1	Cell3	Cell2
$T_{on} \cong T/2$	sw1,sw2	sw3,sw4	sw1,sw2	sw5,sw6	sw3,sw4	sw5,sw6
$T_{off} \cong T/2$	sw2,sw5	sw1,sw3	sw4,sw6	sw1,sw3	sw4,sw6	sw2,sw5

Table1. Operation of Single inductor model

For example if cell 1 has the highest soc and cell 2 has the lowest soc, the energy stored in cell 1 is transferred to inductor during on time, first half cycle, which calculated as below:

$$V_{cell1} = L\frac{di}{dt}, i = \frac{1}{L}\int_0^{t_{on}} V_{cell1} = \frac{T}{2L}V_{cell1} \quad (8).$$

$$E_{cell1} = \frac{1}{2}Li^2 = \frac{1}{2}L\frac{T^2V^2_{cell1}}{4L^2} = \frac{T^2V^2_{cell1}}{8L} \quad (9).$$

During the off time, second half cycle, this energy is transferred from inductor to the cell2.

So, $E_{cell2} = E_{cell1}$

This continues until all cells have same voltage.

Battery model from SIMULINK MATLAB, R2008a has been used.

The equivalent circuit of the battery is shown below:

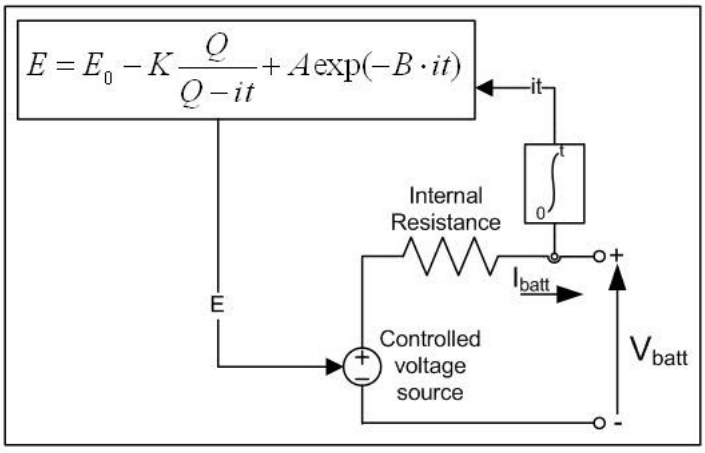

Figure 19. Battery model from MATLAB SIMULINK R2008a

Where

E = No load voltage (V), E0 = Constant voltage (V), K = Polarization voltage (V)

Q = Battery capacity (Ah), A = Exponential voltage (V), B = Exponential capacity (Ah)-1

Assumptions:

The internal resistance is supposed constant during the charge and the discharge cycles and does not vary with the amplitude of the current (MATLAB SIMULINK R2008a).

The capacity of the battery doesn't change with the amplitude of current (MATLAB SIMULINK R2008a).

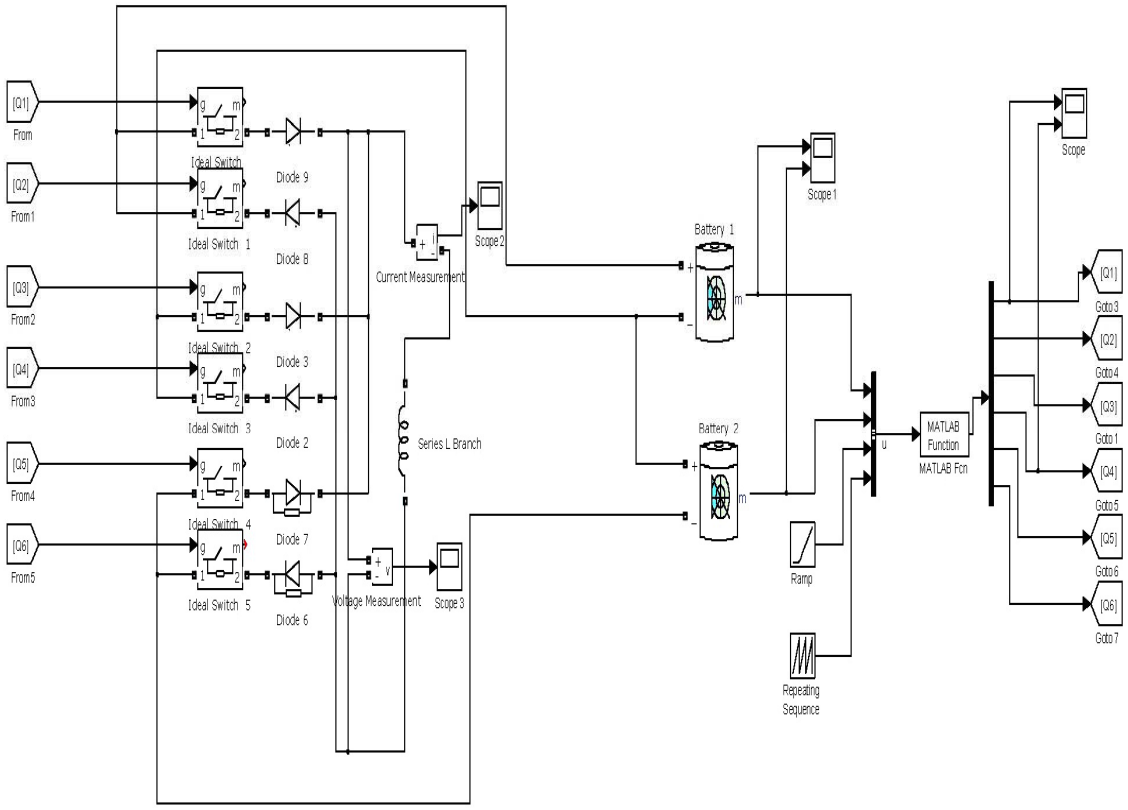

Figure20. Single inductor model in MATLAB SIMULINK

Cell to cell balancer using single inductor for two cells implemented in MATAB SIMULINK. Figure 20 shows the system. Cells are 3.2 volts and with 15AH capacity. Maximum peak current drawing from cells is less than 60 A. Duty cycle is around 50%. $f = 1/T$ is switching frequency.

Two cells will be balanced when neither load applied to the whole pack nor battery pack charged. MATLAB function box in figure 20 reads the SOCs and send commands to the switches.

In order to calculate charge and discharge rate, I considered a cell to cell balancer with two cells using an inductor. Then based on calculated charge and discharge rate, I extended cell balancer to three cells. Charge and discharge rate per ten seconds are accordingly Δsoc 1=0.085, and Δsoc 2=0.102.

Inductance is calculated as below:

$$V_{cell1} = L\frac{di}{dt}, i = \frac{1}{L}\int_0^{t_{on}} V_{cell1} = \frac{T}{2L}V_{cell1}\text{, f=50Hz}$$

$$60 = \frac{3.2}{2L.50}, L = 0.53m\text{H}\ \text{Is considered.}$$

5.2 Cell to battery balancing model

Figure 21 shows a cell to battery balancer model including 3 cells. In this model a boost converter has been utilized. Push-pull topology is utilized in this step-up converter.

Boost converter compromises a multi winding transformer, MOSFET switches, transformer-capacitor snubbers, rectifier bridge, output filters, and current mode control system.

Cell voltages are 3.2 V, and capacity of 15AH. Output voltage of converter is approximately10V. I assumed the cell 3 with soc=40% as the highest state of charge, and cell 1with soc=10% as the lowest state of charge. In order to have three cells balanced faster than usual, two alternatives exist. First alternative is when just one converter which is connected to the cell with highest soc, is turned on. Second alternative is, when two converters which are connected to cells with highest and second highest state of charge are turned on. Configuration parameters for simulation are as below:

For solver option:

Type is Variable-step.

Solver is ode45.

Stop time is 10 seconds.

Simulation type is discretizing electrical mode with sample time of 0.3 μs .

Winding resistance is $5m\Omega$, primary voltage is 3.52V, and secondary voltage is 20.2V.

Circuit description:

Figure 21 shows 3 cells with two converters which are being driven by a current mode control system to control the pulse width given to the gate of MOSFETS, and eliminate the flux imbalance issue at push-pull topology. I did not show the third converter connected to the cell 1 as the lowest soc. The number of units that exist between cells is calculated. This continues until number of units becomes greater or equal one.

Two different tests were done. First when one boost converter is on, which is connected to cell with most SOC.? Let have the boost converter which is connected to cell 3 on.

After 1 second, soc1 which is soc of cell1 and soc2 which is soc of cell 2 increased by $\Delta = 0.01$, results are soc1=38.01, soc2=39.01. Soc3 which is soc of cell 3 decreased by 0.04, soc3=39.96. Figure 19b shows the charge and discharge rate of cells.

$n_1 = \frac{soc3 - soc2}{\Delta soc}$, $n_2 = \frac{soc3 - soc1}{\Delta soc}$, $n_3 = \frac{soc2 - soc1}{\Delta soc}$, are called units.

If $n_3 >= 4$, two converters which are connected to two cells with highest soc, turns on. So, cell with lowest soc which is soc1 charges with charge rate 0.02 per second and soc2 and soc3 discharges with discharge rate 0.04 per second. If $n_3 < 4$, soc1 and soc2 start charging with charge rate 0.01 per second, and soc3 discharges with discharge rate 0.04 per second. That means just one converter which is connected to cell3 is on. This procedure continues until they are balanced. Figure 19a show charge and discharge rate, when two boost converters connected to cell2 and cell3 are on. We can see after 1 second charge rate of cell1 increased by 0.02, 38.08, which charge rate is twice than when one converter is on. And cell 2 and 3 discharged by 0.04, which are 38.96 and 39.96. So whenever state of charge difference between the lowest soc and second highest soc is more than 4 units, two converters turn on and consequently decrease the balancing time.

To calculate RC snubbers for bridge rectifiers, below formulas were considered.

$R_S > 2\frac{T_S}{C_S}$ (10). (Referenced from MATLAB library 2008)

$C_S < \frac{P_n}{1000.2.\pi.f.V_n^2}$ (11). (Referenced from MATLAB library 2008)

P_n Nominal power of converter =60 W

V_n Nominal line to line voltage (rms)= $\sqrt{[\frac{1}{T}\int_0^{T/2} 10.4^2 + \int_{T/2}^{T}(-10.4)^2]} = 14.7V$ (12).

f Frequency=5 kHz, $T = \frac{1}{5000} = 0.2mS$ (13).

T_s Sample time=0.3 μS

$C_S < \frac{60}{1000.2.\pi.5000.(14.7)^2}$, $C_s = 36nF$

$R_S > 2\frac{T_S}{C_S}$, $R_S > 2\frac{0.3\mu S}{36nF}$, $R_S > 18\Omega$ so I assume $R_S = 20\Omega$

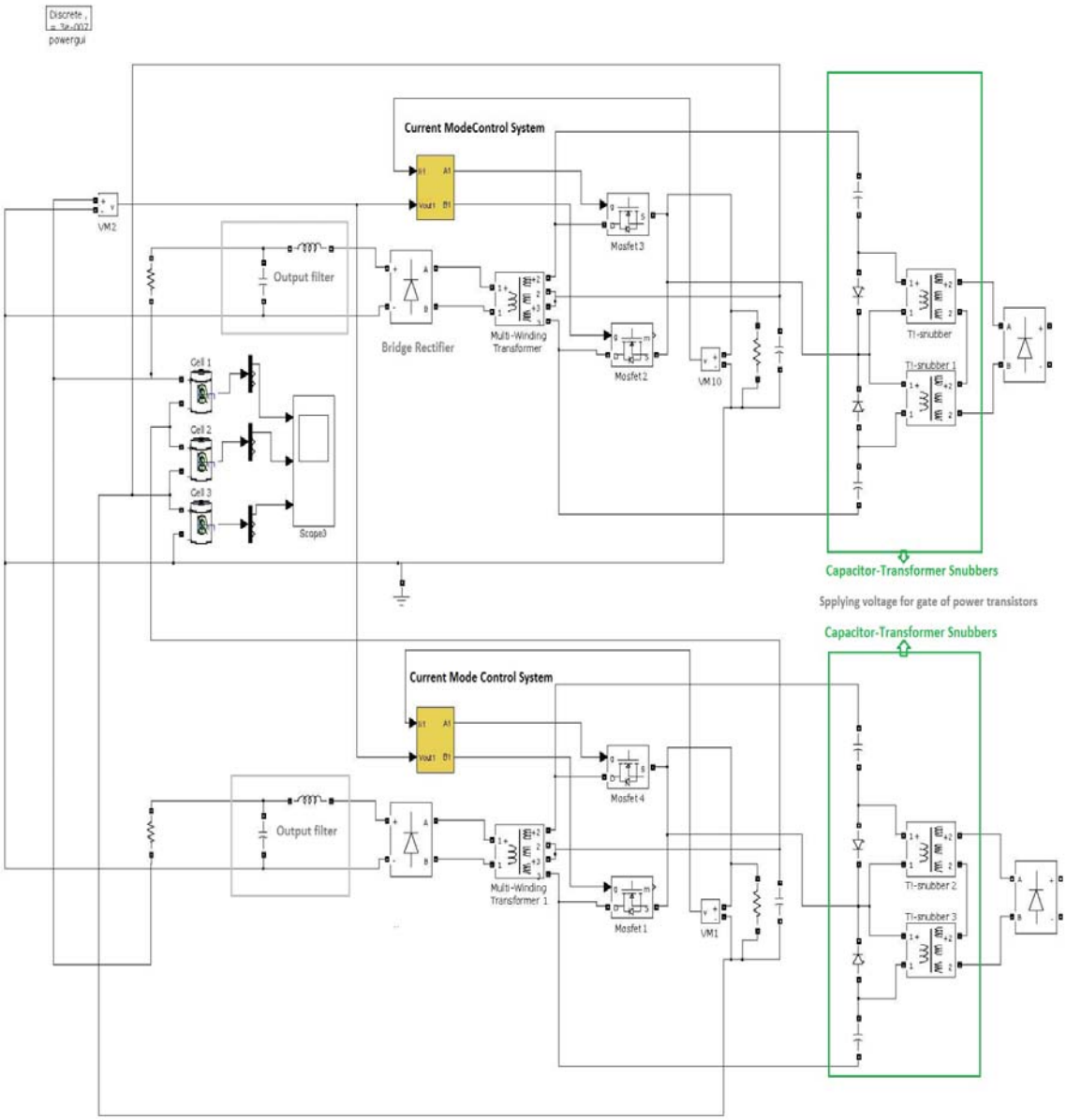

Figure21. Cell to battery balancer model in MATLAB SIMULINK

5.3 Application of DC-DC converters

Step-up converters are remarkably used in radar and ignition systems. DC converters are categorized to two-quadrant and four-quadrant operation. Two-quadrant converters can be part of the power supplies containing battery packs. Selection of a topology of dc-dc converters is basically defined based on input/output voltages with turn's ratio in isolated converters, power levels, voltage, and current stress of semiconductor switches, as well as usage of magnetic components [19]. Fly back converters are used in low power application up to 200 W. Problem associated with that is huge size of transformer core and high voltage stress on switches [19]. Forward converters are used in applications up to several hundreds of watts [19]. And problem associated is, demagnetizing winding is required and high voltage stress is applied on switches [19]. Push pull converters are utilized at medium power levels [19]. Because of bidirectional excitation, transformer size is small. Disadvantage is, likelihood for the core to be saturated in case of asymmetry is high. In application like solar electric systems with battery packs including lots of cells in series, push pull converters may be used to balance cells. Input voltage of solar inverters rage from 600 Vdc to 1000 Vdc. Voltage of battery cells is around 3 to 4 Vdc. and cells are in series to produce 12-, 24-, or 48-volt strings. For example, a 48-volt battery pack containing 16 cells, require a cell balancer made based on push pull topology due to medium power is required for. In order to prevent flux imbalance phenomenon, current mode controller has been used in boost converter.

5.4 Calculation of converter parameters In MATLAB SIMULINK

5.4.1 Primary, secondary peak and RMS currents

All batteries have a capacity of 15A/h, and we want to have the batteries charged with 6A current. With output voltage of 10V. Each battery has a voltage of 3.2V.

$$P_{out} = V_{out}.I_{out} = 10V.6A = 60W \quad (14).$$

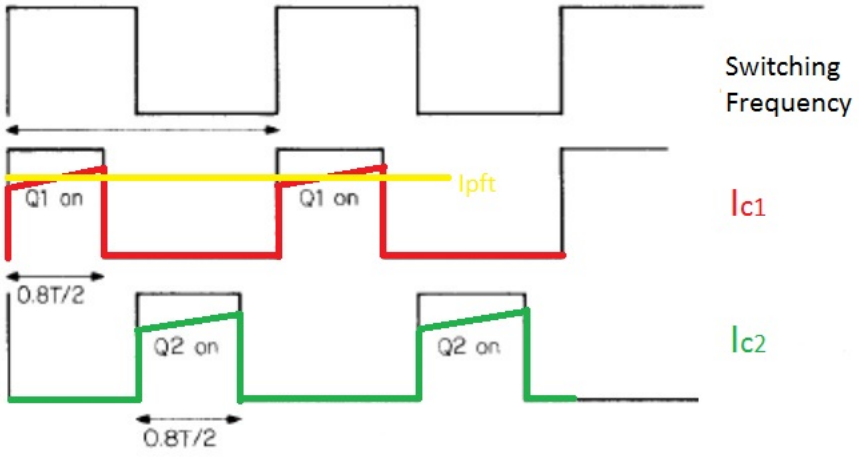

Figure 22. Transistors timing and currents of primary windings

DC-DC Converter Efficiency=80%

Amplitude of Ipft (Primary flatted-topped) is the value of current at center of the ramp, Fig 22.

$$P_{in} = 1.25P_{out} = V_{dc}I_{dc} = V_{dc}.(0.8).I_{pft} \quad (15).$$

$$I_{pft} = 1.56.\frac{P_{out}}{V_{dc}} = 1.56.\frac{60}{3.2} = 29.25A$$

5.4.2 Output filter design

Output of inductor should not be in discontinuous mode. Discontinuous situation happens when front end of inductor current ramp drops to zero. Fig 23.

$$dI = 2I_{dc} = V_L \frac{T_{on}}{L_o} = (V_1 - V_o)\frac{T_{on}}{L_o} \quad (16).$$

But $V_o = V_1(2T_{on}/T)$ (17)., $T_{on} = 0.8T/2$ (18).

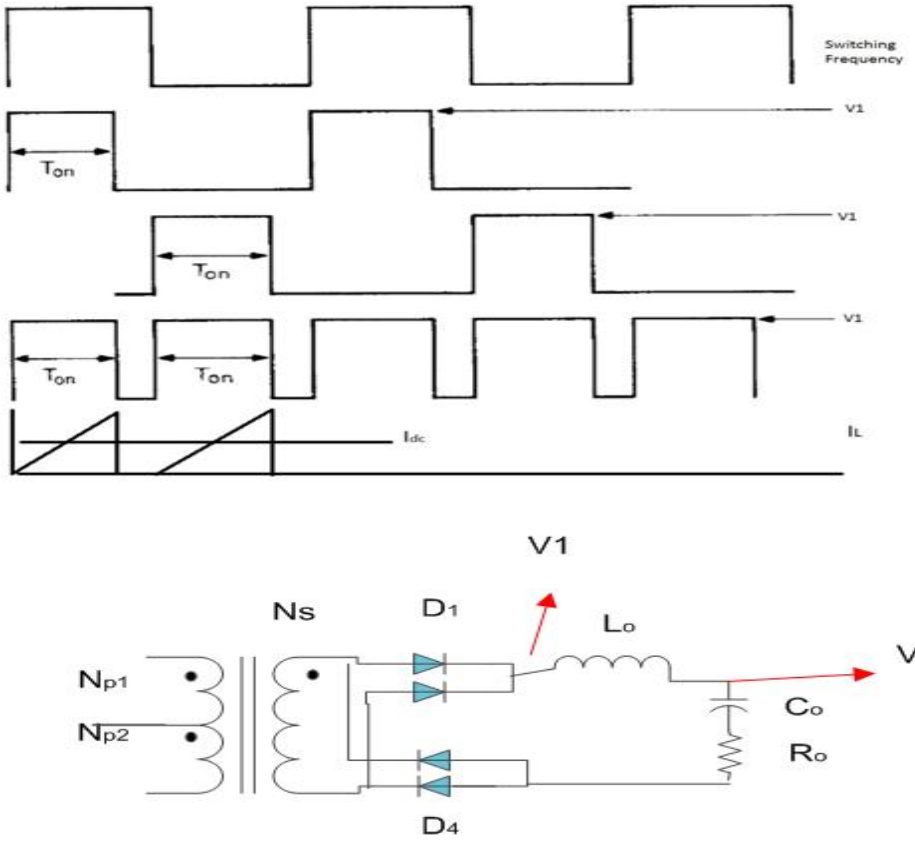

Figure 23. Output circuit for calculation of $L_o, C_o . T_{on}$ will not be greater than 0.4T.

(f) Switching frequency is 5 kHz

$$T_{0n} = \frac{V_o T}{2V_1} \quad (19). \text{ Or } \quad V_1 = 1.25V_0$$

$$dI = \frac{(1.25V_o - V_o).(0.4T)}{L_o} = 2I_{dc}$$ And finally $$L_o = \frac{0.05V_oT}{I_{dc}}$$ (20).

$V_0 = 10.4V$

$I_{dc} = 6A$

$f = \frac{1}{T} = 5kHz$

Hence, $L_o = \frac{(0.05).(10.4)}{6.5.10^3} = 17\mu H$ (21).

5.4.3 Output capacitor design

Output capacitor, C_o, is to decrease output ripple voltage and is combined with R_o.

The peak to peak ripple voltage V_r closely equals to $V_r = R_o dI$ [4] (22).

dI is peak to peak ramp amplitude.

For Aluminum electrolytic, R_oC_o ranges between $50\mu s$ and $80\mu s$ [4].

Hence, $C_o = \frac{50.10^{-6}.dI}{V_r}$ (23).

$V_r = 1\%$ of V_o, so $V_r = (0.01).(10.4) = 0.104V$

$C_o = \frac{50.10^{-6}.2.6}{0.104} = 5.769mF$, So $C_o = 6.800mF$, is selected. This range exists in market.

5.4.4 Snubbers design In MATLAB SIMULINK

In this push-pull converter, power transistors are protected from peak voltage, and power stresses by a separate snubber circuit in parallel with each including a capacitor and an inductor in series, and a diode in parallel with a small transformer [23]. Figure 24 shows the snubber circuit.

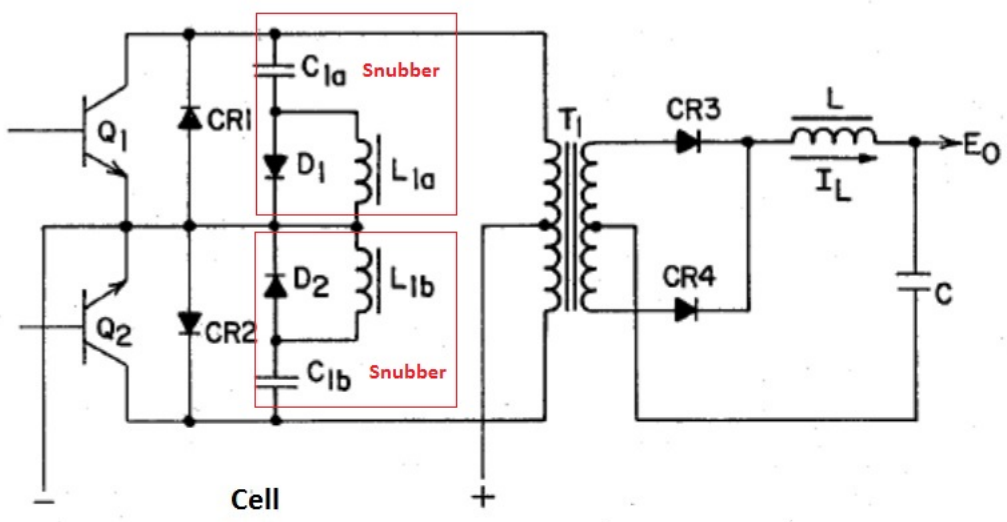

Figure 24. Snubber [23]

Brief description of snubber circuit:

When transistor Q1 is off, C1a starts charging and stores the energy, Figure 24. When Q1 turns on, C1a discharges through L1a, Figure 25a. L1a is half primary of a small transformer used to provide external power for controller and gate voltage of power transistors. Once the capacitor is discharged, half primary winding, L1a, starts discharging its energy and transferring this energy to the secondary winding, figure 25b, where the external power supply is used, Figure 26 shows the external power supply.

Voltage difference across the capacitor is cell voltage.

$\Delta V_c = 3.2V$

Capacitor current at t^{-0}, time before the switch is on, is 60 amperes

$I_c = 60A$

And this happens within 0.5 μs

So, $I_c = C\frac{dV_c}{dt}, C = \frac{60.(0.5).10^{-6}}{3.2} = 10\mu f$ (24).

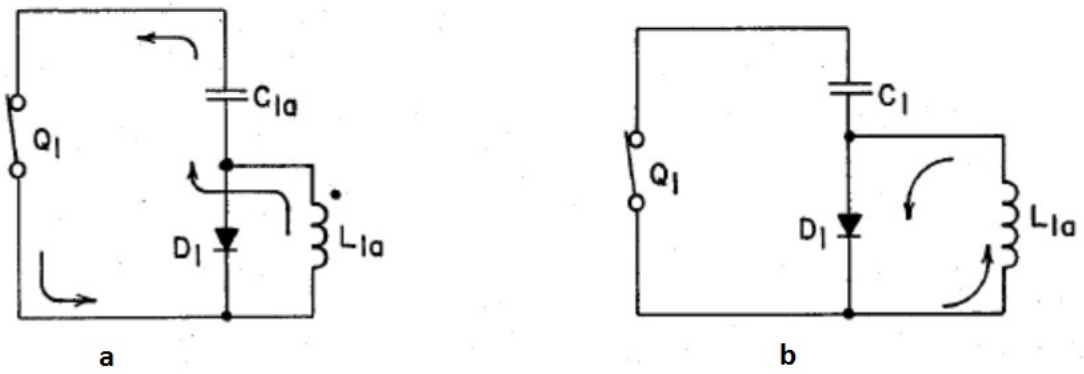

Figure 25.a: Discharge path of C1a, **b:** Discharge path of L1a (half primary winding) [23]

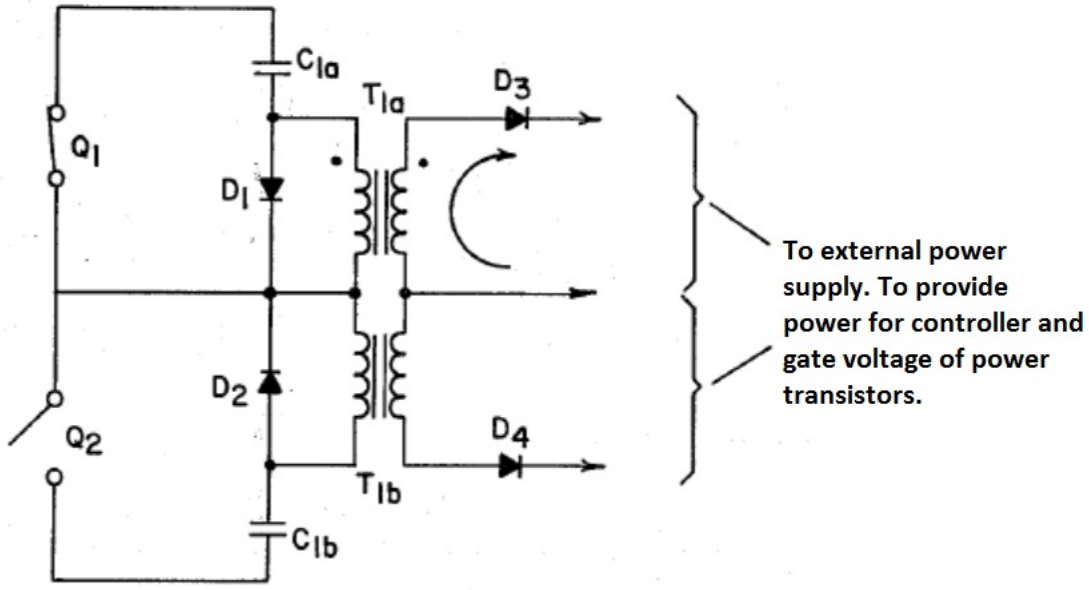

Figure 26. External power supply using snubber [23]

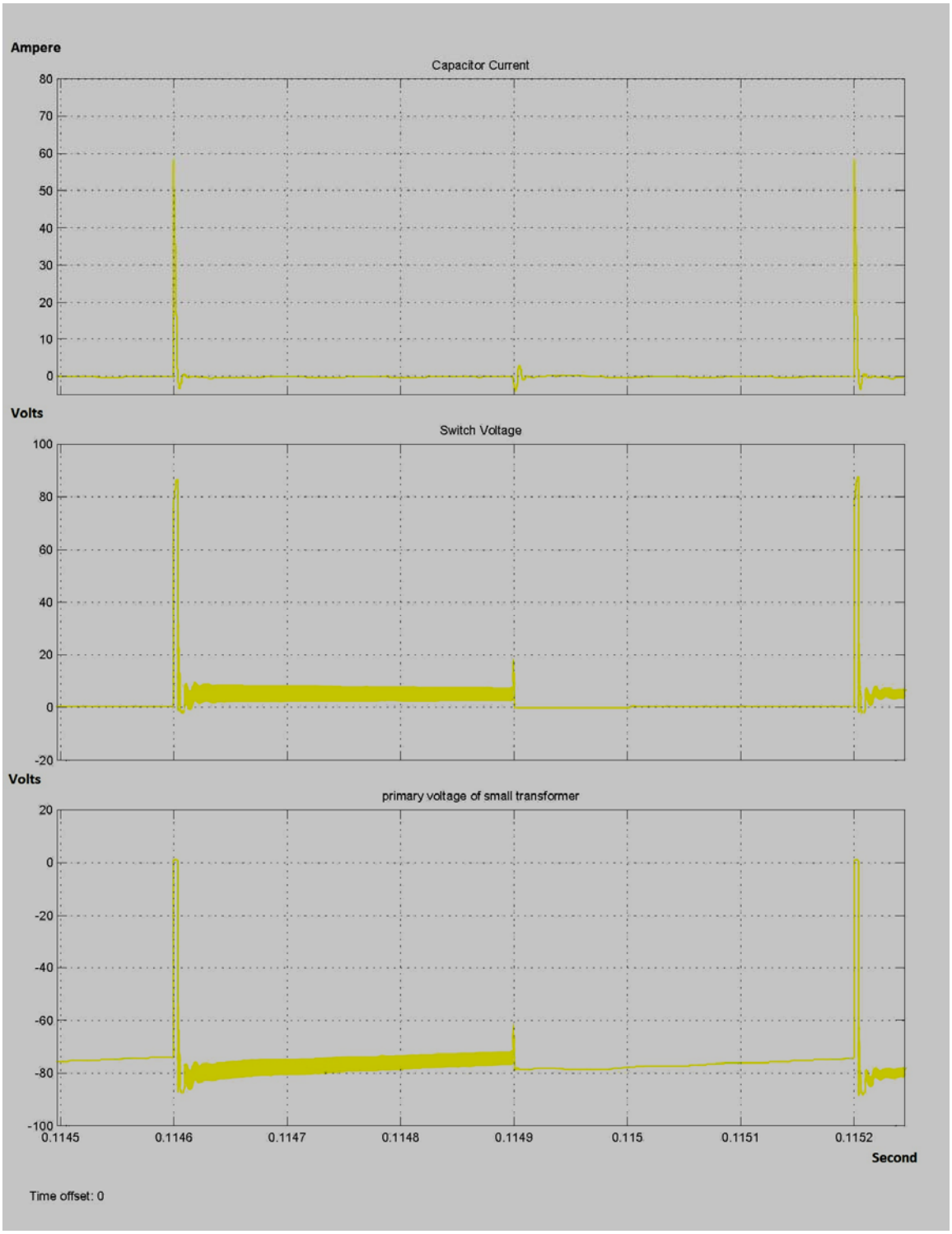

Figure 27. Voltage across the switch and primary voltage of small transformer as well as capacitor current

First top figure 27 shows the maximum current passing through the C_{1a} in Fig 24 when Q1 is off is less than 60A. In second figure 27 (middle one) voltage across the collector-emitter of Q1 is shown which is less than 90Volts and limited by transformer snubber in MATLAB simulation. So power transistors with break down voltage of 100 volts are selected.

CHAPTER 6

MODELS AND SIMULATION RESULTS

6.1 Cell to cell-3 cells

Charge and discharge rate in a cell to cell balancer using two cells calculated. Charge rate is 0.085% and discharge rate is 0.1% after 10 seconds. Then I assume three cells with below state of charges:
soc3=40%,soc2=35%, soc1=10%.

6.2 Cell to battery -3 cells

Figure 28 indicates charge and discharge rate in a cell to battery balancer. Figure28b shows when one converter connected to most SOC (soc3) is on, Δsoc /sec is 0.01%.
Figure 28a shows when 2 converters are on, charge rate is 2Δsoc/sec (soc1 and soc2). Discharge rate for either one converter or two converters on is 4Δsoc/sec.

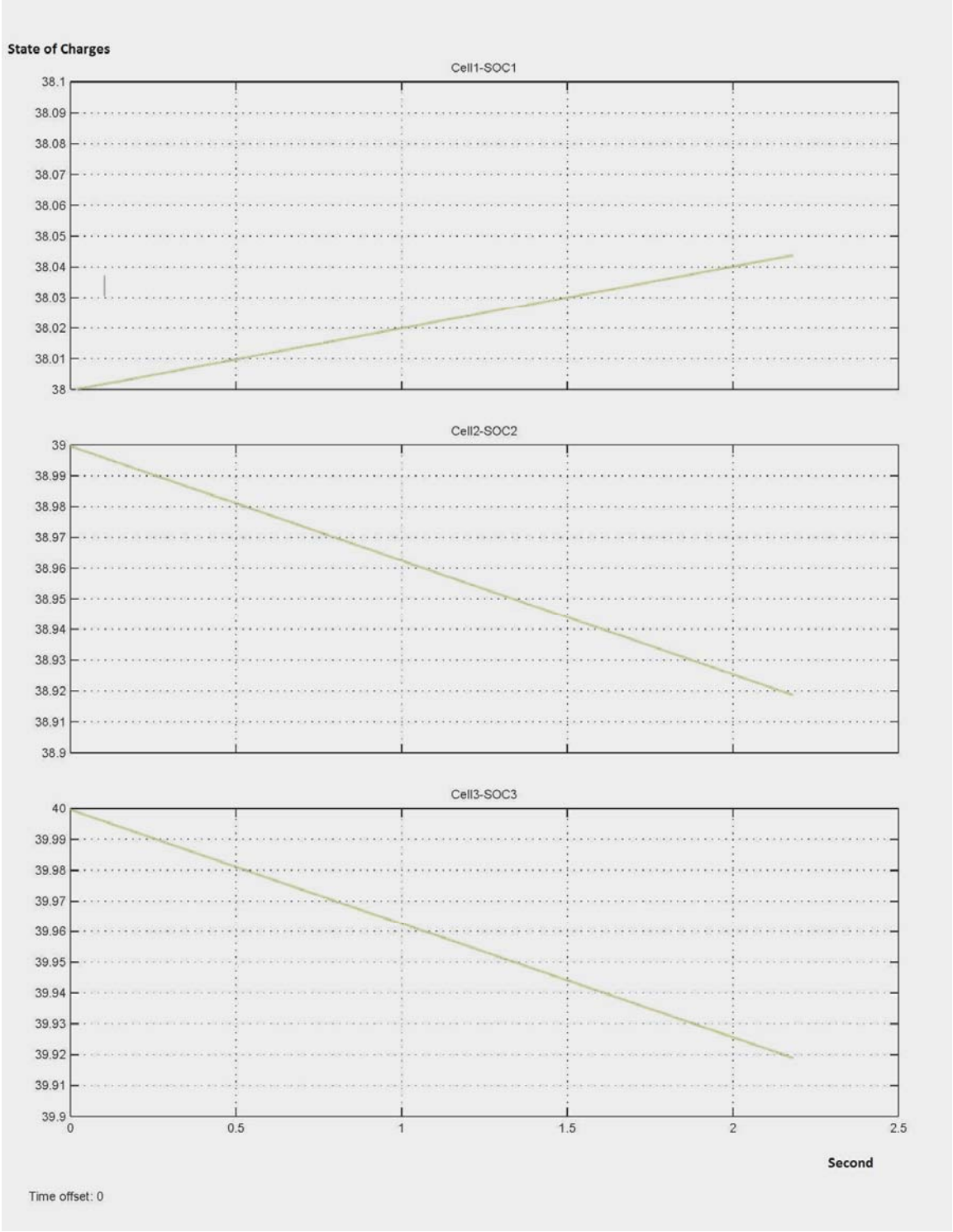

Figure 28a. Charge and discharge rate of three cells, when two converters are on (the converters which are connected to cell3 and cell2) in a cell to battery balancer

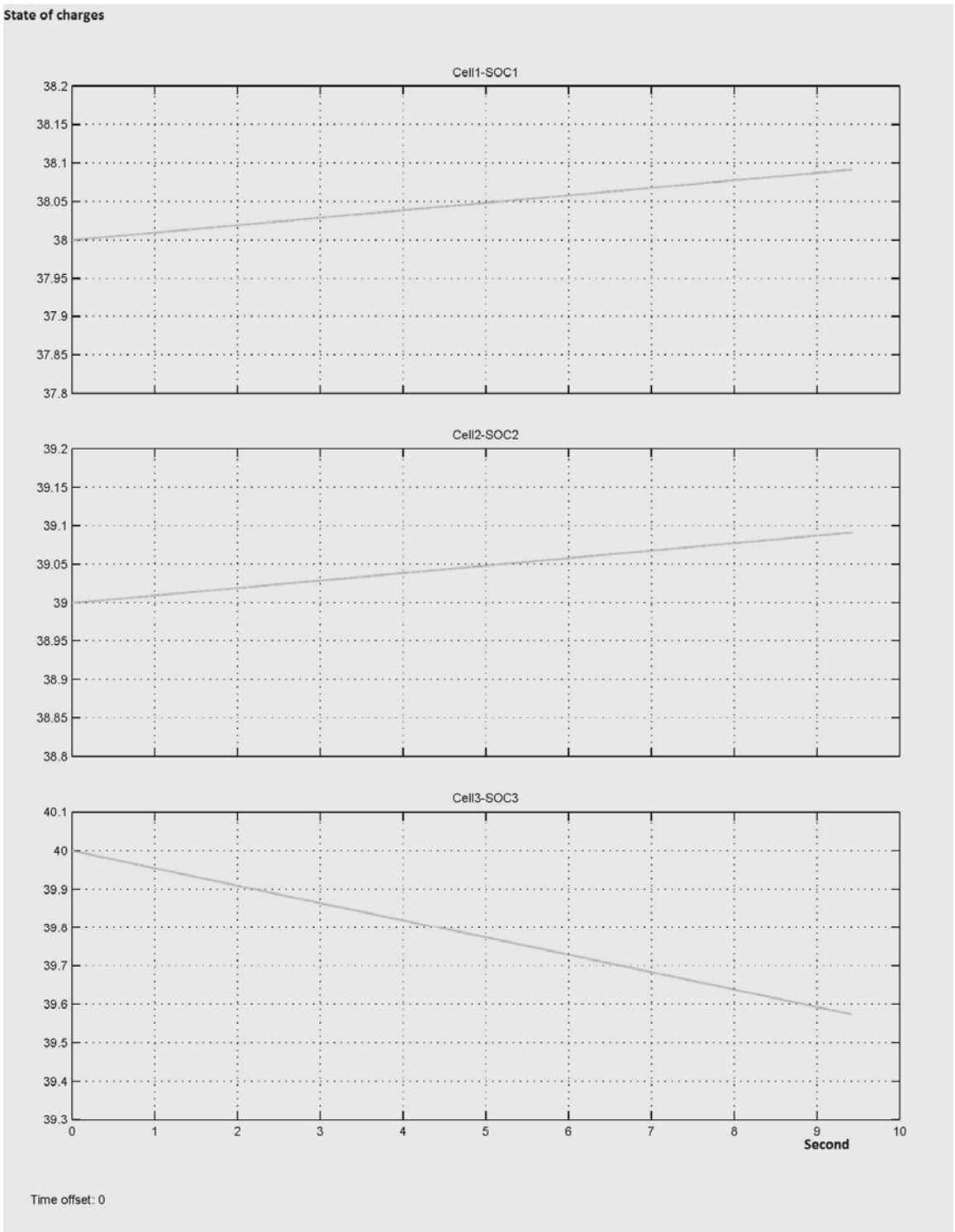

Figure 28b. Charge and discharge rate of three cells, when just one converter is on (the converter which is connected to cell3) in a cell to battery balancer

When difference between least SOC and medium SOC is large, two set-up converters connected to most and medium SOC turn on, so least SOC will charge with less time than one converter is on. When difference between medium SOC and least SOC is small, just one converter which is connected to most soc turns on. So rate charge of other two cells is slower. Figure 29, three bottom graphs, show cure for cell to battery balancer. Figure 29 shows three cells are being balanced with initial SOC 40, 35, and 10 accordingly using cell to cell inductive balancer (first three graphics) and cell to battery balancer (Bottom graphic). Maximum drawing peak current of each cell is 60A. After 3570 seconds all cells get balanced with SOC 26.28 in cell to cell balancer-single inductive topology. In cell to battery balancer, after 518 seconds, cells get balanced with SOC 19.35. So cell balancing in cell to battery balancer is quicker than cell to cell.

Logics could be as below:

1-Voltage of cells measured.

2-A cell with highest soc is selected.

3-Cell-related converter is turned on.

4-Other cells get charged and this cell discharged.

5-State of charge of other cells reached to the state of charge of this cell, and some cells with low state of charge left.

6-Converters connected to cells with highest and equal state of charge turned on.

7-This goes on until all cells have same state of charge then all converters turned off.

Above logic can take more time to have cells balanced rather than below logic.

1-Voltage of cells measured.

2-A system found soc difference between some cells with highest soc.

3-If these differences are low, the converters related to these cells turned on, so other cells with higher speed compared with above logic started charging. If not, just cells having big difference in soc with others turned on.

4- State of charge of other cells reached to the state of charge of these cells and some cells with low state of charge left.

5- Converters connected to cells with highest and equal state of charge turned on.

6-This goes on until all cells have same state of charge then all converters turned off.

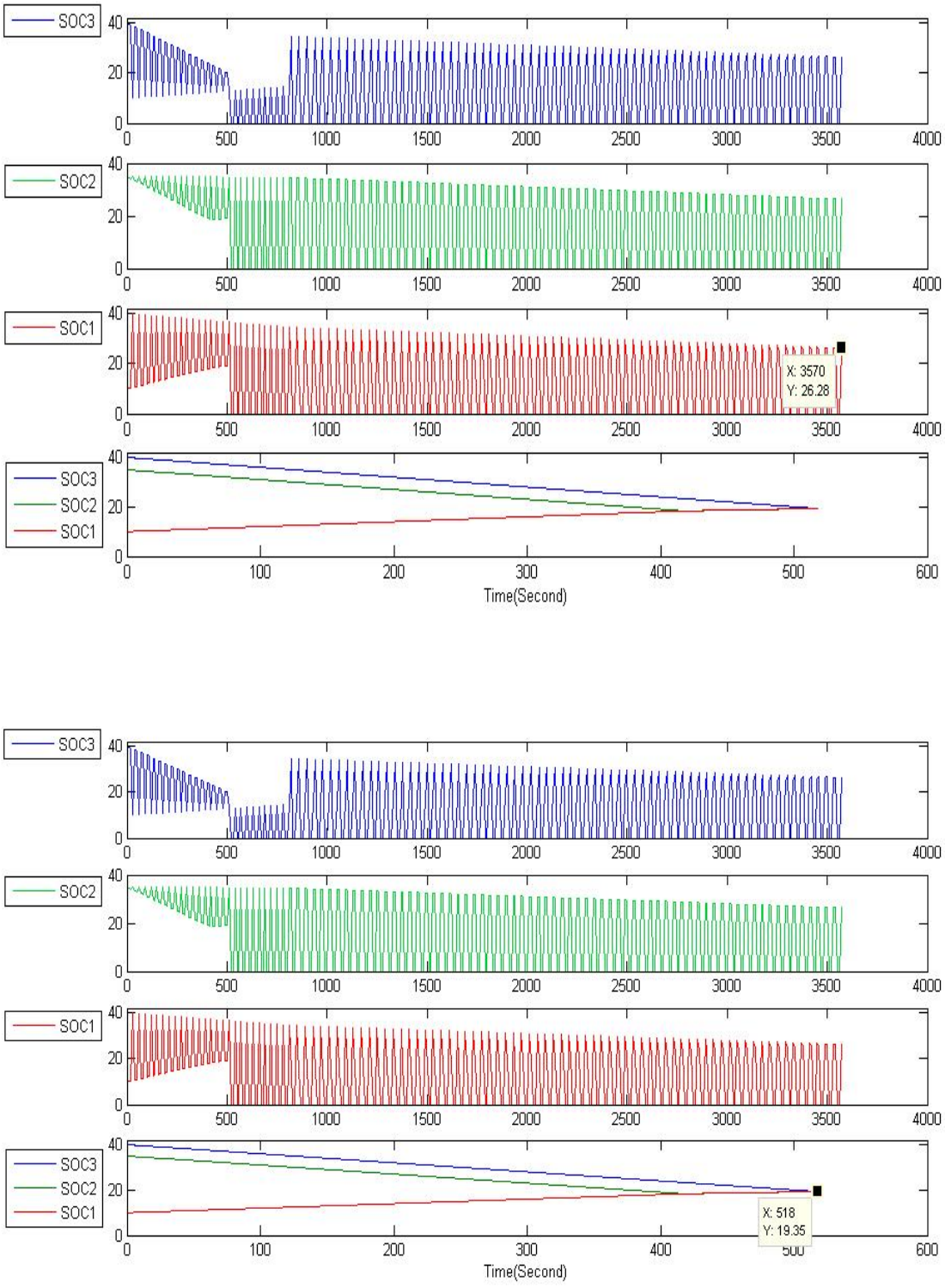

Figure 29. SOC comparison between cell to cell balancer and cell to battery balancer each one having 3 cells. First three graphics are related to SOC of three cells with SOC 40, 35 and 10 using

cell to cell balancing topology, and bottom graphic depicts SOCs of three cells in a cell to battery balancer.

6.3 Flux imbalance elimination

Current passing through MOSFET 3 and 4 in figure 15 are depicted in figure 30.
Current mode control system, keep the peak currents equal. So flux imbalance won't happen. Output resistor value is 0.05Ω. Average DC voltage across the output resistor R1 is 0.3 V. So, the whole battery pack is charged with current of 6 A. Peak currents are about 60 A and ($R_{p1} = 5m\Omega, R_{p2} = 5m\Omega$). In Figure 31, secondary output voltage is shown. In figure 32, resistance of primary windings is different ($R_{p1} = 5m\Omega, R_{p2} = 7.5m\Omega$). So, this can cause flux imbalance. But in figure 32 it is shown that peak currents of FETS are equal and flux imbalance won't happen.

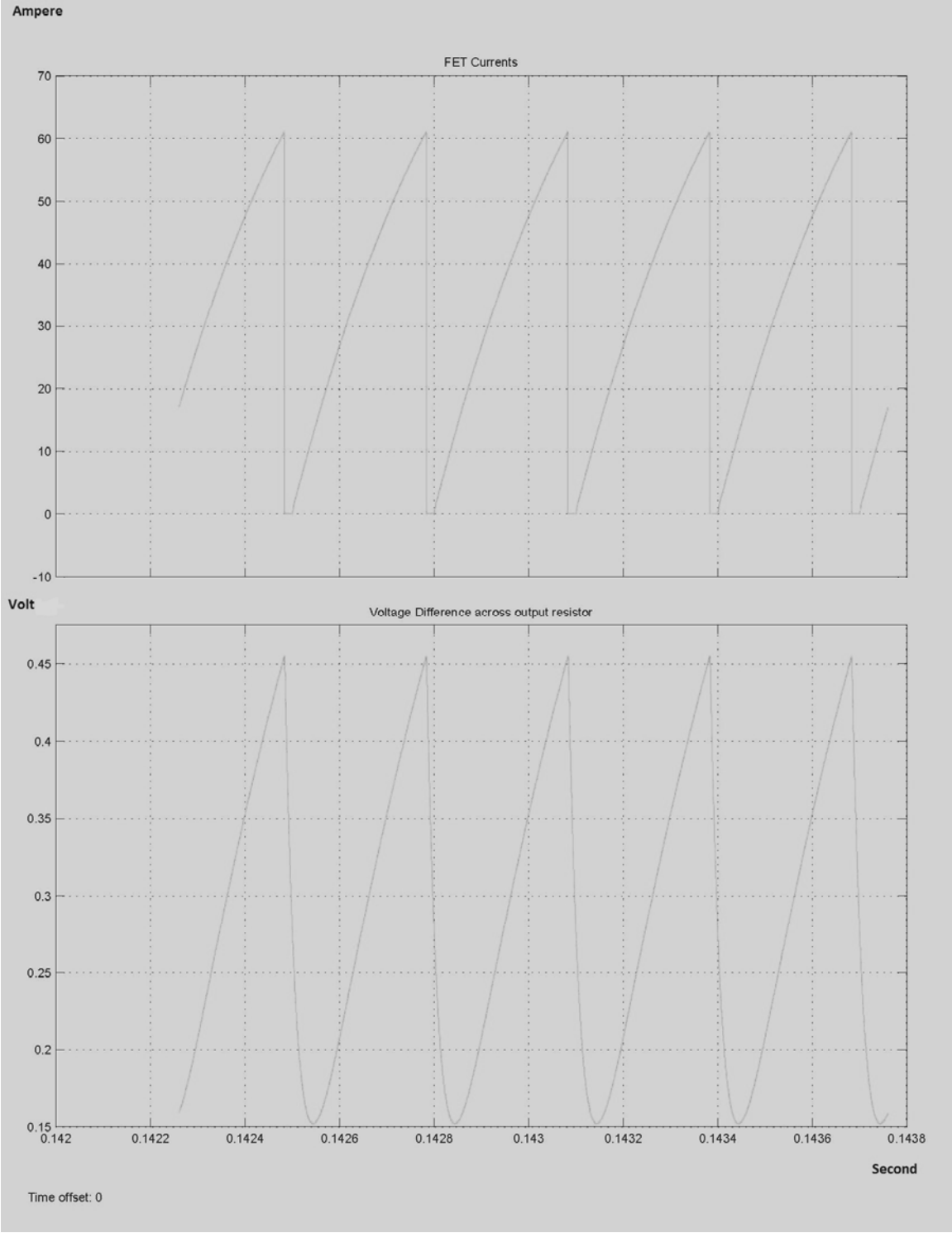

Figure 30. FET currents and voltage across the output resistor. ($R_{p1} = 5m\Omega, R_{p2} = 5m\Omega$).

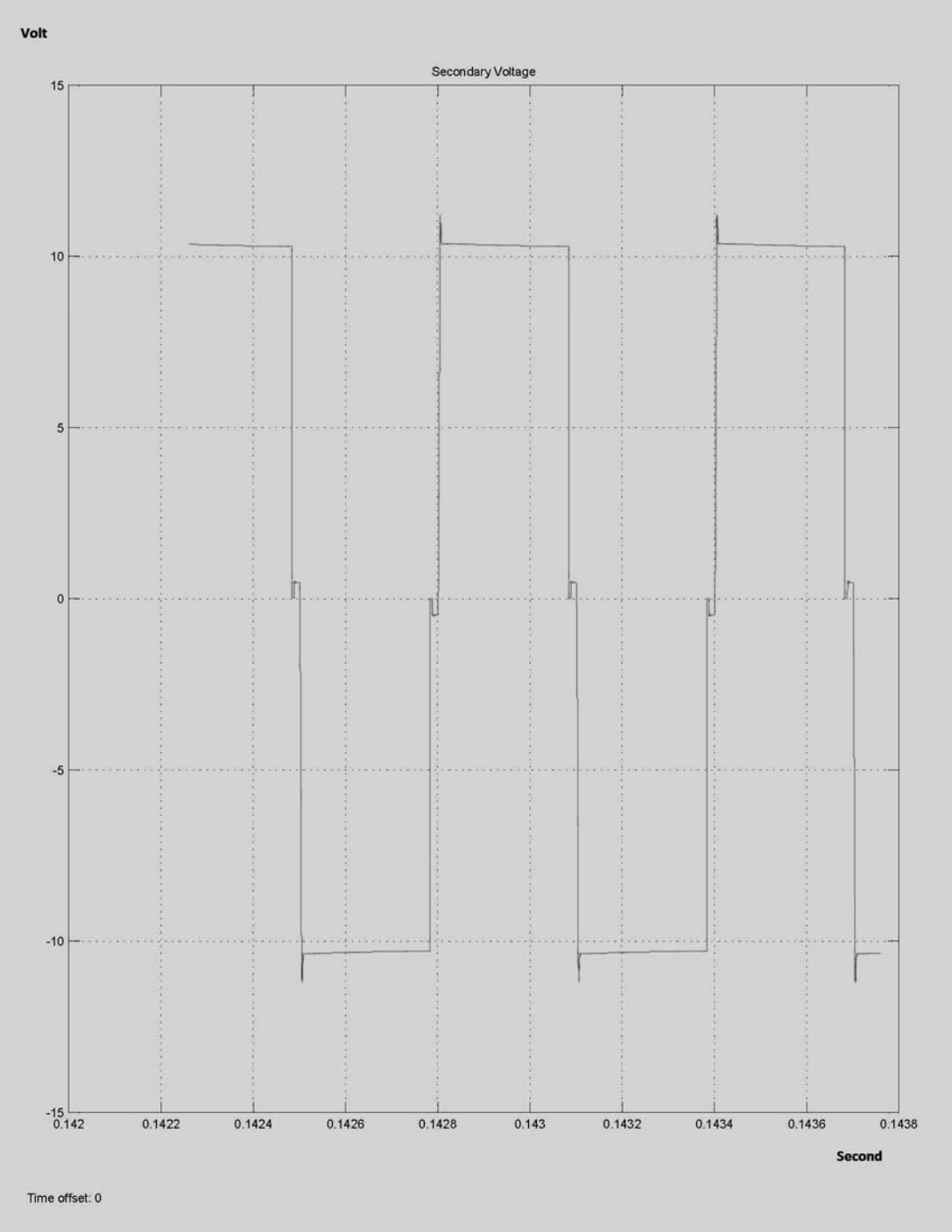

Figure 31. Secondary output voltage of transformer connected to whole battery pack through a bridge rectifier

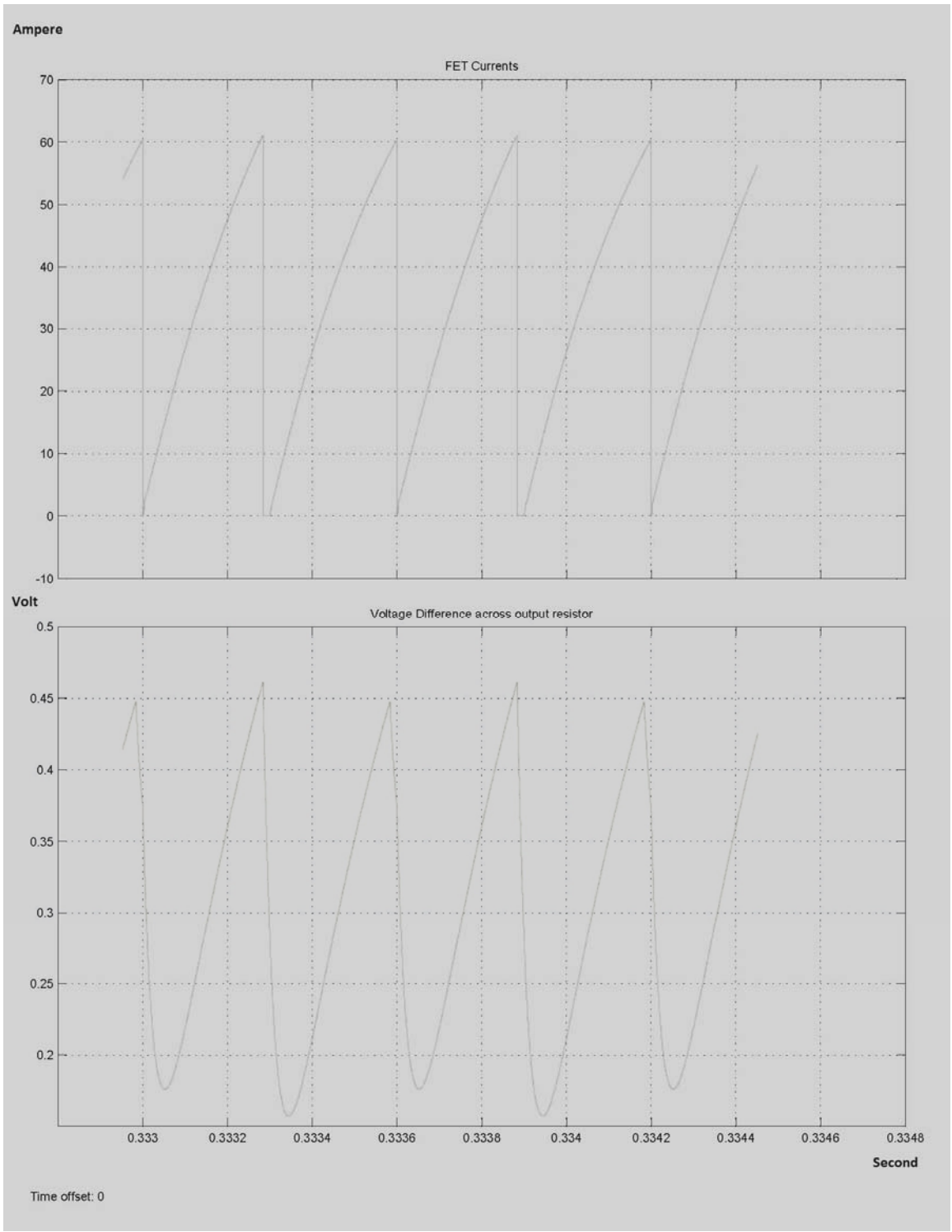

Figure 32. FET currents and voltage across the output resistor. ($R_{p1} = 5m\Omega, R_{p2} = 7.5m\Omega$).

CHAPTER 7

PHYSICAL IMPLEMENTATION OF A CELL TO BATTERY BALANCER

This implementation includes three cells of lithium ion batteries with voltage of 3.7 Volts.

Voltage varies from 3.4 to 4.2 Volts.

I designed three boost converters. Each one connects to one cell directly.

In this design, I performed a test as below:

Two cells have equal and highest voltages and one cell has the lowest voltage.

I charged three cells until their voltage reached 4.25 volts. Then I discharged one of cells until its voltage reached 3.85 volts. Oscilloscope probes were connected to batteries. Their voltages recorded before balancing process starts.

Two converters connected to cells with highest voltage turns on. After 17 minutes voltage of three cells reached to 4.02 volts and three cells got balanced.

In this implementation UCC28085, 8-Pin Current Mode Push-Pull PWM Controllers with Programmable Slope Compensation has been used.

This controller operates at voltage range of 8.3 Volts and 12.5 Volts.

Because each cell voltage ranges from 3.4 Volts to 4.2 Volts and operating voltage of controller is 8.3 Volts to 12.5 Volts, power supplies designed for Current Mode Push-Pull PWM Controllers. Figure 33 indicates a converter. Shutdown command coming from a microcontroller sends to the base of the bipolar transistor working in saturate mode ($V_{ce} = 0.3Volts$), causes to bring down the gate-source voltage of power MOSFETs to $V_{ce} + V_{diode} = 0.3V + 0.5V = 0.8Volts$ (25). So MOSFETs become off.

Figure 35 shows the physical implementation of a cell to battery balancer using three cells.

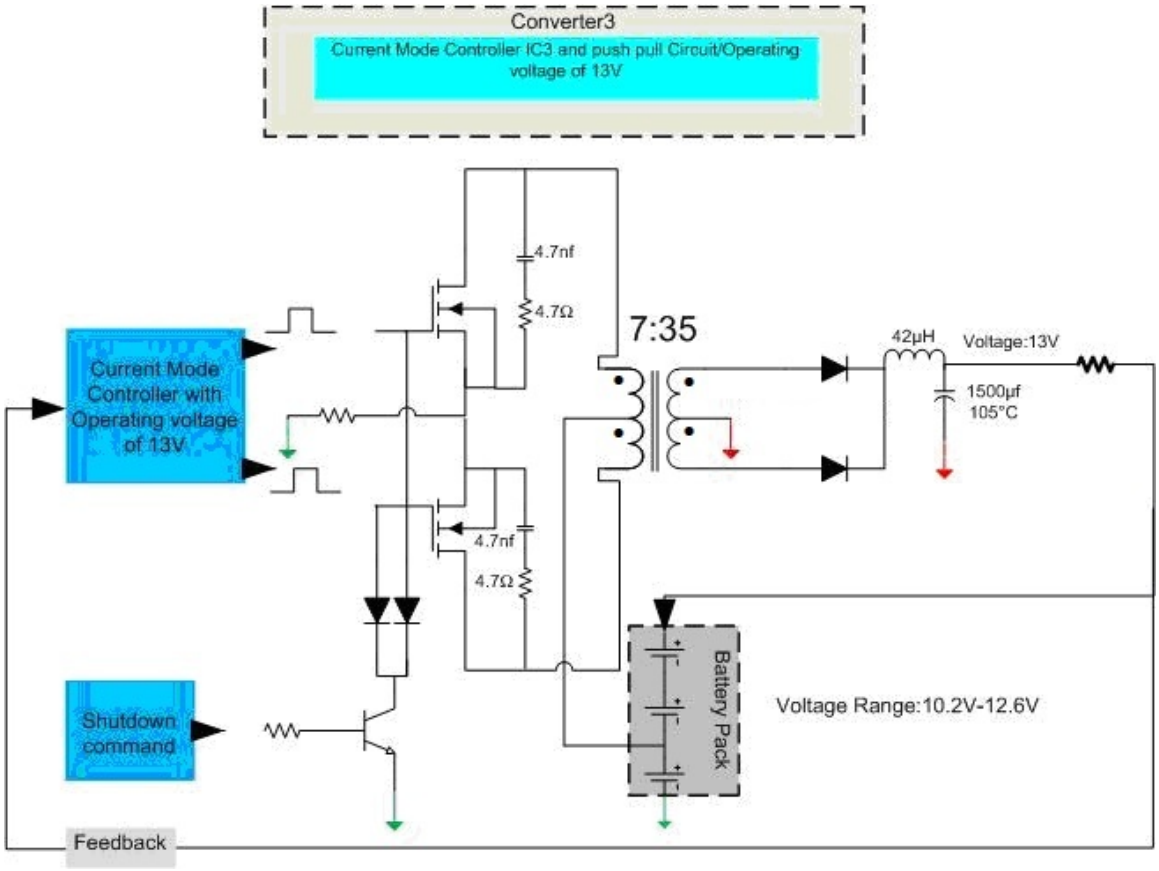

Figure 33. Boost Converter

7.1 Power Supply Design for Current Mode Controller

Cell voltage ranges between 3.4 Volts and 4.2 Volts, and each step-up converter is directly connected to the cells, so it needs to be operational at cell voltage level.

The suggested current mode controller operates above 12.6 Volts.

A converter has been used to provide desired DC voltage for current mode controllers with isolated grounds.

Due to high frequency, fast recovery diodes have been used.

A fast recovery diode will switch off a current in tens of nanoseconds (billionths of a second). A slower diode may take up to one millisecond (thousandths of a second).

During this tiny interval, the diode may produce noise that can interfere with the rest of a circuit.

Capacitors in output filters should be able to abide high temperature (105°C), because in high frequency, high current pulse causes to increase the temperature. These capacitors are well-suited for high frequencies and high current pulse.

$50mA$, Current will be enough to run the current mode controllers.

$$I_D = 50mA, R_{DS(on)} = 0.1\Omega \quad (26).$$

$$V_{Lp(\min)} = (3V_{CC(Cell)} - V_{DS(on)}) = 3.(3.4) - (0.05).(0.1) = 10.2Volts \quad (27).$$

$$V_{Lp(\max)} = (3V_{CC(Cell)} - V_{DS(on)}) = 3.(4.2) - (0.05).(0.1) = 12.6Volts \quad (28).$$

When cells voltage is lowest, 10.2 Volts will be across the primary winding and secondary windings. And when cell voltages are highest, 12.6Volts will be across the primary and secondary windings.

In order to reduce core size and eliminate noise coming out from the circuit, I chose frequency of approximately 20 KHz.

So above voltage range meets the criteria for current mode controller operating voltage.

Figure 34 indicates an external power supply.

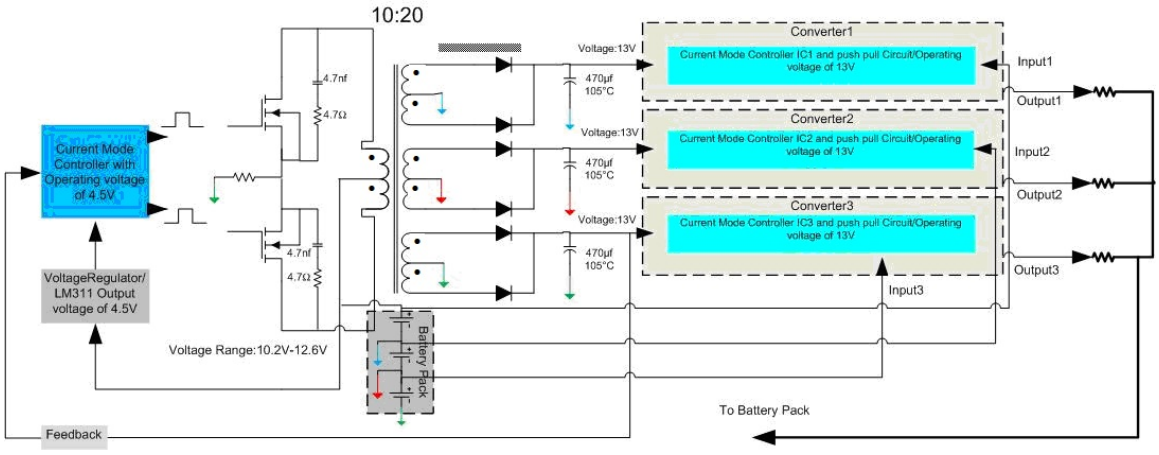

Figure 34. Power Supply for Current Mode Controllers with Separate Grounds

In this design ferrite transformer has three secondary windings with isolated grounds as indicated with green, red and blue colors. Each converter should have its isolated ground connected to negative terminal of its own battery in order for circuit to be operational.

7.2 Transformer Design

7.2.1 Primary, secondary peak and RMS currents

All batteries have a capacity of 2.2A/h, and each battery has a voltage range of 3.7V to 4.2V. So, W/h=(2.2).4.2=9.24 (29).

I want to have the batteries charged with 750mA current at output voltage of 13V, when just one converter is on. So

$$P_{out} = V_{out}.I_{out} = 13V.(0.75A) = 9.75W$$

DC-DC Converter Efficiency=80%

Amplitude of Ipft (Primary flatted-topped) is the value of current at center of the ramp, Fig 22.

$$P_{in} = 1.25.P_{out} = V_{dc}.I_{dc} = V_{dc}.(0.8).I_{pft} \quad (30).$$

$$I_{pft(Max)} = 1.56.\frac{P_{out}}{V_{dc}} = 1.56.\frac{9.75}{3.7} = 4.11A \quad (31).$$

7.2.2 Primary RMS current and wire size

Each primary carries only one of the Ipft pulses per period. So its D (duty cycle) is (0.8T/2)/T or 0.4.

$$I_{rms} = I_{pft}\sqrt{0.4} = 0.632.I_{pft}$$
$$I_{rms} = 0.632.(4.11) = 2.6A \quad (32).$$

Conservative practice in transformer design to operate the windings at a current density of 500 circular mils per rms ampere [4].

A circular mil is the area of a circle 1mil in diameter. Hence, area in square inches is

$\frac{\pi}{4}.10^{-6}$ [4] (33).

So Primary circular mil requirement = 500.(2.6)= 1300

AWG (American Wire Gage) 17 has 2048 C.M. So AWG 17 for primary windings is chosen.

7.2.3 Secondary RMS current and wire size

$$I_{rms(Secondary)} = I_{dc}.\sqrt{0.4} = (0.75).(0.632) = 0.474A \quad (34).$$

$$C.M = 500 * 0.474 = 237 \quad (35).$$

Based on American Wire Gage reference, AWG 25 has 320 C.M.

So for secondary, AWG25 is chosen.

7.2.4 Output filter design

(f) Switching frequency is 20 kHz

$T_{0n} = \frac{V_o T}{2V_1}$ (36). Or $V_1 = 1.25V_0$

$dI = \frac{(1.25V_o - V_o)(0.4T)}{L_o} = 2I_{dc}$ (37). And finally $L_o = \frac{0.05V_o T}{I_{dc}}$ (38).

$V_0 = 13V$

$I_{dc} = 0.75A$

$f = \frac{1}{T} = 20kHz$

Hence, $L_o = \frac{(0.05).13}{(0.75).40.10^3} = 42\mu H$ (39).

7.2.5 Output capacitor design

$C_o = \frac{50.10^{-6}.dI}{V_r}$ (40).

$V_r = 1\%$ Of V_o, so $V_r = (0.01).13 = 0.13V$

$C_o = \frac{50.10^{-6}.2.(1.5)}{0.13} = 1.153mF$ (41). , So $C_o = 1.5mF$,is selected. This range exists in market.

7.2.6 Primary turns selection

Based on Faraday's law:

$V_P = N_p A_e \frac{dB}{dt} 10^{-8}$ (42). , $N_p = \frac{V_p.(0.4).T}{A_e dB}.10^8$

$V_P =$ Primary voltage across a core inductor

$N_p =$ Number of turns per half primary winding

$A_e =$ Iron area of core (cm^2)

$dB =$ Core flux change, 0- $B_{\max}$ (gauss)

dt=time for flux change, 0.4T (seconds)

Let $A_b =$ bobbin winding area, in^2

$A_p =$ Primary winding area, in^2 . $A_s =$ Secondary winding area, in^2 .

$A_{ti} =$ Area of one turn of primary power winding, in^2

SF=0.4 [4], space factor, the fraction of total bobbin winding area occupied by the coil, this includes primary and all secondaries. Half the total coil area devoted to the primary and half to the secondary, $A_p = A_s$

$$A_p = 0.2\,A_b = 2\,N_p A_{ti}, A_{ti} = \frac{0.1A_b}{N_p} \quad (43).$$

Current density in circular mils per RMS ampere, $D_{cma} = \frac{A_{tcm}}{I_{rms}}$ (44).

A_{tcm} = Wire area in circular mils and I_{rms} = rms current per half primary

Area in square inches equals area in circular mils times $\frac{\pi}{4}.10^{-6}$

Now $A_{ti} = A_{tcm}(\frac{\pi}{4}).10^{-6}$

$$A_{tcm} = 0.1273\frac{A_b}{N_p}10^6 \quad (45).$$

Then, $I_{rms} = 0.1273\frac{A_b 10^6}{N_p D_{cma}}$ (46).

$$P_{in} = 1.25P_{out} = V_{dc}I_{dc} = V_{dc}(0.8)I_{pft} \quad (47).\ ,\ P_{out} = 0.64V_{dc}I_{pft} \quad (48).$$

$$I_{rms} = I_{pft}\sqrt{0.4}\ ,\ I_{pft} = 1.58I_{rms} \quad (49).$$

$$P_{out} = (0.64)V_{dc}(1.58)I_{rms} = 1.01V_{dc}I_{rms} = 0.129\frac{V_{dc}A_b 10^6}{N_p D_{cma}} \quad (50).$$

$V_{dc} = V_P = N_p A_e \frac{dB}{dt}10^{-8}$, and in a push pull converter flux swing is $2\,B_{\max}$

$$P_{out} = 0.129(N_p A_e)\frac{2B_{\max}}{0.4T}\frac{A_b}{N_p D_{cma}}10^{-2} = \frac{0.00645B_{\max} fA_e A_b}{D_{cma}} \quad (51).$$

If A_b is expressed in square centimeter, then $P_{out} = \frac{0.001B_{\max} fA_e A_b}{D_{cma}}$ (52).

D_{cma} is assumed 500 [4], and $B_{\max}$ is assumed 1200 gauss

$P_{out} = 9.75W$, $f = 20khz$, then $A_e A_b = 0.203\,cm^4$, **EE375 core, which has** $A_e A_b = 0.9\,cm^4$, and **has** $A_e = 0.9\,cm^2$, and $A_b = 1\,cm^2$ [4] is selected.

$$N_p = \frac{V_p 0.4T}{A_e dB} 10^8 = \frac{(4.2)(0.4)}{1(1200)(20000)} 10^8 = 7 \quad (53).$$

7.2.7 Secondary turns selection

I assume, power MOSFET has $R_{on} = 0.08\ \Omega$, and $I_{pft(Max)} = 4.11A$, then

$V_{dc(Drain-Source)} = (4.11)(0.08)$=0.325 V (54).

$$V_{out} = [(V_{cell} - V_{(Drain-Sorce)}) \frac{N_s}{N_p} - V_{diode}] 2 \frac{t_{on}}{T} \quad (55).$$

$V_{out} = 13$ Volts, $t_{on} = 0.4T$

$V_{(Drain-Sorce)}$=0.5 V (56).

$V_{cell} = 4.2V, R_{on} = 0.08\Omega$ (Transistor on resistance)

$N_s = 28$

In order not to have maximum pulse width, I selected 35 turns for secondary.

7.2.8 Snubbers design

Figure 24 shows the snubber circuit. This circuit is not only used to work as snubber but also to provide the higher voltage for gate of MOSFETS, when battery voltage decreases resulting in decrease of gate voltage. As the gate voltage increases, drain current increases. Gate voltage of power transistors for a good drain current needs to be between 10-12 Volts.

Voltage difference across the capacitor is cell voltage.

$\Delta V_c = 4.2V$

Capacitor current at t^{-0}, time before the switch is on, is 8.22 amperes

$I_c = 4.11A$

And this happens within 0.5 μs

So, $I_c = C\frac{dV_c}{dt}, C = \frac{(4.11)(0.5)10^{-6}}{3.7} = 0.5\mu f$ (57).

7.2.9 Rectifier design

Breakdown voltage of rectifiers

In worst case (no load), $V_{PIV} = V_{Cell}\frac{N_S}{N_P}2 = (4.2).5.2 = 42Volts$ (58). And due to spikes in secondary this voltage might reach to 100 Volts. Rectifiers with breakdown voltage of 100 volts are recommended.

Current of fast recovery diodes

$I_O = \frac{P_O}{V_O} = \frac{10}{13} = 0.9A, I_{D(dc)} = \frac{0.9}{2} = 0.45A$ (59).

Power loss on rectifier diodes

$P_{diode} = V_f I_O \frac{t_{on(\max)}}{T} = (0.5)(0.9)(0.45) = 0.2025W$ (60).

$P_{loss(Bridge)} = (0.2025)4 = 0.81W$ (61).

Fast recovery diodes with above criteria are selected.

CHAPTER 8

EXPERIMENTAL RESULTS

I designed the schematic using Design explorer 99 and then put the electronic components on the PCB. Figure 35 indicates the whole diagram including three Lithium Ion cells with voltage of 3.7 Volts. Each cell has a step-up converter connected to it. If state of charge, here I meant voltage, of one cell or two cells are more than the third cell or two other cells, converters which are connected directly to cells with highest voltage get turned on. So the excess charge is transferred from cells with highest voltage to whole battery pack. Figure 36 shows one step up converter. Figure 37 shows the voltage of the cell with lowest voltage of 3.85 Volts before being balanced. Figure 38 shows voltage of two cells which are same with highest voltage of 4.25 Volts before being balanced. Two converters connected to the cells with highest voltage turned on. After 17 minutes, voltage of cell with lowest voltage increased to 4.04 Volts and voltage of two cells with highest voltage decreased to 4.02 Volts, and three cells became balanced. Figures 39 and 40 show the voltages.

Figure 41 indicates the current of two power transistor passing through a 0.05 ohm-resistance. Peak currents in each cycle are equal, and controlled. Peak current amount is for both transistors is 60mv divided by common resistor 0.05ohm which equals to 1.2 amperes. So, flux imbalance won't happen. UCC28084 and UCC28085 which are current mode controllers with operating voltage of 4.5 Volts and 12.5 Volts have been used to control the pulse width of power transistors based on the peak current of power transistors. Current amount fed to the battery pack is controlled as below:

I wanted to have a constant voltage at output of boost converters, this voltage can be defined by multi turn potentiometers. Voltage on battery pack can change from 10.2 Volts to 12.6 Volts. Output of converters through a 0.127 ohm resistor is connected to battery pack. This resistance can be smaller than this value to reduce loss in resistor. If I want to have output voltage of 12 volts, pulse width changes until output voltage reaches

to 12 volts. So it keeps the voltage across the 0.127 ohm resistor constant, consequently constant current.

If output voltage decreases, $V_o \downarrow$, error amplifier voltage increases, $V_{ea} \uparrow$, and cause more current, $I \uparrow$, to pass through transistors by increasing the pulse width of gates, resulting in output voltage increase.

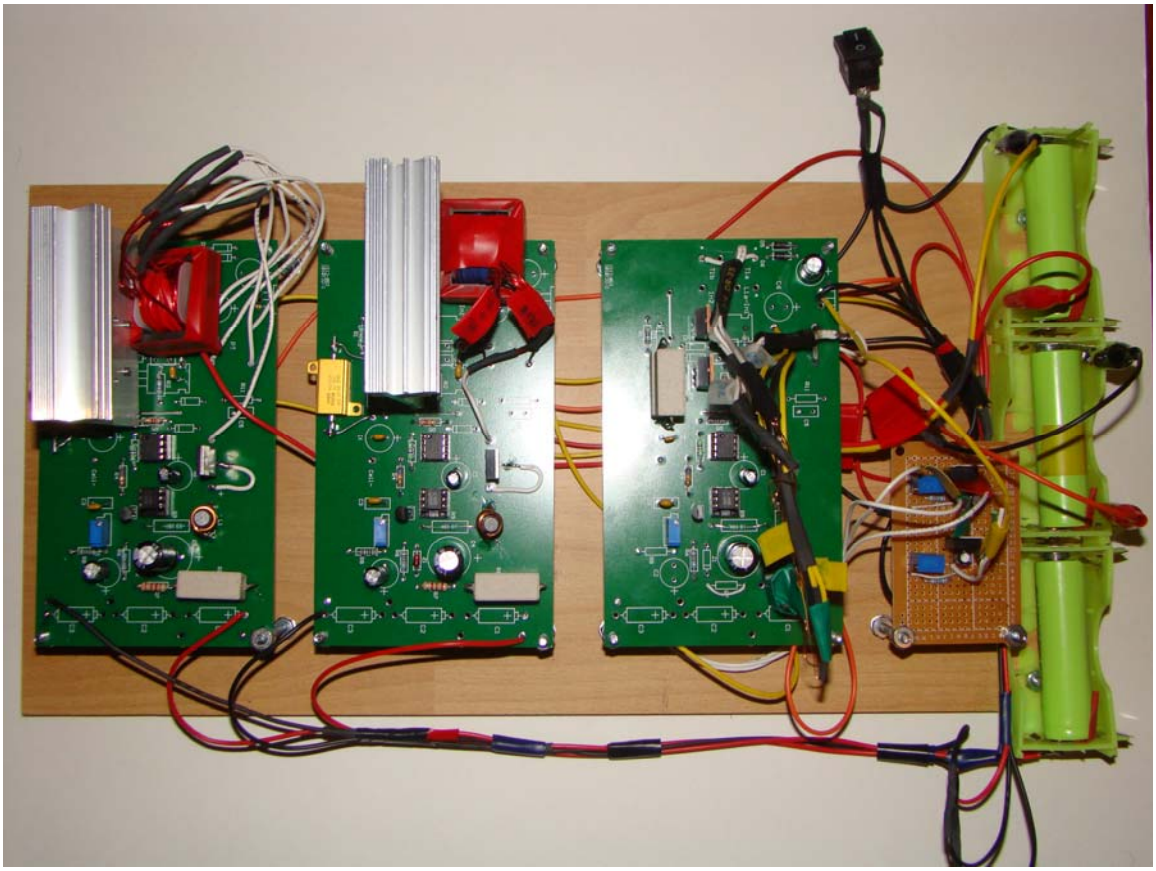

Figure 35. Cell to battery balancer with three cells, two left PCBs are converters and right PCB is external power supply with three secondary winding with isolated ground.

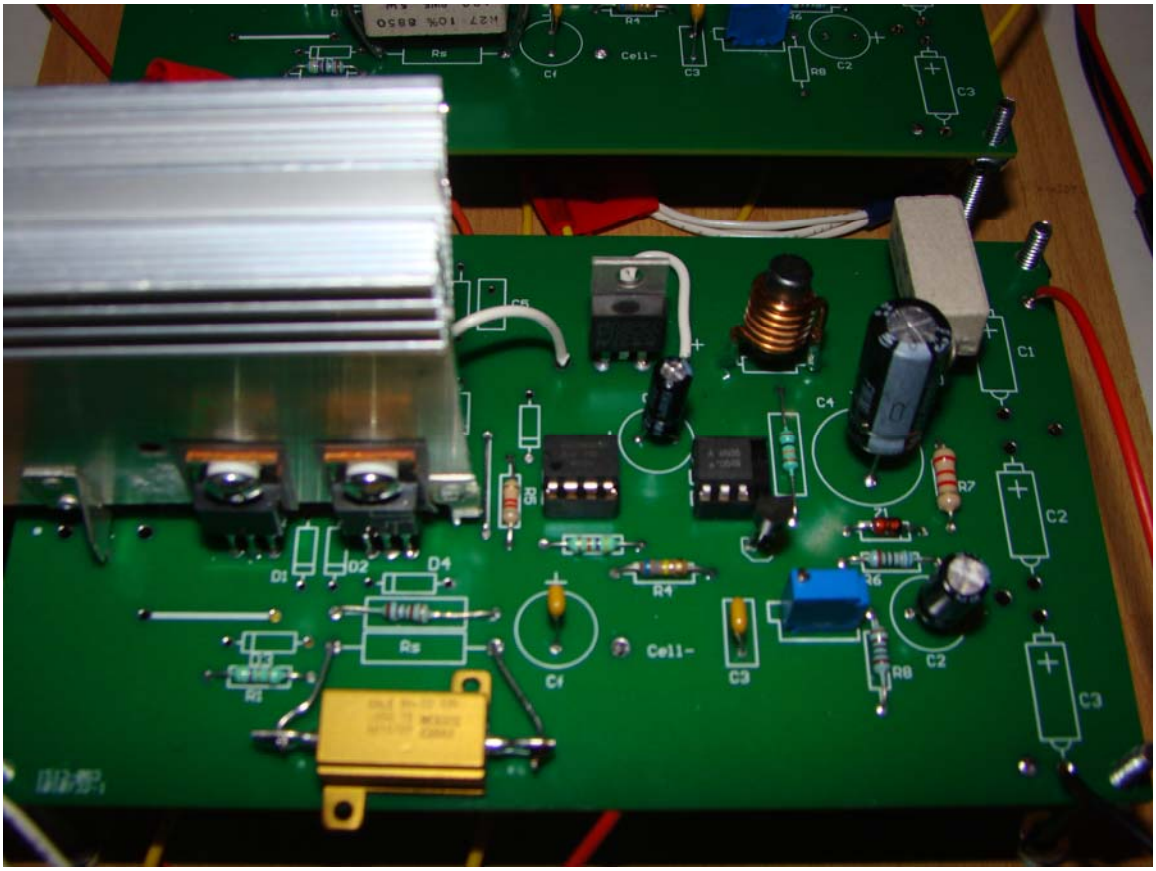

Figure 36. Step up converter indicating power transistors attached to the heat sink, 0.05-ohm-resistor controlling peak currents, output filter, current mode controller, fast recovery diodes, ferrite core transformer behind the heat sink.

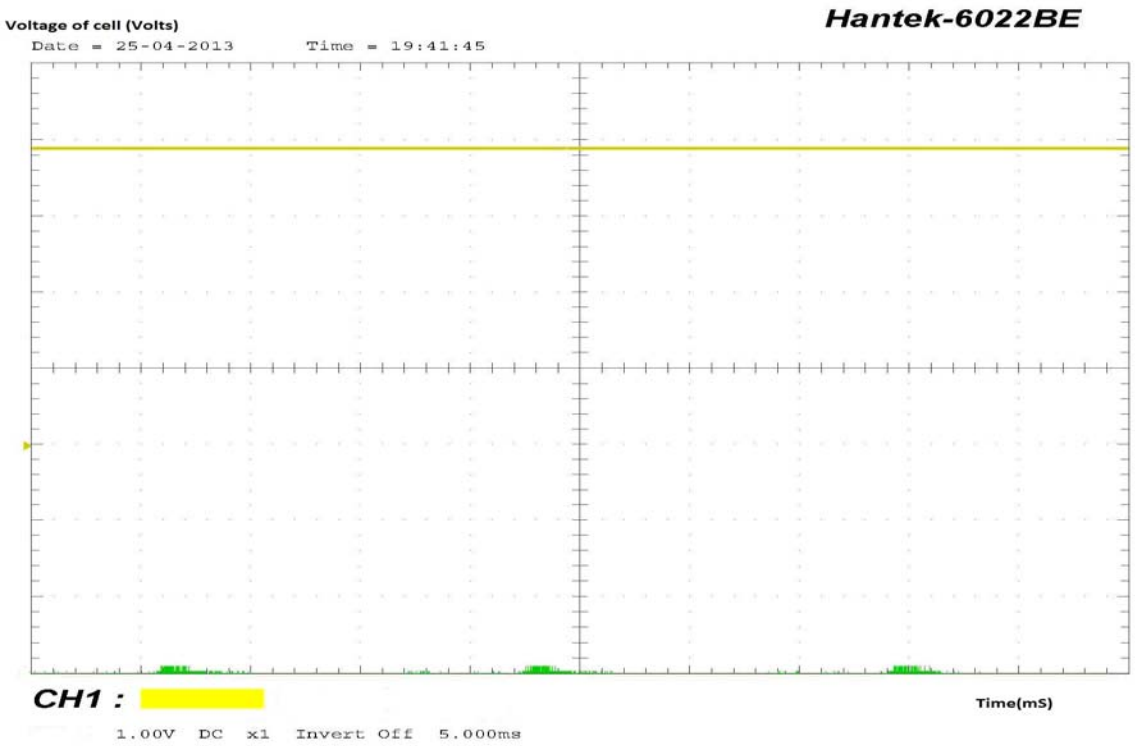

Figure 37. Voltage of cell with lowest SOC before being balanced which is 3.85 volts.

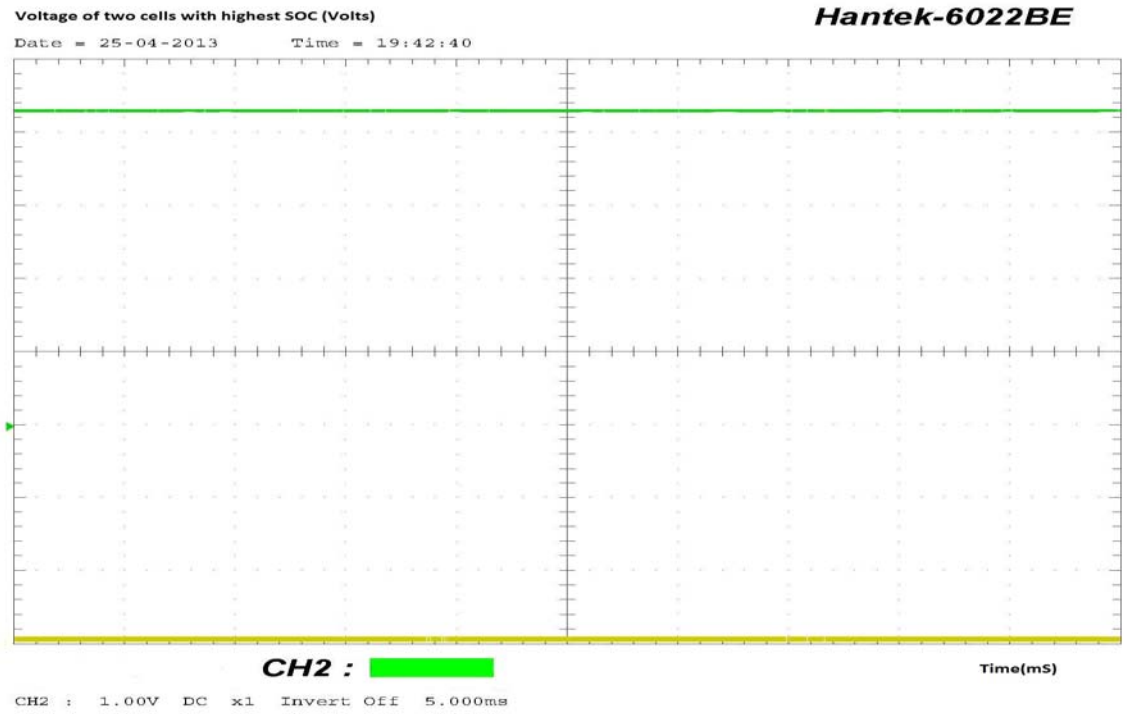

Figure 38. Voltage of two cells with highest SOC which are same before being balanced which is 4.25 volts.

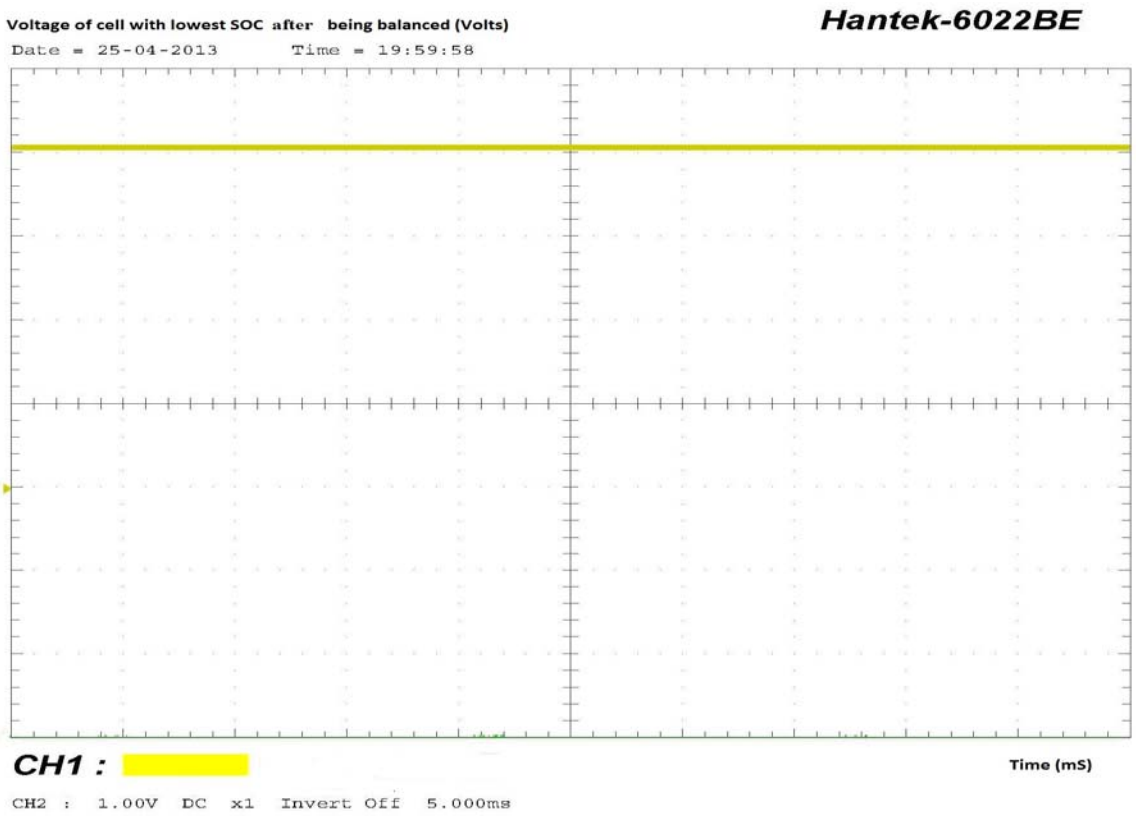

Figure 39. Voltage of cell with lowest SOC after being balanced which is 4 volts.

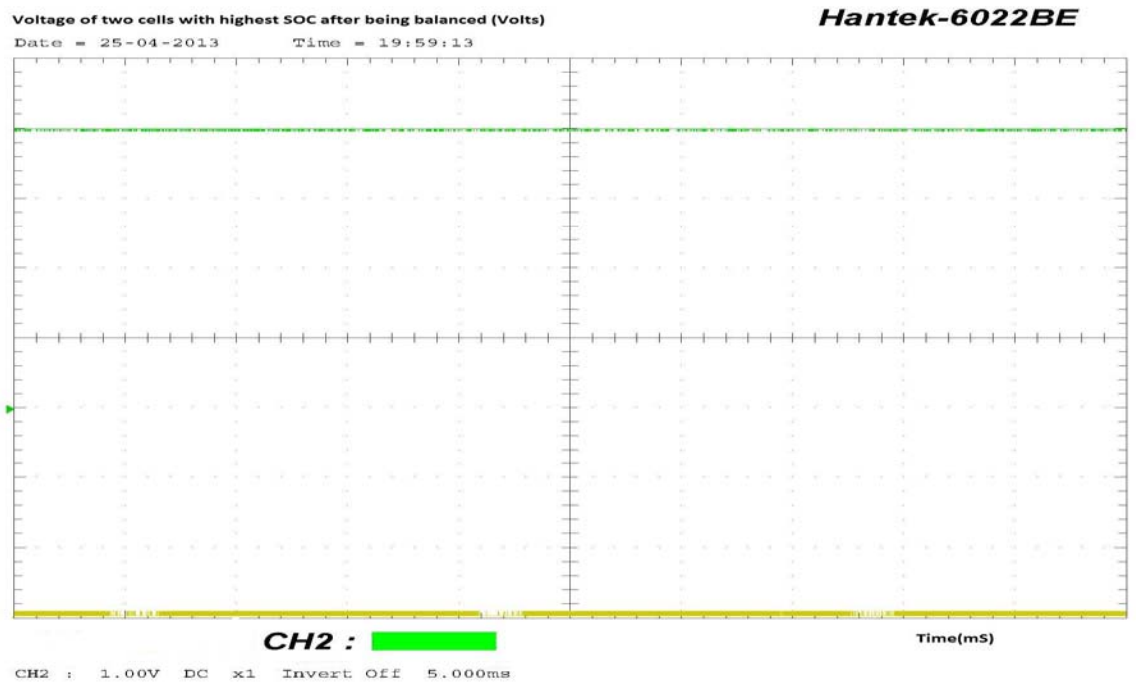

Figure 40. Voltage of two cells with highest SOC which are same after being balanced which is 4 volts.

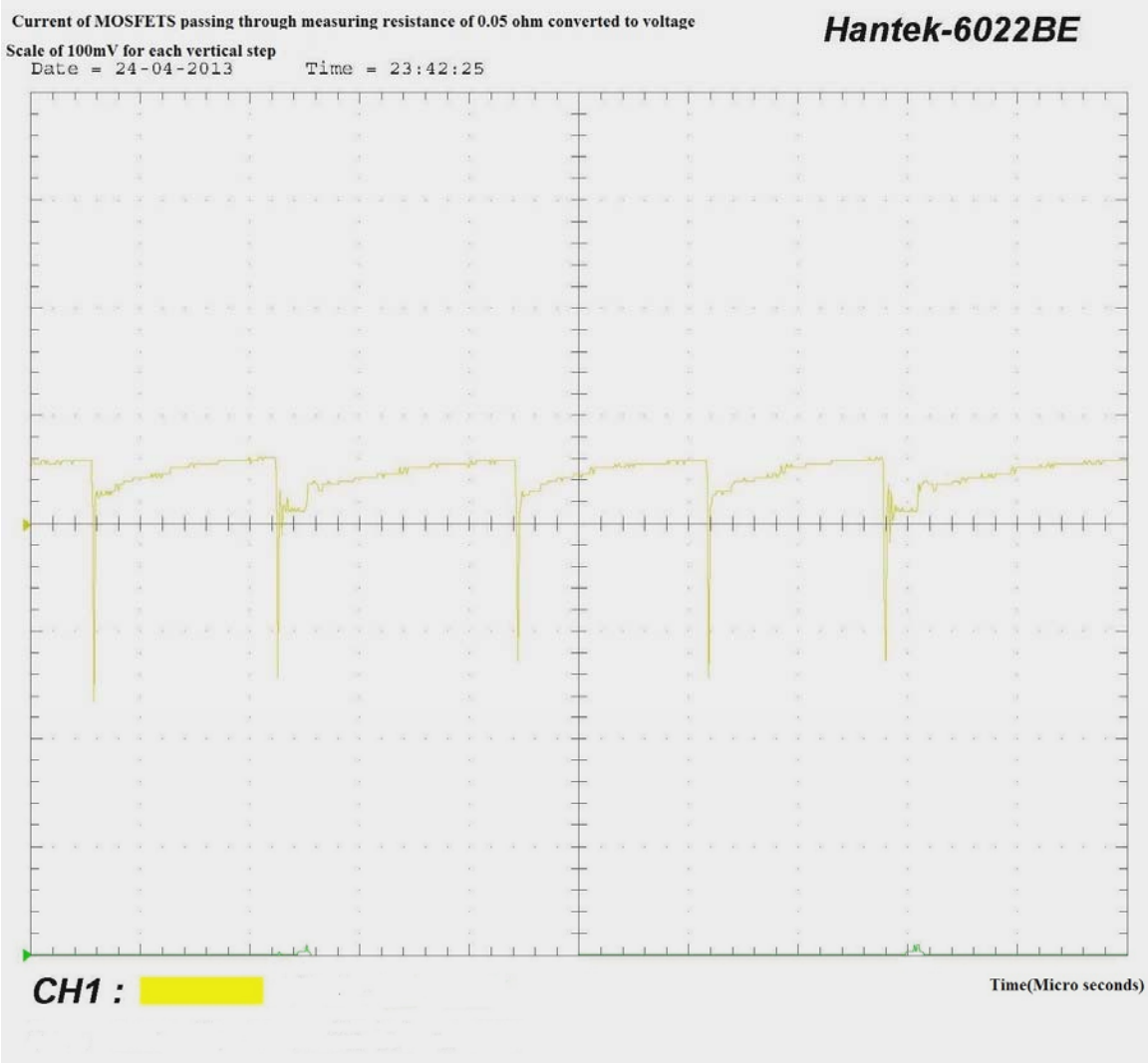

Figure 41. Current of MOSFETS passing through 0.05 ohm converted to voltage.

CONCLUSION

This thesis describes the subject of active balancing methods used in BMS with aid of simulation models and physical implementation. Simulations offer advantage of using current mode controllers in Push-Pull topology which are used at high powers. Other topologies won't stand high power converters. Flux imbalance causing asymmetrical hysteresis loop in a ferrite or magnetic core, exists at push-pull topology used in poor design of converters and this results in destroying power transistors. Current mode topology prevents this issue from happening. Simulation compares speed of balancing for two different active balancing systems, cell to cell using single inductor and cell to battery using step-up converters and results indicated that for a battery pack including three cells, a cell to battery balancer could balance SOC of three cells within 518 seconds, 3052 seconds sooner than a cell to cell balancer using single inductor.

The project was physically built to demonstrate the behavior of an improved BMS transferring charge between cells. Physical implementation is focused on cell to battery balancer. By using a microcontroller, cell voltages can be measured in real time and based on these measurements, commands to each converter is defined. So the balancing time can be reduced. Especially where there are large numbers of cell for example in solar plants. Important tasks of a real BMS include control of the charging process and monitoring of the discharging process to prevent damage to the battery.

Advantage of using a cell to battery balancer over cell to cell balancer is within the less time rather than a cell to cell balancer, all cells can be balanced.

In a cell to battery balancer which uses step-up converters using push pull topology; it is likely for harmonics in secondary windings to be created.

Transformers are also restricted in their performance by the magnetic flux limitations of the core. For ferromagnetic core transformers, saturation limits of the core must be taken into account. Ferromagnetic materials in poor designs tend to be in saturate mode at a certain level which is defined by the material and core dimensions. That means further increases in magnetic field force (mmf) do not result in proportional increases in magnetic field flux.

As a transformer's primary winding is overloaded from excessive current, the core flux is more likely to reach saturation levels during peak voltage. With help of a current mode controller, flux imbalance is eliminated, plus it causes the power transistors not to be destroyed due to flux imbalance and power transistors will last longer. The major benefit of a cell to battery balancer BMS using current mode controllers is a decrease in cost and size by eliminating the need to replace destroyed power transistors and by improved handling of cell-to-cell variation in parameters and aging compared to conventional BMS. The current mode approach can use cells and transistors with more parameter variation, reducing maintenance and warranty costs compared to the conventional BMS. This active BMS enhances performance, reliability of the battery pack.

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