BROADBAND MICROWAVE AMPLIFIERS IN DEEP SUB-MICRON CMOS

BROADBAND MICROWAVE AMPLIFIERS IN DEEP SUB-MICRON CMOS TECHNOLOGY

By

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Abstract

Thanks to geometry scaling, CMOS is becoming the technology of choice for the implementation of radio-frequency and microwave integrated circuits. While CMOS has several advantages over other technologies, such as low-cost and the possibility to integrate analog and digital circuitry on the same chip, its use for high-frequency analog circuits also presents several challenges, because there are some areas where scaling has impaired instead of improving the active and passive device performance. While several techniques can be used to minimize these undesirable effects, many of them only work over very narrow frequency bands; the implementation of circuits that achieve a desired performance over a very wide frequency band is thus a major challenge. Moreover, with further reduction of the transistor dimensions, new effects, such as gate current due to quantum-mechanical tunneling through the gate oxide, will become increasingly significant.

This thesis deals with the analysis and design of CMOS broadband amplifiers. A distributed amplifier in a 0.18 μm standard CMOS technology was designed, implemented and measured. It achieves a bandwidth of 2-13 GHz with a 6 dB gain, and better than -9 dB input and output reflections, while consuming 86 mW from a 1.8 V supply and using 2.6 x 1.3 mm^2 of chip area. The variation of the amplifier characteristics with temperature was studied in the range from 25 °C to 125 °C. It was found that the forward gain and noise figure change significantly with temperature, while the reflection coefficients, reverse gain and group delay are largely unaffected.

A resistive-match amplifier was implemented in 0.18 μm CMOS technology. It has an average gain of 6.5 dB in the 2-7 GHz band with a noise figure lower than 5.4 dB, with input reflection coefficient of less than -3.5 dB and output reflection coefficient of less than -5 dB. It consumes 18.4 mW from a 1.8 V supply, and occupies 1.28 x 0.55 mm^2 of chip area. It was found that the gain reduction with temperature is much smaller than that of the distributed amplifier.

Finally, the effect of the gate tunneling current on the high-frequency performance of MOSFETs is studied, in terms of the changes that the gate current causes to their noise parameters and unity current gain frequency. It was found that the gate current noise affects mostly the optimum source conductance G_{opt} and the minimum noise figure NF_{min} at relatively low frequencies, while the noise resistance R_n, the optimum source susceptance B_{opt} and the unity current gain frequency remain largely unaffected. It was also found that, according to the projected future scaling of MOSFETs, the gate current noise will likely have a significant effect on G_{opt} and NF_{min} at RF and microwave frequencies.

A model was also developed to calculate the power spectral density of the source and drain noise currents caused by tunneling. This model is suitable for compact simulation, and was verified using published numerical simulations and measured data for ultra-thin oxide MOSFETs.

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Symbols

a	Flicker noise exponent
A	Amplitude of transfer function
B_{opt}	Optimum source susceptance for minimum noise figure
B_s	Source susceptance
C	Correlation coefficient
C_A	Chain form of the noise correlation matrix of a linear two-port network
C_{bpass}	DC blocking capacitor
C_d	Drain line capacitance in a distributed amplifier
C_{eq}	Correlation coefficient between gate and drain tunneling noise
C_{FET}	FET capacitance (input or output)
C_g	Gate line capacitance in a distributed amplifier
C_{gb}	Small-signal gate-body capacitance
C_{gc}	Gate-channel capacitance
C_{gd}	Small-signal gate-drain capacitance
C_{gg}	Total small-signal gate capacitance (gate-source and gate-drain)
C_{gs}	Small-signal gate-source capacitance
C_i	Correlation coefficient of channel thermal noise and induced gate noise
$C_{i,j}$	Element of noise correlation matrix (i-th row, j-th column)
C_m	Capacitance of m-derived matching section
C_{ov}	Capacitance of gate and source/drain overlap
C_{ox}	Capacitance between spiral inductor and substrate
C_{ox}^*	Gate oxide capacitance per unit area
C_{oxd}	Capacitance between spiral inductor and substrate (differential)
C_p	Underpass capacitance in spiral inductor
C_{pad}	Capacitance of chip bonding pads
C_{probe}	Capacitance of DC probe

C_{sb}	Small-signal source-body capacitance
C_{shot}	Correlation coefficient of gate and drain shot noise currents
C_{sub}	Substrate capacitance of spiral inductor
C_{subd}	Substrate capacitance of spiral inductor (differential)
C_u	Transmission line capacitance per unit length
d	Distance from spiral inductor to the substrate
E_c	Conduction band energy
E_v	Valence band energy
f	Frequency
f_{0dB}	Unity gain frequency of an amplifier
f_{ctun}	Frequency below which the contribution from GTC to the noise parameters is equal to the contribution of the channel thermal noise
f_H	Upper frequency limit
f_L	Lower frequency limit
f_{max}	Unity power gain frequency
f_o	Center frequency
f_{peak}	Frequency at which the inductor quality factor has a maximum
f_{self}	Frequency at which the inductor quality factor is zero
f_t	Unity current gain frequency
f_{to}	Unity current gain frequency (without gate current)
G	Power gain
GD	Group delay
g_{do}	Channel conductance at zero drain bias
G_{lf}	Low-frequency power gain
g_m	Transconductance
G_{opt}	Optimum source conductance for minimum noise figure
G_s	Source conductance
G_{subd}	Substrate conductance of spiral inductor (differential)
$h(t)$	Impulse response of a linear system

$H(\omega)$	Transfer function of a linear system
$\hbar$	Planck's reduced constant
i_d	Drain noise current
I_D	DC drain current
i_{deq}	Equivalent drain noise current due to tunneling
i_{dsot}	Drain shot noise current
i_g	Gate noise current
I_G	DC gate current
I_{GB}	Gate-body current
I_{GC}	Gate-channel current
I_{GD}	Gate-drain component of gate-channel current
$I_{GD,ov}$	Gate-drain overlap current
i_{geq}	Equivalent gate noise current due to tunneling
I_{GS}	Gate-source component of gate-channel current
i_{gshot}	Gate shot noise current
$I_{GS,ov}$	Gate-source overlap current
i_n	Input-referred noise current of a linear two-port network
i_{Rd}	Source resistance noise current
i_{Rdb}	Drain-body resistance noise current
i_{Rs}	Source resistance noise current
j	Imaginary unit
J_G	Gate current density
k	Boltzmann's constant
k_1	Carrier mobility temperature factor
k_2	Threshold voltage temperature factor
K_D	Drain flicker noise current factor
K_G	Gate flicker noise current factor
l	Transmission line length
L	MOSFET's effective channel length

L_{seff}	Effective spiral inductance
L_d	Drain line inductance in a distributed amplifier
L_{drawn}	MOSFET drawn channel length
L_g	Gate line inductance in a distributed amplifier
L_{m1}, L_{m2}	Inductances of *m*-derived matching section
L_{probe}	Inductance of DC probe
L_s	Series inductance of spiral inductor
l_{tot}	Total spiral inductor length
L_u	Transmission line inductance per unit length
m	Design parameter of *m*-derived matching sections
m_{ox}	Effective mass of electrons in the oxide
n	Number of stages
N	Number of carriers
n_f	Number of fingers in multi-finger MOSFET
NF	Noise figure
NF_{50}	Noise figure with a 50 Ω source impedance
NF_{min}	Minimum noise figure
n_{opt}	Optimum number of stages
N_t	Effective trap density
p	Gate current partition ratio
q	Charge of the electron
Q	Quality factor
Q_{LF}	Low-frequency quality factor
r	Inductor radius
R_d	Drain resistance
R_{db}	Drain-body resistance
r_{ds}	Drain-source incremental resistance
R_g	Gate resistance
R_o	System's characteristic impedance

R_{od}	Low-frequency impedance of drain line in a distributed amplifier
R_{og}	Low-frequency impedance of gate line in a distributed amplifier
R_{om}	Real impedance seen on one arm of m-derived matching sections
R_{sp}	Series resistance of spiral inductor
R_s	Source resistance
R_{sh}	Sheet resistance of polysilicon gate
R_{sub}	Substrate resistance of spiral inductor
R_n	Noise resistance
r_T	Tunneling resistance
S	Staggering factor
$S_{i,j}$	Element of scattering-parameter matrix (i-th row, j-th column)
SiO_2	Silicon dioxide
S_x	Spectral density of signal x
$S_{x,y}$	Cross-spectral density of signals x and y
T	Absolute temperature
t_{ox}	Gate oxide thickness
T_{ref}	Reference temperature
V_C	Cascode transistor gate biasing voltage
V_{drain}	Drain biasing voltage
V_{DS}	DC drain-source voltage
V_{gate}	Gate biasing voltage
v_{gs}	Small-signal gate-source voltage
V_{GS}	DC gate-source voltage
V_{GT}	Gate overdrive voltage
v_n	Input-referred noise voltage of a linear two-port network
V_{Rg}	Gate resistance noise voltage
V_{TH}	Threshold voltage
v_p	Normalized phase velocity of transmission line
w	Spiral inductor width

CPW	Coplanar Waveguide
D/A	Digital/Analog
EOT	Equivalent Oxide Thickness
EM	Electro-Magnetic
FBW	Fractional Bandwidth
FCC	Federal Communications Commission
FET	Field Effect Transistor
GaAs	Gallium-arsenide
GTC	Gate Tunneling Current
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HF	High Frequency
HP	High-Performance
IEEE	Institute of Electrical and Electronic Engineers
InP	Indium-phosphide
ITRS	International Technology Roadmap for Semiconductors
LFN	Low-Frequency Noise
LNA	Low-Noise Amplifier
LOP	Low Operating Power
LSTP	Low Standby Power
MESFET	Metal-Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
nMOSFET	n-channel MOSFET
PA	Power Amplifier
pMOSFET	p-channel MOSFET
PSD	Power Spectral Density

RF	Radio Frequency
SCE	Short-Channel Effect
SDH	Synchronous Digital Hierarchy
Si	Silicon
SiGe	Silicon-germanium
SOI	Silicon-on-Insulator
STM	Synchronous Transport Module (Optical communications standard)
TEM	Transverse Electro-Magnetic
TWA	Traveling-wave Amplifier
UWB	Ultra-Wideband
VLSI	Very Large Scale Integration
VSWR	Voltage Standing-Wave Ratio

Chapter 1
Introduction

1.1. CMOS FOR HIGHLY INTEGRATED AND LOW-COST MICROWAVE INTEGRATED CIRCUITS

Ever since the invention of the semiconductor integrated circuit, there has been an emphasis into integrating as much functionality as possible into a single chip to reduce the size and cost of electronic systems and to simplify their assembly [1].

In the logic or digital domain, Very Large Scale Integration (VLSI) has been achieved in Complementary Metal-Oxide-Semiconductor (CMOS) and Bipolar-CMOS (BiCMOS) technologies, which use silicon as a substrate, that allow for the integration of millions of transistors on a single chip. Also, it has become very common to integrate some analog functions, such as analog-digital (A/D) and digital-analog (D/A) converters in the same chip as the logic elements.

The integration of active and passive components in a single semiconductor substrate for microwave applications, known as Monolithic Microwave Integrated Circuits or MMICs, was first attempted in silicon technology; however, the high losses of the semiconductor substrate were unacceptable for microwave applications [2]. The use of semi-insulating gallium arsenide (GaAs) as a substrate provided better performance, further enhanced by the relatively higher speed of operation provided by GaAs MESFETs compared to silicon devices (due mainly to the higher mobility of electrons in GaAs with respect to Si) [2]. More recently, other technologies such as indium phosphide (InP), and the development of new high-speed devices such as high electron mobility transistors (HEMT) and heterojunction bipolar transistors (HBT) have further increased the frequency of operation of MMICs.

The last decade, however, has seen two trends that are changing the MMIC landscape. First, the "digital revolution", enabled mainly by CMOS device scaling, has

created devices in silicon that can operate at gigahertz frequencies. As shown in Fig. 1.1, MOSFETs can achieve frequencies of operation well above those of early GaAs metal-semiconductor FETs (MESFETs), and even comparable to GaAs HBTs. Second, the use of digital wireless and optical communications has increased significantly, and consumer markets demand more and more bandwidth with the lowest possible cost.

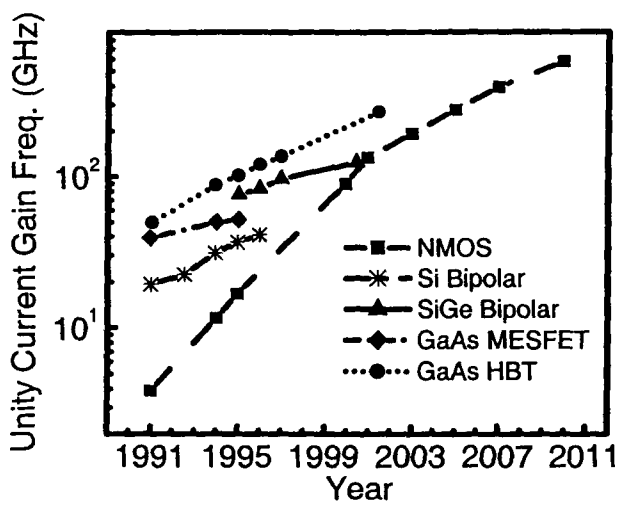

Fig. 1.1. Unity current gain frequency for various transistor technologies [3]. NMOS technology future projections are from the International Roadmap for Semiconductors (ITRS).

Both of the above trends have made CMOS one of the technologies of choice for the implementation of low-cost and highly integrated gigahertz-speed circuits and systems [4], [5]. While silicon-germanium (SiGe) BiCMOS technology also offers low cost and high levels of integration, sometimes with lower power consumption than CMOS, many believe that whenever CMOS can offer the desired performance, it will be the preferred technology [7].

CMOS MMICs however present several challenges, so new circuit techniques and topologies must be devised, and the old topologies have to be adapted to account for these challenges. Some of the most difficult circuit blocks to implement in CMOS (or in any

technology) are broadband amplifiers; the applications and general requirements for this kind of circuit are discussed next.

1.2. BROADBAND AMPLIFIERS: APPLICATIONS AND REQUIREMENTS

Amplifiers that work over a broad frequency range, from the megahertz or kilohertz range (or even zero-frequency) up to the gigahertz range, find applications in various fields such as optical communication systems and broadband radio for wireless communications and ranging. As shown in Fig. 1.2, signals in these applications have frequency components over very broad bandwidths; this in contrast, for example, to conventional narrowband radio-frequency systems, where the signal occupies a relatively small bandwidth around a center frequency. One measure of how "broadband" a signal is, is the fractional bandwidth (*FBW*), defined as

$$FBW \equiv \frac{f_H - f_L}{f_o} \tag{1.1}$$

where f_H and f_L are the limits at which the signal spectral density is below a certain level, and f_o is the center frequency, given by $(f_H - f_L)/f_o$.

Consider now three applications that operate in the gigahertz frequency range, and compare their fractional bandwidths: The IEEE 802.11a standard for Wireless Local-Area Networks uses a 200 MHz bandwidth centered around 5.25 GHz [38], which gives a fractional bandwidth of 3%. Ultra-Wideband (UWB) systems, in contrast, use fractional bandwidths in excess of 25% (this is a common definition of UWB); for example in the US, the FCC has allocated the band between 3.1 GHz and 10.6 GHz for unlicensed operation of UWB equipment [39]; this translates into a fractional bandwidth requirement of 109% if the full band is used. Finally, in the SDH (Synchronous Digital Hierarchy) standard STM-64 for optical communications, the bit rate is 10 Gbit/s, and the front-end bandwidth must extend down to 8 kHz [40]; assuming the high-end of the bandwidth matches the data rate (10 GHz), the fractional bandwidth in this case is 200%.

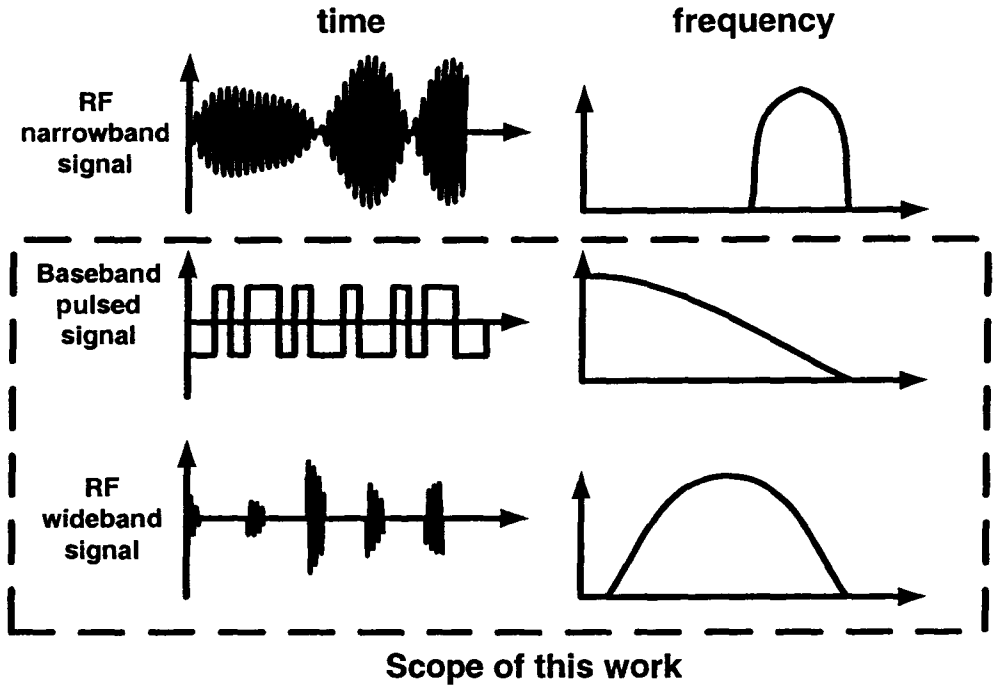

Fig. 1.2. Typical waveforms in the time and frequency domains for three applications of GHz-speed analog circuits: Conventional narrowband Radio-Frequency (RF) communications systems, digital optical communications systems and wideband RF systems for communications and ranging.

The most basic requirement for an amplifier that works with broadband signals is to provide a relatively constant gain in the band of interest in order to minimize signal distortion. Also, the phase of the transfer function should be a linear function of frequency if it is desired to amplify pulses with a very short duration. Indeed, if the transfer function of the amplifier is given by

$$H(\omega) = A\angle\phi(\omega) = A\angle -\omega\tau \tag{1.2}$$

where A and $\phi=-\omega\tau$ are the amplitude and phase of $H(\omega)$ respectively (A and τ are constants), then the impulse response will be

$$h(t) = A\delta(t-\tau) \tag{1.3}$$

which is essentially the same as the input but scaled and shifted in time; deviations from (1.2) will give raise to signal distortion; of course, if the input signal is not an infinitesimal impulse but a signal with a finite bandwidth, the requirement of constant gain and linear phase are limited to that bandwidth. To quantify the "linearity" of the phase, the group delay is defined as

$$GD \equiv \frac{\partial \phi}{\partial \omega} \tag{1.4}$$

and should be as constant as possible in the band of interest.

Fig. 1.3(a) shows the front-end of a typical optical communication system. On the transmitting side, an optical modulator is driven by a broadband amplifier, and on the receiving side, the signal has to be amplified (again by a broadband amplifier) after being converted from the optical to the electrical domain by the photodetector. Fig. 1.3(b) shows a generic front-end for an UWB transceiver. There are several ways to implement the front-end: with down/upconversion mixers, with correlators, or even direct Analog-Digital/Digital-Analog conversion. All front-ends, however, require at least a means to amplify the received signal, and to apply the signal to the transmitting antenna. Both of these require broadband amplifiers.

In both applications, the amplifier used in the receiver must not add much noise to the input signal (it should have low noise figure), and should also provide enough gain to bring the signal to acceptable levels for the following stages. The amplifiers on the transmitting side must handle large signal levels with little distortion, and should provide large amounts of power with high efficiency; in this thesis, however, the focus is on small-signal and low-noise amplifiers.

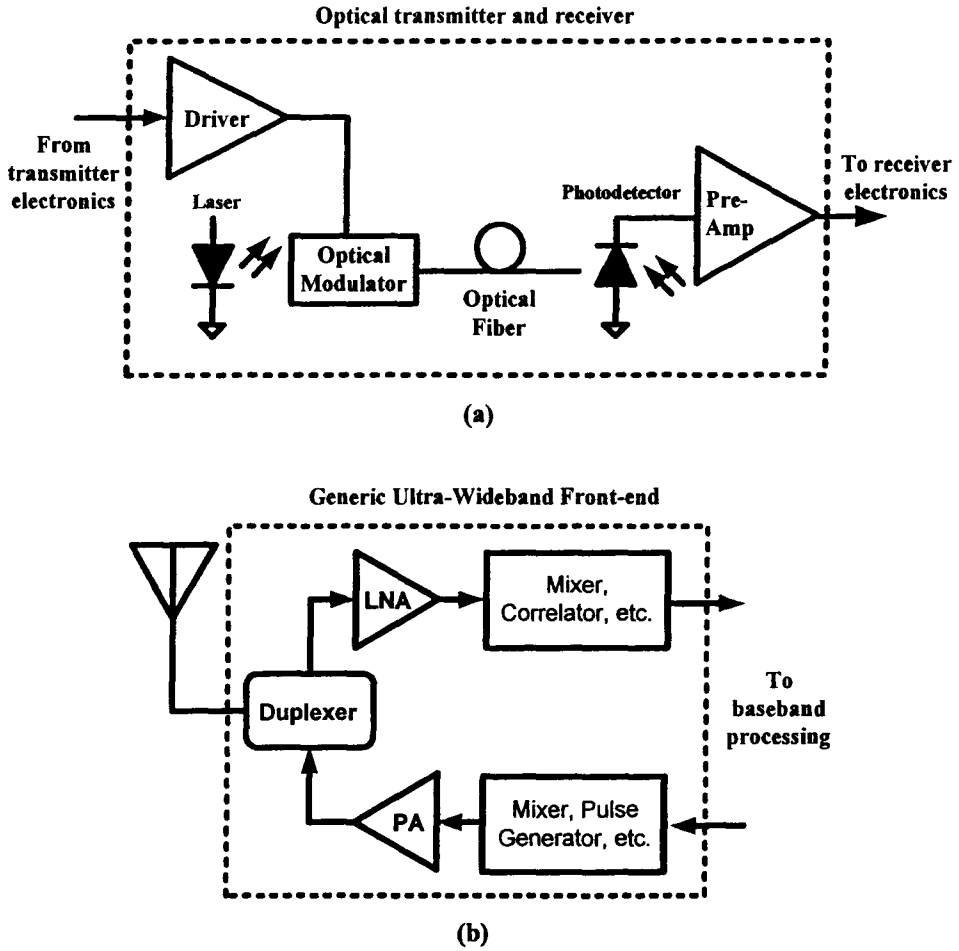

Fig. 1.3. Two typical applications of broadband amplifiers: (a) Optical communications system and (b) Ultra-Wideband radio. The pre-amplifier, driver, low-noise amplifier (LNA) and power amplifier (PA) require broadband amplifiers.

At RF and microwave frequencies (above a few hundred megahertz), circuits are often characterized in terms of Scattering parameters or *S*-parameters. As shown in Fig. 1.4, for a two-port network the parameters S_{11} and S_{22} are essentially the reflection coefficients when the other port is terminated with an impedance equal to R_o, so they must be kept as low as possible (R_o is the impedance of the system used to measure the S-parameters, typically R_o=50 Ω). The parameter S_{21} is related to the forward gain of the

network (the power gain is equal to $|S_{21}|^2$). The parameter S_{12} is related to the reverse transmission of the amplifier, and quantifies how good the output- input isolation is.

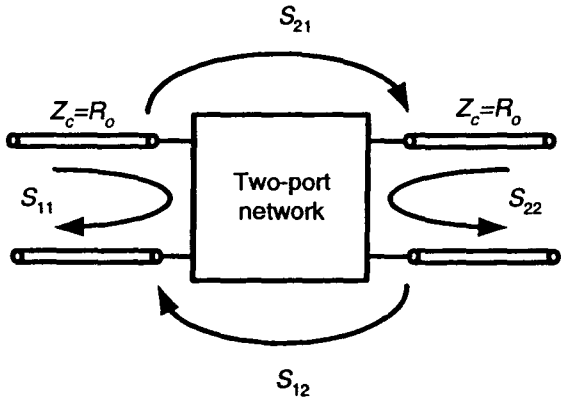

Fig. 1.4. S-parameters of a two-port network.

Another important performance specification for an amplifier is its DC power consumption, especially for portable applications. The circuit should also maintain the minimum required performance over the full temperature range under which it is meant to operate.

The implementation of high-frequency broadband amplifiers is particularly challenging in CMOS technology, because unlike in narrowband amplifiers, the capacitances that limit the high-frequency performance of MOSFETs cannot be resonated using inductors. In this thesis, two broadband amplifier configurations are explored, their designs are explained in detail and the measured performance of both circuits are presented and discussed.

1.3. GATE CURRENT IN MOS DEVICES

MOSFET geometry scaling has enabled the increase in operating frequencies in CMOS analog and digital circuits. As shown in Fig. 1.5, both the lateral dimensions (channel length) and the vertical dimensions (gate oxide thickness) are reduced in every technology generation. The reduction in oxide thickness, which has the purpose of

controlling Short-Channel Effects (SCE) and enhancing the control of the channel by the gate, also has an undesirable effect: carriers can tunnel through the thin oxide causing a gate current.

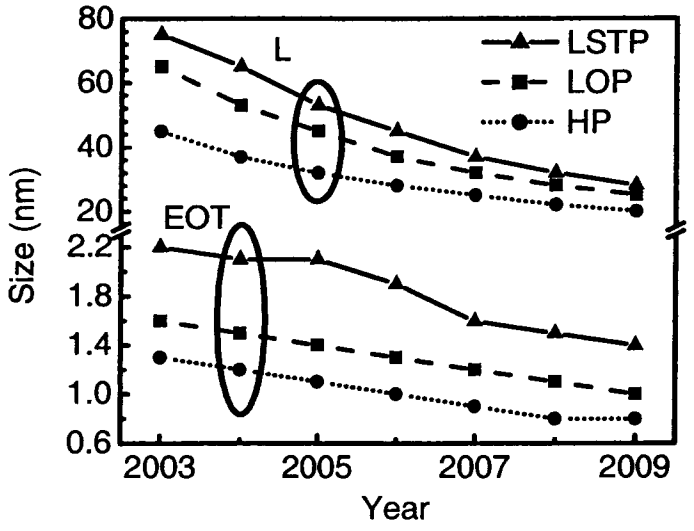

Fig. 1.5. Short-term projections of effective channel length (L) and equivalent oxide thickness (EOT) for Low Standby Power (LSTP), Low Operating Power (LOP) and High-Performance Logic (HP) technologies from the 2004 International Technology Roadmap for Semiconductors (ITRS) [14].

Fig. 1.6 shows the schematic band diagram of a Polysilicon-Oxide-Silicon structure with a very thin oxide. When the oxide thickness is below 2-3 nm, a significant gate current can be observed due to carriers tunneling through the potential barrier of the oxide; this is a purely quantum mechanical effect that has no classical explanation.

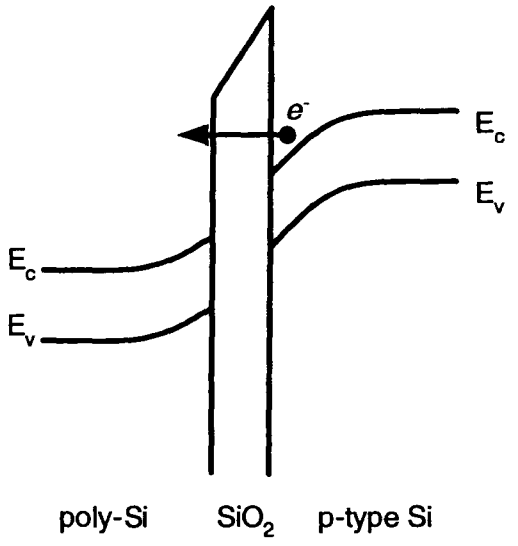

Fig. 1.6. Band diagram of a polySi-SiO_2-pSi structure showing direct tunneling through the oxide potential barrier. E_c is the conduction band and E_v is the valence band.

As shown in Fig. 1.7, gate current is right now a major obstacle for future MOS scaling; for high-performance logic, a point will be reached where the power dissipation caused by gate current is comparable to the static power dissipation from other leakage mechanisms such as sub-threshold conduction. Several solutions are being investigated, most of them involve replacing nitrided silicon dioxide with alternative gate dielectrics with a higher dielectric constant, which should allow using thicker oxides. These solutions, however, are not yet suitable for mass production, and it is likely that MOSFETs with significant gate currents will be the norm for some future technology generations.

For this reason, we study in this thesis the effect of gate current on the high-frequency performance of MOSFETs.

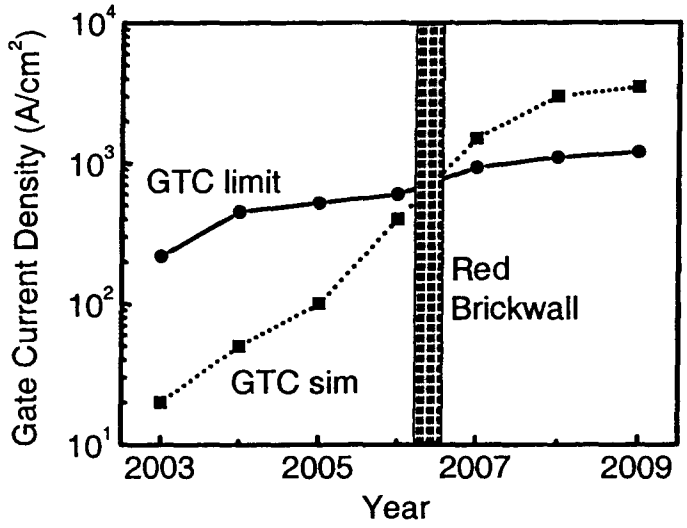

Fig. 1.7. ITRS 2004 simulated gate leakage current ("GTC sim") and gate current limit ("GTC limit") for High-Performance Logic (HP) [14]. The gate current limit is calculated from power dissipation considerations.

1.4. ORGANIZATION OF THE THESIS

In Chapter 2 some of the characteristics of CMOS devices relevant for the design of microwave amplifiers are reviewed, with special emphasis on MOSFETs and integrated inductors and transmission lines.

Chapter 3 presents the theory of broadband distributed amplifiers, including the basic concept and design equations, as well as some of the challenges faced when implementing these in CMOS technology. A review of the published CMOS distributed amplifier implementations is also presented in this chapter.

The detailed design and the measured performance characteristics of a distributed amplifier implemented in a standard 0.18 μm CMOS technology are presented in Chapter 4.

In Chapter 5, the design and measured performance of a CMOS resistive-match amplifier are presented, and its performance is compared to the distributed amplifier.

Chapter 6 deals with the effect of gate tunneling current on the high-frequency and noise performance of MOSFETs.

Finally, in Chapter 7, the main results and conclusions of the thesis are summarized, and some ideas for future work are presented.

Chapter 2
CMOS for RF and Microwave Applications

2.1. INTRODUCTION

Despite the advantages of the use of Silicon as a substrate for monolithic integrated circuits – high thermal conductivity, mechanical stability, low-cost raw material, high yield, ease of growing of a high quality insulator [6] – its use for microwave applications remained a challenge until recent years, because of the poor high-frequency performance of active and passive devices. The improvements in active and passive devices that have enabled their use in microwave applications, as well as some of the remaining challenges, are discussed in section 2.2, specifically in the context of CMOS technology.

In section 2.3 the temperature effects in CMOS devices are reviewed, and the noise properties of MOSFETs are considered in section 2.4.

2.2. CMOS MICROWAVE INTEGRATED CIRCUITS

Complementary Metal-Oxide-Semiconductor (CMOS) technology, introduced in the 1960's [8], is largely responsible for the rapid growth of digital circuit and systems applications in the last two decades. CMOS enables the implementation of digital circuits with low static power dissipation, very good fan-in and fan-out, good noise margins, large levels of integration and its performance has continuously improved due primarily to geometry scaling and improved fabrication technologies.

In addition to this, CMOS is a very mature technology which has been researched extensively and has very high yield levels; this has made it one of the lowest cost technologies for integrated circuit implementation. Thanks to geometrical scaling, the cost and high levels of integration of CMOS can also be leveraged for high-frequency (HF) analog applications, up to the microwave range.

Some of the most important characteristics of CMOS passive and active devices for HF applications are reviewed next.

2.2.1. Sub-micrometer MOSFETs for microwave applications

Fig. 2.1 shows the simplified cross-section of a short-channel MOSFET. A small-signal equivalent circuit when the device operates in saturation is shown in Fig. 2.2. The dimensions W, L_{drawn} and L are the channel width, the drawn channel length and the effective channel length. The total overlap between the drain-source areas and the gate

$$\Delta L = L_{drawn} - L \tag{2.1}$$

is due to the lateral diffusion of the drain and source implants.

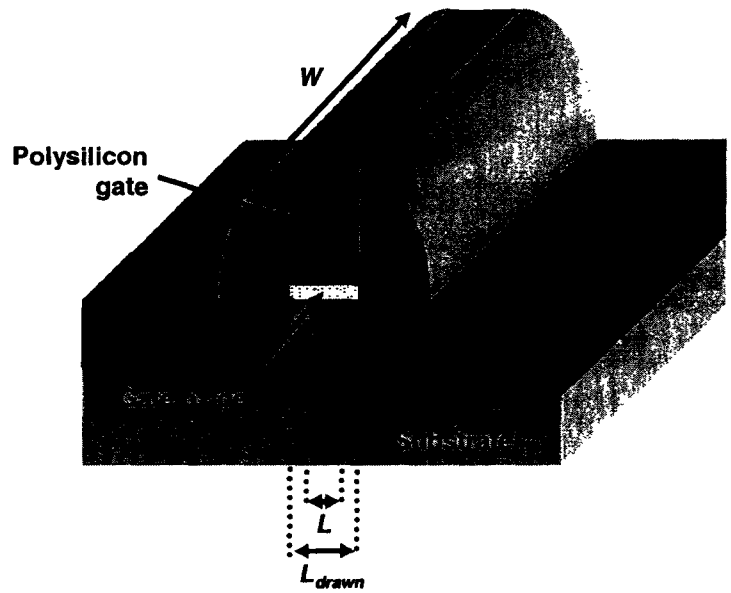

Fig. 2.1. Simplified cross-section of a short-channel MOSFET.

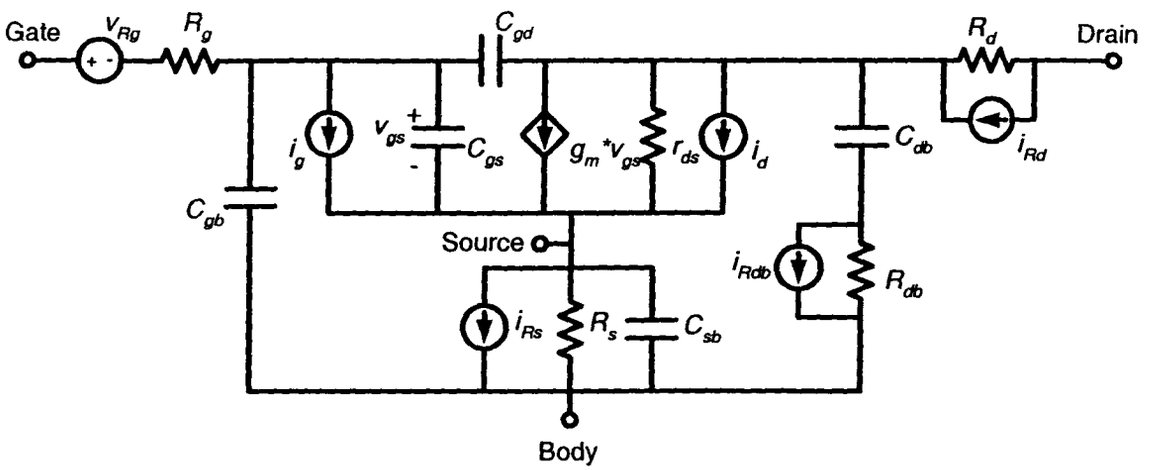

Fig. 2.2. Small-signal equivalent circuit of a MOSFET that is suitable for RF and microwave frequencies including the noise sources [9]. Body effect is not considered.

The capacitor C_{gs} models the gate-source capacitance, and it is a combination of the gate-channel capacitance C_{gc} and the capacitance of the gate-source overlap C_{ov}; using a two-plate model and neglecting fringing capacitances, its value can be estimated for a MOSFET in saturation as

$$C_{gs} = \frac{2}{3} C_{gc} + C_{ov} \tag{2.2}$$

where

$$C_{ov} = C_{ox}^{*} \frac{\Delta L \cdot W}{2}, \tag{2.3}$$

$$C_{gc} = C_{ox}^{*} \cdot L_{eff} \cdot W, \tag{2.4}$$

and

$$C_{ox}^{*} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.5}$$

is the gate oxide capacitance per unit area, where ε_{ox} and t_{ox} are the permittivity and thickness of the insulator. The factor 2/3 in (2.2) accounts for the fact that the charge distribution in the channel is not uniform when the device operates in saturation, so the capacitance is lower than it would be for a two-plate capacitor.

The gate-drain capacitance is mainly due to the gate-drain overlap, and its value, neglecting fringing effects, can be estimated as

$$C_{gd} = C_{ov}. \tag{2.6}$$

The gate resistance R_g is caused by the relatively high resistivity of the polysilicon gate. The source and drain resistances R_s and R_d are dominated by the resistance of the lightly-doped extensions of the source and drain diffusions, and the elements C_{db}, R_{db}, C_{gb} and C_{sb} model various substrate effects.

The noise sources v_{Rg}, i_{Rs}, i_{Rd}, and i_{Rdb} model the thermal noise from the parasitic resistances, and the noise sources i_g and i_d model the gate and channel noise; although there is no phase information associated with the noise sources, the polarities shown in Fig. 2.2 serve as reference for some of the noise calculations in this thesis. The noise properties of the MOSFET are reviewed in a separate section.

The incremental resistor r_{ds}, whose value is given by

$$r_{ds} \equiv \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \tag{2.7}$$

where I_D is the drain-source current and V_{DS} is the drain-source voltage, models the variation of the drain current with drain voltage due to Channel-Length Modulation (CLM) and other short-channel effects.

The transconductance g_m is defined as

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \tag{2.8}$$

where V_{GS} is the gate-source voltage.

A common figure of merit for the high-frequency performance of active devices is f_t, the frequency at which the current gain with the output short-circuited becomes unity. For the model of Fig. 2.2, neglecting the source and drain capacitances and the substrate components, the f_t with the body tied to the source is given by

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{2.9}$$

Because of geometry scaling, the f_t of MOSFETs has increased with every technology generation due to the increase in the transconductance (which is inversely proportional to the channel length) and the simultaneous reduction in the capacitance (the C_{gc} component of C_{gs} is directly proportional to the channel length). There are two elements however that have not improved with scaling: the gate resistance tends to increase with channel length reduction, and the gate-drain capacitance C_{gd} does not scale as fast as C_{gc}.

To see the effect of C_{gd} and R_g on the high-frequency performance of MOSFETs, consider the following approximate expression for f_{max}, the frequency at which the power gain of the MOSFET is unity [10]:

$$f_{max} \approx \frac{1}{2}\sqrt{\frac{f_t}{R_g C_{gd}}}. \tag{2.10}$$

The gate resistance also degrades the noise performance of MOSFETs, since the thermal noise it generates adds directly to the input signal.

While modern CMOS process have an additional step where a metal silicide is added to the polysilicon gate to decrease its resistance (this is also used in the drain and source diffusions for the same purpose), devices with very wide and short channels might still show a significant gate resistance. A common technique to further reduce it is to use several devices connected in parallel (called "fingers") instead of one wide device, as shown in Fig. 2.3.

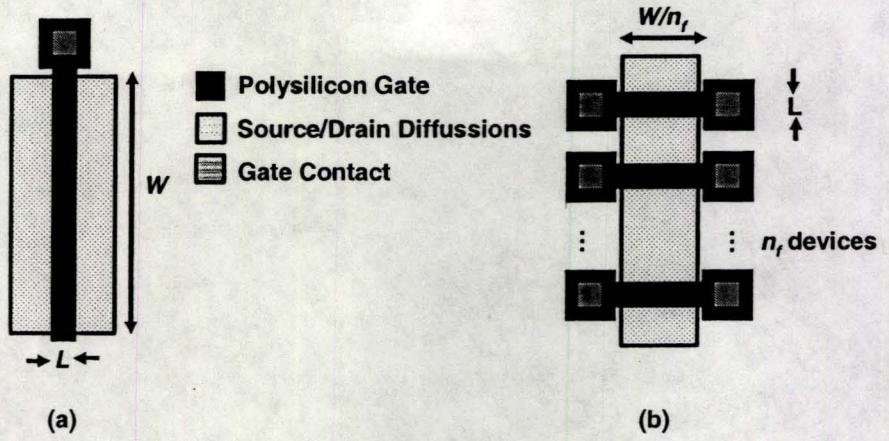

Fig. 2.3. Layout of a wide MOSFET (source and drain contacts not shown) (a) Single device with single gate contact (b) Multi-finger device with double gate contacts.

With this "multifinger" layout, the gate resistance is reduced by a factor that depends on the square of the number of fingers n_f:

$$R_g = \frac{R_{sh}}{3 \cdot 4 \cdot n_f^2} \frac{W}{L} \tag{2.11}$$

where R_{sh} is the sheet resistance of the polysilicon, and the factors 3 and 4 account for the distributed nature of the gate resistance and the use of contact on both sides of the gate, respectively. According to (2.11), there is no limit on the minimum achievable gate resistance (as long as the additional parasitic capacitances incurred on when using very small fingers can be tolerated). For modern sub-micron technologies, however, if the contact resistivity of the interface between the silicide and the polysilicon ρ_{con} is taken into account (Fig. 2.4), the gate resistance is [11]

$$R_g = \frac{R_{sh}}{12 n_f^2} \frac{W}{L} + \frac{\rho_{con}}{WL}. \tag{2.12}$$

The second term depends only on the width and length of the device and can not be reduced by multifinger layout. For this reason, alternative gate materials or structures that minimize the gate resistance, such as metal [12] or T-shaped gates [13] are being studied.

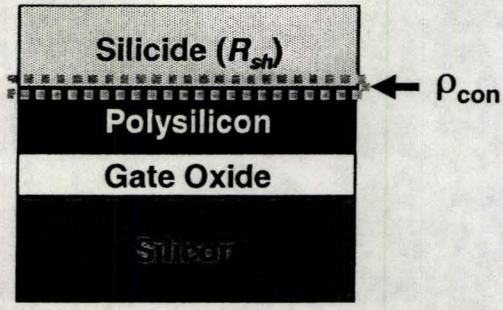

Fig. 2.4. Simplified cross-section of the polysilicon gate of a MOSFET, showing the silicide-poly interface.

As for the gate-drain capacitance C_{gd}, besides its effect on f_{max}, there is an even more important consequence. The feedback created by this capacitance when the transistor is used as common-source amplifier can make the device unstable and cause oscillations at high frequencies [10]. A simple way of minimizing the effect of C_{gd} is to connect a common-gate transistor at the output of the common-source stage. The resulting transistor pair shown in Fig. 2.5(b), known as a "cascode", has a much lower feedback capacitance. The main disadvantage of cascoding is that there must be enough supply voltage headroom to keep both transistors in the saturation region, so this is not suitable for very-low voltage applications.

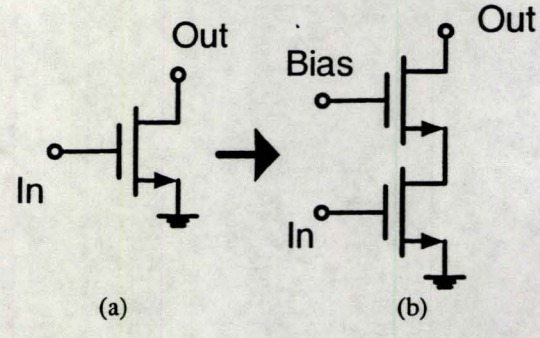

Fig. 2.5. (a) MOSFET in common-source configuration (b) Cascode pair. Biasing details are omitted.

One last thing that will be mentioned in this section is that in RF and microwave CMOS circuits, most of the time, only the nMOS transistors are used in gain stages; the

main reason for this is that the mobility of holes in silicon is approximately one third of that of electrons, and since the transconductance depends on mobility, for a given device size or capacitance, the gain of a pMOSFET is lower than that of a nMOSFET. Conversely, to achieve a certain gain with a pMOS, a larger device must be used, which results in higher capacitance and thus degraded high-frequency performance.

2.2.2. Passive components in CMOS technology

Several options have existed to implement resistors and capacitors in CMOS technology since its early days. In modern mixed-signal processes, capacitors of fixed value are made of two metal plates separated by silicon dioxide – a Metal-Insulator-Metal or MIM capacitor – and linear resistors can be implemented using n-type or p-type diffusions, polysilicon or metal lines. The integration of inductors and transmission lines in CMOS process is a more recent development, and this has been also enabled by scaling, but in this case by *reverse* scaling as will be explained next.

In digital applications, as the component density is increased with scaling, it is also desirable to have many different layers of interconnections. While early CMOS technologies provided one or two interconnection levels, current processes (as shown in Fig. 2.6) offer many more interconnection levels, where the top levels are farther away from the substrate, and the top layers are thicker to provide better power handling [15]. For reasons that will become apparent next, this has enabled the integration of inductors and transmission lines of acceptable quality.

Integrated inductors in CMOS technology are typically realized in spiral form, as shown in Fig. 2.7, using the top metal layer for the process. The underpass, which connects the center of the inductor, is implemented on a lower metal layer.

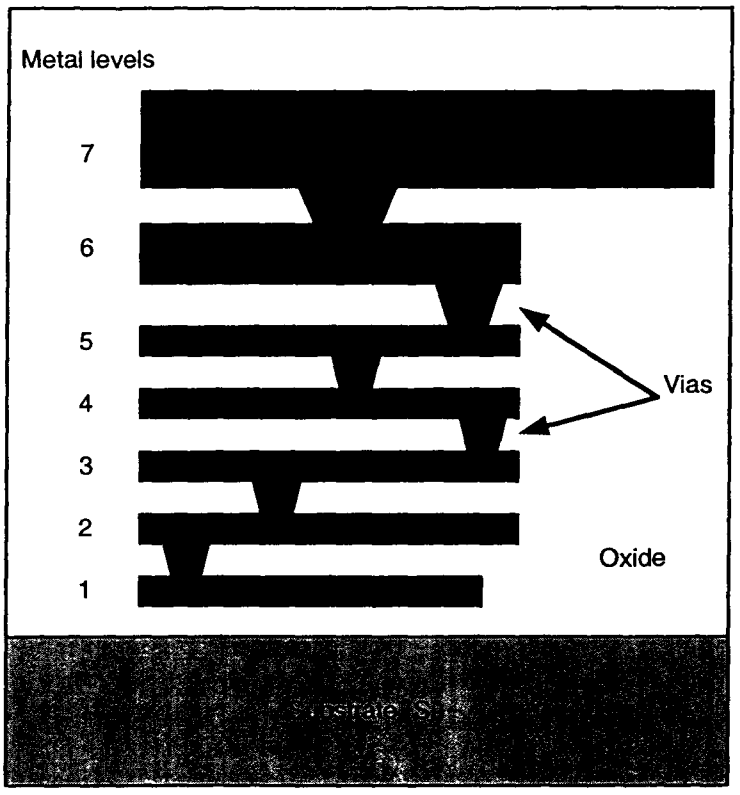

Fig. 2.6. Interconnection levels in a typical modern CMOS process (details such as epitaxial layer and top passivation have been omitted).

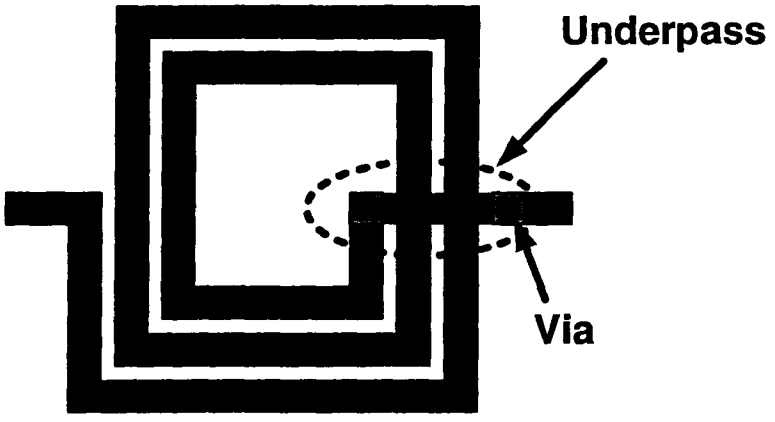

Fig. 2.7. A three-turn square spiral inductor.

A physical model for a spiral inductor in a silicon technology with the substrate grounded is shown in Fig. 2.8 [16]. R_{sp} represents the resistive losses in the metal of the spiral, C_p is the capacitance of the underpass, C_{ox} is the capacitance between the spiral and the silicon substrate[1] and R_{sub} and C_{sub} represent the resistance and capacitance of the semiconductor substrate. More complete models which are more accurate and that include higher-order other effects are available [69] but this model will be used here because it is simple and it includes the most important effects such as metal losses and capacitive coupling to the substrate.

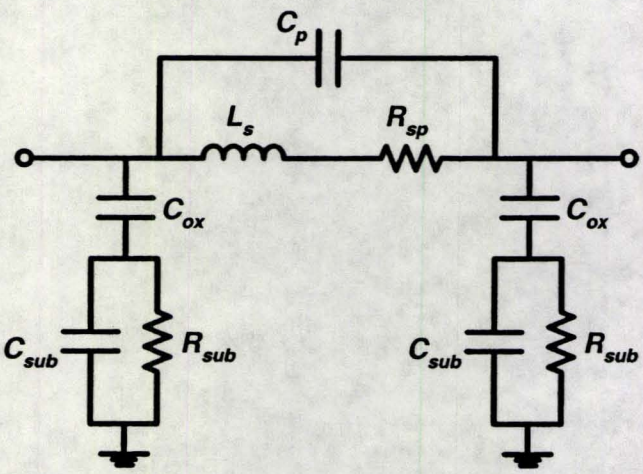

Fig. 2.8. Equivalent circuit model of a spiral inductor on a silicon substrate [16].

An important figure of merit for the inductor is its quality factor. In general, the quality factor is defined as

$$Q \equiv \omega \frac{\text{energy stored}}{\text{average power dissipated}} \tag{2.13}$$

where the exact meaning of "energy stored" depends of the application: for an inductor, it is the energy stored in the magnetic field, for a capacitor it is the energy stored in the

[1] This is different to the gate oxide capacitance per unit area C_{ox}^{*}.

electric field, and for an *LC* tank it is the total energy stored in the magnetic and electric fields. Ideally, an inductor should store energy in the magnetic field; in this case, energy storage in the electric field of the parasitic capacitances is undesirable and thus reduces the quality factor.

Typical variation of the Q of an inductor in a silicon substrate is shown in Fig. 2.9. At low frequencies, the effect of the capacitances C_{ox}, C_p and C_{sub} in Fig. 2.8 is negligible, so the main energy storage element is the inductor, while the losses are dominated by the resistance of the metal, so the quality factor is given approximately by

$$Q_{LF} \approx \frac{2\pi fL}{R_s} \tag{2.14}$$

and it increases with frequency. At higher frequencies, however, the reactance of the capacitors becomes more important; this has two effects: first, part of the total energy is stored in the electric field of the capacitors instead of the inductor, and second, the coupling to the substrate through the C_{ox} capacitors increases the energy dissipated in the R_{sub} resistors; since these two effects tend to lower the Q, it reaches a maximum at a certain frequency f_{peak} and then decreases. At even higher frequencies, a point is reached, called the self-resonance frequency f_{self}, where the same amount of energy is stored in the electric and magnetic fields, so the Q goes to zero. Beyond f_{self}, the spiral behaves as a capacitor and is useless as an inductor.

Several techniques have been proposed to reduce coupling to the lossy silicon substrate to increase both the Q and the maximum frequency of operation. Some rely on adding manufacturing steps to etch the silicon under the substrate [17], ion implantation [18] or the use of high-resistivity silicon as a substrate [19]. While these provide lower losses and higher frequencies of operation, great emphasis is still placed on achieving the best possible performance without significant changes to the digital CMOS processes. One technique to isolate the inductor from the substrate without process changes relies on the use of patterned polysilicon or metal ground shields under the inductors [20]; one disadvantage of this technique is that it increases the parasitic capacitance, thus reducing

the self-resonant frequency. The use of round or octagonal instead of square shape for the inductor can slightly increase the quality factor [10]; however not all technologies support rounded shapes or angles other than 90°.

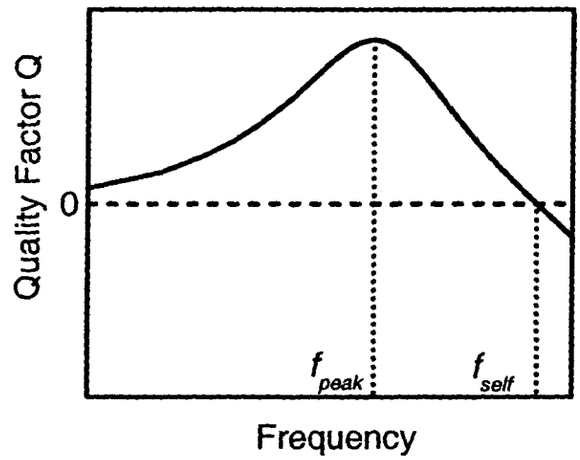

Fig. 2.9. Qualitative variation of Q for a spiral inductor in a silicon substrate. At the frequency f_{peak} the quality factor is maximum, and f_{self} is the frequency where the Q is zero.

The inductance values required in a microwave amplifier for operation beyond 10 GHz are typically very low (less than 1 nH), which can be difficult to achieve with conventional spiral inductors because the underpass capacitance would dominate over the inductance, resulting in very low f_{peak} and f_{self}. If the number of turns in the spiral is reduced to one, the underpass is eliminated and very small inductance values and high maximum frequencies of operation can be achieved [21].

Also important for microwave circuits are transmission lines, which can be used either to replace lumped inductors at very high frequencies, or to provide controlled impedance levels and a current return path in high-frequency interconnections. Several choices exist for the implementation of transmission lines in a planar environment. Some of these include coplanar waveguide (CPW), coplanar strip (CPS), microstrip line and stripline. The cross sections of these lines are shown in Fig. 2.10.

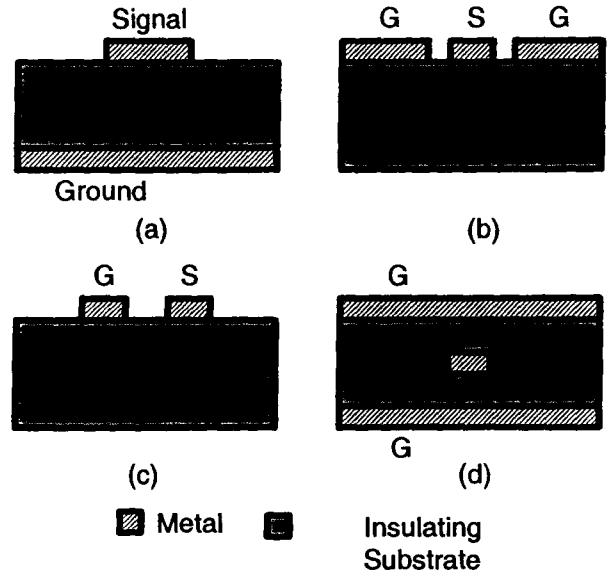

Fig. 2.10. Cross-section of planar transmission lines suitable for monolithic integration (a) Microstrip, (b) Coplanar Waveguide (CPW), (c) Coplanar Strip (CPS) and (d) Strip line.

Key parameters for a transmission line are its characteristic impedance (Z_c), effective dielectric constant (ε_{re}) and losses. Other considerations include size, ease of connection to other passive and active elements and tolerance to geometry variations. For reasons that will become apparent in Chapter 3, when using transmission lines to replace lumped inductors in microwave circuits, it is desirable that they have relatively high characteristic impedance. To see this intuitively, consider the expression for the characteristic impedance of an ideal lossless transmission line:

$$Z_c = \sqrt{L_u / C_u} \tag{2.15}$$

where L_u and C_u are the inductance and capacitance per unit length: the higher the characteristic impedance is, the higher the ratio of inductance to capacitance for a given length of line.

Of the four structures shown in Fig. 2.10, the strip line is the only one that supports a pure Transverse-Electro-Magnetic (TEM) mode, so it has very low dispersion and its characteristic impedance and propagation constant can be calculated exactly. With

a strip line, however, it is relatively difficult to realize the interconnection of active and passive elements because of its geometry, and as will be seen later, for a given cross-sectional area, the characteristic impedances that can be achieved are lower than the other three structures.

Microstrip lines are very popular in discrete and hybrid technologies, because of reasons such as their ease of fabrication and the wide range of characteristic impedances that can be realized just by changing the width of the signal conductor. For CMOS integration, however, two disadvantages are that their characteristics are heavily dependent on vertical dimensions which are not as tightly controlled in CMOS as are the horizontal dimensions, and that achieving high impedances requires narrow conductors, which can exhibit very high resistive losses. While microstrip lines are not TEM, which complicates their analysis, a wide range of models and approximate design equations can be found in the literature, ranging from very accurate ones based on full-wave analyses to rough approximations for first-order design.

Coplanar Strip (CPS) and Coplanar Waveguide (CPW) do not support a pure TEM mode either, and even the first-order models based on quasi-TEM analyses are relatively complex (see Appendix B). One key advantage of CPW and CPS over microstrip for CMOS integration is that the characteristic impedance is controlled both by the width of the conductors and the spacing between them. Even though for both parameters the characteristic impedance is increased at the expense of more losses, because narrower conductors have higher resistance and more spacing between them increases coupling to the silicon substrate, at least there are two parameters that can be changed to achieve a desired impedance-loss tradeoff.

Another advantage of CPW and CPS is that their characteristics depend mostly on the lateral dimensions and very little on the vertical dimensions, so better precision can be achieved in CMOS. As for CPS versus CPW, while CPS can achieve a larger range of impedances for a certain transversal area, CPW has the advantage of being fully balanced, and also the coupling to nearby lines is reduced by the ground planes on both sides of the signal conductor.

An issue with CPW is that, whenever there is a discontinuity or asymmetry in the circuit (such as a bend or connection to a lumped element), the two ground planes have to be connected to make sure they are at the same potential and avoid the propagation of undesired modes (the energy of these modes cannot be recovered, so this would result in an increased loss) [22]. This connection is often referred to as "airbridge", and in hybrid and discrete technologies it is implemented using a small wire over the signal conductor. In CMOS technology, the metal layer below the CPW for the airbridge can be used (this will be discussed in detail in Chapter 4).

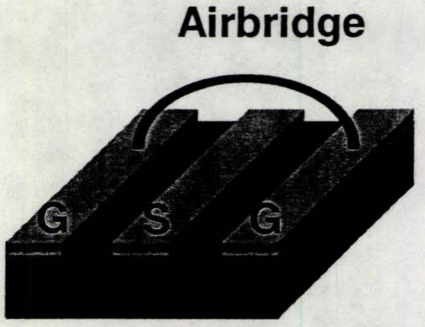

Fig. 2.11. Airbridge connecting the ground (G) lines in a coplanar waveguide.

It was mentioned before that when transmission lines are used to replace lumped inductors in microwave circuits, it is desirable that they have high characteristic impedance. If this is put in the context of the backend of modern CMOS processes, where the number of metal layers and their separation is rather limited, the choice of transmissions line is narrowed down. Consider for example a 7-metal process, with a total separation of 8 μm between the top metal and the bottom one (these are typical of 0.18 μm-0.13 μm mixed-signal CMOS processes); the four transmission lines from Fig. 2.10 implemented in this process would have the dimensions shown in Fig. 2.12. Here, it is assumed for simplicity that all the metal lines are equally spaced, and all conductor lines have the same width. Using the approximate analytical expressions from Appendix B, the characteristic impedances and effective dielectric constants shown in Table 2.1 were

calculated. Microstrip and strip line offer relatively low characteristic impedances, due to the small separation between the top and bottom metal layers.

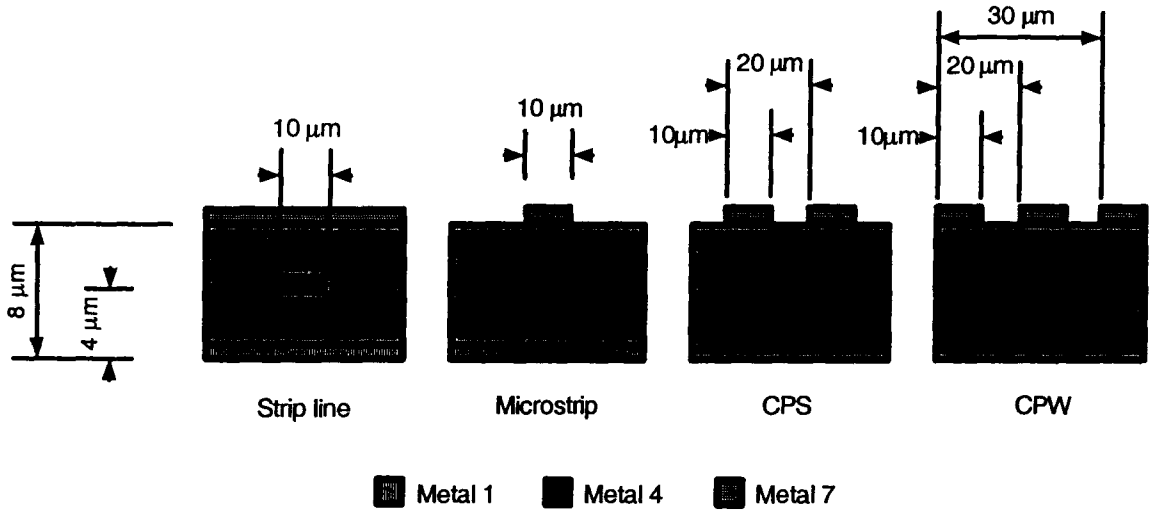

Fig. 2.12. Dimensions of planar transmission lines in a CMOS process used for the calculations of Table 2.1.

Table 2.1. Theoretical characteristics of the transmission lines with the dimensions shown in Fig. 2.12. The metal lines were assumed to be ideal (zero thickness and zero resistance), the dielectric material (silicon dioxide) has a dielectric constant of 3.9, and for CPS and CPW, the presence of the silicon substrate was neglected. Formulas used in the calculations are given in Appendix B.

	Characteristic impedance (Ω)	*Effective permittivity*
Microstrip	67	2.9
CPW	114	2.1
CPS	162	2.0
Stripline	27	3.9

2.3. TEMPERATURE EFFECTS

In this section we review some of the known effects that changes in temperature have in CMOS active and passive devices.

Two main temperature effects are observed in MOSFETs: the mobility decreases exponentially with increasing temperature:

$$\mu(T) = \mu(T_{ref})\left(\frac{T}{T_{ref}}\right)^{-k_1}, \tag{2.16}$$

where T_{ref} is a reference temperature and k_1 is typically between 1.2 and 2 [23]. The threshold voltage also decreases with temperature, and experimentally it has been found that this dependence is almost linear:

$$V_{TH}(T) = V_{TH}(T_{ref}) - k_2(T - T_{ref}), \tag{2.17}$$

where k_2 is between 0.5 mV/°K and 3 mV/°K [23]. Considering the square-law equation for the drain current of a MOSFET in saturation:

$$I_D(T) = \frac{1}{2}\mu(T)\frac{W}{L}C_{ox}^{*}[V_{GS} - V_{TH}(T)]^2 \tag{2.18}$$

it can be seen that the two effects above oppose each other – I_D increases with V_{TH}, but decreases with μ as temperature increases. However, the mobility effect generally dominates in strong inversion. Since the transconductance is also proportional to μ_{eff}, it would also be expected to drop with temperature; this has been confirmed experimentally [24], and this is the dominant temperature effect in MOSFETs at high frequencies (the change in capacitances is very small). Even though (2.18) only applies to long-channel MOSFETs, these conclusions here have been verified experimentally for short-channel MOSFETs [24].

Integrated resistors, whether implemented using polysilicon, metal or n/p diffusions, have a resistance that increases with temperature, while the capacitance of MIM capacitors changes very little with temperature [10].

For integrated inductors, there are two main temperature effects: the resistance of the metal spiral (R_{sp} in Fig. 2.8) and the substrate resistance (R_{sub} in Fig. 2.8). Both R_{sp} and R_{sub} increase with increasing temperature, but the other elements of the equivalent circuit model (inductance and parasitic capacitances) change very little with temperature [25], [26], [27].

The increase of R_{sp} and R_{sub} with temperature has two opposite effects on the quality factor of the inductor: higher series resistance R_{sp} means higher losses and lower Q, while higher shunt resistance R_{sub} means higher Q. These two opposing effects however manifest themselves at different frequencies: as shown in Fig. 2.13, at frequencies below f_{peak}, the series resistance dominates the losses in the inductor, so the Q decreases with temperature; at higher frequencies, the substrate losses start to dominate and the quality factor increases with temperature [25], [26], [27]. Since inductors are normally used below or close to f_{peak}, for most applications, Q will degrade with temperature in the frequency band of interest.

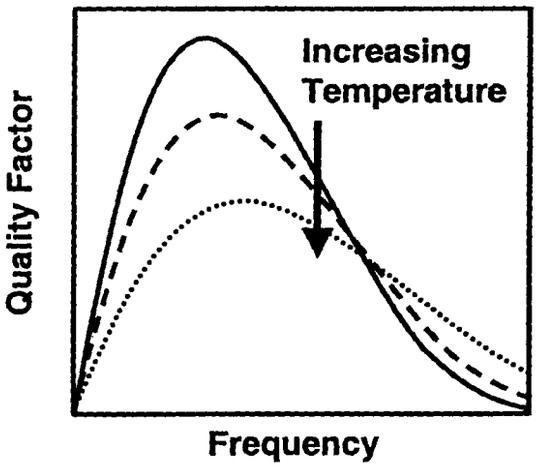

Fig. 2.13. Qualitative variation of the Q of spiral inductors in silicon versus temperature [25], [26], [27].

2.4. NOISE IN MOSFETS

2.4.1. Electrical noise

In this thesis, we refer to noise as the fluctuations in voltages and currents in an electrical circuit or component that are due to intrinsic and unavoidable physical effects such as the thermal motion of charge carriers. Undesirable fluctuations due to, for example, interference from other circuits or cosmic radiation, are not considered here, since these can in principle be reduced to very low levels through shielding and other techniques.

Since noise is a random process, it is characterized in terms of its statistical properties, most commonly through the power spectral density (PSD). Formally, the power spectral density S_x of a random time-varying signal $x(t)$ is defined as the Fourier transform of the autocorrelation of $x(t)$. A detailed discussion of the mathematical foundations of the theory of random processes, including the definition of the autocorrelation function, ensemble averages vs. time averages, etc., is beyond the scope of this thesis and can be found elsewhere [28], so only some key facts about the power spectral density of a noisy current or voltage are discussed.

If a signal with PSD S_x passes through a linear network with a transfer function $H(j\omega)$ (where ω is the angular frequency), the PSD of the signal at the output is

$$S_y(j\omega) = S_x(j\omega)\left|H(j\omega)\right|^2. \tag{2.19}$$

This has two immediate consequences. First, the PSD of a current or voltage at the frequency f_o can be measured with relative ease by passing it through a band-pass filter with a very narrow bandwidth centered around f_o. Second, standard AC circuit analysis techniques with phasors can be used to calculate the noise voltages and currents in any linear circuit, provided that the PSD of the noise sources are known.

Another important quantity for the analysis of noisy circuits is the cross-spectral density $S_{x,y}$ of two signals $x(t)$ and $y(t)$, defined as the Fourier transform of the cross-correlation of $x(t)$ and $y(t)$. Physically, two noise signals have a non-zero cross correlation

if they originate from the same physical process; for example in MOSFETs, the thermal noise in the channel creates noise in both the drain current and the gate current, therefore, these two current noises are correlated. The correlation coefficient is defined as

$$C(j\omega)=\frac{S_{x,y}(j\omega)}{\sqrt{S_x(j\omega)S_y(j\omega)}}, \tag{2.20}$$

and its magnitude is always within the interval [0,1].

2.4.2. Types of electrical noise

There are different kinds of electrical noise, which can be classified according to their physical origins.

Thermal noise (or Johnson noise or Nyquist noise) is due to the random motion of carriers at a finite temperature. In thermal equilibrium, the PSD of the thermal noise current of a resistor of value R at the absolute temperature T is given by

$$S_{i,therm}=\frac{4kT}{R}, \tag{2.21}$$

where k is Boltzmann's constant. Thermal noise is observed on any element that dissipates power. Lossless elements such as ideal capacitors and inductors are noiseless.

Shot noise is caused by discrete charge carriers crossing a potential barrier, and its PSD is proportional to the DC value of the total current I

$$S_{shot}=2qI \tag{2.22}$$

where q is the electron's charge. Shot noise is observed in p-n diodes and in the base-emitter and collector-base junctions of bipolar transistors.

According to (2.21) and (2.22), the PSD of both shot noise and thermal noise are independent of frequency, so they are said to be "white", in analogy to white light, which has a flat spectrum. In reality, as shown schematically in Fig. 2.14(a), the PSD of thermal noise drops to zero at very high frequencies (of the order of terahertz) due to quantum effects; similarly, the PSD of shot noise drops at frequencies which are of the order of the

inverse of the "transit time" of carriers passing through the barrier. For most practical applications at microwave frequencies and below, the white noise approximation of thermal and shot noise are adequate.

Burst noise (or popcorn noise or random-telegraph-signal or generation-recombination noise) is associated with carriers undergoing generation-recombination or trapping-detrapping events, where the carrier enters or leaves the conduction process at random intervals creating a noisy signal that switches between two levels. The PSD of pure burst noise is given by

$$S_{burst} \propto \frac{\tau_{trap}}{1+(2\pi f \tau_{trap})^2}, \tag{2.23}$$

where τ_{trap} is the time constant of the trapping process. As shown in Fig. 2.14(b), the PSD is relatively constant below a certain frequency (related to $1/\tau_{trap}$) and drops as f^2 afterwards.

Flicker noise (or low-frequency noise or $1/f$ noise or pink noise) is observed not only in electrical systems but also in many other disciplines such as biology. In general its PSD, shown in Fig. 2.14(c) depends inversely on frequency

$$S_{flicker} \propto \frac{1}{f^a}, \tag{2.24}$$

with a close to one. Despite having being studied for many years, there is still discussion about the origin of flicker noise. In some instances, flicker noise has been demonstrated to be the result of the superposition of many events that have a Lorentzian spectrum with different time constants.

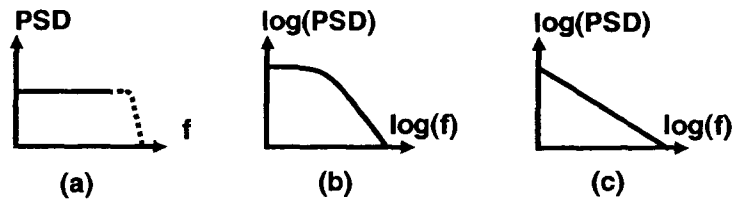

Fig. 2.14. Power spectral densities of (a) White noise, (b) Lorentzian noise, and (c) Flicker or pink noise.

2.4.3. MOSFET noise sources

The main sources of noise in MOSFETs are introduced here, as well as some models to calculate their PSD from the device size and biasing conditions and technology parameters.

When a MOSFET is biased with a very low drain-source voltage, it can be modeled as a linear resistor. As with any resistor, the drain current then shows thermal noise with PSD

$$S_{i_d} = 4kT\frac{I_D}{V_{DS}}, \tag{2.25}$$

where I_D/V_{DS} is the channel conductance. As V_{DS} is increased, the thermal noise decreases, and it is in general given by

$$S_{i_d} = \gamma 4kTg_{do} \tag{2.26}$$

where g_{do} is the channel conductance at zero V_{DS} for a specified V_{GS},

$$g_{do} \equiv \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0}, \tag{2.27}$$

and γ is the channel noise coefficient. For long-channel devices, g_{do} is equal to the device transconductance g_m and γ goes from one at V_{DS}=0 to 2/3 in saturation (V_{DS}>[V_{GS}-V_{TH}]). For short-channel devices, due to effects such as channel length modulation and velocity

saturation, both γ and the ratio g_{do}/g_m increase. A model more appropriate for short channel devices in saturation is [29]:

$$S_{i_d} = 4kT\alpha_b I_D \frac{4V_{GT}^2 + V_0^2 - 2V_0 V_{GT}}{3V_{GT}^2 (V_{GT} - V_0)}, \tag{2.28}$$

where

$$V_0 = \frac{I_D}{WC_{ox}^* v_{sat}}, \tag{2.29}$$

α_b is the bulk charge effect parameter, with typical values between 1 and 1.2 [23], $V_{GT}=[V_{GS}-V_{TH}]$ is the gate overdrive voltage and v_{sat} is the carrier saturation velocity.

The thermal noise from the channel couples to the gate through the oxide capacitance, giving raise to what is called induced gate noise. While induced gate noise is associated with the distributed nature of the MOSFET channel, it is often modeled with a lumped current noise source between the gate and the source terminal (labeled i_g in Fig. 2.2), with a PSD

$$S_{i_g} = \delta \cdot 4kT \cdot g_g, \tag{2.30}$$

where

$$g_g = \frac{(\omega C_{gs})^2}{5g_{do}}, \tag{2.31}$$

and δ is the induced gate noise factor. For long-channel devices in saturation δ=4/3. For short channel devices, since the channel noise is higher, the induced gate noise is also higher; it can be modeled either with (2.31) with a higher value of δ (typically determined from measurements) or by the following expression [30]:

$$S_{i_g} = \frac{4kT\omega^2 W^4 C_{ox}^{*\,4} \mu_{eff}^2}{I_D^3} \left[\begin{array}{l} V_{GT}^2 V_{as}^2 V_{DS} - V_{GT} V_{as} (V_{GT} + V_{as}) V_{DS}^2 \\ + \frac{V_{GT}^2 + 4V_{GT}V_{as} + V_{as}^2}{3} V_{DS}^3 - \frac{V_{GT} + V_{as}}{2} V_{DS}^4 + \frac{V_{DS}^5}{5} \end{array} \right] \tag{2.32}$$

where

$$V_{as} = V_{DS} - \frac{\frac{V_{GT}V_{DS}}{2} - \frac{V_{DS}^2}{6}}{V_{GS} - V_{TH} - \frac{V_{DS}}{2}}. \tag{2.33}$$

Since the drain thermal noise and the induced gate noise share a common origin, they are correlated; the correlation coefficient has a theoretical value of $0.395j$ for long-channel devices at moderately high frequencies and it decreases for short-channel devices [31].

Besides white thermal noise, the drain current of MOSFETs also exhibits flicker noise at low frequencies. While the focus of this thesis is on high-frequency CMOS circuits, we look at low-frequency noise because it has been shown that low-frequency noise can affect the performance of nonlinear RF and microwave circuits such as voltage-controlled-oscillators [32].

Two theories have been proposed to explain MOSFET's flicker noise. The mobility fluctuation theory ($\Delta\mu$) postulates that it is due to fluctuations in the carrier mobility, and the spectral density of the fluctuations is inversely proportional to the frequency and the number of carriers N

$$S_{\Delta\mu} \propto \frac{1}{Nf}. \tag{2.34}$$

The number fluctuation (ΔN) theory postulates that the flicker noise is due to fluctuations in the number of carriers that participate in the conduction process due to trapping and de-trapping at the silicon-oxide interface. While the PSD of each trap is a

Lorentzian, if the traps are distributed uniformly in the oxide, the superposition of Lorentzians results in $1/f$ spectrum.

Even though both the ΔN and $\Delta\mu$ theories predict a $1/f$ spectrum, the key difference between them is the bias dependence of the noise. For example, for a MOSFET operating in strong inversion ($V_{GS}>V_{TH}$) with very low V_{DS} (ohmic region), the drain current noise from the $\Delta\mu$ theory is [33]:

$$S_{i_d} = \alpha_H q \mu_{eff}^2 C_{ox}^* \frac{W}{L^3} \frac{(V_{GS} - V_{TH}) V_{DS}^2}{f} \tag{2.35}$$

while the ΔN theory predicts [33]:

$$S_{i_d} = \frac{1}{f} \frac{q^2 kTN_t \mu_{eff}^2}{\gamma_t} \frac{W}{L^3} V_{DS}^2 \tag{2.36}$$

where α_H is an empirical parameter from the $\Delta\mu$ model called the Hooge parameter, N_t is the trap density and γ_t is the so-called McWorther parameter (or tunneling parameter). We see that the noise from the ΔN theory is independent of the gate voltage, while the $\Delta\mu$ theory gives an increase in the noise as the gate voltage increases. Experimentally, most of the times it is found that the low-frequency noise of nMOSFETs can be explained by the ΔN theory, while the noise from pMOSFETs is better explained by the $\Delta\mu$ model [34].

In an effort to have an "unified" model that applies to both pMOS and nMOS devices, the correlated number-mobility fluctuation theory has been developed [35]. It postulates that the fluctuations in the number of carriers due to trapping can also cause a fluctuation on the mobility, because the trapped carriers act as Coulomb scattering centers for the mobile carriers. The unified model can explain the bias dependence of the noise from both nMOSFETs and pMOSFETs, given an appropriate selection of various empirical factors [36].

2.4.4. Noise figure and noise parameters

The noise figure of a two-port system is defined as

$$NF \equiv \frac{\text{total output noise}}{\text{output noise due to the input source}} \tag{2.37}$$

when the input source is at a reference temperature of 290 °K, and it is a measure of how much noise a circuit or component "adds" to its input signal.

It has been shown that the noise figure of any linear two-port network driven by a source with admittance $Y_s=G_s+B_s$ can be expressed as [37]:

$$NF = NF_{\min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{2.38}$$

where NF_{min} is the minimum noise figure, R_n is the noise resistance, G_{opt} is the optimum source conductance and B_{opt} is the optimum source susceptance.

At RF and microwave frequencies, the noise parameters are a common way to characterize device noise, because they can be measured with relative ease. The noise parameters are also very useful for low-noise circuit design, because they give a measure of the lowest achievable noise figure (NF_{min}) as well as the input termination required to obtain it ($Y_s=Y_{opt}=G_{opt}+B_{opt}$). The noise resistance R_n can be seen as measure of how "sensitive" the network is to a mismatch in the input admittance: the higher the value of R_n, the higher the noise figure will be for a certain deviation from the optimum source impedance.

2.5. SUMMARY

In this chapter, some of the characteristics of active and passive devices in CMOS technology that are relevant for MMIC implementation were reviewed.

Two elements that impair the high-frequency performance of MOSFETs and that are not reduced with technology downscaling are the gate resistance and the gate-drain

overlap capacitance. The first is mitigated by the use of multifinger layout, and the latter by the use of cascode gain stages to replace simple common-source transistors.

Of the passive elements, inductors and transmission lines of good quality are particularly difficult to implement in CMOS, principally due to the resistive losses of the interconnection metals and the losses due to capacitive coupling to the substrate.

When the temperature of a CMOS circuit is increased above room temperature, the main effects that are observed are a decrease in both the mobility and threshold voltage of MOSFETs and an increase in all resistances, including the parasitic resistances of the inductors, while the capacitances and inductances show negligible changes.

The main noise sources of MOSFETs were also reviewed, and models to calculate their spectral densities were presented. The drain current of MOSFETs shows a combination of white noise of thermal origin, and a flicker noise component with an approximate $1/f$ dependence. At high frequencies, the gate current shows induced gate noise, due to the capacitive coupling between the channel and the gate.

Chapter 3
CMOS Distributed Amplifiers

3.1. INTRODUCTION

There are several applications that require broadband amplifiers, that are capable of dealing with signals with spectral contents in a wide range of frequencies. A circuit technique for broadband amplification, known as distributed amplification, is reviewed in section 3.2, where the basic idea behind distributed amplification is discussed, as well as the basic design formulas and the advantages and disadvantages of this approach.

In order to put the work that will be presented in Chapter 4 into context, a review of the published implementations of distributed amplifiers in CMOS technology is presented in 3.3. A summary is included at the end of the chapter in section 3.4.

3.2. DISTRIBUTED AMPLIFIERS

3.2.1. Distributed amplification operating principles

What limits the high-frequency performance of active devices, and MOSFETs in particular? This question has many answers, and there are several factors that in one way or another make difficult the implementation of high-frequency circuits with these devices. For example, considering the small-signal equivalent circuit of Fig. 2.2, we can see that there are several elements that can reduce the gain or bandwidth of a MOSFET-based amplifier: the parasitic resistances R_s, R_g and R_d, for example, dissipate power, while the various parasitic capacitances such as C_{gd} and C_{sb} form low-impedance paths at high frequencies, thus reducing the achievable gain. There is one element however, which is intrinsic to the operation of the MOSFET and cannot be removed, no matter how advanced the process or technology is, or how the device is laid out: the portion of the C_{gs} capacitance that is due to the gate-channel capacitance C_{gc}: even if the length of the channel/source and channel/drain overlaps is reduced, the parasitic resistances are

minimized by changes in processes or materials and careful layout, etc., as long as there are two conducting materials separated by a gate insulator, there will be a gate-source capacitance at the input. This gate-source capacitance shunts the MOSFET input at high frequencies, and is one of the main reasons why the device gain drops at high frequencies.

Consider a Field-Effect-Transistor (FET) whose input and output capacitances are purely capacitive, and for which the only link between input and output is the transconductance (the device is unilateral). The small-signal equivalent circuit of such device would be as shown in Fig. 3.1.

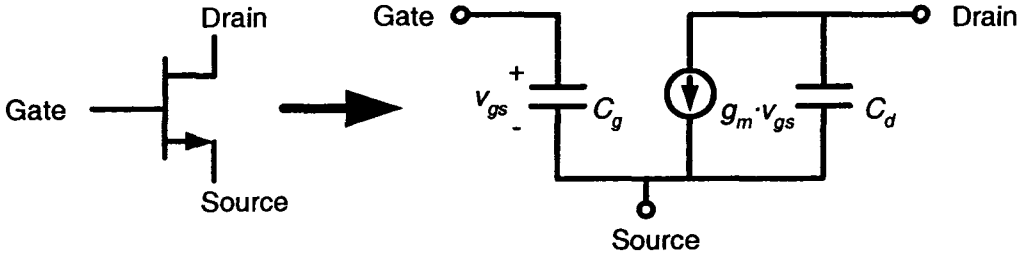

Fig. 3.1. Idealized small-signal equivalent circuit of a perfectly unilateral field-effect transistor with purely capacitive input and output impedances.

Assume now that a number of such devices are connected as shown in Fig. 3.2, by placing inductors between the input and output terminals (the detailed nature of the gate and drain termination impedances will be discussed later). This arrangement is known as a Distributed Amplifier. It operates based on the principle that, if the capacitances that limit the bandwidth of the amplifier are separated with inductors, a structure with properties similar to an uniform transmission line is realized, with a bandwidth that depends only on the values of the inductors and capacitors, and which is independent of the overall gain of the amplifier, thus breaking the gain-bandwidth tradeoff of other amplifier configurations. Moreover, the gate and drain circuits have low-pass characteristics, so the amplifier can provide gain from very low to very high frequencies.

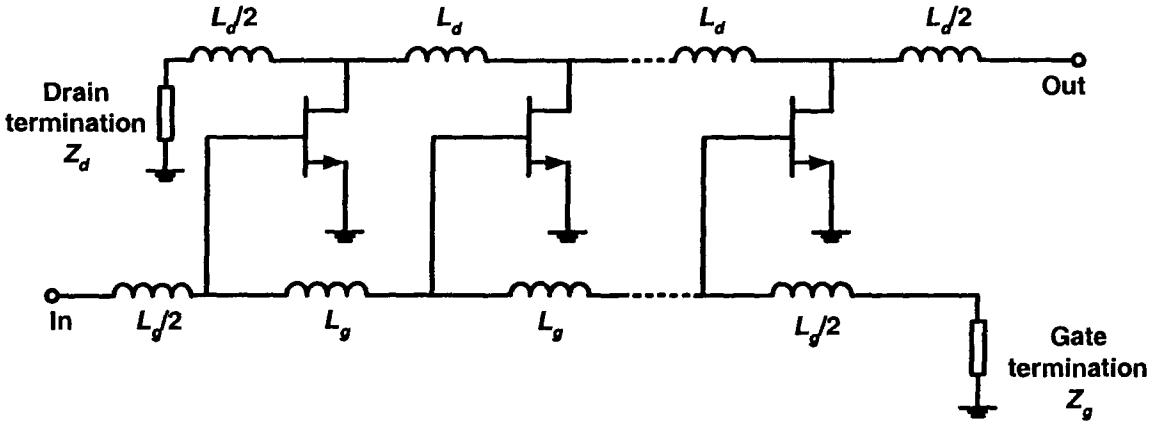

Fig. 3.2. Simplified schematic of a field-effect-transistor (FET) distributed amplifier.

The idea of distributed amplification was first outlined in British patent filed in 1936 by W.S. Percival [41], but it did not go into widespread use until it was studied in detail in a paper by Ginzton *et al.* in 1948 [42]; the term "Distributed Amplification" itself was used for the first time in that paper. Distributed amplifiers have been used for decades in technologies ranging from vacuum tubes [43] to discrete and hybrid silicon [44], [45], [46] to monolithic microwave integrated circuits (MMICs) in III-V technologies such as gallium-arsenide (GaAs) [47] and indium-phosphide (InP) [48].

The emergence of silicon as viable alternative for the realization of low-cost and highly-integrated MMICs has created interest in the implementation of broadband amplifiers in technologies such as silicon-germanium (SiGe) [51] and CMOS [52]-[62].

3.2.2. Gain, bandwidth and matching

The small-signal equivalent circuit of the amplifier of Fig. 3.2 is shown in Fig. 3.3.

Thanks to the assumption that the devices are unilateral (the only coupling between the gate and drain circuits is the transconductance), the gate circuit (top of Fig. 3.3) can be analyzed independently of the drain circuit (bottom of Fig. 3.3). First, we note that the gate and drain networks look very similar to the equivalent circuit of an

infinitesimal section of a lossless transmission line; for this reason, they are often referred to as the input and output "artificial lines".

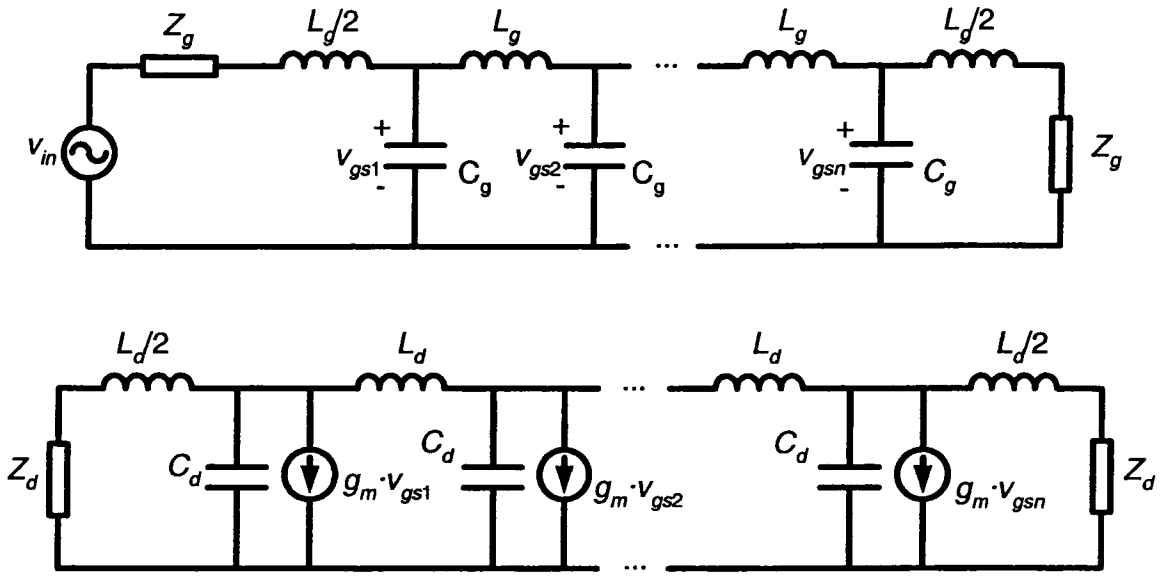

Fig. 3.3. Input and output lines in a distributed amplifier.

There are two important differences however between these lines made up of lumped elements and true distributed lines. First, the "characteristic impedance" of the artificial lines is not constant with frequency, and second, they have a cutoff frequency beyond which propagation is not possible (ideal distributed lines have unlimited bandwidth).

The cutoff frequencies of the gate and drain lines are [94]

$$\omega_{cg} = \frac{2}{\sqrt{L_g C_g}} \tag{3.1}$$

and

$$\omega_{cd} = \frac{2}{\sqrt{L_d C_d}} \tag{3.2}$$

respectively. The image impedance of the lines is defined as the impedance with which they must be terminated at both ends to achieve maximum power transfer, and is given by [94]

$$Z_g = R_{og}\sqrt{1-\omega^2/\omega_{cg}^2} \tag{3.3}$$

and

$$Z_d = R_{od}\sqrt{1-\omega^2/\omega_{cd}^2} \tag{3.4}$$

where

$$R_{og} = \sqrt{L_g/C_g} \tag{3.5}$$

and

$$R_{od} = \sqrt{L_d/C_d} \tag{3.6}$$

are the low-frequency values of these impedances. The impedances "seen" by the MOSFET input and output are given by

$$Z_{g\pi} = \frac{R_{og}}{\sqrt{1-\omega^2/\omega_{cg}^2}} \tag{3.7}$$

and

$$Z_{d\pi} = \frac{R_{od}}{\sqrt{1-\omega^2/\omega_{cd}^2}} \tag{3.8}$$

respectively.

With these quantities defined, the power gain of a distributed amplifier with n stages, assuming that both lines have the same cutoff frequencies ($\omega_{cg}=\omega_{cd}=\omega_c$) and are terminated at both ends by their image impedances, is given by [63]:

$$G = \frac{n^2 g_m^2}{4} Z_{g\pi} Z_{d\pi} = \frac{n^2 g_m^2}{4} \frac{R_{og} R_{od}}{\left(1 - \omega^2/\omega_c^2\right)} \tag{3.9}$$

for $\omega<\omega_c$. It can be seen that the low-frequency gain, given by

$$G_{lf} = \frac{n^2 g_m^2}{4} R_{og} R_{od} \tag{3.10}$$

depends only on the number of stages and the device transconductance, while the maximum frequency of operation of the amplifier depends essentially on the cutoff frequency of the lines. Therefore, at least in principle, it is possible to achieve an arbitrarily large gain by increasing the number of stages, without sacrificing the bandwidth.

Some other observations can be made regarding the gain given by (3.9). First, note that the gain increases rapidly as the cutoff frequency of the lines is approached ($\omega \sim \omega_c$); this is known as peaking, and several techniques have been suggested to reduce it. One which is relatively simple and that does not require the addition of any extra components is the staggering technique [64], which is based on making the cutoff frequency of the drain line smaller than that of the gate. A "staggering" factor, defined as

$$S = \omega_{cd}/\omega_{cg} \tag{3.11}$$

with a value of 0.7-0.8 is found to virtually eliminate peaking in conventional distributed amplifiers. For CMOS amplifiers, however, since the gain tends to decrease at high frequencies for reasons that will be explained later, it is common to take advantage of gain peaking to compensate for this effect; the consequences of this will be discussed in detail in Chapter 4.

Also note that in the derivation of (3.9), it is assumed that the lines are terminated by their image impedances; this means that the source impedance and the gate termination impedance must be equal to Z_g, given by (3.3), and the load impedance and drain termination must be equal to Z_d, given by (3.4). This poses two problems: first, the

impedance values given by (3.3) and (3.4) can not be synthesized exactly with a finite number of passive elements [63]; second, it is not desirable to impose a restriction that the source and load impedances are equal to (3.3) and (3.4). As shown in Fig. 3.4, Z_g and Z_d change significantly with frequency, and most microwave circuits are designed to operate with a constant and real input and output impedance (for example 50 Ω).

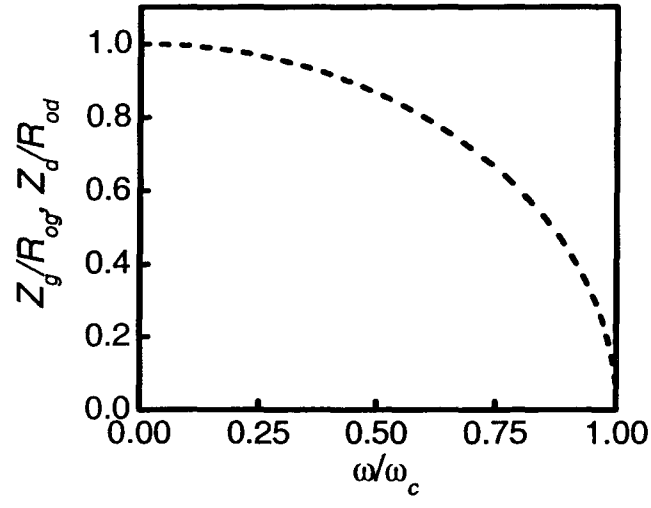

Fig. 3.4. Image impedance of the gate and drain lines normalized with respect to their low-frequency value, as a function of frequency normalized with respect to the cutoff frequency.

A solution for both problems relies on the use of so called *m*-derived matching sections, shown in Fig. 3.5; the component values in this circuit are given by

$$L_{m1} = \frac{mL}{2}, \tag{3.12}$$

$$L_{m2} = \frac{1-m^2}{2m} L \tag{3.13}$$

and

$$C_m = \frac{mC}{2} \tag{3.14}$$

where the parameter m is what gives the name to the circuit. This network has the property that, if the value of m is selected appropriately (m=0.6), the image impedance on one side of the network is nearly constant and equal to

$$R_{om} \approx \sqrt{\frac{L}{C}} \tag{3.15}$$

while the image impedance on the other side is exactly the same of the artificial lines

$$Z_{im} = R_{om}\sqrt{1-\omega^2/\omega_c^2} \tag{3.16}$$

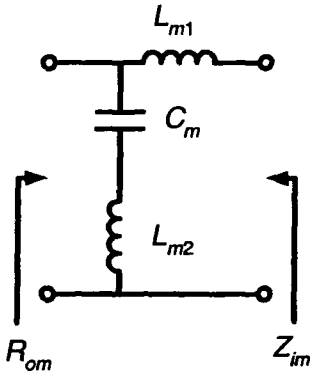

Fig. 3.5. Schematic of an m-derived matching section.

Then, by making L=L_g (L=L_d) and C=C_g (C=C_d) for the gate (drain) line and inserting four matching section at the line ends as shown in Fig. 3.6, two problems are solved at the same time: the line terminations can be implemented with simple resistors, and the input and output impedances of the amplifier (Z_{in} and Z_{out}) are real and approximately constant ($Z_{in} \approx R_{og}$ and $Z_{out} \approx R_{od}$). Since the input and output reflection coefficients are

$$\Gamma_{in} = \frac{Z_{in} - R_o}{Z_{in} + R_o} \tag{3.17}$$

and

$$\Gamma_{out} = \frac{Z_{out} - R_o}{Z_{out} + R_o} \tag{3.18}$$

respectively, where R_o is the system impedance, by selecting L_g, L_d, C_g and C_d such that $R_{og}=R_{od}=R_o$, then the reflections can be made very small.

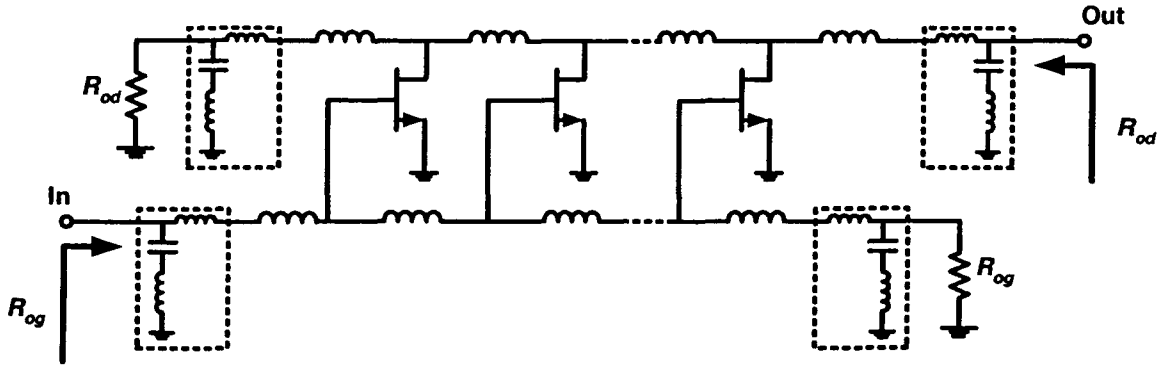

Fig. 3.6. Distributed amplifier with *m*-derived matching sections (inside dashed boxes) at the input and output and at the line terminations. The values of the inductors outside the dashed boxes are the same as in Fig. 3.2 and the values of the elements inside the dashed boxes are the same as in Fig. 3.5.

To summarize, some of the key advantages of distributed amplifiers for broadband applications include:

- The capacitances that limit the high-frequency performance of the active devices are absorbed as part of the design.
- The gain and the bandwidth are independent of each other, and the gain can be incremented theoretically without limit without sacrificing the bandwidth.
- The input and output reflections are very low because it is possible to have nearly constant and real input and output impedances over a wide bandwidth.

Some of the disadvantages that can be mentioned are that, since the gain increases as n^2, the power consumption for a certain gain tends to be larger than other topologies, such as cascaded amplifiers, where the gain depends exponentially on the number of stages. Also, a relatively large number of passive components is required, which can be a disadvantage for monolithically integrated amplifiers.

3.2.3. Non-idealities in distributed amplifiers

In the previous analysis, the FETs were assumed to be unilateral, that is, the only coupling between input and output is the transconductance. As was discussed in Chapter 2, sub-micron MOSFETs tend to have rather large gate-drain capacitances; this parasitic element not only complicates significantly the analysis of distributed amplifiers, but it can severely degrade the high-frequency gain, cause ringing in the transient response and even make the amplifier unstable under certain conditions [63]. For these reasons, the use of cascode gain stages instead of simple common-source MOSFETs is preferred in CMOS implementations.

It was also assumed in the previous section that the input and output impedances of the FETs are purely capacitive, and that the inductors are lossless. In CMOS implementations, these conditions are far from reality: MOSFETs show a resistive component at the gate, due mostly to the gate resistance, and also at the drain, mostly due to the drain-source resistance r_{ds}; also, spiral inductors in MOS technology also suffer from relatively large losses due to metal resistance and coupling to the substrate.

The main effect of the losses in the lines is that it is no longer true that the gain can be increased without limit by adding more stages, because beyond a certain number of stages the signal on the gate of the last FET is so small that the gain provided by that last device is offset by the loss on the drain line. It has been shown that, if the artificial lines have attenuation factors α_g and α_d, then the optimum number of stages for maximum gain is given by [65]

$$n_{opt} = \frac{\ln(\alpha_d/\alpha_g)}{\alpha_d - \alpha_g} \tag{3.19}$$

The effect of the losses is more severe at high frequencies, so it is found that adding more stages increases the gain at low frequencies, but degrades the high-frequency gain [63]. In amplifiers implemented in GaAs or InP technologies, the number of stages can be as high as 9 or 10, but in CMOS implementations, the high losses limit this number to between 3 and 5.

Another effect of the losses in the lines is that they degrade the input and output reflections. As discussed on the previous section, the input and output impedance of ideal distributed amplifiers can be made almost constant with frequency by using *m*-derived matching sections, which would result in nearly zero reflections. Losses, however, change the input and output impedance, and make them frequency-dependent.

3.2.4. Phase response and group delay

As was discussed in section 1.1, in order to minimize signal distortion when amplifying very short pulses, broadband amplifiers must not only provide a constant gain over the passband, but the phase of the transfer function must also depend almost linearly on frequency, or equivalently the group delay must be nearly constant.

It can be shown that the phase of the voltage transfer function of an ideal distributed amplifier is given by [63]:

$$\phi(\omega) = -2n\sin^{-1}\left(\frac{\omega}{\omega_c}\right). \tag{3.20}$$

Using this and the definition of group delay GD in (1.4), then the group delay of a distributed amplifier is

$$GD = \frac{2n}{\omega_c}\frac{1}{\sqrt{1-\omega^2/\omega_c^2}}. \tag{3.21}$$

The group delay of a distributed amplifier then increases linearly with the number of stages, and just as the gain, it peaks close to the cutoff frequency. The first feature shows what the main tradeoff in distributed amplifiers is: instead of gain-bandwidth, gain and delay are traded off. Group delay peaking in CMOS amplifiers will be further discussed in Chapter 4.

3.2.5. Traveling-wave amplifiers

In planar MMIC technology, it is often convenient to replace the lumped inductors in a distributed amplifier with sections of transmission lines, either to reduce the area requirements or to realize with good precision small inductance values for high frequencies. A distributed amplifier with the lumped inductors replaced by transmission lines is often referred to as Traveling-Wave Amplifier (TWA), and it is shown in Fig. 3.7.

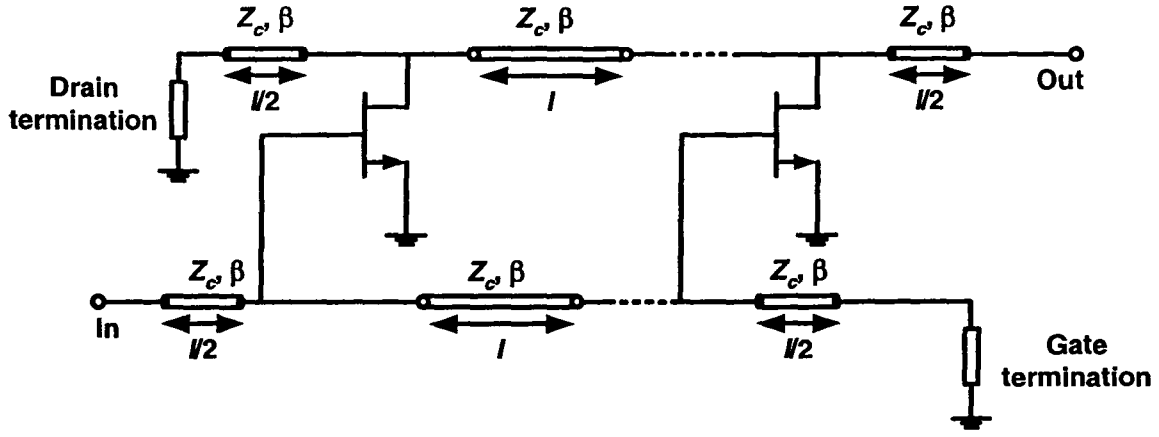

Fig. 3.7. Simplified schematic of a FET traveling-wave amplifier.

Since the first-order design of a distributed amplifier with lumped inductors using (3.1)-(3.9) is relatively straightforward, design formulas for a TWA that take as a starting point the lumped-element case can be useful, and also provide some design insight in the trade-offs made when using transmission lines. We will derive such formulas next, by starting with the parameters of the unloaded transmission line, that is, the transmission

line without the gain cells connected. The analysis is general and can be applied to both the input or output transmission lines [49].

The unloaded transmission line is characterized by two parameters: its characteristic impedance Z_c and its propagation constant β. We assume that Z_c and β/ω are constant with frequency, and will neglect to first order the losses in the lines. For such a lossless line, the characteristic impedance is given by

$$Z_c = \sqrt{L_u / C_u}\,, \tag{3.22}$$

where L_u and C_u are the inductance and capacitance per unit length of the line. The propagation constant is then given by

$$\beta = \omega\sqrt{L_u C_u}\,. \tag{3.23}$$

If the line segments are electrically small, it can be assumed that the capacitance of the transmission line is lumped at its extremes and it adds directly to the capacitance of the FETs, so the total capacitance of the lines is given by $C_g = (C_u l + C_{FET})$, where C_{FET} is the input or output capacitance of the FET and l is the length of line connected between each FET. With that assumption and by analogy with (3.5), the low-frequency characteristic impedance of the loaded line is given by

$$R_o = \sqrt{\frac{L_u l}{(C_u l + C_{FET})}}\,. \tag{3.24}$$

Also, by analogy with (3.1), the cutoff frequency of the loaded line is given by

$$\omega_c = \frac{2}{\sqrt{L_u l (C_u l + C_{FET})}}\,. \tag{3.25}$$

If we want the TWA to have the same input and output impedance as the lumped amplifier, then we must equate (3.5)-(3.6) and (3.24). Solving for l, this gives

$$l = \left(\frac{\beta}{\omega}\right)^{-1} \frac{LC_{FET}}{C_{FET}Z_c - L/Z_c} \tag{3.26}$$

where L is the inductance we would use in a lumped amplifier. This allows us to select the length of line required as a function of the lumped amplifier component values (C_{FET} and L) and the parameters of the transmission line (Z_c and β/ω). If we take the ratio of (3.25) and (3.1), we see that the bandwidth of a TWA is reduced by a factor of

$$\omega_{c,TWA}/\omega_{c,DA} = 1-(R_o/Z_c)^2 \tag{3.27}$$

with respect to the distributed amplifier, where R_o is the desired input/output impedance. Thus, for a given device (C_{FET}), the bandwidth of a TWA designed using (3.26) will be reduced by a factor that depends on the characteristic impedance of the unloaded transmission line. This can be explained by the fact that the lower the characteristic impedance of the unloaded line, the lower inductance per unit length it has, therefore requiring a longer segment of line, which in turn results in a higher total capacitance. Then in order to achieve bandwidths in a TWA comparable to those of the lumped-component case without degrading the matching, the transmission lines need to be of high-impedance, which as was shown in Chapter 2, often conflicts with the requirement of low-loss.

Equations (3.26) and (3.27) are plotted in Fig. 3.8 for values of L, C_{FET} and R_o corresponding to a 22 GHz, 50 Ω distributed amplifier. It can be seen that, for example, if planar transmission lines with Z_c=70 Ω are used to replace the lumped inductors, a line with a length of 1-3 mm would be required, depending on the effective permittivity of the line, and the bandwidth would be reduced almost by half.

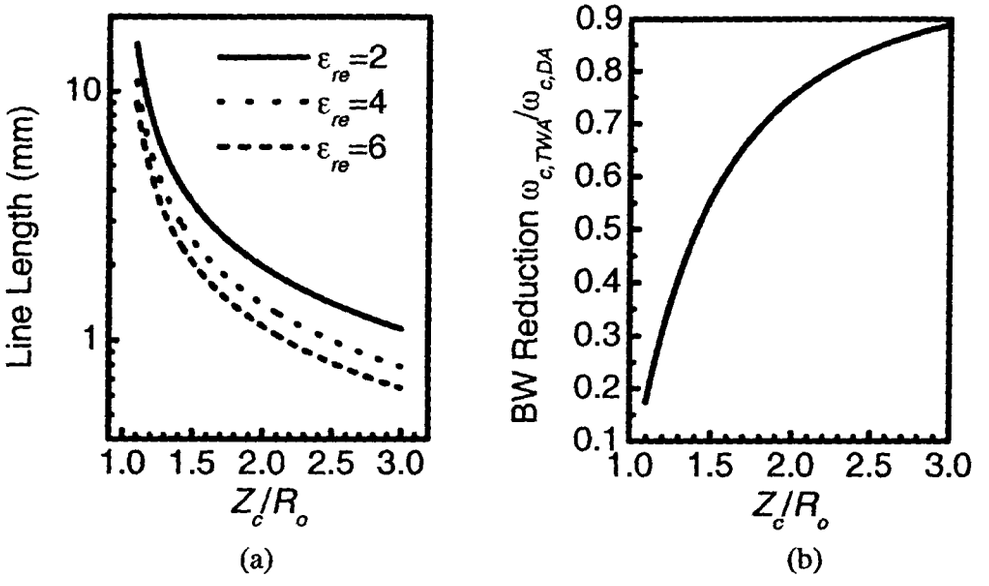

Fig. 3.8. Effect of replacing the lumped inductors with transmission lines as a function of the unloaded transmission line characteristic impedance. (a) Required transmission line length. (b) Bandwidth reduction with respect to the lumped case. The following values were used: R_o = 50 Ω, C_{FET}=280 fF, L=0.7 nH. ε_{re} is the effective permittivity of the transmission line, used to calculate the phase constant $\beta/\omega = \sqrt{\varepsilon_{re}}/c$ where c is the speed of light in vacuum.

Equations (3.26) and (3.27) are verified in Fig. 3.9, which shows the magnitude of the forward gain S_{21} of a 5-stage CMOS DA, simulated using the transistor models provided by the foundry for a 0.18 μm CMOS process and three different elements as inductors: ideal lumped inductors and ideal transmission lines with two different characteristic impedances; the arrows indicate the bandwidth predicted by (3.1) and (3.27). The bandwidth reduction caused by the use of low-impedance transmission lines is clear.

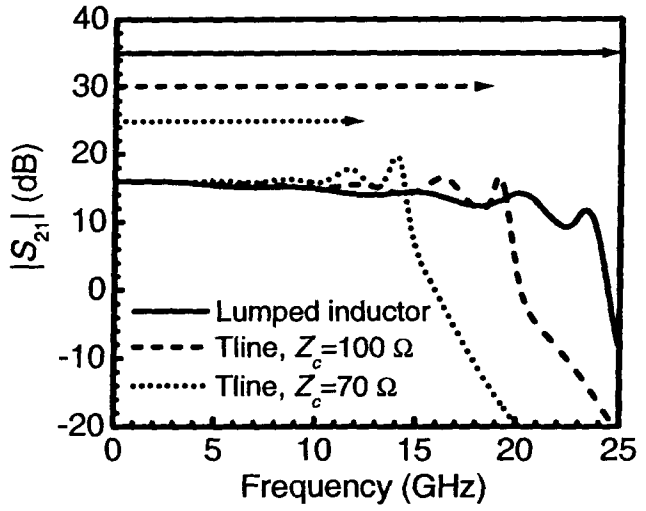

Fig. 3.9. Effect of replacing the ideal lumped inductors with ideal transmission lines (Tlines) on the gain of a 5-stage CMOS distributed amplifier [50]. The arrows indicate the bandwidth predicted by (3.1) and (3.27).

3.2.6. Noise in CMOS distributed amplifiers

The noise figure of a lossless distributed amplifier, considering channel thermal noise (S_{id}) and induced gate noise (S_{ig}) from the FETs and thermal noise from the gate and drain termination resistances is given by [66]

$$NF = 1 + \left(\frac{\sin n\theta}{n\sin\theta}\right)^2 + \frac{4}{n^2 g_m{}^2 Z_{\pi g} Z_{\pi d}} + \frac{S_{id}}{kT}\frac{1}{n g_m^2 Z_{\pi g}} + \frac{S_{ig}}{4kT}\frac{Z_{\pi g}\sum_{r=1}^{n} f(r,\theta)}{n^2 g_m}, \tag{3.28}$$

where θ is the propagation constant of the artificial lines given by

$$\theta = 2\sin^{-1}(\omega/\omega_c), \tag{3.29}$$

and the auxiliar function $f(r,\theta)$ is given by

$$f(r,\theta) = (n-r+1)^2 + \left(\frac{\sin[(r-1)\theta]}{\sin(\theta)}\right)^2 + \frac{2(n-r+1)\sin[(r-1)\theta]\cos(r\theta)}{\sin(\theta)}. \tag{3.30}$$

The second term in (3.28) is the contribution from the gate termination resistor; it varies with frequency, and normally it is very small except at very low frequencies and close to cutoff. The third term is the contribution of the drain termination resistor. The fourth term involving S_{id} is the contribution from the MOSFET channel thermal noise, and it is typically the dominant noise generator if losses in the lines are not considered. Finally, the fifth term is the induced gate noise, which is most important at very high frequencies.

While (3.28) was derived assuming ideal conditions: perfect terminations at the gate and drain lines, no losses, etc., it can still be a useful approximation for CMOS amplifiers if it is put in terms of the power gain G given by (3.9):

$$NF = 1 + \left(\frac{\sin n\theta}{n \sin \theta}\right)^2 + \frac{1}{G} + \frac{S_{id}}{4kT}\frac{nZ_{d\pi}}{G} + \frac{S_{ig}}{4kT}\frac{Z_{g\pi}\sum_{r=1}^{n} f(r,\theta)}{n^2} \tag{3.31}$$

so the losses in the lines and other effects are accounted for by the variations of the gain with frequency.

3.3. REVIEW OF CMOS DISTRIBUTED AMPLIFIER IMPLEMENTATIONS

A summary of the characteristics of various implementations of distributed amplifiers and TWAs on bulk CMOS technology reported in the literature is presented in Table 3.1 (Silicon-On-Insulator implementations are not considered). The performance indicators that most authors focus on when reporting the performance of their circuits such as bandwidth, gain, input and output reflection coefficients, chip area and power consumption are shown. Note that most authors do not report group delay.

The bandwidth (BW) column in Table 3.1 refers to the frequency range over which the gain is relatively constant within a certain margin as reported by the authors, while the unity-gain frequency f_{0dB} refers to the frequency beyond which the amplifier provides no power gain. Since most distributed amplifiers provide a very sharp gain roll-off after the cutoff frequency of the lines, the higher end of the bandwidth is typically

very close to f_{0dB}, so the different criteria used by different authors when reporting their results should not result in an unfair comparison. Some highlights of each implementation, as well as the design approaches and tradeoffs, will be discussed next.

In order to avoid the complications caused by low-quality inductors in CMOS processes, Sullivan *et al.* proposed the use of bond wires as inductors in a CMOS distributed amplifier [52]. This was the first reported implementation of an integrated CMOS distributed amplifier. Since the inductance of the bond wires is fixed for a given packaging, the lines were designed using the transistor sizes as design parameters. Their amplifier achieved a bandwidth of 3 GHz with a 5 dB gain in a 0.8 μm technology.

Kleveland *et al.* implemented a TWA employing coplanar strips as on-chip inductors in a 0.18 μm technology [53]. The process they used provided an extra-thick (2 μm) copper top metal layer, which resulted in a unity-gain frequency of 23 GHz. The gain, however, rolls off from its low-frequency value (5 dB) down to 0 dB, providing virtually no constant gain range. In this implementation, the line termination resistors were connected externally to the chip.

The amplifier designed by Ballweber *et al.* [54] used on-chip spiral inductors in a standard 0.6 μm CMOS process with only aluminum metal layers. This amplifier provided a relatively flat gain of 6.5 dB up to 4 GHz when probed on-wafer, and significant performance degradation was observed for a packaged version. Computer-aided optimization techniques were used to improve the performance of the amplifier, after taking into account the non-idealities of the inductors. Unlike previous CMOS implementations, this design included an *m*-derived matching section at the input, output and line terminations. Also, the "staggering" technique was employed with a staggering factor of 0.7.

Table 3.1. Summary of published CMOS distributed amplifier implementations.

Ref.	BW (GHz)	Gain (dB)	f_{0dB} (GHz)	NF (dB)	$\lvert S_{11}\rvert$ max (dB)	$\lvert S_{22}\rvert$ max (dB)	Power Cons. (mW)	Area (mm^2)	Tech. (μm)	Inductor type[a]	Gain cell[b]
[52]	0.3-3	5	4.7	5.1	-6	-9	54	0.72x0.32	0.8	Bond wires	CS
[53]	-	5	23	-	-13	-	90	0.3x1.5	0.18	CPS	CS
[54]	0.5-4	6.5	5.5	6.86	-7	-10	83.4	0.79	0.6	Spiral	CS
[55]	1 5-7.5	5.5	8.5	8.7-13	-6	-9.5	216	1.3x2.2	0.6	Spiral	Diff CS
[56]	1-10	8	18[c]	4-8	-	-	-	1.8x1.3	0.18	CPW	Darl CC
[57]	0.5-14	10.6	18[c]	3.4-5.4[c]	-11	-12	52	1.0x1.6	0.18	Spiral	CC
[58]	0.6-22	7.3	24	4.3-6.1	-8	-9	52	0.9x1.5	0.18	Spiral	CC
[59]	0.5-3.5[c]	20	5.5	1.5-3[c]	-15[c]	-15[c]	86.7	0.95x1.8	0.35	Spiral	CC
[60]	-	10	12	-	-8	-8	75[c]	2.4x0.8	0.18	CPW	CS
[61]	1-25[c]	6	27	6	-10[c]	-10[c]	68.1	1.8x0.9	0.18	CPW	CC
[62]	2-8	17	10.5[c]	-	-	-5	100	-	0.13	Mstrip	CS

[a] CPS: Coplanar Strip; CPW: Coplanar Waveguide, Mstrip: Microstrip

[b] CS: Common-source, Diff: Differential, CC: Cascode, Darl: Darlington

[c] Data extracted approximately from plots or calculated from other parameters.

In order to reduce the effect of the interconnections, bond wires and packaging parasitics in the frequency response of the amplifier, Ahn and Allstot [55] proposed a differential distributed amplifier, based in the work of Ballweber *et al.* [54]. A higher bandwidth with respect to the amplifier in [54] was achieved, but at the expense of more gain ripple (1.5 dB ripple as opposed to 1.2 dB in [54]), reduced gain, more than twice the power dissipation and chip area, and a noise figure increase of more than 3 dB.

Frank *et al.* used for the first time coplanar waveguides as inductors on their CMOS TWA design, achieving a bandwidth of 10 GHz [56] in a 0.18 μm technology. The gain cell used by them was a four-transistor combination of Darlington and cascode stages. They also designed an amplifier with an on-chip bias network, as opposed to all the previous designs which employed external bias networks; the on-chip bias network degraded the gain by about 3 dB. Note that the gain quoted in Table 3.1 does not correspond to the measured value; the actual gain was higher than 15 dB at DC, and rolled off down to 0 dB at approximately 18 GHz. The quoted values correspond to the

simulated gain response obtained by inserting a decoupling capacitor at the amplifier input.

Liu *et al.* designed two distributed amplifiers [57], [58]. The first one achieved a bandwidth of 14 GHz [57], the second design [58] achieved a 22 GHz bandwidth and a f_{0dB} of 24 GHz at the expense of increased input and output reflections. Both designs were implemented in a 0.18 μm process optimized for RF applications that provides a 2 μm thick copper top metal layer. They used spiral inductors and cascode gain cells. Also, *m*-derived matching sections were included in both ends of the drain and gate lines. The DC blocking capacitors were provided off-chip to extend the bandwidth to very low frequencies.

Using a relatively older technology (0.35 μm), Amaya and Plett [59] designed a high-gain distributed amplifier (20 dB), at the expense of a relatively low bandwidth of 3.5 GHz and an f_{0dB} of 5.5 GHz.

Bhattacharyya and Deen [60] designed an amplifier in a standard 0.18 μm process, and evaluated the temperature effects on the amplifier performance for the first time. Coplanar Waveguides were used as on-chip inductors. The amplifier provided a DC gain of 10 dB and a unity-gain frequency of 12 GHz. They showed that the magnitude of the gain decreases at high temperatures up to 75 °C, while the phase remains almost unchanged.

A higher operating frequency was achieved by Amaya *et al.* [61] by using coplanar waveguides and cascode gain stages. The unity-gain frequency of the amplifier is 27 GHz in a 0.18 μm process, and as opposed to the other traveling-wave amplifiers [53], [56], [60], which were terminated with simple resistors, this employed *m*-derived matching sections. This amplifier however used a 3.3 V supply, which is above the nominal supply voltage for this technology (1.8 V); when using the nominal supply voltage the gain dropped to approximately 2-3 dB.

The use of a CMOS TWA as a power amplifier for ultra wideband (UWB) applications was reported by Grewing *et al.* [62]. Implemented on a 0.13 μm process

with microstrip lines as inductors, the amplifier has a bandwidth of 8 GHz, while able to deliver up to 3.5 dBm of linear power to a 50 Ω load.

3.4. SUMMARY

Distributed amplification, a principle that has been used for decades in technologies from vacuum tubes to compound semiconductor technologies, can provide gain over very wide bandwidths with very low input and output reflections, and is especially well suited for active devices with capacitive input and output impedances. If the inductors in distributed amplifiers are replaced with transmission lines to form a traveling-wave amplifier (TWA), the bandwidth is reduced by a factor that depends on the characteristic impedance of the lines used.

The implementation of distributed amplifiers and TWAs in CMOS presents several challenges: the losses in the passive and active elements limit the number of stages and thus the gain, and the parasitic capacitances of the inductors and interconnections reduces the bandwidth. Moreover, the difficulty of implementing transmission lines in CMOS with low loss and high characteristic impedance limits the achievable bandwidths of TWAs.

Finally, published implementations of CMOS distributed amplifiers were reviewed; very wide bandwidths with acceptable gains are often achieved by the use of special processes, or at the expense of input/output reflections.

Chapter 4
CMOS Distributed Amplifier Design and Experimental Results

In this chapter we describe the design, simulation and measured performance of a CMOS distributed amplifier. The amplifier was fabricated in a standard mixed-signal 0.18 μm technology with 6 aluminum metal layers. The amplifier is fully integrated, including the termination resistors and bypass capacitors. As was discussed in section 3.3, this is in contrast to some other CMOS implementations which provide the termination resistors and/or DC blocking capacitors off-chip.

Section 4.1 presents the design and simulation of the distributed amplifier, including a detailed discussion of the design equations, the models used for design and simulation, and some important design considerations such as layout and element interconnection. The experimental setup, as well as the measured performance of the amplifier in terms of gain, input and output matching, group delay and noise in the temperature range of 25 °C to 125 °C, are presented in section 4.2. A summary of the chapter is presented in section 4.3.

4.1. DISTRIBUTED AMPLIFIER DESIGN

4.1.1. Circuit design

It was decided that, for the reasons discussed in Chapter 3, lumped inductors would be used for the on-chip inductances instead of transmission lines. Coplanar waveguides were still used as interconnection elements, as will be discussed in section 4.1.3.

The first-order design of the amplifier was done using the simple equations (3.1)-(3.2) for the bandwidth, (3.5)-(3.6) for the input/output impedances and (3.10) for the gain, but keeping in mind the following limitations of real CMOS amplifiers:

- The parasitic capacitances from the inductors and interconnections can significantly reduce the bandwidth below what is predicted by (3.1), so there must be enough design margin.
- The resistive losses in the inductors, interconnections and MOSFETs also reduce the gain from what is predicted by (3.10), and they limit the number of stages, so also a comfortable implementation margin is required.
- While the "optimum" number of stages can in principle be determined from (3.19), it is very difficult to obtain a first-order estimate of the attenuation constants of the artificial lines, so the optimum number of stages is in fact determined from simulations. Moreover, chip area limitations have to be taken into account when setting the number of stages, since each additional stage requires two more inductors to be added.
- Deep-Submicron MOSFETs are far too complicated to use simple first-order models to determine parameters such as gate capacitance and transconductance, due to effects such as velocity saturation, mobility degradation, drain/source diffusion extensions and fringing capacitances. For this reason, the calibrated SPICE models provided by the foundry were used to estimate these parameters from simulations.

The complete schematic of the designed distributed amplifier is shown in Fig. 4.1. Matching sections (C_1, L_3) were inserted at the input and output and also at the line terminations. Cascode gain cells were used for unilateralization, and capacitors were added at the output of each gain cell (C_D) to make the total capacitance of the drain line equal to the capacitance of the gate line. The staggering technique mentioned in section 3.2.2 was not used here, because in this CMOS amplifier gain peaking around the cutoff frequency is used to compensate for the losses at high frequencies and maintain a

relatively flat gain over the passband; therefore, the gate and drain artificial lines have the same characteristics.

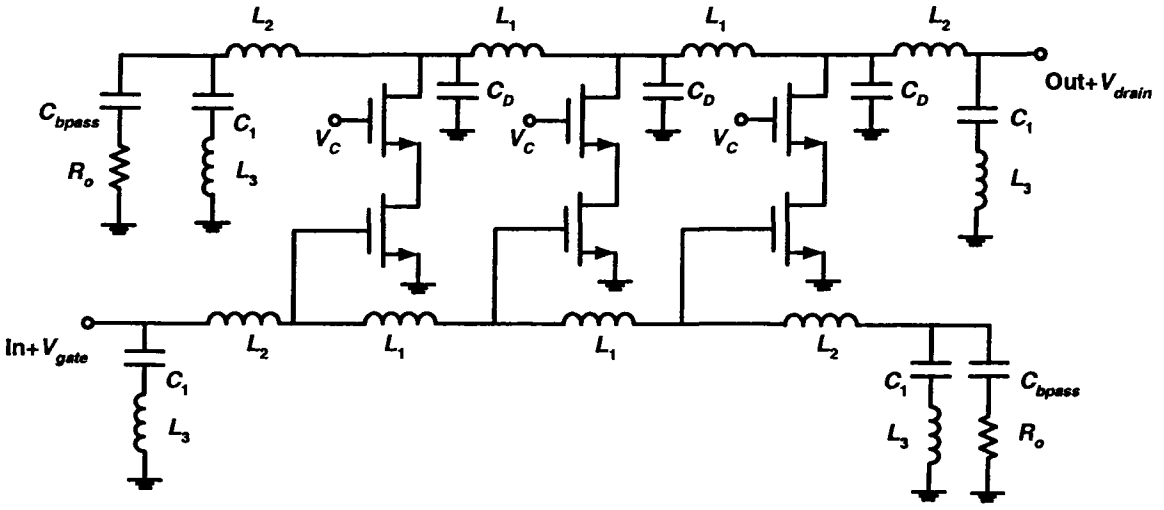

Fig. 4.1. Complete schematic of the CMOS Distributed Amplifier.

The number of stages was fixed at three, since more stages would result in a steep reduction of gain at the higher frequencies due to losses in the artificial lines.

Minimum channel length was used for the transistors (drawn length of 0.18 μm for this technology) for the best high-frequency performance.

To determine the width of the transistors, recall from section 3.2.2 that the gate-source capacitance of the MOSFETs determines the capacitance of the input lines. From SPICE simulations with the calibrated models provided by the foundry, it was determined that the total input capacitance of the MOSFETs is approximately given by

$$C_g \approx 2\times10^{-9} \cdot W \tag{4.1}$$

where C_g is in Farad and W in meters. Using this, the transistor width was determined by combining (3.1) and (3.5):

$$W = \frac{2}{2\times10^{-9}\cdot R_o\cdot 2\pi\cdot f_c} \tag{4.2}$$

where f_c is the cutoff frequency and W is in meters, R_o in Ohms and f_c in Hertz. With R_o=50 Ω and f_c=23 GHz, the device width is chosen as 138 μm. Multi-finger layout was used to reduce the gate resistance, with a finger width of 2.5 μm because the transistor model from the foundry is calibrated for this finger width; this results in $138/2.5 \approx 55$ fingers. To simplify the design, the cascode transistors were sized the same as the common-source transistors.

An external capacitor C_D has to be added on the drain line to make the drain capacitance equal to the gate capacitance. From simulations, it was determined that the output capacitance of the MOSFETs in Farad is given approximately by

$$C_{out} \approx 0.92\times10^{-9}\cdot W \tag{4.3}$$

where W is in meters, so a capacitor with value $C_D = (2-0.92)\times10^{-9}\cdot W \approx 150\,\text{fF}$ is required.

The required inter-stage inductance L_1 follows directly from the input/output impedance equation (3.5):

$$L = R_o^{\,2}\cdot C_g, \tag{4.4}$$

which gives $L \approx 690\,\text{pH}$ for R_o=50 Ω.

The *m*-derived matching sections were designed according to equations (3.12)-(3.14). The series inductor on each m-derived section (L_{m1} in Fig. 3.5) was combined with the last inductor on each artificial line ($L_d/2$ and $L_g/2$ in Fig. 3.2) to form a single inductor (L_2 in Fig. 4.1).

DC-blocking capacitors (C_{bpass}) were added in series with the termination resistors, in order to prevent the biasing currents from flowing through these termination resistors, which would significantly increase the power consumption of the amplifier. Also, if these capacitors are not used, very large currents would flow through the input

and output lines, which would then require very wide lines to avoid electromigration problems. It is this capacitor which determines the lower end of the bandwidth of the distributed amplifier. It was determined from simulations that a capacitance value of 7 pF would provide a reasonable tradeoff between bandwidth and chip area.

The DC biasing of the transistors is provided directly through the input and output lines (V_{gate} and V_{drain}), and the biasing at the gate of the cascode transistors (V_C) is provided through a dedicated DC connection. A 2 pF capacitor, not shown in Fig. 4.1, was added close to the gate of each one of the cascode transistors to ensure a good AC ground at these nodes. The nominal supply voltage for this technology (1.8 V) was used for V_{drain} and V_C; V_{gate} was selected to be 0.9 V to have acceptable gain.

The component values for the amplifier are summarized in Table 4.1, including the biasing voltages.

Table 4.1. Component values for the distributed amplifier shown in Fig. 4.1.

Element	*Value*
L_1	690 pH
L_2	550 pH
L_3	360 pH
C_1	85 fF
C_D	150 fF
C_{bpass}	7 pF
MOSFETs (all)	0.18 μm (L) x 2.5 μm (W) x 55 fingers
R_o	50 Ω
V_{gate}	0.9 V
V_{drain}	1.8 V
V_C	1.8 V

4.1.2. Inductor design and modeling

While the foundry provides sample layouts and measurement-calibrated models for most elements, including MOSFETs, resistors and capacitors, the available values of inductance are rather limited and the inductors are not optimized for very high frequencies. For this reason, an inductor structure was developed for the inductors to be used in the distributed amplifiers; these inductors were modeled based on electromagnetic simulations.

Since the required inductance values for the distributed amplifier are very small (see Table 4.1), it is possible to use single-turn inductors, which eliminates the capacitance of the underpass. Octagonal shape instead of square was used to increase the quality factor [10]. The width of the metal lines was selected as 20 μm, which gives a low DC resistance of approximately 1 Ω; a wider metal trace would not decrease the resistance significantly, while it would increase the capacitance to the substrate.

Since Coplanar Waveguides (CPW) were used to connect the components in the amplifier (see section 4.1.3 below), and in order to simplify the connection of those CPWs to the inductor, a ground plane around the inductor in the same metal layer was added as shown in Fig. 4.2. As shown in this figure, the spacing between the inductor and the ground plane is equal to one half of the radius of the inductor, and the width of the ground plane is 10 μm, which matches the width of the ground plane of the CPWs, as will be discussed in the next section.

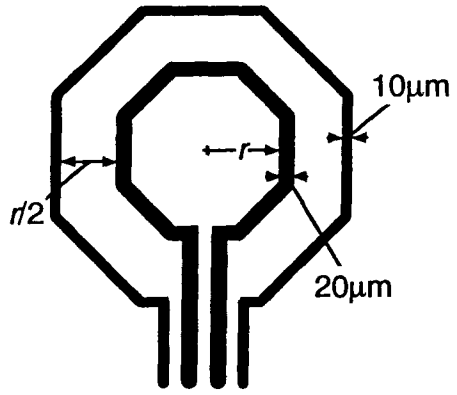

Fig. 4.2. Single-turn coplanar inductor. The external trace is grounded, and provides a smooth transition between the CPW interconnections and the inductor.

While the coplanar ground plane slightly increases the parasitic capacitance of the inductor, it has the advantage of providing some shielding against other signals and reducing the mutual coupling between inductors placed close together. To verify this, the coupling between closely placed inductors was simulated as shown in Fig. 4.3 using Agilent Momentum [67] for an inductor of radius r=100 μm. The resulting transmission S_{21} with and without ground plane is shown in Fig. 4.4; the use of the ground plane results in a reduction in coupling of up to 7 dB.

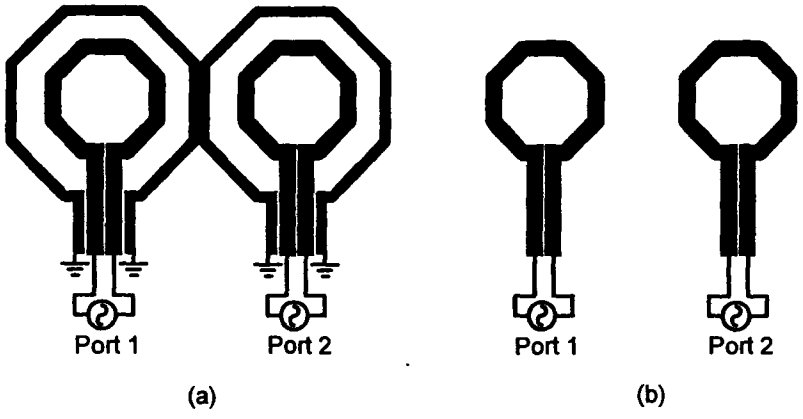

Fig. 4.3. Setup for coupling simulations. Ports are connected differentially to each inductor, and the simulation was performed (a) with and (b) without the ground plane.

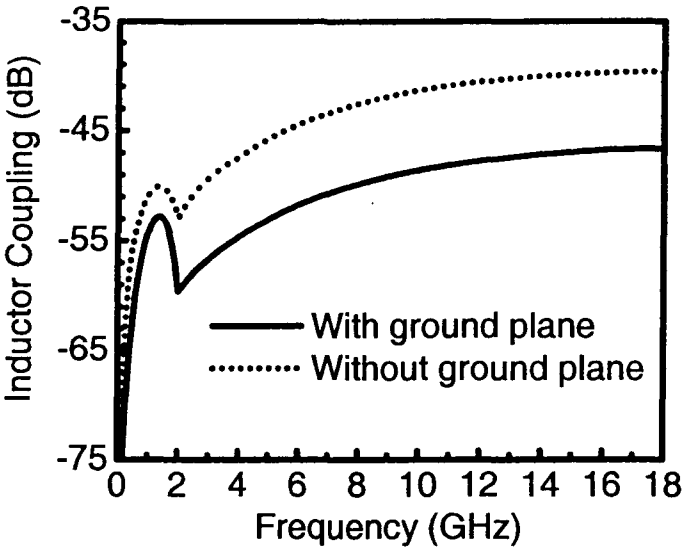

Fig. 4.4. Simulated coupling between coplanar inductors. This coupling is the transmission S_{21} from the setups in Fig. 4.3(a) (solid line) and Fig. 4.3(b) (dotted line).

Different approaches can be used for inductor modeling. Scalable physical models allow, in principle, to calculate the inductor model parameters from technology parameters [16], [69]. Most of such models, however, do not apply to coplanar inductors, and for calculating the substrate components they require either measuring special test structures or knowledge of process details which the foundry does not provide. Another option for modeling is purely measurement-based: many different inductor sizes and geometries are fabricated and tested, and a model is extracted for each one of them; this approach might be very accurate, but it is very expensive and time-consuming. We used an approach similar to the latter, but based on numerical Electromagnetic (EM) simulations instead of measurements. While in principle full-wave EM simulation should give accurate results, it is not feasible to use EM simulations for design because of the time required for each simulation (typically several hours). For this reason, only four different inductor sizes were simulated, and from the extracted equivalent circuit, a scalable model was developed.

Since the single-turn coplanar inductors are fully symmetrical, a simplified version of the full model of Fig. 2.8 was used. This simplified model, shown in Fig. 4.5, has only one port.

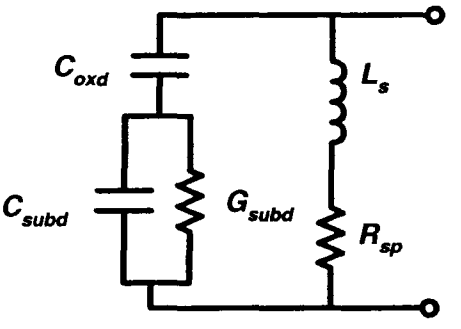

Fig. 4.5. Equivalent circuit model for the single-turn coplanar inductors [20]. The "d" subscripts in the substrate network components refer to the fact that this model is especially well-suited for differential applications, and the underpass capacitance was removed because there is no underpass in the single-turn inductors.

The real and imaginary parts of the admittance of the equivalent circuit of Fig. 4.5 are given by

$$\mathrm{Re}\{Y_{11}\} = \frac{R_s}{R_s^2 + \omega^2 L^2} + \frac{\omega^2 C_{oxd}^2 G_{subd}}{G_{subd}^2 + \omega^2 (C_{oxd} + C_{subd})^2} \tag{4.5}$$

and

$$\mathrm{Im}\{Y_{11}\} = -\frac{\omega L}{R_s^2 + \omega^2 L^2} + \frac{\omega C_{oxd} G_{subd}^2 + \omega^3 C_{oxd} C_{subd} (C_{oxd} + C_{subd})}{G_{subd}^2 + \omega^2 (C_{oxd} + C_{subd})^2} \tag{4.6}$$

The modeling proceeds as follows. First, each inductor size (r=80 μm, 100 μm, 120 μm and 160 μm) was simulated with Agilent Momentum using a setup similar to that shown in Fig. 4.3(a), but with only one inductor. The output from Momentum is a single complex number S_{11} versus frequency. Eleven frequency points were simulated– one point at 100 MHz and ten points from 2GHz to 20 GHz every 2 GHz.

Next, the simulated S_{11} is converted to a complex admittance Y_{11} using the formulas shown in Appendix A.

Using a nonlinear fitting program the set of parameters L_s, R_{sp}, C_{oxd}, G_{subd} and C_{subd} that give the best fitting of (4.5) and (4.6) to the EM-simulated Y_{11} was extracted. Matlab's least-squares "lsqnonlin" routine [68] was used in this case for simplicity.

For the extraction process, the following approximate expressions were used for each parameter as an "initial guess" [10]

$$L_s \approx \mu_0 n^2 r, \tag{4.7}$$

$$R_s \approx R_{sh} \frac{w}{l_{tot}}, \tag{4.8}$$

$$C_{oxd} \approx \frac{\varepsilon_{ox}}{2d} w \cdot l_{tot}, \tag{4.9}$$

$$C_{sub} \approx \frac{C'_{sub}}{2} w \cdot l_{tot}, \tag{4.10}$$

and

$$G_{sub} \approx \frac{G'_{sub}}{2} w \cdot l_{tot}, \tag{4.11}$$

where w=20 μm is the width of the spiral, l_{tot} is the total length of the inductor given by

$$l_{tot} = 2r \tan\left(\frac{\pi}{8}\right), \tag{4.12}$$

and d is the distance between the spiral and the substrate, ε_{ox} is the electrical permittivity of the silicon dioxide, and typical published values were used for the substrate's capacitance and conductance per unit area $C'_{sub} = 10^{-3}\, fF/\mu m^2$ and $G'_{sub} = 10^{-7}\, S/\mu m^2$ respectively.

Fig. 4.6 shows the simulated real and imaginary part of the admittance for a coplanar inductor with r=100 μm. Also shown are the calculated values from equations (4.5) and (4.6) using both the initial guess from (4.7)-(4.10) and the extracted model.

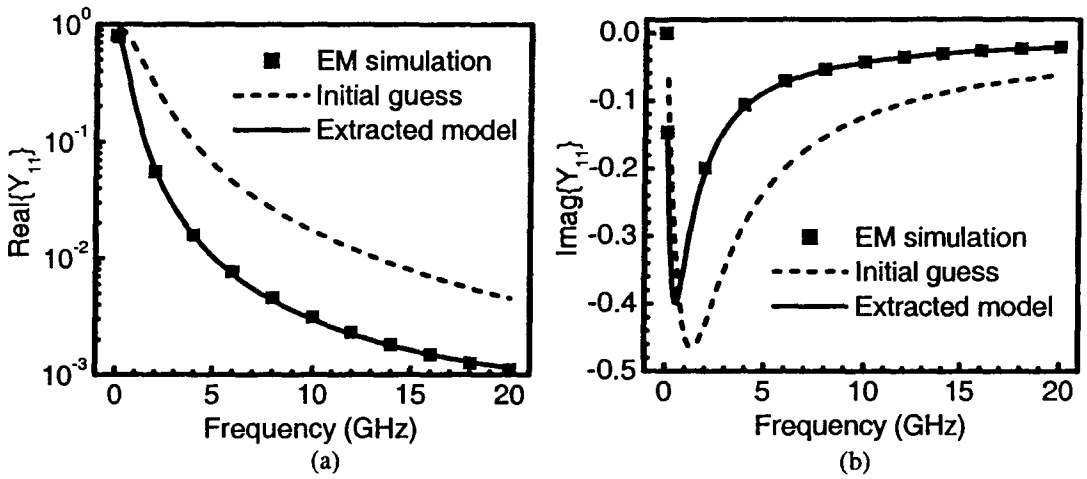

Fig. 4.6. Simulated and calculated admittance of single-turn inductor with r=100μm. (a) Real part. (b) Imaginary part.

To further verify the extracted model, Fig. 4.7 shows the "effective" inductance, defined as [69]:

$$L_{seff} \equiv -\frac{1}{2\pi f \,\mathrm{Im}\{Y_{11}\}} \tag{4.13}$$

and the quality factor calculated from

$$Q = -\frac{\mathrm{Im}\{Y_{11}\}}{\mathrm{Re}\{Y_{11}\}}. \tag{4.14}$$

A very good Q of 20 at 20 GHz is observed, and the inductance remains essentially constant over the 0-20 GHz band, showing that these inductors are suitable for use in a distributed amplifier up to 20 GHz.

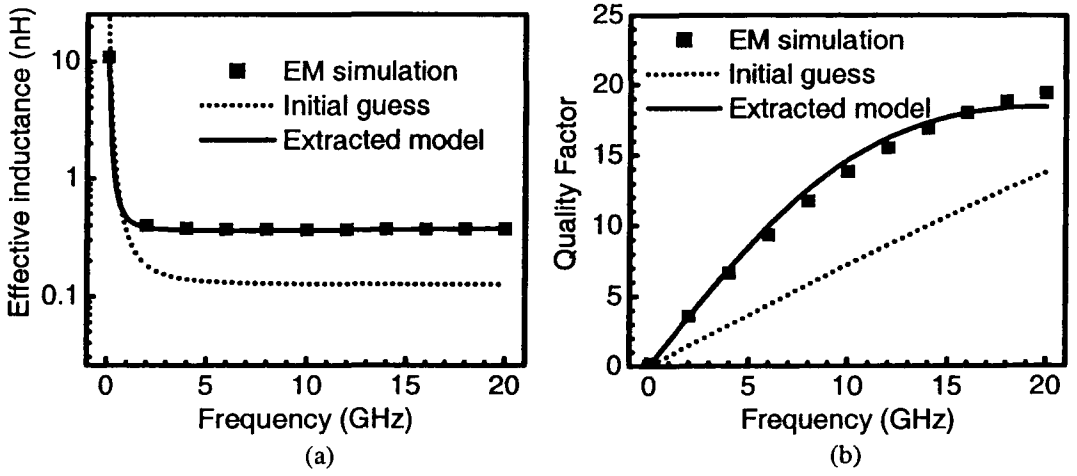

Fig. 4.7. (a) Simulated and calculated "effective" inductance and (b) Simulated and calculated quality factor of single-turn inductor with r=100μm.

The final step in the extraction process is to create a model whose equivalent circuit parameters (L_s, R_{sp}, C_{oxd}, C_{subd} and G_{subd} in this case) scale with the inductor geometry. This was obtained by performing a polynomial fitting of each of these extracted parameters versus the inductor radius, as shown in Fig. 4.8, Fig. 4.9, Fig. 4.10, Fig. 4.11 and Fig. 4.12.

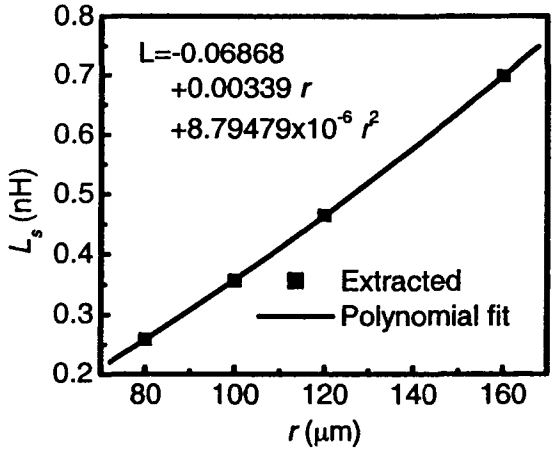

Fig. 4.8. Extracted inductance versus inductor radius and polynomial fit.

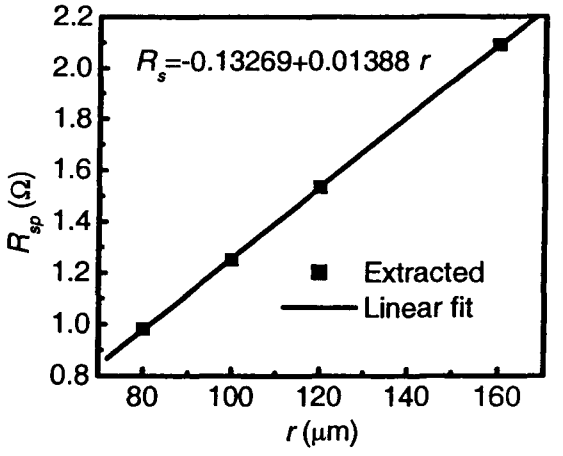

Fig. 4.9. Extracted series resistance versus inductor radius and linear fit.

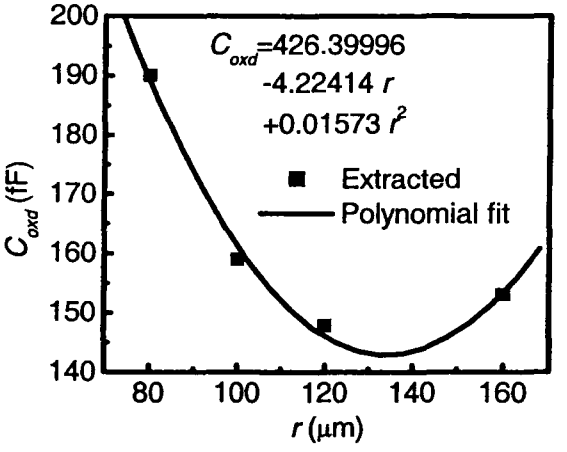

Fig. 4.10. Extracted oxide capacitance inductance versus inductor radius and polynomial fitting.

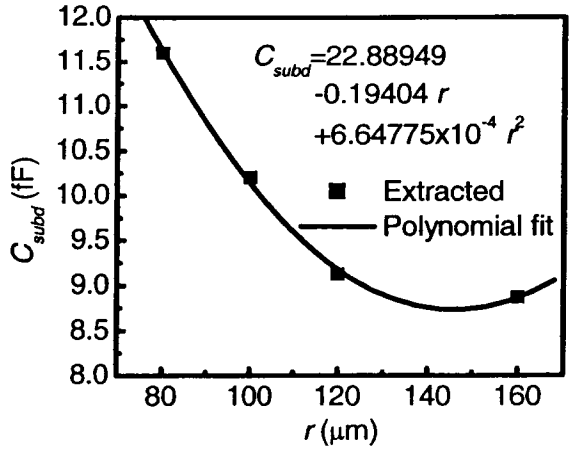

Fig. 4.11. Extracted substrate capacitance versus inductor radius and polynomial fitting.

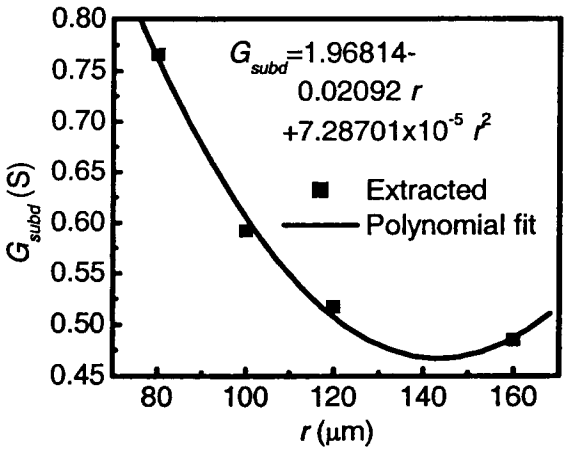

Fig. 4.12. Extracted substrate conductance versus inductor radius and polynomial fitting.

Both the inductance L_s and the series resistance R_{sp} increase with increasing radius, as would be expected from physical considerations. The other components C_{oxd}, G_{subd} and C_{subd}, however, present and abnormal behavior which is not consistent with equations (4.9)-(4.11). Note, for example, the presence of a minimum in these three parameters for r~140 μm. Nevertheless, while this modeling technique is not very physical, it gives a good compromise between accuracy and computational efficiency. For example, the required radii to achieve the inductances in Table 4.1 can be easily

calculated (see Table 4.2), and this model can be easily incorporated into a circuit simulator.

Table 4.2. Inductor sizes for the distributed amplifier.

Element	*Inductance*	*Approximate radius*
L_1	690 pH	160 μm
L_2	550 pH	135 μm
L_3	360 pH	100 μm

One last thing that should be mentioned here is that for the fitting/extraction process described above, the use of Y-parameters should be preferred over other parameter sets. We found that when trying to use the *Z* parameters for this process, there were problems associated with singularities at low frequencies. Also, trying to directly use the EM-simulated S-parameters for the fitting is not a good choice: it was found that there are many sets of parameters L, R_{sp}, C_{oxd}, C_{subd} and G_{subd} that give very good fitting to the S-parameters, but that are entirely non-physical (they include, for example, negative capacitances or resistances). When using Y-parameters, on the other hand, the extraction process was very robust, and even when using different initial parameters, the same extracted values were obtained.

4.1.3. Interconnections

The components in the distributed amplifier were connected using coplanar waveguides (CPW) for the paths carrying RF signals. This allows having well-controlled impedance levels, and provides a proper return path for all the high-frequency currents. The use of planar transmission lines as interconnections is standard practice in conventional discrete and hybrid microwave circuit design [22].

Since the amplifier operates with input and output impedances of 50 Ω, the CPWs connecting the amplifier to the input and output pads should ideally have the same

characteristic impedance to minimize reflections. All the other CPWs were also designed to be 50 Ω to simplify the layout.

There are two main geometrical parameters that control the characteristic impedance of a CPW: the width of the central conductor (*W* in Fig. 4.14) and the spacing from the central conductor to the ground planes (*S* in Fig. 4.14). Also, while typical discrete designs have ground planes that fill every space where there is no CPW (the ground planes are said to have "infinite" width), in CMOS technology large metal areas are not allowed, so we used what is known as Finite Ground Plane CPW, where the ground plane is a metal trace with a finite thickness (see Fig. 4.13). The main effect of the finite ground plane is that the characteristic impedance is slightly increased compared to the ideal CPW [22].

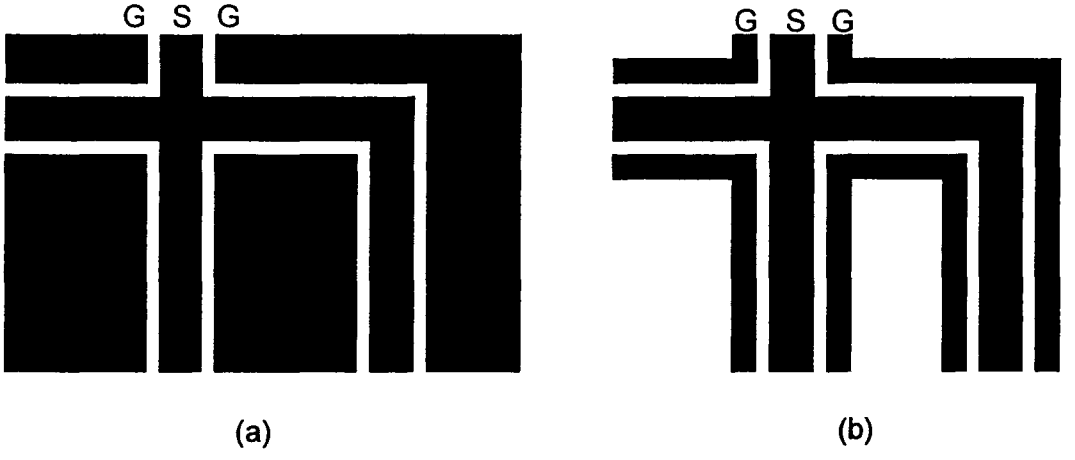

Fig. 4.13. Sample layout of a circuit using (a) Coplanar Waveguide (CPW) and (b) Finite Ground Plane CPW.

The first-order design of the CPW was done using equations (B.7)-(B.10) in Appendix B for a target impedance of 50 Ω, keeping the width of the central conductor fixed at 20 μm to have low loss and to simplify the connection to the coplanar inductors. The resulting dimensions are shown in Fig. 4.14. The design was verified using EM

simulations with Agilent's Momentum; the resulting characteristic impedance versus frequency is shown in Fig. 4.15.

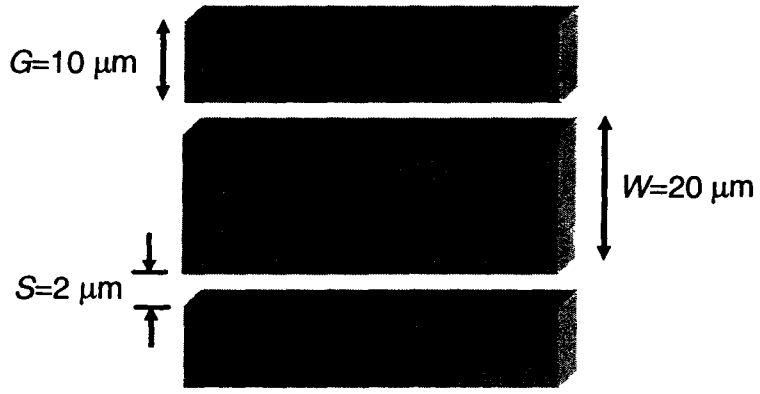

Fig. 4.14. Geometry of the 50 Ω coplanar waveguide with finite ground planes.

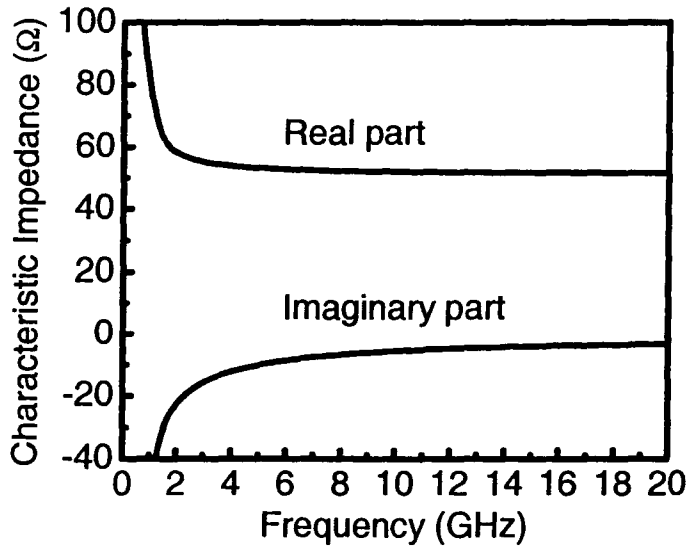

Fig. 4.15. Simulated characteristic impedance of the CPW with the dimensions shown in Fig. 4.14. The characteristic impedance was calculated from the simulated S-parameters using the equation (A.10) in Appendix A. Since the lines are lossy, the characteristic impedance is a complex number.

As discussed in Chapter 2, coplanar waveguides require the addition of "airbridges" that connect the two ground planes wherever there is a discontinuity. The

metal layer below the top one was used to implement such connection, as shown in Fig. 4.16. These bridges where placed on every "T" and "L" connection, and also where the CPW was connected to the input/output pads and to the active and passive components.

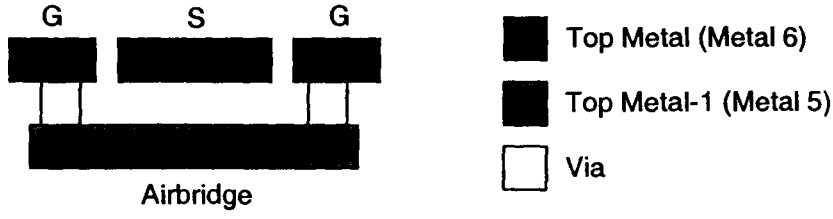

Fig. 4.16. Airbridge in CMOS technology.

Since the spacing between ground and signal pads at the input and output is much bigger than the spacing between the central conductor and the ground planes of the CPW, tapering of the coplanar waveguides was required to connect them to the pads, as shown in Fig. 4.17. Ideally, the tapering angle should be small (or equivalently the tapering distance should be large) to minimize reflections. In the CMOS technology used, however, angles are limited to multiples of 45°.

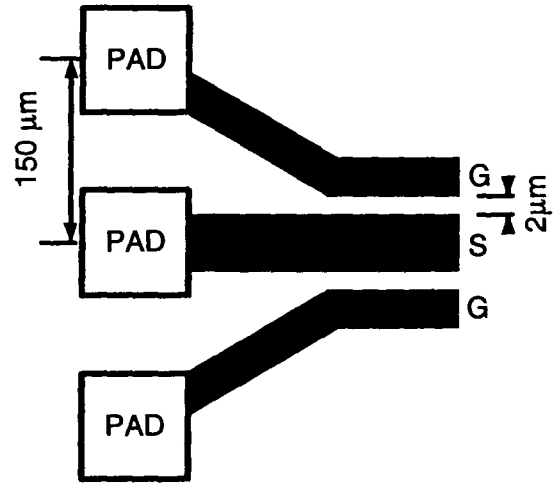

Fig. 4.17. Tapered connections between the coplanar waveguides and the input/output pads (not to scale). The angle of the tapered connections with respect to the horizontal is 45°.

4.1.4. Other components

The transistors, capacitors and resistors were implemented using the standard components provided by the foundry library. The library includes simulation models which are calibrated based on measurement data, and also include temperature parameters.

The capacitors are Meta-Insulator-Metal, and the termination resistors are low-resistivity polysilicon strips.

4.1.5. Layout and simulation

Fig. 4.18 shows a photograph of the complete layout. All 12 coplanar inductors can be clearly seen, as well as the tapered input and output connections and the pads.

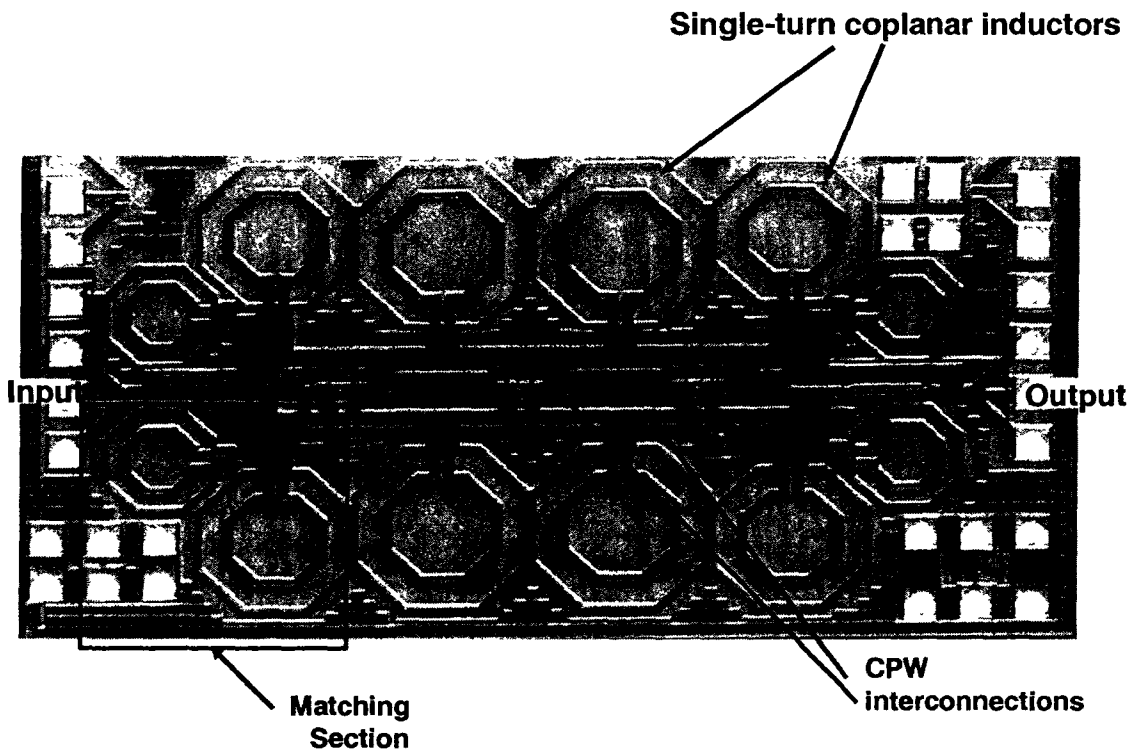

Fig. 4.18. Photograph of the distributed amplifier chip.

After the layout was completed, a final simulation was performed including all the interconnections. All the inductors and CPWs were simulated together as a single structure using Momentum, with ports at the points where the lumped elements are connected. The simulation results will be presented in the next section together with the measurement results.

4.2. EXPERIMENTAL RESULTS

4.2.1. Experimental setup

The distributed amplifier chip was probed on-wafer using Cascade Microtech Ground-Signal-Ground RF probes (model 40A-GSG-150-LPW).

The scattering parameters of the amplifier were measured using an HP 8722ES S-Parameter Network Analyzer, calibrated using Open-Short-Thru-Load method with a Picoprobe CS-5 calibration substrate. The DC voltages were provided by an HP4156B Semiconductor Parameter Analyzer, and the DC biasing of the input and output lines was provided through the internal bias-tees of the Network Analyzer. The complete test setup is shown in Fig. 4.19.

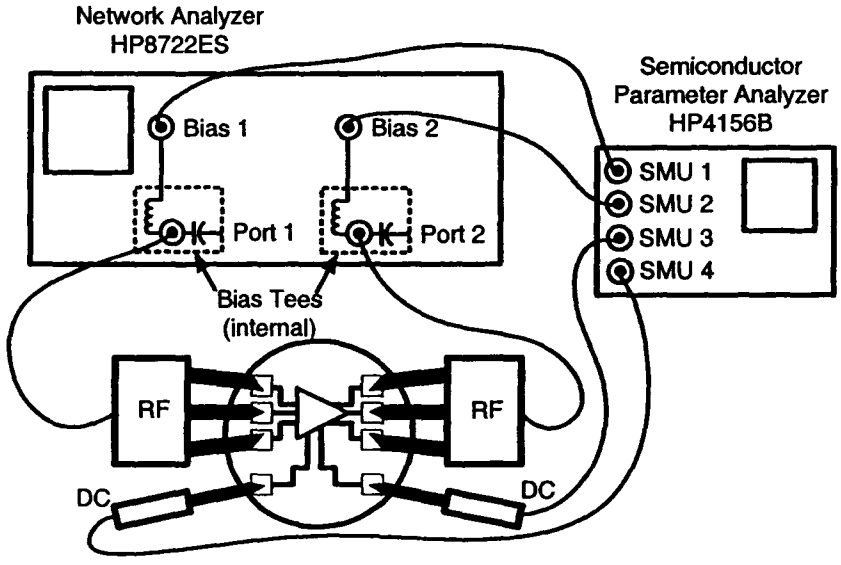

Fig. 4.19. Experimental setup for S-Parameter measurements.

The noise figure of the amplifier was measured using an Agilent 8975A Noise Figure Analyzer. The DC voltages were also provided by an HP4156B Semiconductor Parameter Analyzer, but connected to the amplifier by external bias-tees. The test setup for the noise figure measurements is shown in Fig. 4.20. The losses of all the cables and connectors were measured separately, and their values entered into the Noise Figure Analyzer for loss compensation.

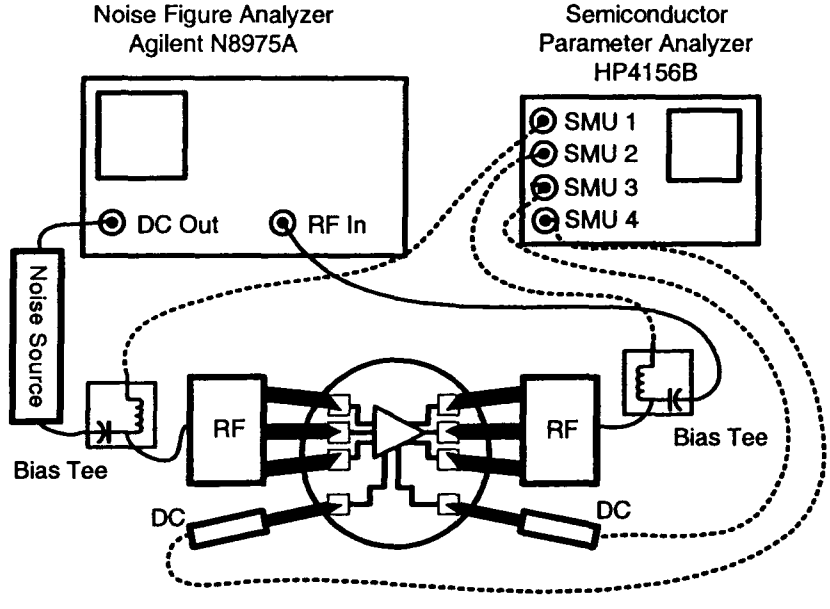

Fig. 4.20. Experimental setup for noise figure measurements.

The S-parameters and the noise figure were measured in the temperature range of 25 °C to 125 °C in 25 degree steps. A probe station with a heated chuck was used for this purpose, controlled by a Temptronic TPO315 system. After every temperature change, a waiting period of at least thirty minutes was allowed to make sure the whole system, including the chip, was at the same temperature.

Since one of the target applications of the amplifier is a fully integrated optical front-end, where the photodetector and transceiver electronics are included on the same chip as the amplifier, we de-embedded the effect of the pads and the probe connections by

using an "open" test structure similar to that shown in Fig. 4.17. The measured scattering parameters of the amplifier and open test structure were converted to Y-parameters using the equations in Appendix A, then the de-embedded Y parameters were calculated as [70]

$$Y_{AMP} = Y_{MEAS} - Y_{OPEN} \tag{4.15}$$

and finally the de-embedded Y-parameters were converted back to S-parameters.

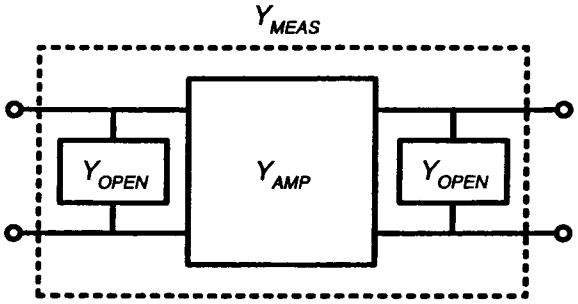

Fig. 4.21. De-embedding of the pad parasitics.

This de-embedding scheme removes the shunt component of the input connections, which in this case is dominated by the capacitance of the pads to the substrate. No de-embedding was performed for the noise figure measurements; noise de-embedding is a rather involved process, which requires measuring not only the noise figure but all the four noise parameters R_n, G_{opt}, B_{opt} and NF_{min}, and also several test structures besides the "open" [71] are needed. Since the pads add mostly capacitance to the input and output of the amplifier, but little resistive losses (which are most likely dominated by the relatively long input and output CPWs), their effect on the noise figure measurements should be very small. It could be argued that the pads also affect the input and output reflections and this might affect the noise measurements, but as will be shown in the next section, the effect of the pads on the reflections coefficients S_{11} and S_{22} is relatively small.

All the measurements were performed on at least three different chips. Unless otherwise stated, the results presented in the next two sections correspond to typical performance.

4.2.2. Room temperature results

Fig. 4.22 shows the measured and simulated power gain of the amplifier at room temperature (25 °C). The de-embedded high-frequency gain is approximately 5 dB, and the unity-gain frequency is 14 GHz. The gain is higher at lower frequencies due to the blocking capacitors inserted in series with the termination resistors (C_{bpass} in Fig. 4.1). Note that since the gain is proportional to the termination impedance (equation (3.9)), C_{bpass} has the opposite effect of typical DC blocking capacitors inserted at the input or output, which decrease the gain at lower frequencies. The measured gain before de-embedding is lower, and the difference is more significant at higher frequencies, which is to be expected, since the capacitive effect of the pads degrades the gain at high frequencies.

The bandwidth of the amplifier is significantly lower than what the first-order design predicted; recall that in section 4.1.1 a cutoff frequency of f_c=23 GHz was used for design. This difference can be attributed mostly to the parasitic capacitances of the inductors and interconnections.

The magnitude of the input and output reflection coefficients S_{11} and S_{22} are shown in Fig. 4.23. The input reflection coefficient is below -10 dB, which corresponds to a Voltage Standing Wave Ratio of 1:1.93, in the 2-14 GHz band. The output reflection coefficient is below -9 dB, which gives a VSWR of 1:2.1. The effect of de-embedding on the input and output reflections is relatively small.

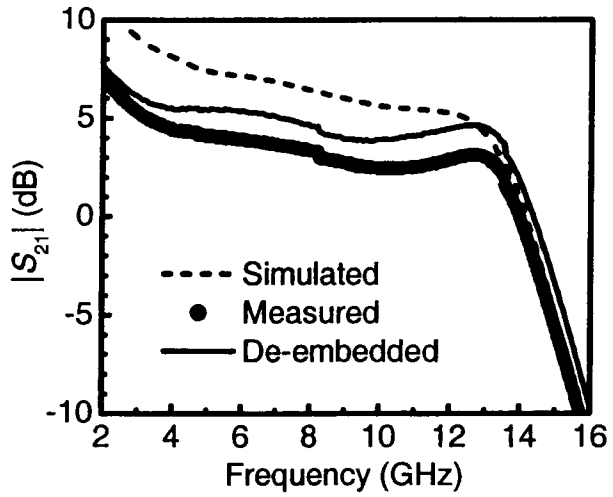

Fig. 4.22. Measured and simulated magnitude of the forward gain of the distributed amplifier at room temperature. The measured data is shown before and after de-embedding of the pads.

Note that the frequency dependences of S_{11} and S_{22} are relatively similar; since the input and output impedances of the MOSFET are very different, this suggests that the input and output reflections are not dominated by the MOSFETs, but by the interconnections, which are very similar between input and output due to the layout symmetry.

The magnitude of the reverse gain S_{12} is shown in Fig. 4.24. It is below -29 dB in the 2-14 GHz band, which provides a good amount of input-output isolation. The agreement between measurement and simulation is not good below 8 GHz; this might be attributed to the difficulties associated with measuring accurately high levels of attenuation of less than -35 dB. Also, part of the reverse feedback is originated by parasitic elements which are not well characterized in the MOSFET model because they are highly process and layout-dependent. These include the inductance at the source terminal, which provides series feedback, and the gate-drain capacitance C_{gd}.

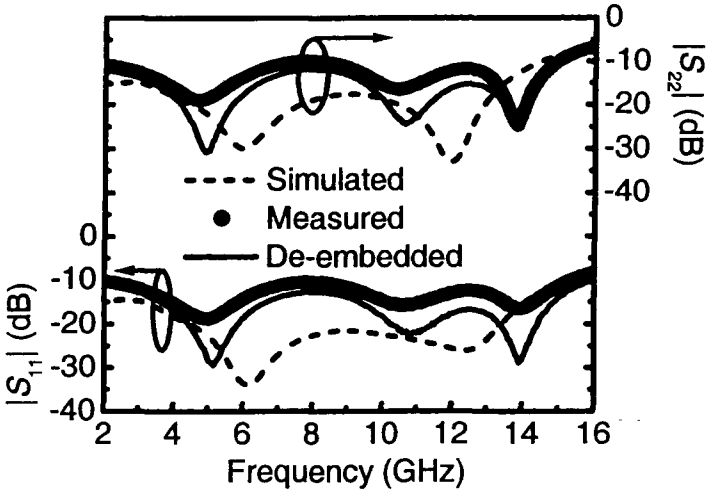

Fig. 4.23. Measured and simulated magnitudes of the input and output reflection coefficients of the distributed amplifier at room temperature. The measured data is shown before and after de-embedding of the pads.

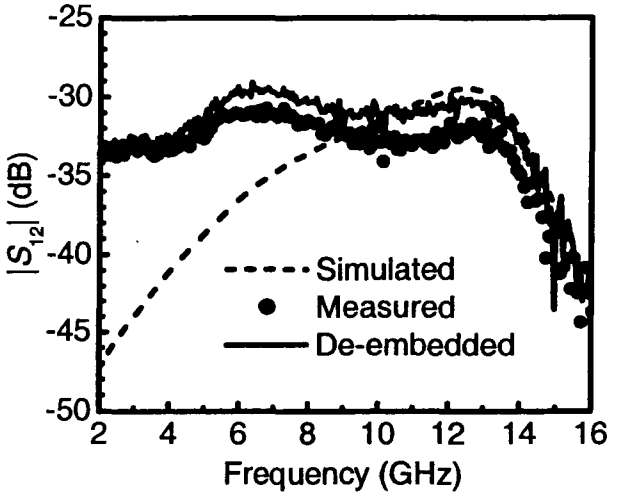

Fig. 4.24. Measured and simulated reverse gain of the distributed amplifier at room temperature. The measured data is shown before and after de-embedding of the pads.

Fig. 4.25 shows the group delay, calculated as

$$GD = -\frac{1}{2\pi}\frac{\partial \angle S_{21}}{\partial f} \tag{4.16}$$

where $\angle S_{21}$ is the phase of S_{21} in radians. It can be seen that GD is approximately 80 ps at low frequencies, in good agreement with the calculations from (3.21), using n=3 and f_c=13 GHz we get GD=74 ps for $f<<f_c$, but it peaks significantly as the cutoff frequency is approached. This shows a disadvantage of using gain peaking to compensate for losses in CMOS distributed amplifiers: while a relatively flat gain is achieved, the group delay peaks close to cutoff. This is often overlooked in CMOS distributed amplifiers, and none of the published implementations we reviewed reported group delay measurements [52]-[62].

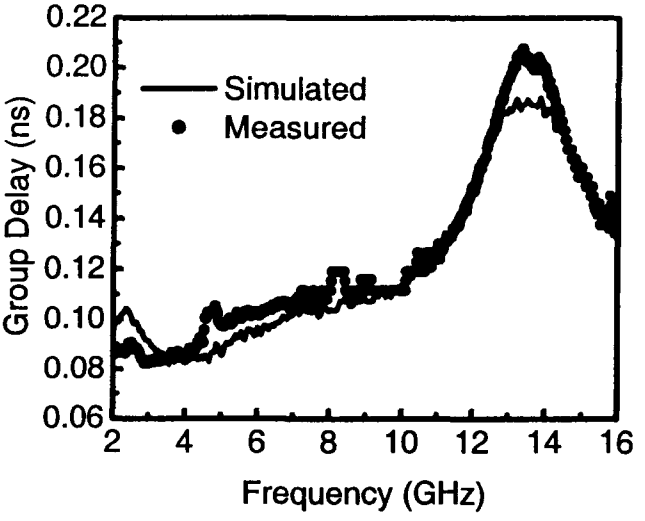

Fig. 4.25. Measured and simulated group delay of the distributed amplifier at room temperature. De-embedded data not shown for clarity because de-embedding has negligible effect on the group delay.

The measured noise figure is shown in Fig. 4.26. It is between 6 and 8 dB in the 2 GHz-10 GHz frequency range, and then increases sharply up to 13 dB close to the cutoff frequency. Again, while gain peaking can help compensate for the losses as far as the amplifier gain is concerned, this compensation does not work for the noise figure. Also

shown in Fig. 4.26 is the noise figure calculated from (3.31), with the gain G taken from the measurements, the channel thermal noise calculated from (2.28) and the induced gate noise from (2.32). The noise figure was not simulated with a circuit simulator because the noise model of the MOSFETs is not calibrated and the EM simulations of the inductors and interconnections do not include their thermal noise.

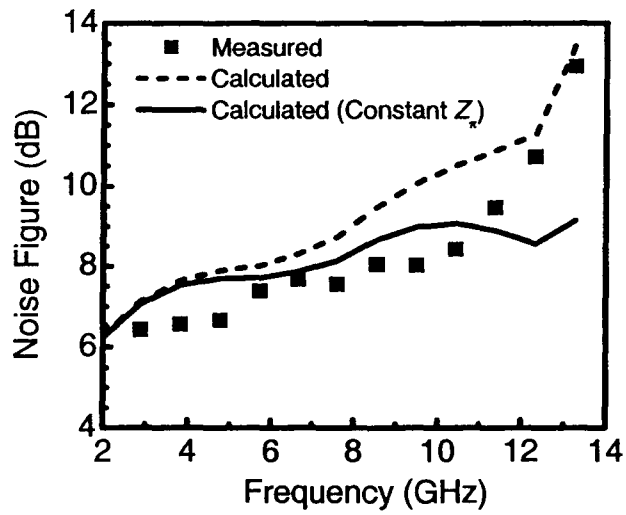

Fig. 4.26. Measured and calculated noise figure of the distributed amplifier at room temperature. The dashed line shows the noise figure calculated with (3.31) with the values of $Z_{g\pi}$ and $Z_{d\pi}$ from (3.7) and (3.8), the solid line shows the noise figure calculated with (3.31) assuming $Z_{g\pi} = Z_{d\pi}$=50 Ω.

The dashed line in Fig. 4.26 corresponds to the noise figure calculated using the values of $Z_{g\pi}$ and $Z_{d\pi}$ given by (3.7) and (3.8). It can be seen that (3.31) overestimates the noise figure at medium-high frequencies; this can be attributed to the fact that the impedances $Z_{g\pi}$ and $Z_{d\pi}$ given by (3.7) and (3.8) go to infinity as the cutoff frequency is approached, which would be the case only if lossless elements were used in the artificial lines. For comparison, the solid line in Fig. 4.26 shows the noise figure calculated also with (3.31) but assuming constant impedances $Z_{g\pi}$ and $Z_{d\pi}$, equal to 50 Ω; in this case the agreement is better in the middle of the band, but the noise figure is underestimated close to cutoff due to the lack of peaking. A more accurate model for the noise figure would

require explicitly including the effects of the losses in the artifficial lines, not only because of the noise they generate, but also because they significantly affect other parameters of the distributed amplifier, such as the gain and reflection coefficients, which in turn affect the noise figure.

4.2.3. Temperature measurements

Fig. 4.27 shows the de-embedded gain[2] of the amplifier when the temperature was varied between 25 °C and 125 °C in 25 degree steps. As expected from the discussion in Chapter 2, the gain decreases with temperature above room temperature; also, the degradation is slightly more significant at higher frequencies. The reason for this is that the resistive losses of the passives increase with temperature, and as was discussed in Chapter 3, resistive losses in the artificial lines affect more the gain at the higher frequencies.

Note that Fig. 4.27 shows the measured gain for two different chips. It was not possible to measure the same chip at all five temperatures because after two or three measurements, it was very difficult to make a good contact with the pads because the probe tips makes deep scratches on them, and it was not feasible to just leave the probes connected in the whole temperature range because thermal expansion of the chip caused the pads to move with respect to the probes. This is the reason why in Fig. 4.27, the gains at 50 °C and 75 °C almost overlap: due to chip-to-chip gain variation, the second chip had almost the same gain at 75 °C as the first one at 50 °C.

[2] The S-parameters of the "open" structure were measured at all the temperature points and used to de-embed the corresponding amplifier S-parameters (for example, the measured open at 50 °C was used to de-embed the amplifier at 50 °C).

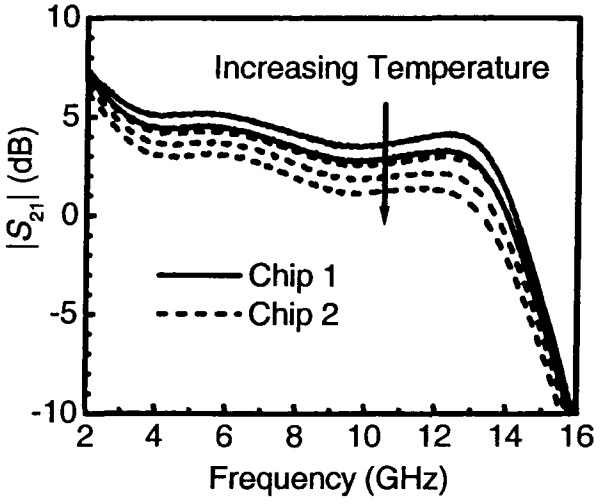

Fig. 4.27. Measured forward gain with temperature as a parameter between 25 °C and 125 °C in 25 degree steps.

Fig. 4.28 shows the average high-frequency gain degradation (with respect to room temperature) for three different chips at 12.5 GHz. The averaging should minimize the effect of chip-to-chip variation on the results. The measured gain drops by approximately 0.37 dB per every 10 °C of temperature increase, while the simulated gain degradation is 0.22 dB per 10 °C; the differences are most likely due to the fact that, while the simulation uses a temperature-dependent model for the transistors, resistors and capacitors, the inductors and interconnections were simulated at a single temperature.

Note that temperature is not an explicit parameter in most commercial EM simulators, so any temperature effect must be included through parameters such as material resistivity. This would require knowing the temperature dependence of these parameters, either by calculating them from first principles or from measurements of special test structures.

It is also apparent from Fig. 4.28 that the agreement between simulated and measured gain degradation is better at the lower temperature range; this would suggest that close to room temperature, the dominant temperature effect is the reduction of MOSFET transconductance (which is included in the simulation); beyond 75 °C,

however, the increase in the losses in the inductors and interconnects becomes more important and the agreement between measurements and simulation gets worse.

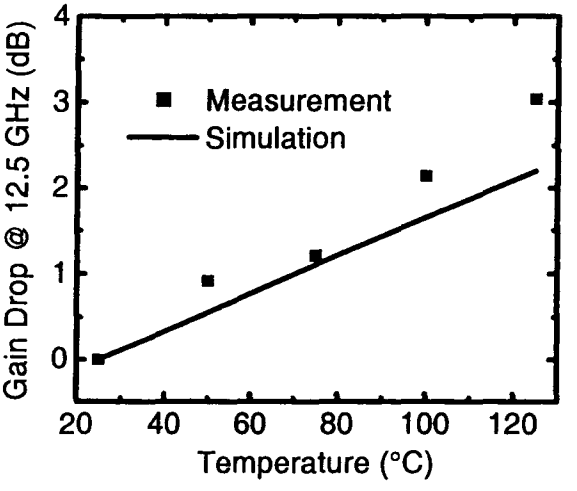

Fig. 4.28. Measured and simulated gain drop at 12.5 GHz with respect to room temperature (measurement is average for three different chips).

As shown in Fig. 4.29, Fig. 4.30 and Fig. 4.31, the change in the magnitude of the input and output refection coefficients, the magnitude of the reverse gain and the phase of the forward gain with temperature are very small, and in some cases the chip to chip variation is more significant than the change with temperature. The reason for this is that these parameters depend mostly on reactive elements (capacitances and inductances), which have very small temperature dependence.

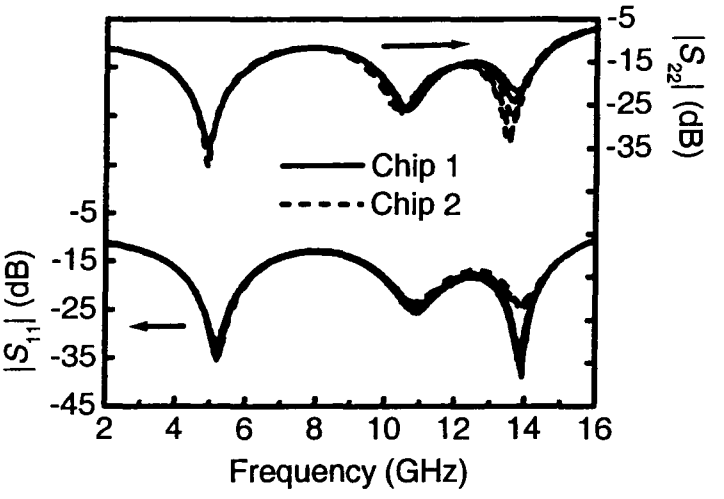

Fig. 4.29. Measured input and output reflection coefficients with temperature as a parameter between 25 °C and 125 °C in 25 degree steps. Almost no temperature dependence was observed.

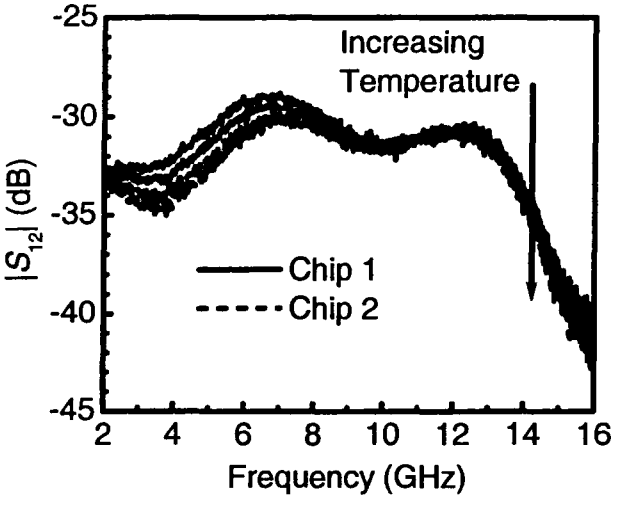

Fig. 4.30. Measured reverse gain with temperature as a parameter between 25 °C and 125 °C in 25 degree steps.

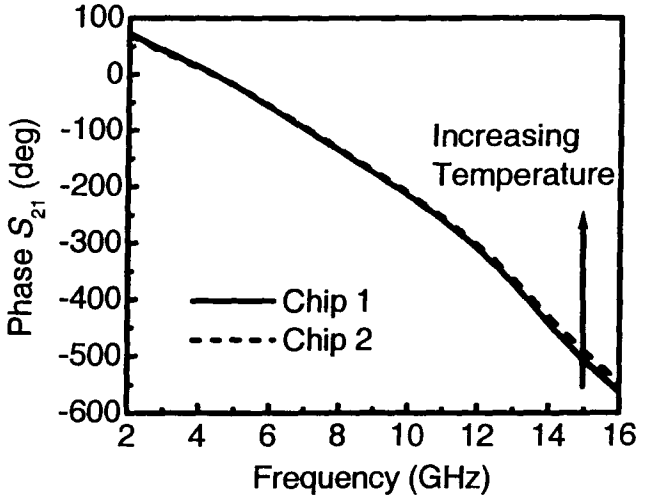

Fig. 4.31. Measured phase of the forward transmission S_{21} with temperature as a parameter between 25 °C and 125 °C in 25 degree steps. Phase is shown instead of group delay because the scattering caused by numeric differentiation completely masks the small difference between the curves.

The change of the noise figure with temperature is shown in Fig. 4.32. For the same reasons as before, it was not possible to measure the same chip in the whole temperature range, so the results for two different chips are shown.

The noise figure increases with temperature, due both to the increase of the losses in the passives, as all dissipative elements generate noise, and because of the reduction in MOSFET transconductance (the noise figure depends on the gain, which in turn depends on the transconductance). The increase in noise figure with temperature is approximately 0.17 dB per 10 °C at 12.5 GHz , which is lower than the gain degradation. A detailed explanation of this trend would require an accurate temperature-dependent noise model for the MOSFETs and for the passive elements.

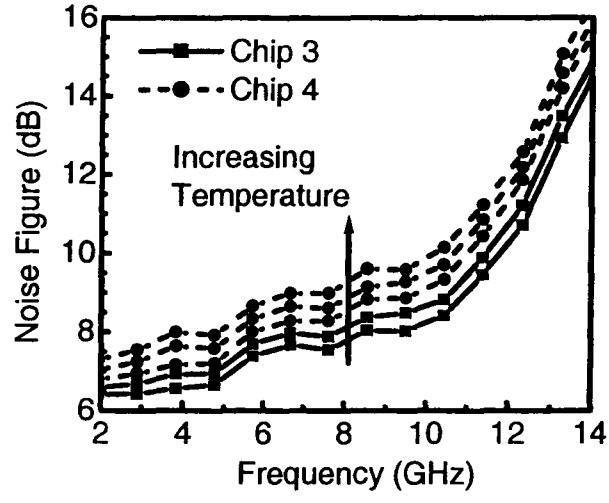

Fig. 4.32. Measured noise figure with temperature as a parameter between 25 °C and 125 °C in 25 degree steps.

4.3. SUMMARY

The measured performance of the amplifier at room temperature is summarized in Table 4.3. The results are comparable or better than recent published implementations in standard CMOS technologies [56], [60]. Some other implementations achieve improved gain or bandwidth through the use of special processes [53], [57], [58].

In the temperature range of 25 °C to 125 °C, the high-frequency gain of the amplifier drops at approximately 0.37 dB per every 10 °C, due to reduction of MOSFET transconductance and increase of the resistive losses in the inductors and interconnections. The noise figure also drops at high temperatures, due to similar reasons, but a lower rate of 0.17 dB per 10 °C at high frequencies.

More research is required for the development of temperature-dependent models for the inductors and interconnections, which should also include the thermal noise contributed by these elements

Table 4.3. Summary of measured distributed amplifier performance at room temperature.

Forward Gain	7-5 dB @ 2 GHz - 13.5 GHz
Unity-gain frequency	14 GHz
Input reflection coef. (max.)	-10 dB
Output reflection coef. (max.)	-9 dB
Reverse transmission (max.)	-29 dB
Group delay	80-210 ps
Noise Figure	6 dB - 8 dB @ 2 GHz-10 GHz 6 dB - 13 dB @ 2 GHz-13.5GHz
Power Consumption	86 mW with 1.8 V supply
Chip Area	2.6 x 1.3 mm^2

Chapter 5
CMOS Resistive-Match Amplifier Design and Experimental Results

5.1. INTRODUCTION

While distributed amplifiers have the potential of offering very wide bandwidths with low input and output reflections, this is achieved at the expense of relatively high power consumption, and a large chip area due to the number of inductors required. Moreover, while distributed amplifiers can in principle be designed to be low-pass, with bandwidths extending down to DC, doing so considerably increases the power consumption due to the power dissipated on the termination resistors, and this further complicates the design because the input and output interconnections have to be made very wide to support the large currents that would flow.

In this chapter, we explore an alternative design technique for broadband amplifiers with bandwidths that extend down to very low frequencies.

The concept of resistive-reactive matching is introduced in section 5.2. Section 5.3 describes the design of a CMOS resistive-match amplifier; the experimental results for the designed amplifier are presented in section 5.4, while a summary of the key results and a comparison with the distributed amplifier is presented in section 5.5.

5.2. RESISTIVE MATCH AMPLIFIERS

A major challenge in implementing broadband amplifiers is to achieve low input and output reflections while at the same time having a flat gain response over the desired bandwidth. This is especially difficult to achieve when using field-effect transistors as the active elements, because the input impedance of these devices is mainly capacitive, while a constant and real impedance is desired for low reflections. One approach to realize this constant real impedance is to simply place resistors at the input and output of the device

as shown in Fig. 5.1(a). If the resistors R_{in} and R_{out} are selected equal to the load and source resistances, then very low reflection coefficients can be achieved and the amplifier has a low-pass response. However, a disadvantage of this approach is that, due to the capacitances of the FET, the high-frequency gain is limited.

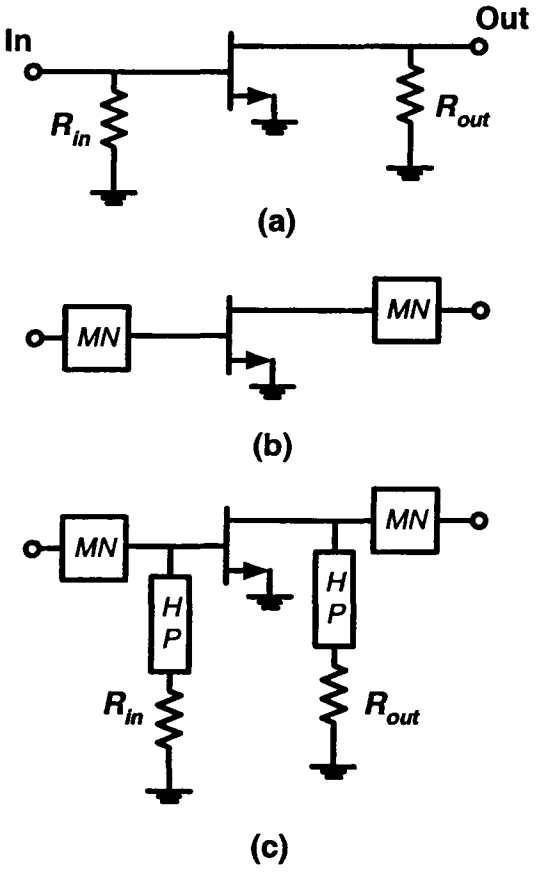

Fig. 5.1. (a) Resistive-coupled amplifier (b) Reactive-match amplifier (MN: Matching network) (c) Resistive match amplifier (HP: High-pass network) [72].

A common approach to obtain the maximum possible gain at high frequencies is to use reactive matching networks (MN) at the input and output of the active device, as shown in Fig. 5.1(b); by doing this the effect of the capacitances is reduced, and it is possible to achieve gains closer to the maximum available gain of the device with low

reflections. The disadvantage of this approach is that it only works in a narrow band of frequencies, so it is unsuitable for broadband amplifiers.

If the two approaches above are combined, it is possible to realize amplifiers with flat gain and low reflections over several octaves [72]. As shown in Fig. 5.1(c), low-pass reactive matching networks are inserted before the termination resistors. At low frequencies, these matching networks have no effect and the input and output impedances are essentially determined by the resistors. At higher frequencies, where the effect of the FET capacitances becomes important, the high-pass networks, which can be as simple as a series inductor, "remove" the resistors, and the amplifier becomes similar to a reactive-matched amplifier.

In order to apply the idea above to fully-integrated CMOS amplifiers, some modifications can be made to the basic approach of Fig. 5.1(c). First, the single common-source FET can be replaced with a cascode to improve stability and reverse isolation. Second, at the input, the high-pass network (HP) can be removed and only the shunt resistor and the reactive matching network will remain, as shown in Fig. 5.2. The idea is that at lower frequencies, the resistor R_1 dominates the input impedance, while at higher frequencies the matching network transforms the complex impedance Z_{in} into a real impedance.

In order to minimize reflections at low frequencies, the condition

$$R_1 = R_o \tag{5.1}$$

has to be satisfied, which would result in a low-frequency power gain of

$$G = \frac{g_m^2}{4} R_o^2, \tag{5.2}$$

where it has been assumed that the output and input resistances of the amplifier and the load and source resistances are equal to R_o.

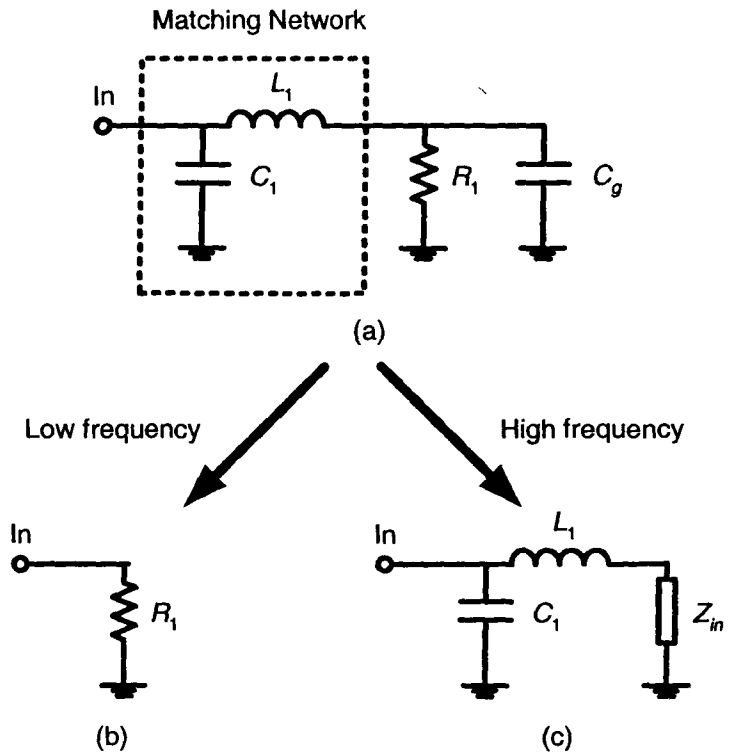

Fig. 5.2. (a) Input circuit of the resistive-match amplifier; the input impedance of the MOSFET is assumed to be purely capacitive (C_g), and an external resistor has been added in parallel; also a low-pass matching network is added. (b) At low frequencies, the resistor R_1 dominates the input impedance and the matching network has no effect. (c) At high frequencies, the matching network transforms the complex impedance Z_{in} to a real impedance.

The values of the elements of the matching network required to transform the parallel combination of C_g and R_1 into a purely resistive impedance R_o at the frequency ω are

$$L_1 = \frac{2C_g R_o^2}{1+(\omega C_g R_o)^2} \tag{5.3}$$

and

$$C_1 = C_g . \tag{5.4}$$

One additional modification that can be implemented in CMOS resistive-match amplifiers is to remove the output matching network. The reason for this is that the output impedance of the MOSFET is dominated by the drain-source resistance r_{ds} even at moderately high frequencies, so acceptable output reflection coefficients can be achieved using only the termination resistor R_{out} in Fig. 5.1(c).

5.3. CMOS RESISTIVE MATCH AMPLIFIER DESIGN

The complete schematic of the designed CMOS resistive match amplifier is shown in Fig. 5.3, and the component values are shown in Table 5.1.

An inductor was added between the transistors of the cascode pair; this inductor has the effect of increasing the gain at high frequencies, to compensate for the parasitic capacitances of the MOSFETs and achieve a relatively constant gain. The main tradeoff from the addition of this element is that the reverse isolation and the input matching are degraded [73].

The cascode pair is biased through dedicated DC pads. Also, not shown in Fig. 5.3 are three 2 pF capacitors connected close to the points labeled V_C, V_{gate} and V_{drain} to create a good AC ground in these nodes.

The transistor M_1 was sized to achieve a reasonable gain-bandwidth tradeoff (wider devices have more gain but higher capacitance too) with a low power consumption (the drain current was fixed at 10 mA). A device with minimum length (L=0.18 μm) and W=320 μm was found to have a transconductance of approximately 90 mS for I_D=10 mA with V_{gate}=0.64 V, which according to (5.2) gives a gain of 7 dB, and allows for a bandwidth of approximately 8 GHz; larger devices or higher currents decrease the bandwidth or increase the power consumption significantly with a very small increase in gain. While this gain is relatively low, two or more amplifiers can be connected in cascade to increase it.

The size of the transistor M_2 and the values of the inductor L_2 and the resistor R_2 were determined using SPICE simulations to achieve a flat gain over the passband and a low output reflection coefficient.

The initial design of the input matching network was done using (5.1), (5.3) and (5.4) with R_o=50 Ω at a frequency $\omega = 2\pi$ x 7 GHz, with the value of C_g determined using (4.1). This gives L_1=1.1 nH and C_1=640 fF and these values were fine-tuned using SPICE simulations.

The drain voltage V_{drain} and the cascode gate biasing V_C were chosen equal to the nominal supply voltage for the technology (1.8 V). In order to explore the highest gain that could be achieved with this amplifier, a second set of biasing voltages (which will be called the "high bias" condition in what follows) was chosen, with V_{drain}=V_C=3.3 V and V_{gate}=0.7 V (this gate voltage gives the maximum gain with a 3.3 V supply). While this supply is higher than the nominal voltage for the technology, this should not pose any reliability problems because the supply voltage drops across two transistors in series.

The square 1.5 turn spiral inductors were designed using Agilent Momentum [67], and 50 Ω coplanar waveguides were used for all the high-frequency the interconnections.

The simulated gain and reflection coefficients of the amplifier are shown in Fig. 5.4 and Fig. 5.5. The low-frequency gain for the low biasing condition is approximately 7 dB, in good agreement with (5.2), and drops to approximately 6.5 dB at 6 GHz. In the high biasing condition, the low-frequency gain increases by 2 dB, while the high-frequency gain increases by 1 dB; since the components M_2, L_2 and R_2 were optimized for flat gain in the low-biasing condition, changing the voltages results in a steeper gain roll-off.

The input and output reflection coefficients are lower than -10 dB between 0 and 7 GHz; the output reflection coefficient increases in the high-biasing condition, because of the change in the output resistance of the M_2 MOSFET.

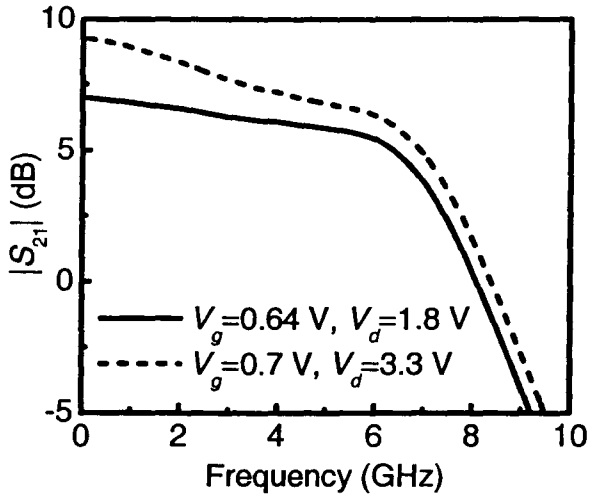

Fig. 5.4. Simulated magnitude of the forward gain of the designed resistive-match amplifier temperature at two biasing conditions.

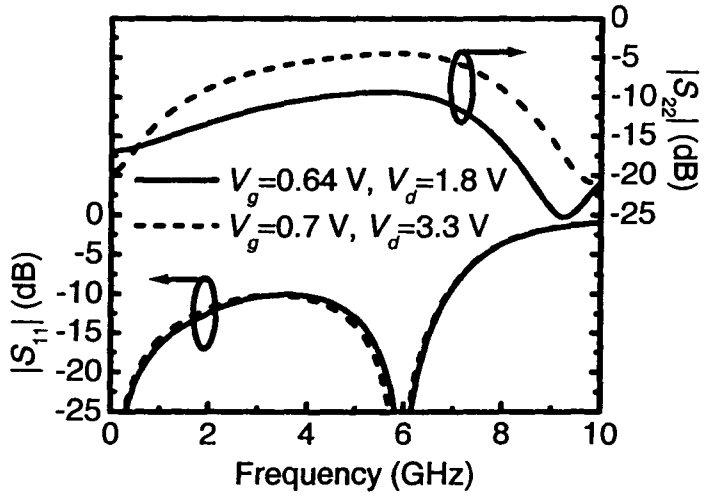

Fig. 5.5. Simulated magnitudes of the input and output reflection coefficients of the designed resistive-match amplifier at two biasing conditions.

A photograph of the fabricated amplifier is shown in Fig. 5.6. The chip occupies an area of 1.28 x 0.55 mm^2, including the connection pads.

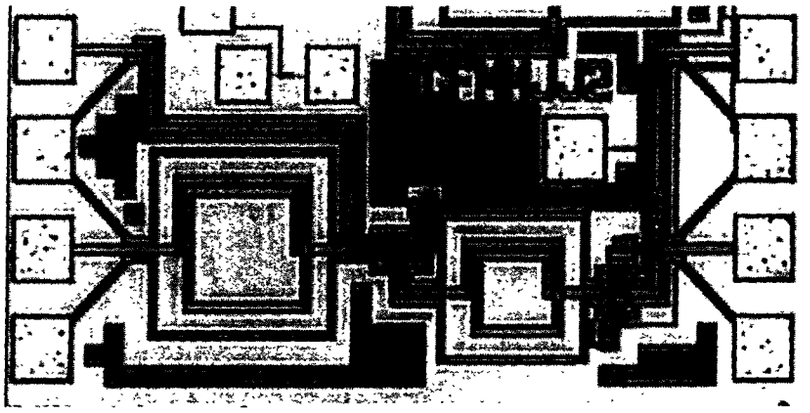

Fig. 5.6. Chip photograph of the resistive match amplifier.

5.4. EXPERIMENTAL RESULTS

The S-parameters and the noise figure of the resistive-match amplifier were measured using setups similar to Fig. 4.19 and Fig. 4.20 in the temperature range from 25°C to 125°C. Since it was found that the variation of most of the parameters with temperature is relatively small, then the results are shown only for a few temperatures in section 5.4.2.

Unlike the distributed amplifier where the gate and drain biasing were connected through the RF probes, in this case all the DC biasing voltages were connected through DC probes. It was found that de-embedding of the pads did not have a significant effect on the measured S-parameters below 8 GHz, so the results are reported without de-embedding only.

It was also found that the S-parameters deviated significantly from the simulations below 2 GHz. The reason is that at those frequencies, the DC connections V_{gate} and V_{drain} have significant effect on the amplifier performance, and since simple DC probes (not Ground-Signal-Ground probes) were used to supply these voltages, the probes themselves as well as the cables connected to them modify the amplifier characteristics. The simulations were modified to include these effects by adding an equivalent circuit for the

DC probes and cables as shown in Fig. 5.7; these are the simulation results used in what follows.

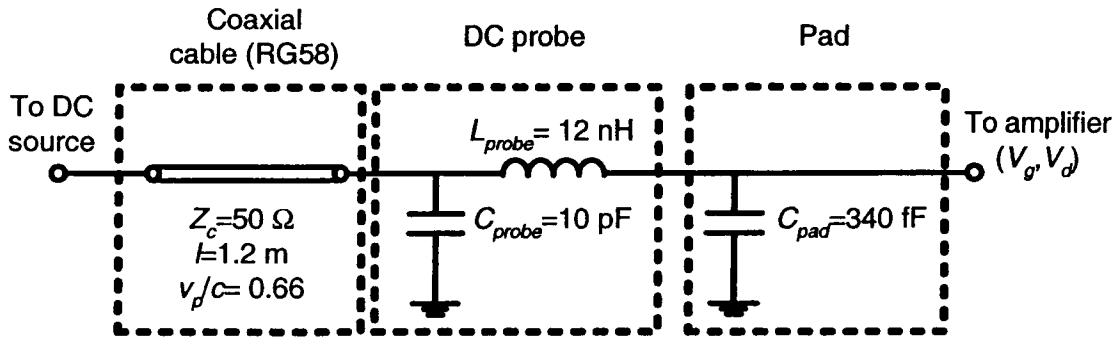

Fig. 5.7. Equivalent circuit of the DC pad, probe and cable. The elements L_{probe} and C_{pad} were calculated using the formulas for the inductance of a straight piece of wire and a two-plate capacitor respectively. C_{probe} was selected to give good fit to the experimental data and the cable characteristics are standard (v_p/c is the normalized phase velocity of the cable).

To minimize this effect, RF connections with controlled impedance levels should be used for the DC connections in future versions of the amplifier, with large filtering capacitors connected as close as possible to the pads.

5.4.1. Room temperature results

Fig. 5.8 shows the measured and simulated power gain of the amplifier at room temperature (25 °C) at the low and high bias conditions. The gain increases at lower frequencies because of the effect of the DC probes as discussed before; it can be seen that the simple model of Fig. 5.7 accounts for this effect.

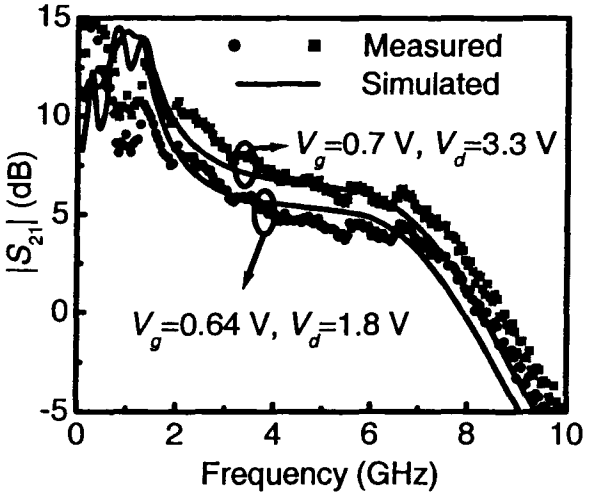

Fig. 5.8. Measured and simulated magnitude of the forward gain of the resistive-match amplifier at room temperature at two biasing conditions.

The magnitude of the input and output reflection coefficients S_{11} and S_{22} are shown in Fig. 5.9, where only the low biasing voltage is shown because the difference with respect to high biasing is negligible. The input reflection coefficient is below -3.5 dB except at very low frequencies, where it increases for the reasons explained before. The output reflection coefficient is below -5 dB. The difference with respect to the simulated values are probably due to parasitics that are not accounted for in the simulation. The fact that the measured S_{22} has no dependence on the biasing voltage (unlike the simulations in Fig. 5.5) further confirms this, because this indicates that the reflections are dominated by the passive elements and not by the MOSFET.

The magnitude of the reverse gain S_{12} is shown in Fig. 5.10. It is below -19 dB, and the agreement between measurement and simulation is not very good; as with the distributed amplifier, this is probably due to the fact that some of the reverse feedback is originated by parasitic elements which are not well characterized such as the inductance at the source terminal and the gate-drain capacitance C_{gd}.

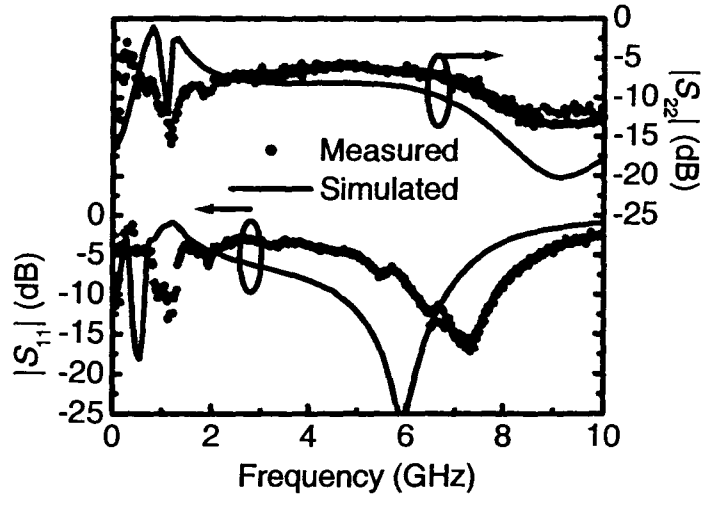

Fig. 5.9. Measured and simulated magnitudes of the input and output reflection coefficients of the resistive-match amplifier at room temperature. Only low-biasing condition shown since the results for the high-biasing condition are essentially the same.

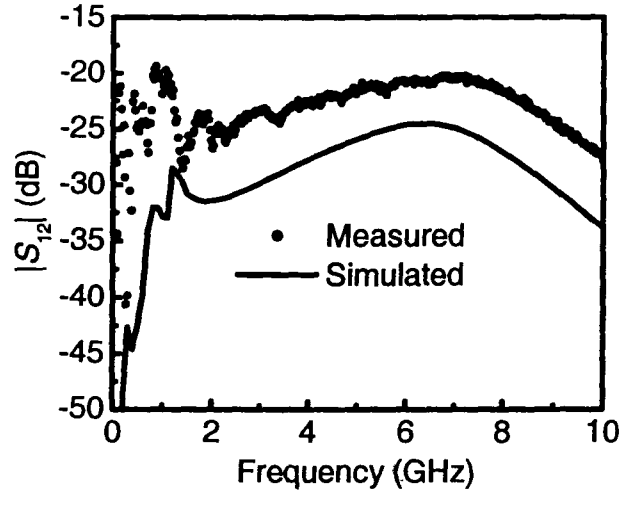

Fig. 5.10. Measured and simulated reverse gain of the resistive-match amplifier at room temperature. Only low-biasing condition shown since the results for the high-biasing condition are essentially the same.

Fig. 5.11 shows the group delay calculated from the phase of S_{21} using (4.16). It is between 40 ps and 150 ps in the 2 GHz-7 GHz band, and oscillates between higher and lower values below 2 GHz due to the effect of the DC probes.

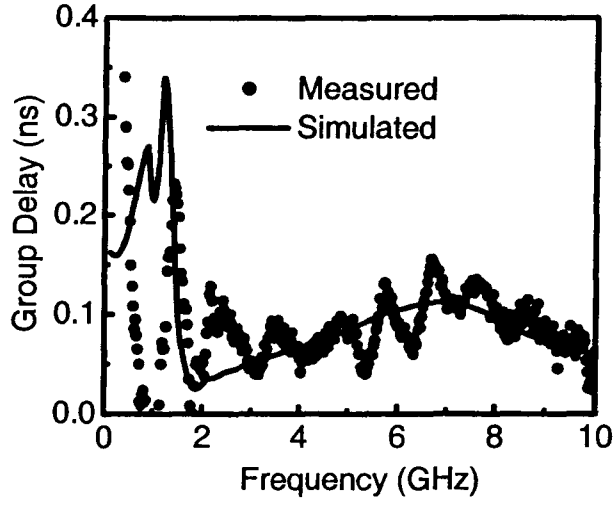

Fig. 5.11. Measured and simulated group delay of the resistive-match amplifier at room temperature. Only low-biasing condition shown since the results for the high-biasing condition are essentially the same.

The measured noise figure is shown in Fig. 5.12. It is between 4.1 dB and 5.4 dB in the low-bias condition and between 3.9 dB and 5.1 dB in the high-bias condition.

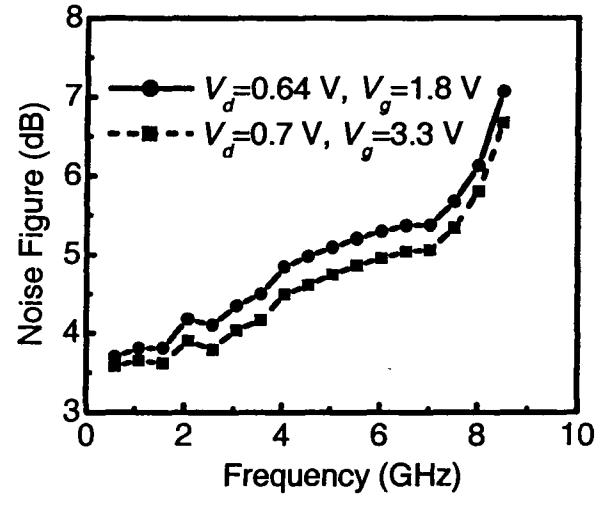

Fig. 5.12. Measured noise figure of the resistive-match amplifier at room temperature and at two different biasing points.

This shows that the use of a resistive termination in CMOS amplifiers does not necessarily imply excessively high noise figures, as has been stated in the literature (in [10] it is mentioned that the use of resistive matching can result in noise figures in excess of 11 dB).

5.4.2. Temperature measurements

Fig. 5.13 shows the measured gain of the amplifier at 25 °C and 125 °C in the low bias condition. The low-frequency gain changes very little, while the high-frequency gain drops by approximately 1 dB (at 6 GHz) for this 100 °C increase in temperature. This reduction in gain is lower than what was expected from simulations as shown in Fig. 5.14. An explanation for this effect could not be found.

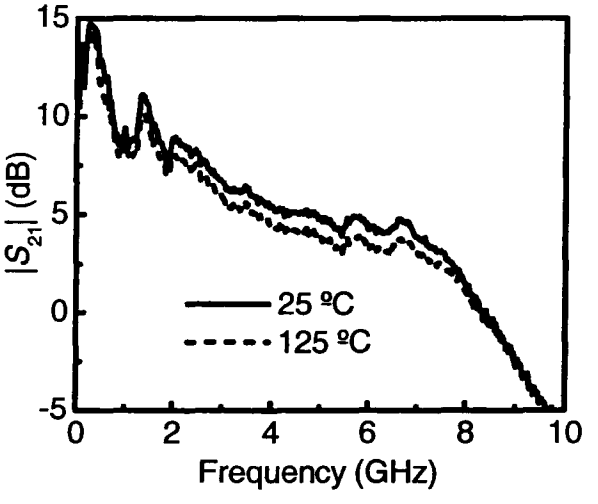

Fig. 5.13. Measured forward gain at two temperatures (low bias condition only).

As shown in Fig. 5.15 and Fig. 5.16, the changes in the magnitude of the input and output refection coefficients, and the phase of the forward gain with temperature are very small. This is expected since these parameters depend heavily on the reactive components (inductances and capacitances), which have very small temperature coefficients.

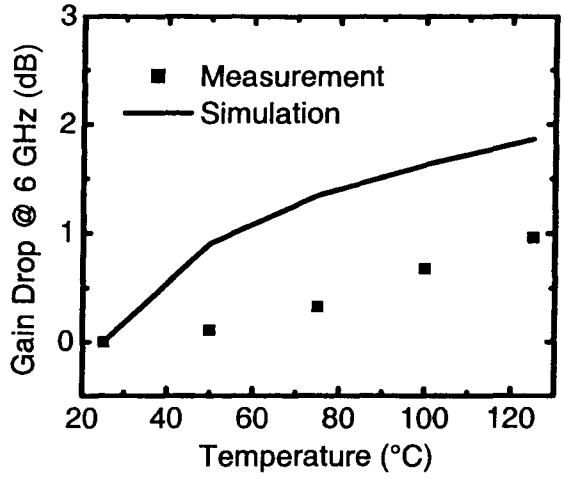

Fig. 5.14. Measured and simulated gain drop at 6 GHz with respect to room temperature.

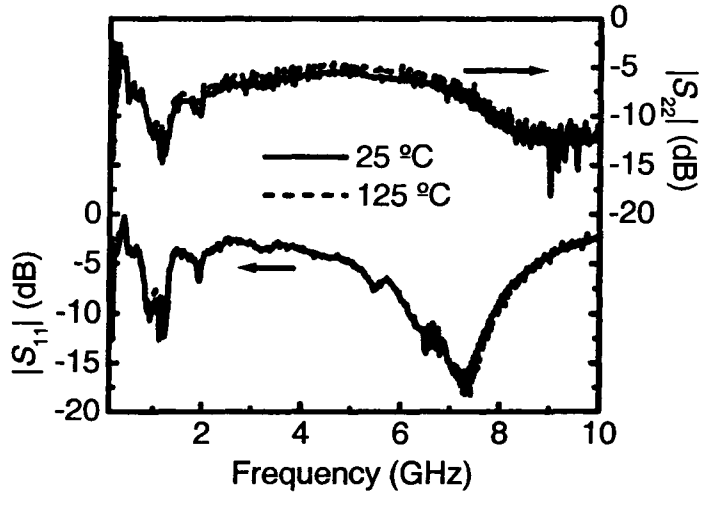

Fig. 5.15. Measured input and output reflection coefficients at two temperatures (low bias condition only).

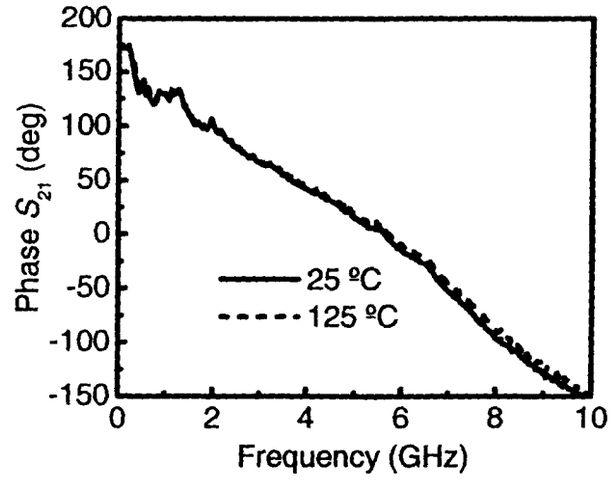

Fig. 5.16. Measured phase of the forward transmission S_{21} at two temperatures (low bias condition only). Phase is shown instead of group delay because the scattering caused by numeric differentiation completely masks any difference between the two curves.

The change of the noise figure with temperature is shown in Fig. 5.17. As expected, the temperature dependence follows a trend similar to the gain but in the opposite direction: it increases slightly at low frequencies, and the increase is more significant at the higher frequencies.

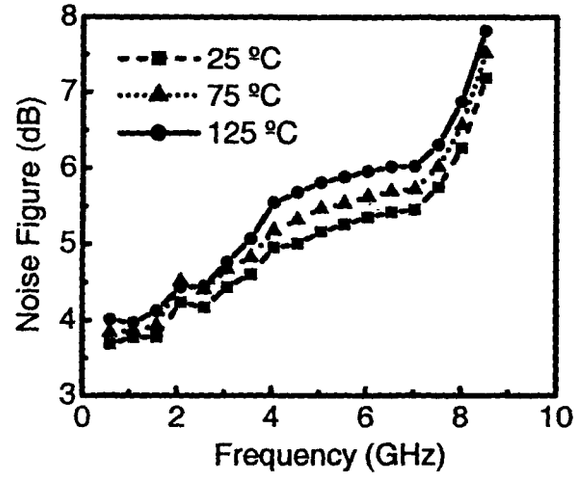

Fig. 5.17. Measured noise figure at three temperatures (low bias condition only).

5.5. SUMMARY

The design of a resistive-match broadband amplifier in CMOS technology was presented. To the best of our knowledge, this is the first implementation of a multi-octave broadband resistive-match amplifier in CMOS technology. The performance of the amplifier at room temperature is summarized in Table 5.2.

Table 5.2. Summary of measured resistive match amplifier performance at room temperature. The values in parentheses correspond to the high biasing condition, with a supply voltage higher than the nominal value for the technology.

Forward Gain	8-5 dB @ 2 GHz – 7 GHz
Bandwidth (0 dB)	8.4 GHz (8.7 GHz)
Input reflection coef. (max.)	-3.5 dB
Output reflection coef. (max.)	-5 dB
Reverse transmission (max.)	-19 dB
Group delay	40-150 ps @ 2 GHz-7 GHz
Noise Figure	4.1 dB – 5.4 dB @ 2 GHz-7 GHz (3.9 dB – 5.1 dB @ 2 GHz-7 GHz)
Power Consumption	18.4 mW with 1.8 V supply (32.4 mW with 3.3 V supply)
Chip Area	1.28 x 0.55 mm^2

When compared to the distributed amplifier, the resistive-match amplifier has a similar gain and a lower noise figure but with half the bandwidth, while consuming less than one fourth of the DC power and chip area. Therefore, if it is not necessary to have the highest possible bandwidth, resistive match amplifiers provide a good alternative for broadband amplification in CMOS technology from very low frequencies (in the MHz

range) up to the gigahertz range, especially in applications where input and output reflections are not critical.

It was also found that the resistive match amplifier is less sensitive to temperature variations than the distributed amplifier, most likely due to the use of fewer passive components and the reduced number of interconnections that result from its compact size.

Chapter 6
Gate Current in High-Frequency CMOS Circuits

6.1. INTRODUCTION

As the dimensions of MOSFETs are reduced to increase the operating speeds, several undesired effects can appear. One such effect is the flow of gate current due to quantum-mechanical tunneling of carriers through the gate oxide. Research on this gate tunneling current (GTC) has focused on its effect on digital circuits and to a lesser extent analog circuits, but its effect on RF circuits has not been studied systematically.

In section 6.2 an introduction to GTC is presented, including modeling of gate current and the physical origin of gate current noise. Compact modeling of gate current noise in MOSFETs is studied in section 6.3, where a model is developed to calculate the effect of the gate current noise on the drain and source currents. In section 6.4 an analysis of the effect of the gate current on the small-signal model and the high-frequency noise parameters of the MOSFET is presented, and some predictions are made regarding the importance of gate current noise as MOS devices are further scaled in the following years.

6.2. GATE CURRENT

6.2.1. Gate current modeling

Modeling of the gate tunneling current is still an active area of research. Most of the GTC models can generally be classified into three categories:

- **Physical models:** In principle, the tunneling current can be calculated from basic quantum mechanics. In general the tunneling current density [74], [75] is given by

$$J_G = \frac{2q}{(2\pi)^3 \hbar} \int_0^{\infty} (f_1 - f_2) \left\{ \int\int P \, dk_y \, dk_z \right\} dE \tag{6.1}$$

where $\hbar$ is Planck's reduced constant, P is the tunneling probability, E is the total electron energy, k_y and k_z are the wave vectors in the plane of the barrier (perpendicular to the tunneling direction), and f_1 and f_2 are the probabilities of occupation of the states on each side of the barrier, given by the Fermi-Dirac distribution functions. Using this to actually calculate the gate current, however, requires either a number of simplifying assumptions that compromise the accuracy, or solving numerically several coupled differential equations (Schrodinger's wave equation, Poisson's equation, etc.). While this is appropriate to achieve insight into the physics of tunneling or for device and process optimization, it is not appropriate for circuit simulation.

- **Semi-empirical models:** Most MOSFET compact models for circuit simulation use a combination of physics-based models and empirical expressions with fitting parameters. An example is the gate current model of the Berkeley Short-channel IGFET Model (BSIM); the expression it uses to model the gate current density [76] is

$$J_G = \frac{q^3}{16\pi^2 \hbar \phi_B} \left(\frac{T_{oxref}}{t_{ox} P} \right)^{ntox} \frac{V_{aux} V_{appl}}{(t_{ox} p)^2} \cdot \exp\left[-\frac{4}{3} \frac{\sqrt{2m_{ox}} \phi_B^{3/2}}{\hbar q} (\alpha - \beta |V_{ox}|)(1 + \gamma |V_{ox}|) t_{ox} P \right] \tag{6.2}$$

where t_{ox} is the oxide thickness, m_{ox} is the electron effective mass in the insulator, ϕ_b is the barrier height at the semiconductor-oxide interface, T_{oxref} is a reference oxide thickness at which the parameters are extracted, $ntox$ is a fitting parameter, V_{appl} is the applied voltage (which has a different meaning depending on the current component), and the function V_{aux} and the parameters α, β, γ and p depend on the tunneling mechanism and the region of operation. While this can model

very accurately the gate current, it requires the calculation or extraction of up to 22 parameters, some of which do not necessarily have a physical meaning.

- **Simple empirical models:** Starting from physical models such as (6.1) and using a number of simplifying assumptions, it is possible to develop analytical models that, while not very accurate, allow to estimate the gate current in terms of the gate voltage and physical constants. One such model [77] is

$$J_G = \frac{q^3}{16\pi^2\hbar\phi_b}\left(\frac{V_G}{t_{ox}}\right)^2 \exp\left\{-\frac{4}{3}\frac{\sqrt{2m_{ox}}\phi_b^{3/2}}{\hbar q}\frac{t_{ox}}{V_G}\left[1-\left(1-\frac{qV_G}{\phi_b}\right)^{3/2}\right]\right\} \tag{6.3}$$

where V_G is the gate voltage.

6.2.2. Gate tunneling current components

In an MOS transistor, several different gate current components can be identified, as shown in Fig. 6.1. When the device operates in inversion, tunneling takes place between the gate and the channel (I_{GC}); current also flows between the gate and the bulk (I_{GB}) both in accumulation and inversion, and in all the operating regions there is tunneling in the overlaps between the gate and the source/drain regions ($I_{GS,ov}$ and $I_{GD,ov}$).

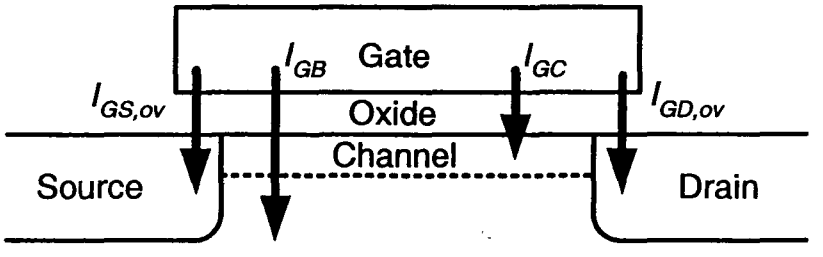

Fig. 6.1. Gate tunneling current components in an MOS transistor.

In the remainder of this thesis, we consider only the gate-channel current, that is, we assume $I_G = I_{GC}$.

6.2.3. Gate tunneling current partition

For MOS transistors, when a voltage is applied between drain and source, the tunneling current density becomes a function of the position x along the channel. The total gate current is then given by:

$$I_G = W \int_0^L J_G(x)\,dx \tag{6.4}$$

where J_G is the gate current density and x is the position along the channel (x=0 for the source and x=L for the drain).

In this case, the question arises as to what portion of the gate-channel current goes to the drain (I_{GD} component) and what portion to the source (I_{GS} component), as shown in Fig. 6.2.

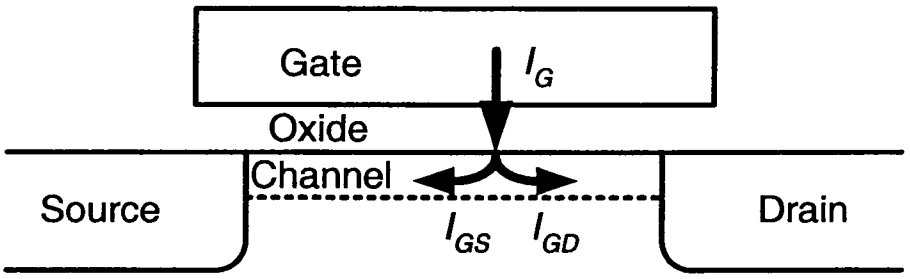

Fig. 6.2. Gate-source and gate-drain components of the gate-channel current.

The partitioning formulas currently used by most compact MOS models [78], [79] are:

$$I_{GS} = W \int_0^L J_G(x)\left(1-\frac{x}{L}\right)dx \tag{6.5}$$

and

$$I_{GD} = W \int_0^L J_G(x)\left(\frac{x}{L}\right) dx. \tag{6.6}$$

The partition ratios I_{GS}/I_G and I_{GD}/I_G, calculated using (6.5) and (6.6), are shown in Fig. 6.3 as a function of the drain-source bias for different gate voltages. For zero drain voltage, the current is equally split between drain and source, and as the drain-source voltage increases, a larger fraction of the current goes to the source terminal.

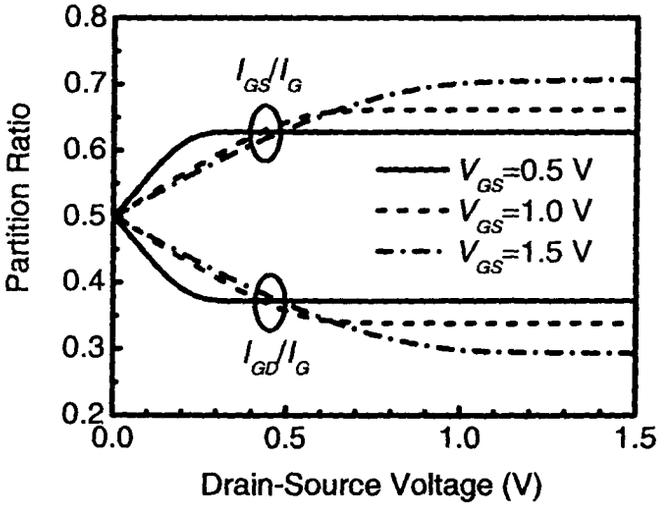

Fig. 6.3. Calculated gate current partition [80].

6.2.4. Gate current noise

Since gate current is caused by carriers randomly crossing a potential barrier, it would be expected to exhibit shot noise, with a PSD given by

$$S_{i_g} = 2qI_G \tag{6.7}$$

where I_G is the total gate current. This has been verified experimentally as shown in Fig. 6.4. The gate current in MOSFETs also shows low-frequency noise with an approximate $1/f$ PSD. Several models have been proposed to explain this noise component, such as

trap-assisted tunneling and barrier height fluctuations [82], [83]. As shown in Fig. 6.5, the gate current flicker noise has been found experimentally to depend approximately on the square of the current [33]:

$$S_{i_g} \propto \frac{I_G^{\,2}}{f}. \tag{6.8}$$

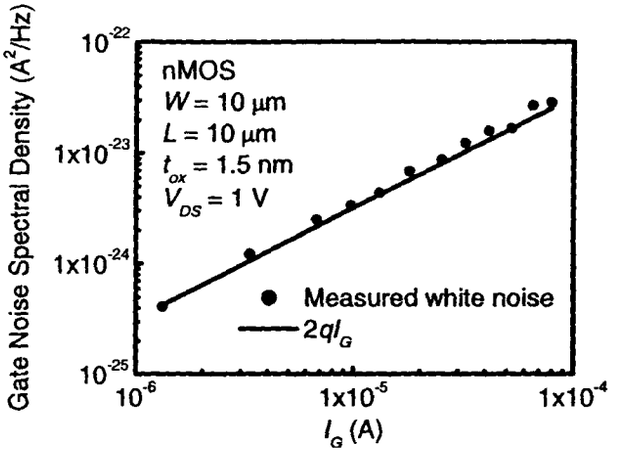

Fig. 6.4. Measured and modeled white noise component of the gate current [81].

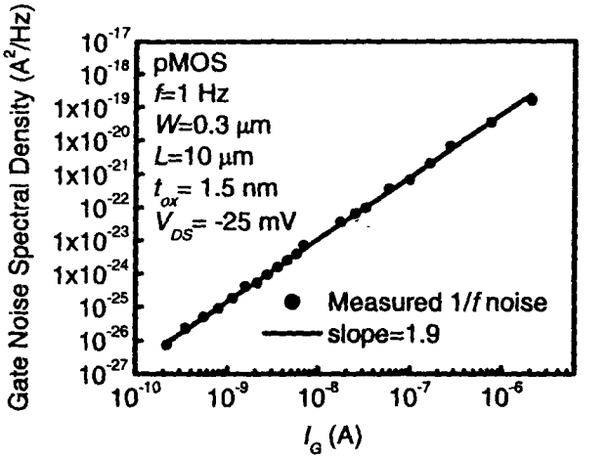

Fig. 6.5. Measured low-frequency noise in the gate current [33].

6.3. COMPACT MODELING OF GATE CURRENT NOISE

The effect of gate current noise on the noise performance of MOSFETs has been studied recently, mostly in terms of measurements and numerical simulations [84], [85], [86]. Compact modeling of the gate current noise for circuit simulation, on the other hand, has received less attention, and while most modern MOSFET models do include gate current [78], [80], [87], its noise is not considered.

In this section, a model is developed that allows for calculating the drain and gate noise PSD due to the gate current. The model, which is suitable for compact simulation, is compared with published results from numerical device simulations and measurements, and it is shown to be valid for both shot noise and flicker noise from the gate current. This was published in [88], and a more detailed derivation is included here.

6.3.1. Gate current noise partition

As discussed before, the noise mechanisms in the gate current of MOSFETs are relatively well understood. A question however remains open: how the gate current noise reflects into the drain and source currents, and how this depends on biasing. As shown in Fig. 6.6(a), the gate current noise can be modeled by many microscopic noise sources located along the channel. For circuit modeling, however, it is more convenient to lump all these microscopic noise sources into macroscopic noise current sources, connected, for example, between the gate and the drain and between the gate and the source, as shown in Fig. 6.6(b). The key question then is what are the spectral densities of these macroscopic noise sources. Also, since the macroscopic noise sources share a common origin, they would be expected to be correlated, and their correlation coefficient is also of interest.

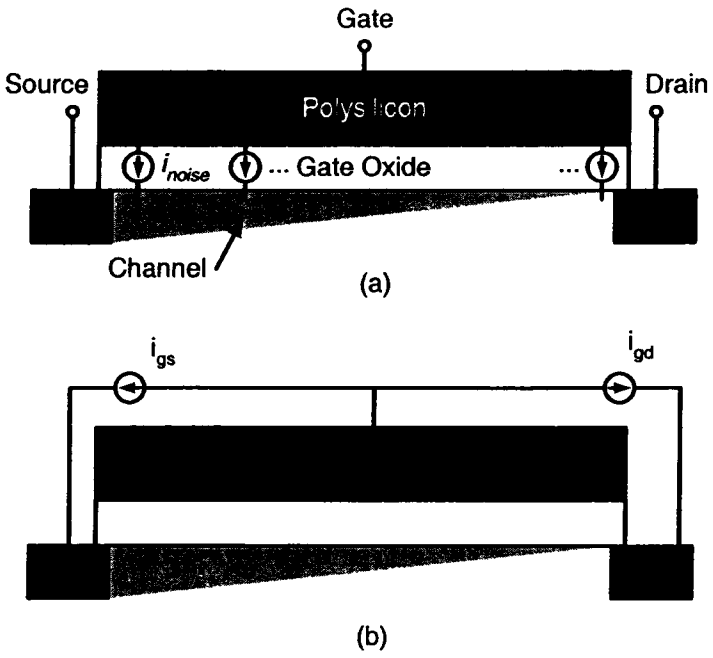

Fig. 6.6. (a) Microscopic gate noise currents. (b) Macroscopic gate-source and gate-drain noise currents.

It was shown in [85], through numerical simulations of Silicon-On-Insulator (SOI) MOSFETs, that the microscopic shot noise sources between the gate and the channel can be represented by two correlated macroscopic shot noise sources between the gate and source and between the drain and source as shown in Fig. 6.7, with spectral densities given by [85]

$$S_{i_{gshot}} = 2qI_G \tag{6.9}$$

and

$$S_{i_{dshot}} = 2q\alpha I_G \tag{6.10}$$

respectively, where the factor α depends on biasing and has typical values between 0.15 and 0.3, and with correlation $C_{shot} = 0.8$. It is not clear in [85] however, how this factor α can be calculated and what is its bias dependence. In the following, we develop a model

for the calculation of the gate and drain noise sources and their correlation, using the DC currents as parameters.

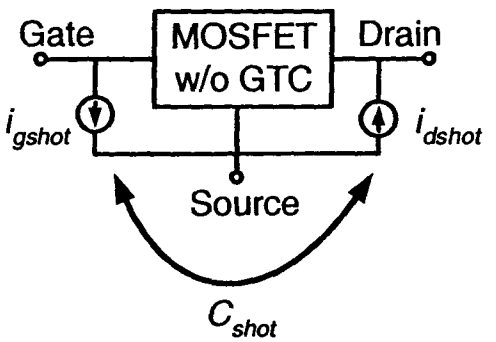

Fig. 6.7. Correlated shot noise currents from the gate current [85].

Consider a fluctuation in the tunneling current δi_g flowing from the gate to the channel between two points x and $x+\Delta x$, as shown in Fig. 6.8.

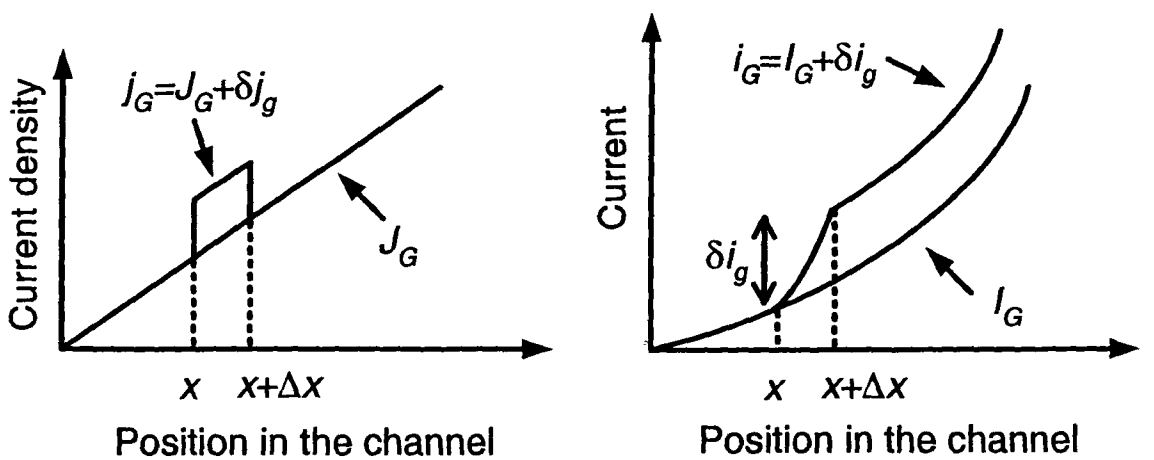

Fig. 6.8. Gate current and gate current density versus position along the channel, showing a fluctuation in the gate current δi_g. Upper case letters with uppercase subscripts are values without fluctutation, lower case letters with lower case subscripts are the noise components and upper case letters with lowercase subscripts are the sum of the two.

It can be shown by solving the current continuity equation in the channel that the corresponding fluctuation in I_{GS} is given by (see Appendix C):

$$\delta i_{gs}(x) = \delta i_g \left(1 - \frac{x}{L}\right) \tag{6.11}$$

in the limit when Δx goes to zero. The spectral density of the I_{GS} noise current is found by integrating the square of this along the channel. If I_G shows full shot noise this results in

$$S_{i_{gs}} = 2qW \int_0^L J_G(x)\left(1 - \frac{x}{L}\right)^2 dx. \tag{6.12}$$

Solving this integral and using (6.6) results in

$$S_{i_{gs}} = 2q\left(I_G - 2I_{GD} + I^*\right) \tag{6.13}$$

where we have defined

$$I^* \equiv W \int_0^L J_G(x)\left(\frac{x}{L}\right)^2 dx. \tag{6.14}$$

To find the noise in I_{GD} we have by definition

$$I_{GD} = I_G - I_{GS} \tag{6.15}$$

then

$$\delta i_{gd}(x) = \delta i_g(x) - \delta i_{gs}(x) = \delta i_g\left(\frac{x}{L}\right) \tag{6.16}$$

and therefore

$$S_{i_{gd}} = 2qI^*. \tag{6.17}$$

Finally, the cross spectral density is found by integrating the product of (6.11) and (6.16):

$$S_{i_{gs},i_{gd}} = 2q\left(I_{GD} - I^*\right) . \tag{6.18}$$

Note that (6.13), (6.17) and (6.18) are valid for any drain voltage. These equations give the spectral densities of the gate-drain and gate-source noise currents (Fig. 6.9(a)); in compact MOSFET modeling, however, it is more common to place the noise sources between the gate and source and the drain and source as shown in Fig. 6.9(b).

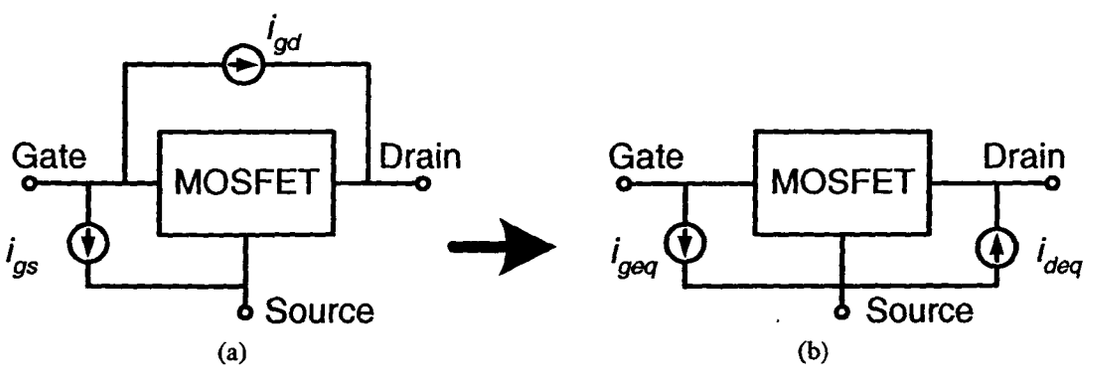

Fig. 6.9. Equivalent gate and drain noise currents. The box represents the MOSFET without gate current noise.

To find the spectral densities of these "equivalent" gate-source and drain-source noise currents as shown in Fig. 6.9(b), we solve Kirchoff's equations in the drain, gate and source nodes of Fig. 6.9:

$$i_{geq} = i_{gs} + i_{gd} \tag{6.19}$$

and

$$i_{deq} = i_{gd} \tag{6.20}$$

The spectral densities are then

$$S_{i_{geq}} = S_{i_{gs}} + S_{i_{gd}} + 2\mathrm{Re}\left\{S_{i_{gs},i_{gd}}\right\}, \tag{6.21}$$

$$S_{i_{deq}} = S_{i_{gd}} \tag{6.22}$$

and

$$S_{i_{geq},i_{deq}} = S_{i_{gs},i_{gd}} + S_{i_{gd}}. \tag{6.23}$$

Substituting (6.13), (6.17) and (6.18) into (6.21), (6.22) and (6.23) we get

$$S_{i_{geq}} = 2qI_G, \tag{6.24}$$

$$S_{i_{deq}} = 2qI^* \tag{6.25}$$

and

$$S_{i_{geq},i_{deq}} = 2qI_{GD}. \tag{6.26}$$

We can see that, except for the term I^* defined in (6.14), the spectral densities of the shot noise currents can be expressed in terms of the macroscopic currents I_{GS}, I_{GD} and I_G. Next we develop an expression for I^* in terms of these three currents.

We begin by assuming a linear variation of the gate current with position. This linearization has been proposed before in the context of compact modeling, and has been justified from numerical simulations [87]. Let $J_G(0)$ and $J_G(L)$ be the gate current densities at the source and drain ends of the channel, respectively. The linearized gate current density is then given by

$$J_G(x) = J_G(0) - \frac{x}{L}[J_G(0) - J_G(L)]. \tag{6.27}$$

Substituting this into (6.5), (6.6) and (6.14), the currents I_{GD} and I_G and the term I^* are given by

$$I_G = WL\left(J_G(0) - \frac{J_G(0) - J_G(L)}{2}\right), \tag{6.28}$$

$$I_{GD} = WL\left(\frac{J_G(0)}{2} - \frac{J_G(0) - J_G(L)}{3}\right) \tag{6.29}$$

and

$$I^* = WL\left(\frac{J_G(0)}{3} - \frac{J_G(0) - J_G(L)}{4}\right). \tag{6.30}$$

From (6.28), (6.29) and (6.30), it can be shown that

$$I^* = \frac{5}{6} I_G - I_{GS}. \tag{6.31}$$

Defining the partition ratio p as

$$p \equiv \frac{I_{GS}}{I_G} \tag{6.32}$$

then the spectral densities of i_{geq} and i_{deq} are given by

$$S_{i_{geq}} = 2qI_G \tag{6.33}$$

and

$$S_{i_{deq}} = \left(\frac{5}{6} - p\right) S_{i_{geq}} \tag{6.34}$$

with cross-spectral density

$$S_{i_{geq}, i_{deq}} = S_{i_{geq}} (1 - p) \tag{6.35}$$

and correlation

$$C_{eq} = \frac{1-p}{\sqrt{5/6 - p}}. \tag{6.36}$$

The expressions (6.33)-(6.36) are suitable for compact modeling because the only required quantities are I_G and p, which are available in most MOSFET compact models [78], [80], [87]. Also note that while we have assumed only shot noise in the gate current, these equations are still valid if there are other noise components present in the gate current, such as flicker noise as will be discussed later, provided that the appropriate expression for S_{igeq} is used in (6.33) and (6.34).

Equations (6.33)-(6.36) only have physically meaningful values when p is in the range 0.21-0.79. It can be shown that if the gate current density depends linearly on the position along the channel, p stays well within that range. Moreover, results from numerical solution of the current continuity equation [79], a channel segmentation model [78] and physical surface-potential based models [78], [80] indicate that p is limited to values within this range even at relatively high gate and drain biases (see Fig. 6.3).

6.3.2. Gate current partition verification

Typical partition ratios are between 0.5 (for V_{DS}=0) and 0.7 (for high gate and drain bias) [78], [80]. The calculated ratio between the equivalent drain and gate shot noise and their correlation for these values of p are shown in Fig. 6.10; also shown are the limit values reported in [85]. Good agreement is found.

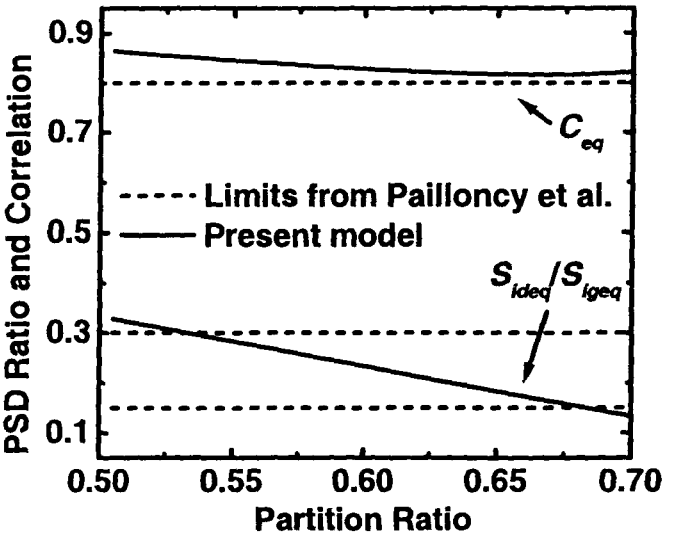

Fig. 6.10. Calculated ratio between the equivalent gate and drain current noise spectral densities and correlation (solid lines) and limit values from [85] (dashed lines).

6.3.3. Gate current and low-frequency noise

We saw above how the shot noise from the gate current results in a correlated drain noise component, and we showed how to calculate the spectral density of this drain noise and the correlation from the biasing conditions. Next, we look at how the expressions also apply to low-frequency noise.

Fig. 6.11 shows the measured low-frequency (LF) drain current noise for a 0.3x10 μm (*W/L*) p-MOSFET with a 1.5 nm gate oxide at low drain bias [33]. The dashed line shows the drain current noise calculated from

$$S_{i_d} = \frac{4kTI_D}{V_{DS}} + \frac{K_D(V_{GS} - V_{TH})V_{DS}}{f}. \tag{6.37}$$

The first term in (6.38) is the thermal noise modeled using (2.25), and the second term is the drain current flicker noise from the mobility fluctuation model (2.35); the constant K_D was extracted from the S_{i_d}-V_{GS} data at low gate bias (see Fig. 6.11 and Table 6.1). As discussed in [33], the bias dependence of the LF drain noise can be also explained using a

carrier number fluctuation model with correlated mobility fluctuations, but we have chosen the $\Delta\mu$ model for convenience here because it requires fewer empirical parameters.

We see in Fig. 6.11 that at high gate biases ($|V_{GS}|>0.5$ V), an increase in the low-frequency drain current noise of thin-oxide MOSFETs is observed beyond what is predicted by traditional low-frequency noise models; this was attributed in [33] to the flicker noise from the gate current, but no quantitative information was presented there to explain the enhanced drain noise. In the following we show that the formulas developed in the previous section can explain this excess noise.

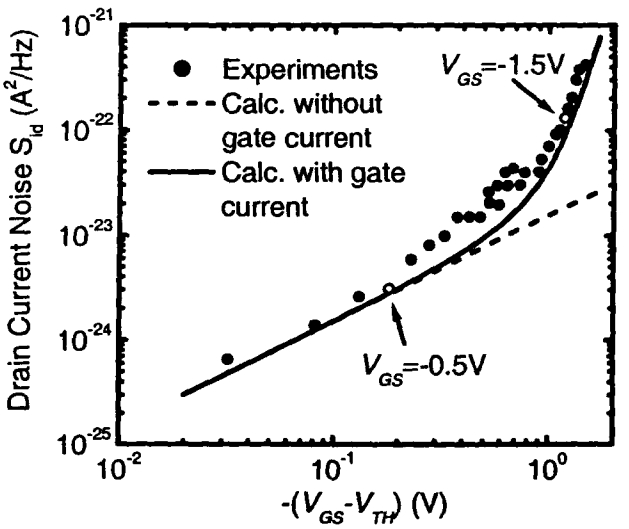

Fig. 6.11. Measured [33] and calculated drain current noise spectral density at f=1Hz for a 0.3 x 10 μm (W/L) p-MOSFET with 1.5 nm oxide at V_{DS}=-25 mV. The solid and dashed lines correspond to calculated noise without and with gate current respectively.

For low drain biases such as the ones used for the experiments in Fig. 6.11, the partition ratio is approximately p=0.5, that is, half of the gate current goes to the drain and half to the source (Fig. 6.3). Then, according to the noise partition formulas (6.33)-(6.34), we must add to (6.37) the noise from the gate current for this value of p, which results in

$$S_{i_d} = 0.33 S_{i_g} + \frac{4kTI_D}{V_{DS}} + \frac{K_D (V_{GS} - V_{TH}) V_{DS}}{f} \tag{6.38}$$

where S_{i_g} is the total gate current noise spectral density. This total gate current noise has two components: shot noise, given by (6.7) and flicker noise, given by (6.8), and it can be calculated as

$$S_{i_g} = 2qI_G + \frac{K_G I_G^{\,2}}{f}. \tag{6.39}$$

The constant K_G was determined from the experimental LF noise data (see Fig. 6.5 and Table 6.1), and the gate current was taken from the DC measurements [33, Fig. 2]. The solid line in Fig. 6.11 shows the drain current noise calculated from (6.38); clearly, the noise from the gate current can account for the excess drain noise at high gate bias.

If the increase of drain noise at high gate bias indeed comes from the gate current noise "propagating" to the drain, we would expect the gate and drain currents to show a high degree of correlation. Fig. 6.12 shows the measured coherence for the same MOSFET discussed before at two different gate voltages, where the coherence is defined as the square of the correlation between the total drain and gate noise currents; indeed, the coherence is significantly higher at high gate biases. Next, we show that this coherence data can be explained quantitatively by the partition equations (6.33)-(6.36).

The coherence between the gate and drain current is given by

$$\Gamma = \frac{S_{i_g, i_d}^2}{\left| S_{i_g} S_{i_d} \right|} \tag{6.40}$$

where S_{i_g,i_d} is the cross spectral density, and the spectral densities S_{i_d} and S_{i_g} are given by (6.38) and (6.39) respectively. Since the drain thermal noise, drain flicker noise and gate flicker noise are all uncorrelated, and making use of (6.35), the coherence is given by

$$\Gamma = (1-p)^2 \frac{S_{i_g}^2}{\left|S_{i_g} S_{i_d}\right|}. \tag{6.41}$$

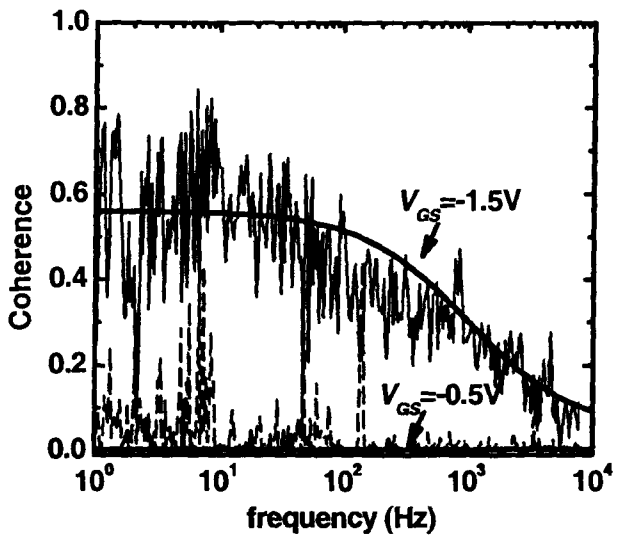

Fig. 6.12. Measured [33] (light lines) and calculated (heavy lines) coherence between the total drain and gate noise for a 0.3 x 10 μm (*W/L*) p-MOSFET with a 1.5 nm oxide for two different gate voltages and V_{DS}=-25 mV.

This equation is plotted in Fig. 6.12 for p=0.5; very good agreement with the experimental data is found.

Table 6.1. Parameters used for the noise calculations of Fig. 6.11 and Fig. 6.12. The values of the constants K_D and K_G were determined from the experimental low-frequency noise (Fig. 6.11 and Fig. 6.5 respectively) and the drain and gate currents from the experimental data of [33].

Parameter	*Value*
K_D	2.4×10^{-20} A^2/V^3
K_G	$K_G=10^{-7}$
I_G	0.6 pA (V_{GS}=-0.5V)
	40 nA (V_{GS}=-1.5V)
I_D	20 nA (V_{GS}=-0.5V)
	0.1 μA (V_{GS}=-1.5V)
V_{TH}	0.3 V

6.4. EFFECT OF GATE CURRENT ON THE HIGH-FREQUENCY PERFORMANCE OF MOSFETS

The purpose of this section is to study how the gate current affects the high-frequency performance of MOSFETs. For this purpose, the small-signal model of the MOSFET is modified to include the effect of gate current, and analytical expressions are derived for the high-frequency noise parameters including gate current.

While some works have been published in this area [84], [85], [86], they either rely on numerical device simulations, which gives little insight into the impact of GTC, or they use very simplified equivalent circuit models that neglect important elements; in particular, the gate resistance can degrade significantly the noise performance of MOSFETs, and it is expected that the gate resistance will not scale as fast as the other elements in the small-signal circuit [11], so any analysis of the effect of gate current in future devices should include the gate resistance.

6.4.1. Small-signal modeling with gate current

A high-frequency small-signal equivalent circuit for the MOSFET in saturation is shown as a two-port network in Fig. 6.13. To simplify the derivations while keeping the most important elements in the equivalent circuit, the drain and source parasitic resistances R_s and R_d, and the substrate network composed of C_{db}, R_{db}, C_{gb} and C_{sb} from the model of Fig. 2.2 are not considered here. An incremental resistor r_T was added to the conventional MOSFET equivalent circuit to model the AC resistance associated with the GTC; its value is given by

$$r_T \equiv \left(\frac{\partial I_{GS}}{\partial V_{GS}} \right)^{-1} \tag{6.42}$$

Note that since r_T is an incremental resistor, it does not generate thermal noise, as does the real resistor R_g. No tunneling resistance is added to the drain side because, as shown in Fig. 6.3, when the device operates in saturation the gate current depends very little on the drain voltage.

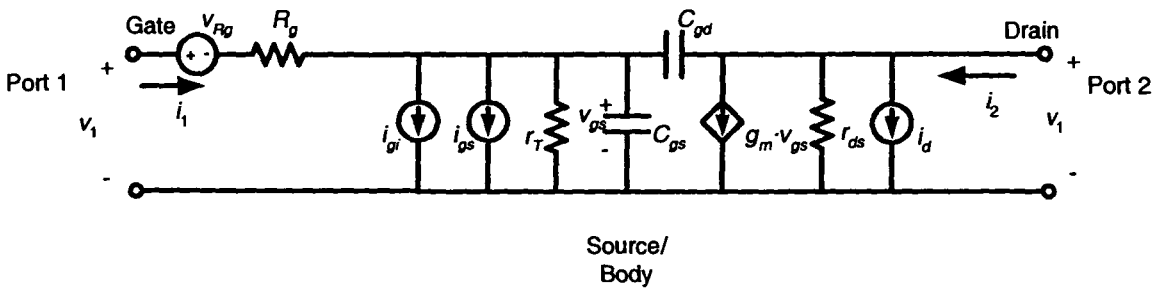

Fig. 6.13. MOSFET high frequency small-signal equivalent circuit with noise sources and gate tunneling.

The noise current source i_d models the channel thermal noise, while the sources i_{gi} and i_{gs} model the induced gate noise and the gate current shot noise respectively; the noise voltage source v_{Rg} models the thermal noise of the gate resistance. Flicker noise of the drain and gate currents is not included in this model.

The Y-parameters of the circuit of Fig. 6.13 are

$$Y_{11} \equiv \left.\frac{i_1}{v_1}\right|_{v_2=0} = \frac{sC_{gg} + 1/r_T}{sR_gC_{gg} + R_g/r_T + 1}, \tag{6.43}$$

$$Y_{21} \equiv \left.\frac{i_2}{v_1}\right|_{v_2=0} = \frac{g_m - sC_{gd}}{sR_gC_{gg} + R_g/r_T + 1}, \tag{6.44}$$

$$Y_{12} \equiv \left.\frac{i_1}{v_2}\right|_{v_1=0} = -\frac{sC_{gd}}{sR_gC_{gg} + R_g/r_T + 1}, \tag{6.45}$$

and

$$Y_{22} \equiv \left.\frac{i_2}{v_2}\right|_{v_1=0} = sC_{gd} + \frac{1}{r_{ds}} + \frac{sR_gC_{gd}\left(g_m - sC_{gd}\right)}{sR_gC_{gg} + R_g/r_T + 1} \tag{6.46}$$

with $s = j\omega$ and $C_{gg}=C_{gs}+C_{gd}$.

The current gain with the output short-circuited is given by

$$\left.\frac{i_2}{i_1}\right|_{v_2=0} = \frac{g_m}{sC_{gg} + 1/r_T} \tag{6.47}$$

and since by definition f_t is the frequency where this is equal to unity this results in

$$f_t = \frac{1}{2\pi}\sqrt{\frac{g_m^2}{C_{gg}^2} - \frac{1}{r_T^2 C_{gg}^2}} \tag{6.48}$$

The first term under the square root corresponds to the square of the unity current gain frequency without gate current

$$f_{to} = \frac{g_m}{2\pi C_{gg}} \tag{6.49}$$

so the unity current gain frequency with gate current can be expressed as

$$f_t = \sqrt{f_{to}^2 - \frac{1}{(2\pi C_{gg} r_T)^2}}. \tag{6.50}$$

6.4.2. Noise parameters and gate current

The main goal of this section is to calculate the four noise parameters (NF_{min}, R_n, G_{opt} and B_{opt}) for the circuit of Fig. 6.13. For this, all the noise sources are first transferred to the input of the network as a series noise voltage and a shunt noise current, as shown in Fig. 6.14. Next, the correlation matrix [89], which is defined in its chain form as

$$C_A = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \equiv \frac{1}{4kT} \begin{bmatrix} S_{v_n} & S_{i_n,v_n} \\ S_{v_n,i_n} & S_{i_n} \end{bmatrix} \tag{6.51}$$

is calculated, where v_n and i_n are the input-referred noise sources shown in Fig. 6.14(b).

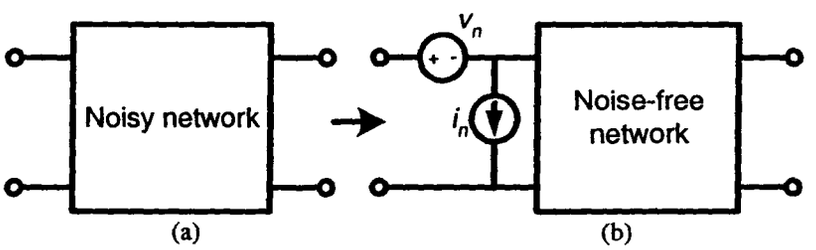

Fig. 6.14. Equivalent noise source transformation (a) Original noisy network (b) Equivalent network with input-referred noise sources.

The four noise parameters are then given by [89]

$$R_n = C_{11}, \tag{6.52}$$

$$G_{opt} = \sqrt{\frac{C_{22}}{C_{11}} - \left(\frac{\mathrm{Im}\{C_{12}\}}{C_{11}}\right)^2}, \tag{6.53}$$

$$B_{opt} = \frac{\mathrm{Im}\{C_{12}\}}{C_{11}} \tag{6.54}$$

and

$$NF_{min} = 1 + 2\left(\mathrm{Re}\{C_{12}\} + C_{11}G_{opt}\right). \tag{6.55}$$

It can be shown that the elements of the correlation matrix for the circuit of Fig. 6.13 are (see Appendix D)

$$\begin{aligned} C_{11} = {} & R_g^2 \frac{S_{i_{gi}}}{4kT} + R_g^2 \frac{S_{i_{gs}}}{4kT} + R_g + \frac{1}{|Y_{21}|^2}\frac{S_{i_d}}{4kT} \\ & - 2R_g \frac{\sqrt{S_{i_{gi}} S_{i_d}}}{4kT} \mathrm{Re}\left\{\frac{C_i}{Y_{21}}\right\} \end{aligned}, \tag{6.56}$$

$$C_{22} = \frac{S_{i_{gi}}}{4kT} + \frac{S_{i_{gs}}}{4kT} + \frac{|Y_{11}|^2}{|Y_{21}|^2}\frac{S_{i_d}}{4kT} - 2\frac{\sqrt{S_{i_{gi}} S_{i_d}}}{4kT} \mathrm{Re}\left\{\frac{Y_{11}}{Y_{21}} C_i\right\}, \tag{6.57}$$

$$\begin{aligned} C_{21} = {} & R_g \frac{S_{i_{gi}}}{4kT} + R_g \frac{S_{i_{gs}}}{4kT} + \frac{Y_{11}}{|Y_{21}|^2}\frac{S_{i_d}}{4kT} - \\ & - R_g \frac{Y_{11}}{Y_{21}} \frac{\sqrt{S_{i_{gi}} S_{i_d}}}{4kT} C_i - \frac{\sqrt{S_{i_{gi}} S_{i_d}}}{4kT} \frac{C_i^*}{Y_{21}^*} \end{aligned}, \tag{6.58}$$

and

$$\begin{aligned} C_{12} = {} & R_g \frac{S_{i_{gi}}}{4kT} + R_g \frac{S_{i_{gs}}}{4kT} + \frac{Y_{11}^*}{|Y_{21}|^2}\frac{S_{i_d}}{4kT} - \\ & - R_g \frac{Y_{11}^*}{Y_{21}^*} \frac{\sqrt{S_{i_{gi}} S_{i_d}}}{4kT} C_i^* - \frac{\sqrt{S_{i_{gi}} S_{i_d}}}{4kT} \frac{C_i}{Y_{21}} \end{aligned} \tag{6.59}$$

where Re{} denotes the real part and Im{} the imaginary part and C_i is the correlation between the drain thermal noise and the induced gate noise.

The four noise parameters can then be calculated using (6.52)-(6.55) and (6.56)-(6.59). The correlation C_i will be neglected in the calculations, since its effect on the noise parameters is typically very small [90].

To gain more insight into the effect of the gate current in the noise parameters, we can perform some simplifications in (6.56)-(6.59) that allow us to obtain explicit expressions for the noise parameters as a function of the small-signal parameters and the gate and drain noise spectral densities. Assuming $R_g << r_T$, $\omega C_{gd} << g_m$ and $\omega R_g C_{gg} << 1$ and neglecting the correlation, the noise parameters are given by

$$R_n \approx R_g + R_g^2 \frac{S_{i_g}}{4kT} + \frac{S_{i_d}}{4kTg_m^2}, \tag{6.60}$$

$$B_{opt} \approx -\left(\frac{f}{f_{to}}\right)\frac{S_{i_d}}{4kTg_m R_n}, \tag{6.61}$$

$$G_{opt} \approx \sqrt{\frac{S_{i_g}}{4kTR_n} + \left[\left(\frac{f}{f_{to}}\right)^2 + \frac{1}{r_T^2 g_m^2}\right]\frac{S_{i_d}}{4kTR_n} - B_{opt}^2} \tag{6.62}$$

and

$$NF_{min} \approx 1 + \frac{R_g S_{i_g}}{2kT} + \left[\left(\frac{f}{f_{to}}\right)^2 + \frac{1}{R_g r_T g_m^2}\right]\frac{R_g S_{i_d}}{2kT} + 2R_n G_{opt} \tag{6.63}$$

where f_{to}, the unity current gain frequency without GTC, is given by (6.49), and $S_{i_g} = S_{i_{gi}} + S_{i_{gs}}$ is the total gate noise spectral density (including both shot noise and induced gate noise). The approximations above should be valid up to moderately high frequencies (around 10 GHz or more for technologies below 0.18 μm), and for practical ranges of tunneling current.

6.4.3. Small-signal model calibration

Before using the model developed above to discuss the effect of tunneling current on the noise performance of MOSFETs, the calculations performed using this model are compared to published experimental data [91], in order to have a better idea of the values of the model parameters in a realistic situation. Several assumptions and approximations will be made; the purpose is not to have a very accurate model, but to have a reasonably realistic small-signal model that can be used later to draw some conclusions regarding the effect of the gate current.

Few experimental data has been reported for MOSFETs with ultra thin oxides, especially noise measurements. In [91], the minimum noise figure NF_{min} and the noise figure with a 50 Ω input impedance (NF_{50}) were reported for a MOSFET with a 1.5 nm SiO_2 insulator and a channel length (drawn) of 130 nm. The maximum transconductance per unit width was also reported. Neither the tunneling current I-V data (I_{GT} vs. V_{GS}) nor the small-signal parameters were reported in [91].

Since the data for the tunneling current was not reported for the devices in [91], a different set of data published by the same group was used [92]; the gate current density and the associated tunneling resistance per unit area from [92] are shown in Fig. 6.15.

The device capacitances were estimated using (2.2)-(2.6). The gate shot noise, drain thermal noise and induced gate noise were calculated using (6.7), (2.26) and (2.30) respectively, and the parameter values shown in Table 6.2 and Table 6.3 were used. The values of γ and δ are based on published data for 0.13 μm transistors without gate current [93], the parameters R_g, g_{do} and ΔL were selected to give a good fit, but within reasonable limits for modern sub-micron devices, and the values of I_G and r_T from Fig. 6.15 for V_{gs}=1.5 V were used.

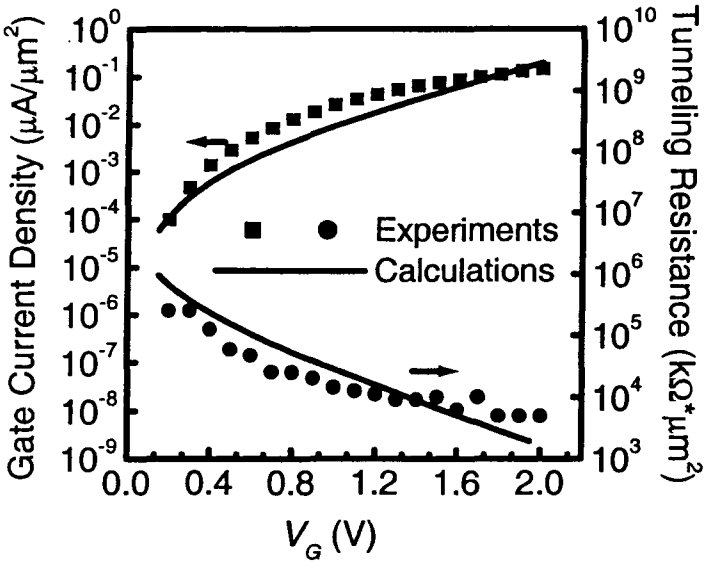

Fig. 6.15. Tunneling current density and associated tunneling resistance per unit area for nMOS capacitors with 1.5 nm oxide thickness [92] (symbols). The lines show the values calculated with the empirical gate current model from (6.3) with ϕ_b=3.1 eV and m_{ox}=0.5m_e, where m_e is the electron mass.

Table 6.2. Parameters provided in [91] for ultra thin-oxide MOSFETs.

t_{ox} (nm)	W (μm)	L (μm)	g_m/W (mS/mm)
1.5	200	0.13	802

Table 6.3. Parameters used for noise calculations not provided in [91].

γ	δ	R_g (Ω)	$\varepsilon_{ox}/\varepsilon_o$	ΔL (nm)	g_{do}	I_{GT} (μA)	r_T (kΩ)
1.3	3.8	15	3.9	50	g_m/0.65	4.4	190

The NF_{min} and NF_{50} calculated using (6.52)-(6.55) and (6.56)-(6.59) are compared to the experimental data from [91] in Fig. 6.16 (both induced gate noise and gate current were included, but their correlation was neglected). Good agreement is observed for NF_{min} and there is reasonable agreement for NF_{50}, except in the range 3-5 GHz where the

experimental data presents an abnormal behavior (sharp increase and then decrease in both NF_{min} and NF_{50}).

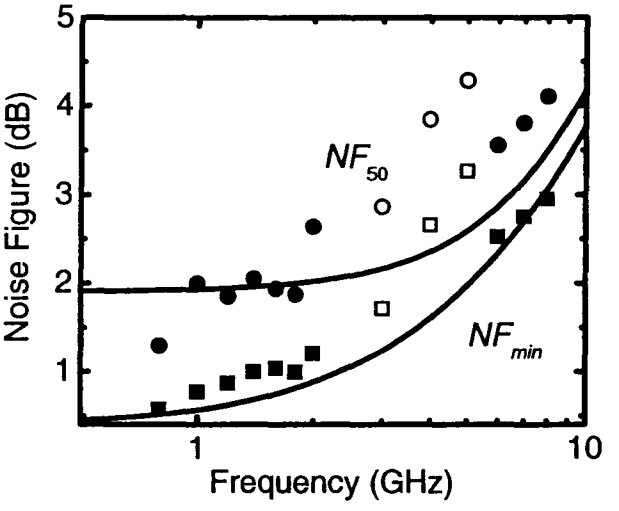

Fig. 6.16. Calculated (solid lines) and measured (symbols) [91] NF_{50} and NF_{min} for a nMOSFET with L_{drawn}=0.13 μm, W=200 μm and t_{ox}=1.5 nm.

6.4.4. Effect of the gate tunneling current on HF performance

Fig. 6.17 shows the calculated noise parameters using equations (6.52)-(6.55) and (6.56)-(6.59) for three different combinations of tunneling current and tunneling resistance: (a) No tunneling current (and infinite tunneling resistance) (b) Values of Table 6.3, and (c) Ten times the tunneling current of Table 6.3. It can be seen that the gate current has a significant effect on the noise parameters G_{opt} and NF_{min} at lower frequencies, while the other noise parameters are mostly unaffected by the gate current.

With the help of (6.60)-(6.63), we can make some conclusions regarding the effect of the tunneling current on the noise parameters, and the effect of further oxide scaling below 1.5 nm. In what follows, we will neglect induced gate noise and assume that all the gate noise in S_{i_g} comes from the gate current. Since the effect of GTC is most important at relatively low frequencies, this is justified for the analysis we want to perform because in that range, the induced gate noise is negligible.

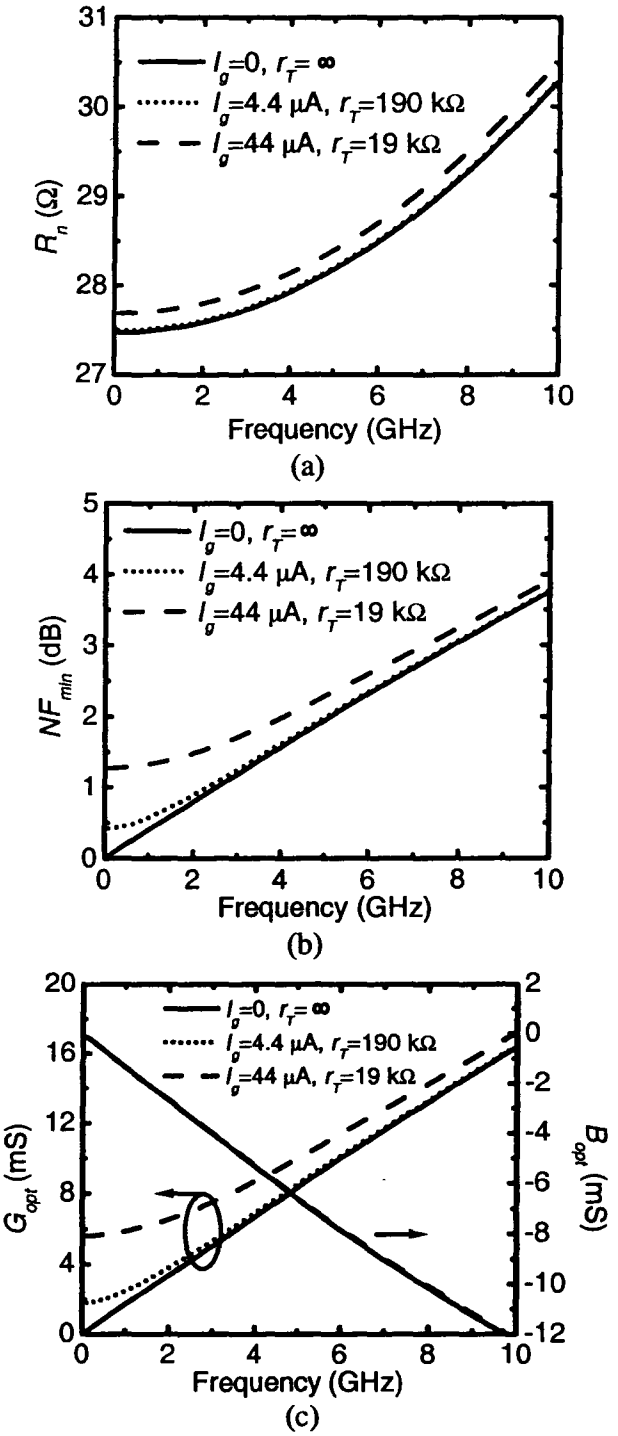

Fig. 6.17. (a) Noise resistance (b) Minimum noise figure and (c) Optimum source conductance and susceptance for different values of tunneling current and tunneling resistance.

From (6.60), the effect of the tunneling current on the noise resistance R_n is relatively small at all frequencies because we have $S_{i_d}/g_m^2 >> R_g^2 S_{i_g}$. To have a rough idea of the implications of this, consider the thermal noise model from (2.26) with γ=1 and g_{do}=g_m and the gate noise model from (6.7). In that case, for the gate current to contribute as much to R_n as the thermal noise would require $I_G \approx 100\text{mV}/R_g^2 g_m$ at room temperature. Assuming very high values of R_g=20 Ω and a g_m of 2 mS per micron width, this would mean that the gate current should be approximately 125 mA per micron width. This clearly indicates that even for aggressive oxide scaling, the effect of the GTC on the noise resistance will be very small.

According to (6.61), the parameter B_{opt} depends on the GTC only through the noise resistance R_n; this explains why B_{opt} is nearly independent of the tunneling current at all frequencies, and as was the case for R_n, this will most likely be the case even with aggressive oxide scaling.

As for G_{opt} and NF_{min}, it is clear from (6.62) and (6.63) why the effect of the GTC is more important at lower frequencies. At high frequencies, the drain thermal noise dominates because it is multiplied by the factor $(f/f_{to})^2$. At lower frequencies, on the other hand, the contribution from S_{i_g} can be much more significant than that of S_{i_d}. If we neglect the terms that depend on r_T in the expressions for G_{opt} and NF_{min}, we can have a simple approximate expression for the frequency f_{ctun} at which the tunneling current contributes as much to NF_{min} and G_{opt} as the drain thermal noise:

$$f_{ctun} \approx f_{to}\sqrt{\frac{S_{ig}}{S_{id}}} \tag{6.64}$$

wehre f_{to} is the f_t without gate current. As shown schematically in Fig. 6.18, at frequencies below f_{ctun}, the noise parameters NF_{min} and G_{opt} are significantly affected by the gate current.

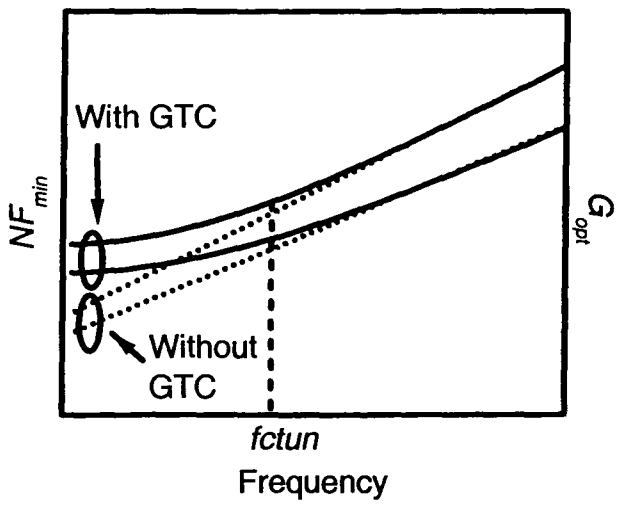

Fig. 6.18. The f_{ctun} frequency. At frequencies below f_{ctun}, the noise from the gate tunneling current affects significantly the noise parameters NF_{min} and G_{opt}.

In order to estimate how f_{ctun} will change with further scaling, the gate noise and drain thermal noise were calculated using the technology projections from the ITRS 2004 for Analog and Mixed Signal (AMS) technologies (Table 6.4) and the analytical models from (6.3), (6.7) and (2.26) for the gate current, gate current noise and drain thermal noise respectively. As shown in Fig. 6.19, the gate current noise increases at a much faster rate than the drain noise with scaling; from (6.64), this means that the f_{ctun} frequency will increase significantly, and as shown in Fig. 6.20, that is indeed the case: the f_{ctun} frequency falls into the gigahertz range even for current technology generations.

Direct verification of this is complicated by the fact that measuring the noise parameters of small geometry MOSFETs is typically very challenging, and the few noise parameter measurements that have been published for current technologies (90 nm) show significant amounts of scattering [86].

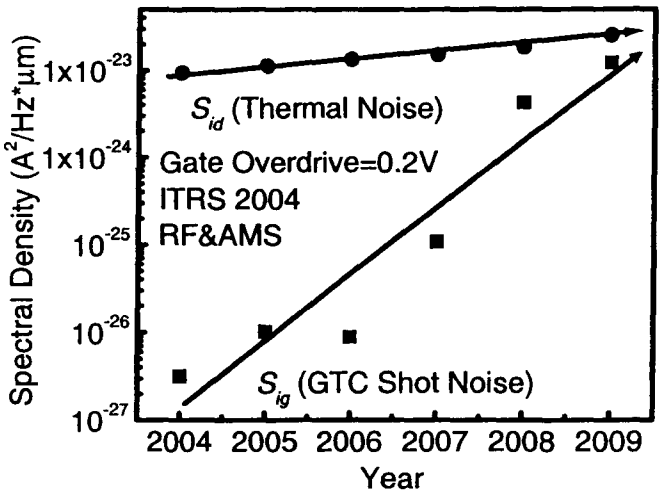

Fig. 6.19. Calculations of the thermal noise and GTC noise from ITRS 2004. A fixed overdrive voltage (gate voltage above threshold) of 200 mV was assumed.

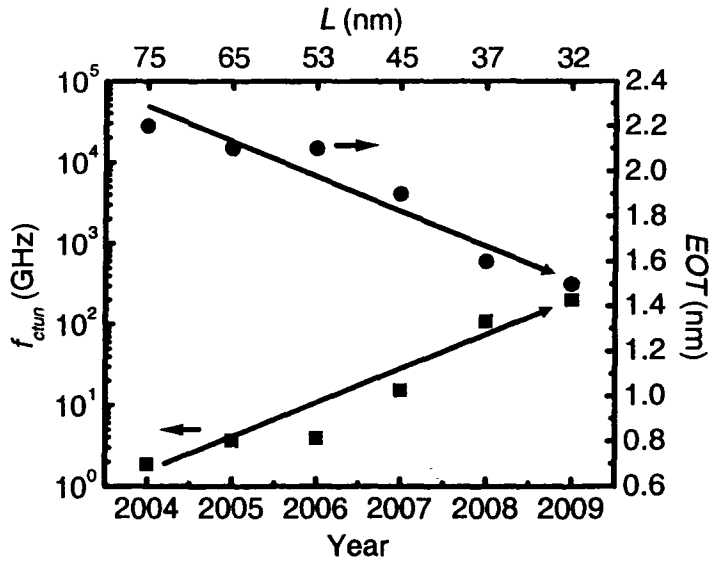

Fig. 6.20. Calculations of the frequency f_{ctun} using the ITRS 2004 projections [14].

To have an idea of the effect of GTC on f_t, it can be shown from (6.50) that, in order to have a reduction of 10% or more on the f_t due to the GTC (that is, for $f_t/f_{to}<0.9$) the condition $r_T<5.3/g_m$ must be satisfied. Assuming a relatively low transconductance of

100 μS per micron width and a W=200 μm device, this would require a tunneling resistance of less than 270 Ω, which is unlikely to be reached even for very thin oxides.

Table 6.4. ITRS 2004 parameters used for the noise calculations of Fig. 6.19 and Fig. 6.20 [14]. The transconductance and drain current were calculated for a fixed gate overdrive of 200 mV using the program available at [14].

Year	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Equivalent oxide thickness (nm)	2.2	2.1	2.1	1.9	1.6	1.5
Effective gate length (nm)	75	65	53	45	37	32
Threshold voltage (V)	0.5	0.5	0.51	0.52	0.5	0.47
Drain current per unit width (μA/μm)	60	70	80	90	110	140
Transconductance per unit width (μS/μm)	517	570	645	726	870	1129
Oxide capacitance per unit width (fF/μm)	0.86	0.77	0.65	0.6	0.56	0.58
Overlap+fringing capacitance per unit width (fF/μm)	0.24	0.24	0.24	0.24	0.24	0.24

6.4.5. Summary

A simple analytical model for the partition of gate shot noise was developed. This model allows calculating the gate-source and drain-source noise currents caused by GTC, and only requires knowing the values of the DC gate current and the partition ratio between source and drain.

It was shown that this partition model can also be extended to the flicker noise from the gate current, and the model explains quantitatively why for MOSFETs with very thin gate oxides, the low-frequency noise increases beyond what is predicted by conventional low-frequency noise theories.

The gate current noise affects mainly the noise parameters G_{opt} and NF_{min}, and its effect on R_n and B_{opt} is very small. A frequency f_{ctun} was defined, below which the GTC has an appreciable effect in G_{opt} and NF_{min}; at frequencies higher than f_{ctun}, the effect of GTC on the noise parameters is relatively small.

For current technologies, the GTC should affect the noise parameters at frequencies below 1-2 GHz. For future technologies, however, this limit moves well into the gigahertz range due to the exponential increase in GTC.

Chapter 7
Conclusions

7.1. SUMMARY

In this thesis, the design of broadband amplifiers in CMOS technology was studied. A distributed amplifier was designed and characterized. It achieves a 5-7 dB gain in the 2 GHz - 13.5 GHz band with input and output reflections lower than -10 dB and -9 dB respectively, while consuming 86 mW from a 1.8 V supply and using 3.4 mm^2 of chip area. It was found that the high-frequency gain of the amplifier drops by approximately 0.37 dB per every 10 °C increase in temperature above room temperature, due to the combined effect of reduced MOSFET transconductance and increased losses in the inductors and interconnections, while the input an output reflections depend very little on temperature.

It was also found that, while gain peaking in distributed amplifiers can be used to compensate for the losses in the artificial lines and achieve a relatively flat gain, this compensation does not work for the group delay and the noise figure, which tend to peak near the cutoff frequency.

A resistive-match amplifier was designed, implemented and characterized. It achieves a 8-5 dB gain in the 2 GHz - 7 GHz band, with input and output reflection coefficients lower than -3.5 and -5 dB respectively and a noise figure of less than 5.4 dB. The DC power consumption is 18.4 mW from a 1.8 V supply and the chip size 0.7 mm^2. This demonstrates the feasibility of using the resistive match technique to achieve low-noise broadband amplification. Improvements to the resistive match amplifier that would extend the lower end of the bandwidth to the megahertz range were discussed.

The effect on the RF performance of MOSFETs of the gate tunneling current cause by gate oxide scaling was also studied in this thesis. A model was developed that allows to calculate the gate and drain noise currents caused by gate tunneling, and it was

shown that the model can be applied both to gate shot noise and gate flicker noise; the model was verified using published experimental results and device simulations. A MOSFET small-signal model including the effect of gate current was also developed, and it was used to evaluate the effect of the gate current noise on the MOSFET noise parameters and unity current gain frequency f_t. It was found that for current technologies, gate current noise affects mainly the minimum noise figure NF_{min} and the optimum source conductance G_{opt} below 1-2 GHz, while the noise resistance R_n and the optimum source susceptance B_{opt} are affected very little by the gate current. A figure of merit f_{ctun} was defined, below which the effect of gate current on the noise parameters is significant, and it was found that, following the ITRS scaling roadmap, the f_{ctun} frequency will move well into the gigahertz range due to the exponential increase of gate current with oxide scaling.

7.2. FUTURE WORK

During the course of this work some areas of further research were identified.

It was found that the use of electromagnetic (EM) simulations to design and simulate microwave circuits has two disadvantages. First, the noise contributed by the resistive losses of the passive elements is not considered by the EM simulations, so the noise in the designed circuits can be significantly underestimated. The ability to obtain noise information from EM simulations would improve the design process of low-noise circuits. While some relatively simple ways to include this into an EM simulator can be envisioned (a thermal noise generator can be added to each point in the simulation mesh), the challenge would be to implement such functionality without significantly increasing the computational cost in terms of time, memory and processor usage.

Second, commercial EM simulators do not include explicitly temperature as a parameter, so in order to accurately predict the temperature dependence of the amplifier characteristics, it would be necessary to repeat the simulation several times by manually changing parameters such as resistivities and electrical permittivities whose temperature dependence must be determined by some means. A major challenge is to find alternate

ways to do this automatically and in a way that does not require so much time and computing power.

Regarding the resistive-match amplifier, an explanation of the temperature dependence of the high-frequency gain is still lacking. This is closely related to the previous point, since the disagreement between measurements and simulations is probably due to the fact that the inductors were designed using single-temperature EM models.

Experimental verification of the effect of gate current effect in the noise parameters of MOSFETs in sub-100 nm technologies is another area of future work. Since measuring directly the noise parameters of small-geometry MOSFETs is very challenging, indirect means of verification probably have to be developed; for example, a Low-Noise Amplifier (LNA) can be designed and fabricated in one such technology and its noise performance measured. Then, with the help of CAD tools, the MOSFET model can be adjusted until the simulated performance matches the measurements.

Another area of improvement is on the models used to study the gate current. The model developed in this thesis for the calculation of the gate and drain noise currents due to tunneling assumed that the tunneling current density varies linearly with position along the channel. While this is a useful first-order approximation that is also used in MOSFET compact models, the implications of a deviation from this linear dependence deserves more detailed consideration.

Also of interest is to consider the effect of the tunneling current between the gate and the drain-source overlaps; in our studies, we neglected this component for simplicity, but in future devices this component will become more and more important as the lateral dimensions are further reduced.

Appendix A

Network Parameter Conversion Formulas

The following formulas are used to convert from S-parameters to Y-parameters [94]:

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_o[(1+S_{11})(1+S_{22})-S_{12}S_{21}]}, \tag{A.1}$$

$$Y_{12} = \frac{-2S_{12}}{Z_o[(1+S_{11})(1+S_{22})-S_{12}S_{21}]}, \tag{A.2}$$

$$Y_{21} = \frac{-2S_{21}}{Z_o[(1+S_{11})(1+S_{22})-S_{12}S_{21}]}, \tag{A.3}$$

and

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{Z_o[(1+S_{11})(1+S_{22})-S_{12}S_{21}]} \tag{A.4}$$

where Z_o is the characteristic impedance used for the S-parameter measurement (typically 50 Ω). To convert from Y-parameters to S-parameters:

$$S_{11} = \frac{(1-y_{11})(1+y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}, \tag{A.5}$$

$$S_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}, \tag{A.6}$$

$$S_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}, \tag{A.7}$$

and

$$S_{22} = \frac{(1+y_{11})(1-y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}} \tag{A.8}$$

where

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = Z_o \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{A.9}$$

are the normalized Y-parameters.

To calculate the transmission line parameters from the S-parameters [95]:

$$Z_c = Z_o \sqrt{\frac{(1+S_{11})-S_{21}^2}{(1-S_{11})^2-S_{21}^2}} \tag{A.10}$$

and

$$\gamma = \alpha + j\beta = \frac{\ln\left[\frac{1-S_{11}^2+S_{21}^2}{2S_{21}^2} \pm \sqrt{\frac{(S_{11}^2-S_{21}^2+1)^2-4S_{11}^2}{4S_{21}^2}}\right]}{l} \tag{A.11}$$

where l is the line length. The signs are selected to give appropriate results for γ (positive α and β).

Appendix B

Planar Transmission Lines

In this appendix equations to calculate the characteristic impedance and the effective dielectric constant of several planar transmission lines are presented.

B.1. COPLANAR WAVEGUIDE [22]

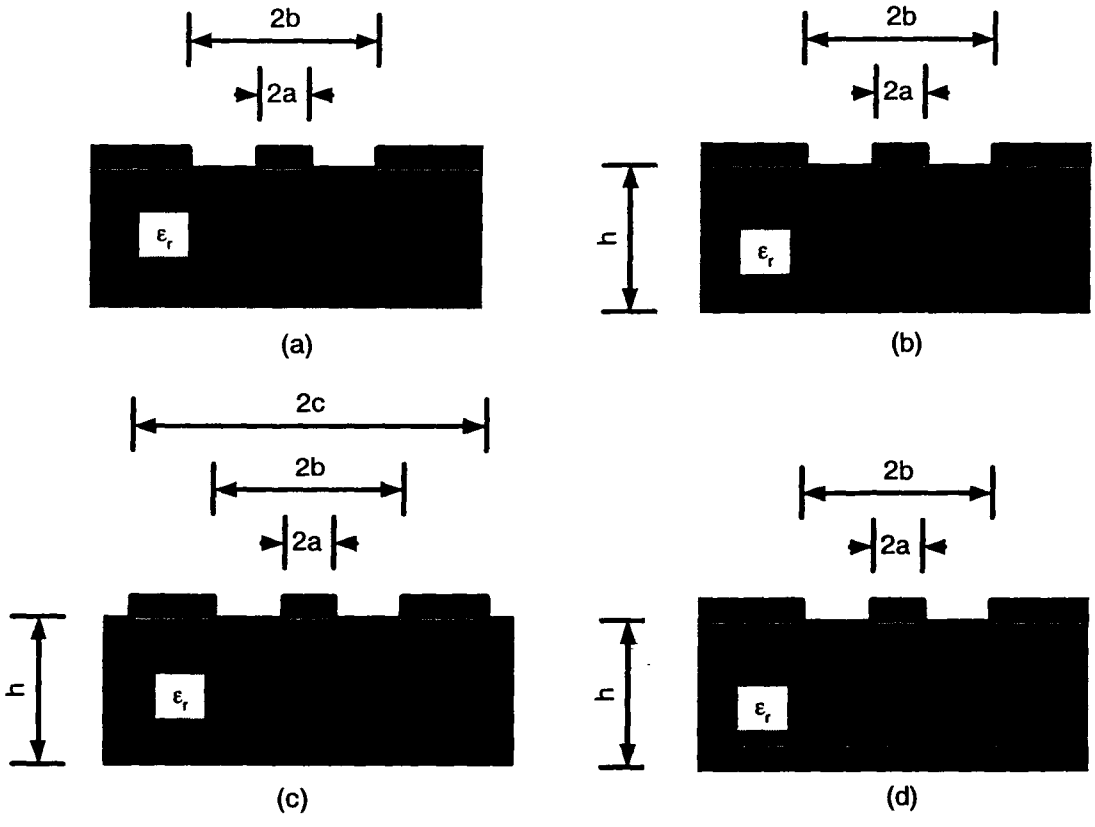

Fig. B.1. Coplanar waveguide cross-sections: (a) Infinite ground planes and infinite dielectric (b) Infinite ground plane and finite dielectric (c) Finite dielectric and ground planes (d) Conductor-backed with infinite ground planes.

B.1.1. Infinite ground planes and infinite dielectric, Fig. B.1(a):

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} \tag{B.1}$$

and

$$Z_c = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K\left(\sqrt{1-k_1^2}\right)}{K(k_1)} \tag{B.2}$$

where

$$k_1 = \frac{a}{b} \tag{B.3}$$

B.1.2. Infinite ground plane and finite dielectric, Fig. B.1(b):

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K\left(\sqrt{1-k_1^2}\right)}{K(k_1)} \frac{K(k_2)}{K\left(\sqrt{1-k_2^2}\right)} \tag{B.4}$$

and

$$Z_c = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K\left(\sqrt{1-k_1^2}\right)}{K(k_1)} \tag{B.5}$$

where

$$k_2 = \frac{\sinh(\pi a/2h)}{\sinh(\pi b/2h)} \tag{B.6}$$

B.1.3. Finite dielectric and finite ground planes, Fig. B.1(c):

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K\left(\sqrt{1-k_3^2}\right)}{K(k_3)} \frac{K(k_4)}{K\left(\sqrt{1-k_4^2}\right)} \tag{B.7}$$

and

$$Z_c = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K\left(\sqrt{1-k_3^2}\right)}{K(k_3)} \tag{B.8}$$

where

$$k_3 = k_1 \sqrt{\frac{1-b^2/c^2}{1-a^2/c^2}} \tag{B.9}$$

and

$$k_4 = k_2 \sqrt{\frac{1-\sinh^2(\pi b/2h)/\sinh^2(\pi c/2h)}{1-\sinh^2(\pi a/2h)/\sinh^2(\pi c/2h)}} \tag{B.10}$$

B.1.4. Conductor-backed, infinite ground planes, Fig. B.1(d):

$$\varepsilon_{re} = 1 + (\varepsilon_r - 1) \frac{K(k_5)/K\left(\sqrt{1-k_5^2}\right)}{K(k_1)/K\left(\sqrt{1-k_1^2}\right) + K(k_5)/K\left(\sqrt{1-k_5^2}\right)} \tag{B.11}$$

and

$$Z_c = \frac{60\pi}{\sqrt{\varepsilon_{re}}} \frac{1}{K(k_1)/K\left(\sqrt{1-k_1^2}\right) + K(k_5)/K\left(\sqrt{1-k_5^2}\right)} \tag{B.12}$$

where

$$k_5 = \frac{\tanh(\pi a/2h)}{\tanh(\pi b/2h)} \tag{B.13}$$

and

$$k_4 = k_2\sqrt{\frac{1-\sinh^2(\pi b/2h)/\sinh^2(\pi c/2h)}{1-\sinh^2(\pi a/2h)/\sinh^2(\pi c/2h)}} \tag{B.14}$$

B.2. COPLANAR STRIPS [22]

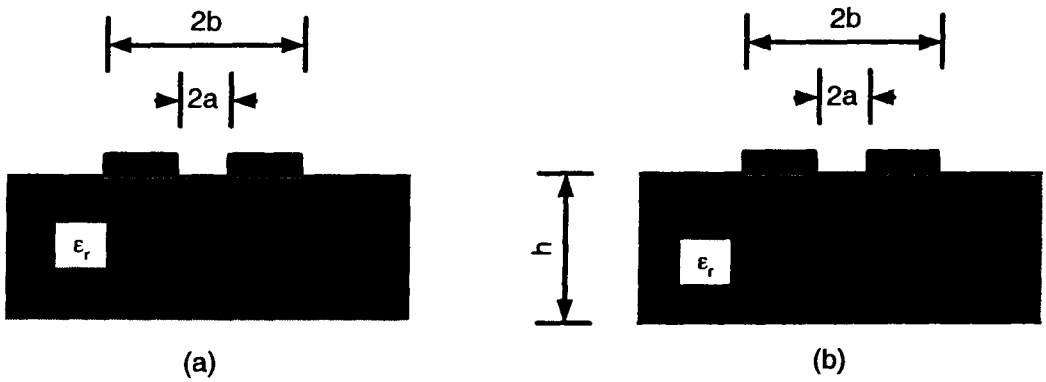

Fig. B.2. Coplanar strip cross-sections: (a) Infinite dielectric (b) Finite dielectric.

B.2.1. Infinite dielectric, Fig. B.2(a)

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} \tag{B.15}$$

and

$$Z_c = \frac{120\pi}{\sqrt{e_{re}}} \frac{K(k_1)}{K\left(\sqrt{1-k_1^2}\right)} \tag{B.16}$$

where

$$k_1 = \frac{a}{b} \tag{B.17}$$

B.2.2. Finite dielectric, Fig. B.2(b)

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K\left(\sqrt{1-k_1^2}\right)}{K(k_1)} \frac{K(k_2)}{K\left(\sqrt{1-k_2^2}\right)} \tag{B.18}$$

and

$$Z_c = \frac{120\pi}{\sqrt{e_{re}}} \frac{K(k_1)}{K\left(\sqrt{1-k_1^2}\right)} \tag{B.19}$$

where

$$k_2 = \frac{\sinh(\pi a/2h)}{\sinh(\pi b/2h)} \tag{B.20}$$

B.3. MICROSTRIP AND STRIP LINE [97]

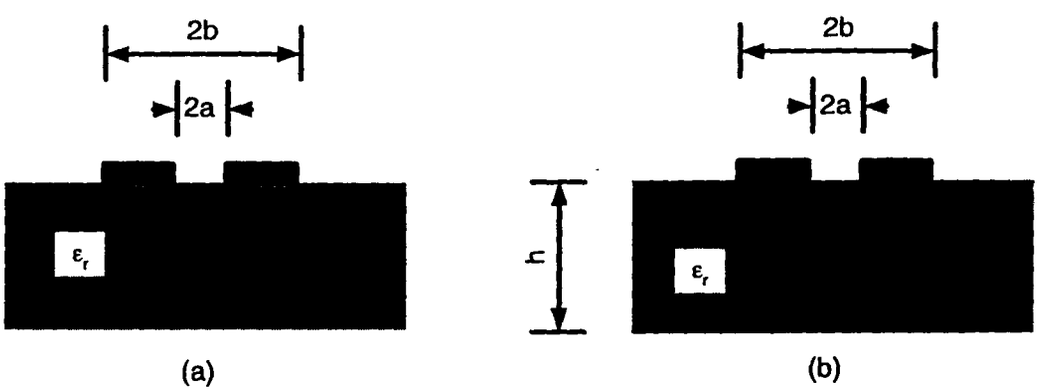

Fig. B.3. (a) Microstrip (b) Strip line.

B.3.1. Microstrip, Fig. B.3(a):

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} F\left(\frac{W}{h}\right) \tag{B.21}$$

and

$$Z_c = \begin{cases} \dfrac{\eta_0}{2\pi\sqrt{\varepsilon_{re}}} \ln\left(\dfrac{8h}{W} + 0.25\dfrac{W}{h}\right) & \dfrac{W}{h} \le 1 \\ \dfrac{\eta_0}{\sqrt{\varepsilon_{re}}}\left[\dfrac{W}{h} + 1.393 + 0.667\ln\left(\dfrac{W}{h} + 1.444\right)\right]^{-1} & \dfrac{W}{h} \ge 1 \end{cases} \tag{B.22}$$

where

$$F\left(\frac{W}{h}\right) = \begin{cases} \left(\sqrt{1+12\dfrac{h}{W}}\right)^{-1} + 0.04\left(1-\dfrac{W}{h}\right)^2 & \dfrac{W}{h} \le 1 \\ \left(\sqrt{1+12\dfrac{h}{W}}\right)^{-1} & \dfrac{W}{h} \ge 1 \end{cases} \tag{B.23}$$

and $\eta_0 = 120\pi\ \Omega$.

B.3.2. Stripline, Fig. B.3(b)

$$\varepsilon_{re} = \varepsilon_r \tag{B.24}$$

and

$$Z_c = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{K\left(\sqrt{1-k_1^2}\right)}{K(k_1)} \tag{B.25}$$

where

$$k_1 = \tanh\left(\frac{\pi W}{2h}\right) \tag{B.26}$$

Appendix C

Derivation of Gate Noise Partition from the Current Continuity Equation

Here we show how to derive (6.11) following an approach similar to that used in [96] to calculate the gate current partition. We start with the equations

$$\frac{\partial i_{DS}}{\partial x} = -W \cdot j_G(x) \tag{C.1}$$

and

$$i_{DS}(x) = g(v)\frac{\partial v}{\partial x}, \tag{C.2}$$

where j_G, i_{DS} and v are the gate current density, drain-source current and quasi-Fermi potential in the channel respectively, all of them including fluctuations caused by δi_g. Without gate current, the corresponding equations are

$$\frac{\partial I_{DS}}{\partial x} = 0 \tag{C.3}$$

and

$$I_{DS}(x) = g(V)\frac{\partial V}{\partial x}, \tag{C.4}$$

where I_{DS} and V are the drain current and channel potential without gate current. Finally, we define I_{DS}' and V' as the "corrections" to I_{DS} and V due to the presence of gate current, and δi_{ds} and δv as the fluctuations in i_{DS} and v caused by δi_g, that is

$$i_{DS}(x) = I_{DS} + I_{DS}'(x) + \delta i_{ds}(x, x_0) \tag{C.5}$$

and

$$v(x) = V(x) + V'(x) + \delta v(x, x_0). \tag{C.6}$$

Solving (C.3) and (C.4), we have

$$I_{DS} = \frac{1}{L} \int_{V_{SB}}^{V_{DB}} g(V) dV, \tag{C.7}$$

and from (C.2), (C.5) and (C.6) we get

$$\int_0^L [I_{DS} + I_{DS}'(x) + \delta i_{ds}(x, x_0)] dx = \int_{V_{SB}}^{V_{DB}} g[v(x)] d[v(x)]. \tag{C.8}$$

Substituting (C.7) in (C.8) and assuming that the change of the channel conductance caused by the gate current is small, we get

$$\int_{V_{SB}}^{V_{DB}} g[v(x)] d[v(x)] \approx \int_{V_{SB}}^{V_{DB}} g(V) dV = I_{DS} L. \tag{C.9}$$

Thus

$$\int_0^L [I_{DS}'(x) + \delta i_{ds}(x, x_0)] dx = 0 \tag{C.10}$$

Substituting (C.5) into (C.1) and remembering that I_{DS} does not depend on x, gives

$$\frac{\partial I_{DS}' + \delta i_{ds}}{\partial x} = -W \cdot j_G(x). \tag{C.11}$$

Integrating this equation from 0 to x results in

$$[I_{DS}'(x)+\delta i_{ds}(x,x_0)]-[I_{DS}'(0)+\delta i_{ds}(0,x_0)]=-W\int_0^x j_G(t)dt\,, \tag{C.12}$$

where t is a dummy variable. Integrating again from x=0 to x=L we get

$$\begin{aligned}&\int_0^L I_{DS}'(x)dx+\int_0^L \delta i_{ds}(x,x_0)dx-\int_0^L I_{DS}'(0)dx-\int_0^L \delta i_{ds}(0,x_0)dx=\\&=-W\int_0^L\left[\int_0^x j_G(t)dt\right]dx\end{aligned} \tag{C.13}$$

Taking advantage of (C.10) and noting that by definition,

$$I_{DS}'(0)=I_{GS} \tag{C.14}$$

and

$$\delta i_{ds}(0,x_0)=\delta i_{gs}(x_0), \tag{C.15}$$

we have

$$I_{GS}+\delta i_{gs}(x_0)=\frac{W}{L}\int_0^L\left[\int_0^x j_G(t)\,dt\right]dx. \tag{C.16}$$

From the definition of current density, we have

$$\int_0^x j_G(t)\,dt=\frac{i_G(x,x_0)}{W}. \tag{C.17}$$

Then

$$I_{GS}+\delta i_{gs}(x_0)=\frac{1}{L}\int_0^L i_G(x,x_0)\,dx\,, \tag{C.18}$$

since

$$i_G(x,x_0) \equiv \begin{cases} I_G(x) & x < x_0 \\ \delta i_g + I_G & x > x_0 + \Delta x \end{cases}, \tag{C.19}$$

(see Fig. 6.8). Then, in the limit when Δx goes to zero, we get

$$I_{GS} + \delta i_{gs}(x_0) = \frac{W}{L}\int_0^L \left[\int_0^x J_G(t)\,dt\right] dx + \frac{1}{L}\int_{x_0+\Delta x}^{L} \delta i_g(x,x_0)\,dx. \tag{C.20}$$

It is easily shown using integration by parts that the first term in the right-hand side of (C.20) is just the gate-source current I_{GS} given by (6.5). Therefore, we finally get

$$\delta i_{gs}(x_0) = \frac{1}{L}\int_{x_0+\Delta x}^{L} \delta i_g(x,x_0)\,dx \tag{C.21}$$

Solving this integral results in (6.11) in the limit when Δx goes to zero. We have substituted x_0 with x in (6.11).

Appendix D

Noise Parameter Calculation

For the calculation of the parameters of the correlation matrix, the noise sources i_{gi}, i_{gn} and v_{Rg} must be reflected back to the input as a series noise voltage and shunt noise current. Since we have characterized the network in terms of Y-parameters, a convenient intermediate step is to convert the internal noise sources to two current sources at the input and output, and then reflect these to the input, as shown in Fig. D.1.

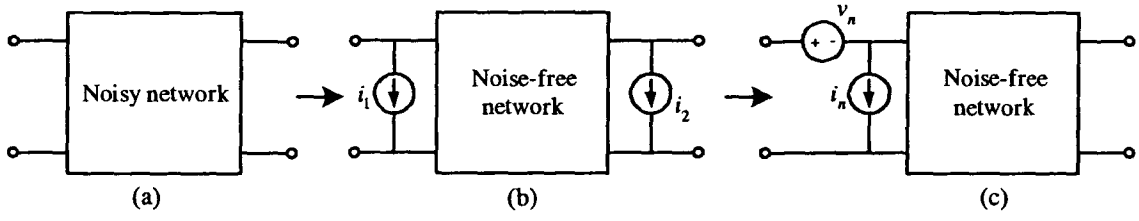

Fig. D.1. Equivalent noise source transformation: (a) Original network with internal noise sources (b) Equivalent circuit with input and output noise currents (c) Equivalent circuit with input noise current and voltage.

In this case, the input noise currents i_1 and i_2, defined as the noise current at ports 1 and 2 when both are short-circuited as shown in Fig. D.2, are given by

$$i_1 = -\frac{i_{gi}+i_{gs}}{sR_g\left(C_{gs}+C_{gd}\right)+R_g/r_T+1}+\frac{v_{R_g}}{R_g}\left(\frac{1}{sR_g\left(C_{gs}+C_{gd}\right)+R_g/r_T+1}-1\right) \qquad \text{(D.1)}$$

and

$$i_2 = -\frac{R_g\left(g_m-sC_{gd}\right)\left(i_{gi}+i_{gs}\right)}{sR_g\left(C_{gs}+C_{gd}\right)+R_g/r_T+1}-\frac{\left(g_m-sC_{gd}\right)v_{R_g}}{sR_g\left(C_{gs}+C_{gd}\right)+R_g/r_T+1}+i_d \qquad \text{(D.2)}$$

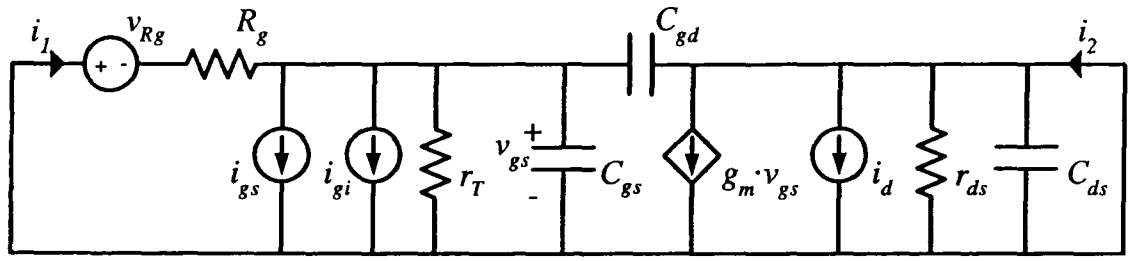

Fig. D.2. Circuit for calculation of input and output noise currents.

The input noise voltage and current will thus be:

$$v_n \equiv -\frac{1}{Y_{21}} i_2 = R_g i_{gi} + R_g i_{gs} + v_{R_g} - \frac{i_d}{Y_{21}} \tag{D.3}$$

and

$$i_n \equiv i_1 - \frac{Y_{11}}{Y_{21}} i_2 = i_{gi} + i_{gs} - \frac{Y_{11}}{Y_{21}} i_d \tag{D.4}$$

Then the self and cross PSD of the input current and voltage are given by

$$S_{v_n} = R_g{}^2 S_{i_{gi}} + R_g{}^2 S_{i_{gs}} + S_{v_{Rg}} + \frac{S_{i_d}}{|Y_{21}|^2} - 2R_g \sqrt{S_{i_{gi}} S_{i_d}}\, \mathrm{Re}\left\{\frac{C_i}{Y_{21}}\right\}, \tag{D.5}$$

$$S_{i_n} = S_{i_{gi}} + S_{i_{gs}} + \frac{|Y_{11}|^2}{|Y_{21}|^2} S_{i_d} - 2\sqrt{S_{i_{gi}} S_{i_d}}\, \mathrm{Re}\left\{\frac{Y_{11}}{Y_{21}} C_i\right\}, \tag{D.6}$$

and

$$S_{v_n,i_n} = R_g S_{i_{gi}} + R_g S_{i_{gs}} + \frac{Y_{11}}{|Y_{21}|^2} S_{i_d} - \frac{Y_{11}}{Y_{21}} R_g \sqrt{S_{i_{gi}} S_{i_d}}\, C_i - \frac{\sqrt{S_{i_{gi}} S_{i_d}}}{Y_{21}^*} C_i^* \tag{D.7}$$

where C_i is the correlation coefficient between the induced gate noise and the drain thermal noise. The correlation between i_d and i_{gs} and between i_{gi} and i_{gs} are both zero, as they have different physical origins.

Using the definition of the correlation matrix parameters in (6.51), this results in (6.56)-(6.59).

References

[1] J. S. Kilby, "The integrated circuit's early history", *Proc. IEEE*, vol. 88, no. 1, pp. 109-111, Jan. 2000.

[2] R. A. Pucel, "Design considerations for monolithic microwave circuits", *IEEE Trans. Microwave Theory Tech.*, vol. 29, no. 6, pp. 513-534, June 1981.

[3] C. H. Diaz, D. D. Tang and J. Sun, "CMOS technology for MS/RF SoC", *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 557-566, Mar 2003.

[4] B. Razavi, "Prospects of CMOS technology for high-speed optical communication circuits", *IEEE J. Solid-State Circuits*, vol. 37, no. 9, Sept. 2002.

[5] A. A. Abidi, "RF CMOS comes of age", *2003 Symp. VLSI Circuits Dig. Tech. Papers*, pp. 113-116, June 2003.

[6] J. D. Cressler, "SiGe HBT technology: A new contender for Si-based RF and microwave circuit applications", *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 5, pp. 572-589, May 1998.

[7] J. Newey, "The changing shape of the RF microelectronics landscape", *Compound Semiconductor Magazine*, vol. 9, no. 6, pp. 2-3, Jun. 2003.

[8] F. M. Wanlass and C. T. Sah, "Nanowatt logic using field effect metal oxide semiconductor triodes", *1963 IEEE ISSC Dig. Tech. Papers*, vol. VI, pp. 32-33, Feb. 1963.

[9] C. H. Chen and M. J. Deen, "High frequency noise of MOSFETs I - Modeling", *Solid-State Electronics*, vol. 42, no. 11, pp. 2069 - 2081, Nov. 1998.

[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge University Press, 1998.

[11] A. Litwin, "Overlooked interfacial silicide-polysilicon gate resistance in MOS transistors", *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2179-2181, Sept. 2001.

[12] Y. Ma, D. R. Evans, T. Nguyen, Y. Ono, and S. T. Hsu, "Fabrication and characterization of sub-quarter-micron MOSFET's with a copper gate electrode", *IEEE Electron Device Lett.*, vol. 20, pp. 254-255, May 1999.

[13] H.-C. Lin, R. Lin, W.-F. Wu, R.-P. Yang, M.-S. Tsai, T.-S. Chao and T.-Y. Huang, "A novel self-aligned T-shaped gate process for deep submicron Si MOSFET's fabrication", *IEEE Electron Device Lett.*, vol. 19, no. 1, pp. 26 - 28, Jan. 1998.

[14] *International Technology Roadmap for Semiconductors, 2004 Update*, available at: http://public.itrs.net.

[15] B. Kleveland, C. H. Diaz, D. Vook, L. Madden, T. H. Lee and S. S. Wong, "Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design", *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1480-1488, Oct. 2001.

[16] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon", *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560 - 568, Mar. 2000.

[17] J. Y. -C. Chang, A.A. Abidi and M. Gaitan, "Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier", *IEEE Electron Device Lett.*, vol. 14, no. 5, pp. 246–248, May 1993.

[18] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, S. C. Pai, C. C. Chi and C. P. Liao, "RF loss and cross talk on extremely high resistivity (10K-1MΩ-cm) Si fabricated by ion implantation", *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 221-224, June 2000.

[19] A.C. Reyes, S. M. El-Ghazaly, S. Dorn, M. Dydyk, and D. K. Schroder, "Silicon as a microwave substrate", *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1759-1762, vol. 3, May 1994.

[20] C. P. Yue, and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's", *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743-752, May 1998.

[21] L. F. Tiemeijer, R. J. Havens, N. Pavlovic, and D. M. W. Leenaerts, "Record Q symmetrical inductors for 10-GHz LC-VCOs in 0.18-μm gate-length CMOS", *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 713-715, Dec. 2002.

[22] K. C. Gupta, R. Garg and I. J. Bahl, *Microstrip Lines and Slotlines*, Second edition. Boston, MA: Artech House, 1996.

[23] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, Second edition. Boston, MA: McGraw-Hill, 1999.

[24] S. M. Nam, B. J. Lee, S. H. Hong, C. G. Yu, J. T. Park and H. K. Yu, "Experimental investigation of temperature dependent RF performance of RF-CMOS devices", *Proc. 6th Int. Conf. on VLSI and CAD*, pp. 174-177, Oct. 1999.

[25] R. Groves, D. L. Harame and D. Jadus, "Temperature dependence of Q and inductance in spiral inductors fabricated in a Silicon-Germanium/BiCMOS technology", *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1455-1459, Sept. 1997.

[26] J. L. Shi , K. Kang , T. S. Yeo, B. Gu, H. Liao, Y. Z. Xiong and S. C. Rustagi, "Temperature effects on the performance of on-chip spiral inductors used in RF(MM)ICs", *Int. J. Infrared and Millimeter Waves*, vol. 25, no 10, pp. 1511-1522, Oct. 2004.

[27] Y. -S. Lin, "Temperature and substrate-impedance dependence of noise figure of monolithic RF inductors on silicon", *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 397-400, June 2005.

[28] A. Van der Ziel, *Noise*. New York, NY: Prentice-Hall, 1954.

[29] S. Asgaran, M. J. Deen and C. H. Chen, "Analytical modeling of MOSFETs channel noise and noise parameters", *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2109-2114, Dec. 2004.

[30] Y. Cheng, M. J. Deen, and C.H. Chen, "MOSFET modeling for RF IC design", *IEEE Trans. Electron Devices*, accepted for publication, 2005.

[31] C. H. Chen, M. J. Deen, Y. Cheng and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements", *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2884 - 2892, Dec. 2001.

[32] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators", *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179-194, Feb. 1998.

[33] M. Valenza, A. Hoffmann, D. Sodini, A. Laigle, F. Martinez and D. Rigaud, "Overview of the impact of downscaling technology on 1/f noise in p-MOSFETs to 90 nm", *IEE Proc. G - Circuits, Devices and Systems*, vol. 151, no. 2, pp. 102-110, April 2004.

[34] J. Chang, A. Abidi and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures", *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1965-1971, Nov. 1994.

[35] R. Jayaraman and C. G. Sodini, "A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon", *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1773-1782, Sept. 1990.

[36] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors", *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654-665, Mar. 1990.

[37] H. Rothe and W. Dahlke, "Theory of noisy fourpoles", *Proc. IRE*, vol. 44, pp. 811-818, 1956.

[38] *IEEE Standard 802.11a-1999, Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: High-speed Physical Layer in the 5 GHZ Band*, The Institute of Electrical and Electronics Engineers, 1999.

[39] *Code of Federal Regulation CFR 47, Part 15 - Radio Frequency Devices*, U.S. Federal Communications Commission, Jan. 2005.

[40] Z. Lao, M. Lang, V. Hurm, Z. Wang, A. Thiede, M. Schlechtweg, W. Bronner, G. Kaufel, K. Köhler, A. Hülsmann, B. Raynor and T. Jakobus, "20-40 Gbit/s GaAs-HEMT Chip Set for optical data receiver", *Int. J. High Speed Electronics and Syst.*, vol. 9, no. 2, pp. 437-472, 1998.

[41] W. S. Percival, *Improvements in and relating to thermionic valve circuits*, British Patent 460562, Jan. 1937.

[42] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg and J. D. Noe, "Distributed amplification", *Proc. IRE*, vol. 36, pp. 956-969, Aug. 1948.

[43] W. H. Horton, J. H. Jasberg and. J. D. Noe, "Distributed amplifiers: practical considerations and experimental results", *Proc. IRE*, vol. 38, pp. 748-753, July 1950.

[44] W. Jutzi, "A MESFET distributed amplifier with 2-GHz bandwidth", *Proc. IEEE*, pp. 1195-1196, June 1969.

[45] F. Schar, "Distributed amplifiers using microstrip", *Int. J. Electron.*, vol. 34, no. 6, pp. 721-730, 1973.

[46] F. Meyer, "Wide-band pulse amplifier", *IEEE J. Solid-State Circuits*, vol. SC-13, no. 3, pp. 409-411, June 1978.

[47] Y. Ayasli, J. L. Vorhaus, R. Mozzi and L. Reynolds, "Monolithic GaAs traveling-wave amplifier", *Electron. Lett.*, vol. 17, no. 12, pp. 413-414, June 1981.

[48] S. Masuda, T. Takahashi and K. Joshin, "An over-110-GHz InP HEMT flip-chip distributed baseband amplifier with inverted microstrip line structure for optical transmission system", *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1479-1484, Sept. 2003.

[49] M. Jamal Deen, J. C. Ranuárez and Y. K. Ramadass, "Distributed and traveling-wave amplifiers in CMOS technology", *2004 Asia-Pacific Microwave Conference (APMC04)*, Dec. 2004.

[50] J. C. Ranuárez, Y. K. Ramadass and M. Jamal Deen, "CMOS Distributed Amplifiers", *Proc. 5th International Caracas Conference in Devices, Circuits and Systems (ICCDCS04)*, pp. 29-36, Nov. 2004.

[51] J. Aguirre and C. Plett, "A 0.1 - 50 GHz SiGe HBT distributed amplifier employing constant-k m-derived sections", *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 923-926, June 2003.

[52] P. J. Sullivan, B. A. Xavier and W. H. Ku, "An integrated CMOS distributed amplifier utilizing packaging inductance", *IEEE Trans. Microwave Theory Tech.*, vol. 45, no. 10, pp. 1969-1976, Oct. 1997.

[53] B. Kleveland, C. H. Diaz, D. Vock, L. Madden, T. H. Lee and S. S. Wong, "Monolithic CMOS distributed amplifier and oscillator", *1999 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 70-71, Feb. 1999.

[54] B. M. Ballweber, R. Gupta and D. J. Allstot, "A fully integrated 0.5-5.5 GHz CMOS distributed amplifier", *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 231-239, Feb. 2000.

[55] H. -T. Ahn and D. J. Allstot, "A 0.5-8.5 GHz fully differential CMOS distributed amplifier", *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 985-993, August 2002.

[56] B. M. Frank, A. P. Freundorfer and Y. M. M. Antar, "Performance of 1-10-GHz traveling wave amplifiers in 0.18-μm CMOS", *IEEE Microwave Wireless Comp. Lett.*, vol. 12, no. 9, pp. 327-329, Sept. 2002.

[57] R. -C. Liu, C. -S. Lin, K. -L. Deng and H. Wang, "A 0.5-14-GHz 10.6-dB CMOS cascode distributed amplifier", *2003 Symp. VLSI Circuits Dig. Tech. Papers*, pp. 139-140, June 2003.

[58] R. -C. Liu, K. -L. Deng and H. Wang, "A 0.6-22-GHz broadband CMOS distributed amplifier", *2003 IEEE RFIC Symp. Dig.*, pp. 103-106, June 2003.

[59] R. Amaya and C. Plett, "Design of high gain fully-integrated distributed amplifiers in 0.35 μm CMOS", *Proc. 29th European Solid-State Circuits Conf.*, pp. 145-148, Sept. 2003.

[60] K. Bhattacharyya and M. J. Deen, "Microwave CMOS traveling wave amplifiers: performance and temperature effects", *IEEE Microwave Wireless Comp. Lett.*, vol. 14, no. 1, pp. 16 - 18, Jan. 2004.

[61] R. E. Amaya, N. G. Tarr and C. Plett, "A 27 GHz fully integrated CMOS distributed amplifier using coplanar waveguides", *2004 IEEE RFIC Symp. Dig.*, pp. 193-196, June 2004.

[62] C. Grewing, K. Winterberg, S. van Waasen, G. Friederich, G. L. Puma, A. Wiesbauer and C. Sandner, "Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitters", *2004 IEEE RFIC Symp. Dig.*, pp. 87-90, June 2004.

[63] T. T. Y. Wong, *Fundamentals of Distributed Amplification*. Norwood, MA: Artech, 1993.

[64] D. G. Sarma, "On distributed amplification", *Proc. IEE*, vol. 102B, pp. 689-697, 1954.

[65] J. B. Beyer, S.N. Prasad, R.C. Becker, J.E. Nordman and G.K. Hohenwarter, "MESFET distributed amplifier design guidelines", *IEEE Trans. Microwave Theory Tech.*, vol. 32, no. 3, pp. 268 - 275, Mar. 1984.

[66] C. S. Aitchison, "The Intrinsic Noise Figure of the MESFET Distributed Amplifier", *IEEE Trans. Microwave Theory Tech.*, vol. 33, no. 6, pp. 460 - 466, Jun 1985.

[67] *Advanced Design System 2003: Momentum*, Agilent Technologies, Palo Alto, CA, 2003.

[68] *Matlab, Version 6.5*, The MathWorks Inc., Natick, MA, 2002.

[69] Y. K. Koutsoyannopoulos and Y. Papananos, "Systematic analysis and modeling of integrated inductors and transformers in RF IC design", *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Proc.*, vol. 47, no. 8, pp. 699-713, Aug. 2000.

[70] P. J. van Wijnen, H.R. Claessen and E.A.Wolsheimer, "A new straight forward calibration and correction procedure for 'on-wafer' high frequency S-parameter measurements (45 MHz–18 GHz)", *Proc. 1987 Bipolar Circuits Tech. Meeting (BCTM97)*, pp. 70–73, 1987.

[71] C. H. Chen and M. J. Deen, "A General Noise and S-Parameter De-Embedding Procedure for On-Wafer High-Frequency Noise Measurements of MOSFETs", *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 5, pp. 1004-1005, May 2001.

[72] K. Honjo and Y. Takayama, "GaAs FET ultrabroad-band amplifiers for Gbit/s data rate systems", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 629-636, July 1981.

[73] W. -S. Kim, X. Li and M. Ismail, "A 2.4 GHz CMOS low noise amplifier using an inter-stage matching inductor", *42nd Midwest Symp. Circuits and Syst.*, vol. 2, pp. 1040 - 1043, Aug. 1999.

[74] W. A. Harrison, "Tunneling from an independent-particle point of view", *Phys. Rev.*, vol. 123, no. 1, pp. 85-89, July 1961.

[75] P. J. Price and J. M. Radcliffe, "Esaki tunneling", *IBM J. Res. Dev.*, vol. 3, pp. 364-371, 1959.

[76] K. M. Cao, W. -C. Lee, W. Liu, X. Jin, P. Su, S. K. H. Fung, J. X. An, B. Yu and C. Hu, "BSIM4 gate leakage model including source-drain partition", *IEDM Tech. Dig.*, pp. 815-818, 2000.

[77] K. F. Schuegraf and C. Hu, "Hole injection SiO2 breakdown model for very low voltage lifetime extrapolation", *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 761-767, May 1994.

[78] R. van Langevelde, A. J. Scholten, R. Duffy, F. N. Cubaynes, M. J. Knitel and D. B. M. Klaasen, "Gate current: Modeling, ΔL extraction and impact on RF performance", *IEDM Tech. Digest*, pp. 289-292, 2001.

[79] W. K. Shih, R. Rios, P. Packan, K. Mistry and T. Abbott, "A general partition scheme for gate leakage current suitable for MOSFET compact models", *IEDM Tech. Digest*, pp. 293-296, 2001.

[80] X. Gu, G. Gildenblat, G. O. Workmann, S. Veeraraghavan, S. Shapira and K. Stiles, "A Surface Potential-Based Compact Model of n-MOSFET Gate-Tunneling Current", *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 127-135, Jan. 2004.

[81] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven and V. C. Venezia, "Noise Modeling for RF CMOS Circuit Simulation", *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618-632, March 2003.

[82] J. Lee, G. Bosman, K. R. Green and D. Ladwig, "Noise model of gate-leakage current in ultrathin oxide MOSFETs", *IEEE Trans. Electron Devices*, vol. 50, no. 12 , pp. 2499-2506, Dec. 2003.

[83] J. Lee and G. Bosman, "Comprehensive noise performance of ultrathin oxide MOSFETs at low frequencies", *Solid-State Electron.*, no. 48, pp. 61-71, 2004.

[84] C. Fiegna, "Analysis of gate shot noise in MOSFETs with ultrathin gate oxides", *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 108-110, Feb. 2003.

[85] G. Pailloncy, B. Iñiguez, G. Dambrine and F. Danneville, "Influence of a tunneling gate current on the noise performance of SOI MOSFETs", *Proc. 2004 IEEE International SOI Conference*, pp. 55-57, Oct. 2004.

[86] H. -O. Vickes, M. Ferndahl, A. Masud and H. Zirath, "The influence of the gate leakage current and the gate resistance on the noise and gain performances of 90-nm CMOS for micro- and millimeter-wave frequencies", *2004 IEEE MTT-S Int. Microwave Symp. Digest*, vol. 2, pp. 969-972, June 2004.

[87] Q. Ngo, D. Navarro, T. Mizoguchi, S. Hosakawa, H. Ueno, M. Miura-Mattausch and C. Y. Yang, "Gate current partitioning in MOSFET models for circuit simulation", *Tech. Proc. 2003 Nanotechnology Conference and Trade Show*, vol. 2, pp. 322-325, Feb. 2003.

[88] J. Ranuárez, M. J. Deen and C. H. Chen, "Modeling the partition of noise from the gate tunneling current in MOSFETs", *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 550-552, Aug. 2005.

[89] H. Hillbrand and P. H. Russer, "An efficient method for computer aided noise analysis of linear amplifier networks", *IEEE Trans. Circuits and Systems*, vol. CAS-23, no. 4, pp. 235-238, April 1976.

[90] A. van der Ziel, "Gate noise in field effect transistors at moderately high frequencies", *Proc. IEEE*, vol. 51, pp. 461-467, Mar. 1963.

[91] H. S. Momose, R. Fujimoto, S. Otaka, E. Morifuji, T. Ohguro, T. Yoshitomi, H. Kimijima, S. Nakamura, T. Morimoto, Y. Katsumata, H. Tanimoto, and H. Iwai, "RF noise in 1.5 nm gate oxide MOSFETs and the evaluation of the NMOS LNA circuit integrated on a chip", *1998 Symp. VLSI, Digest of Technical Papers*, pp. 96 - 97, June 1998.

[92] H. S. Momose, T. Ohguro, K. Kojima, S. Nakamura, and Y. Toyoshima, "1.5-nm gate oxide CMOS on (110) surface-oriented Si substrate", *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1001-1008, Apr. 2003.

[93] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, R. de Kort, V. C. Venezia and D. B. M. Klaasen, "Compact modeling of noise for RF CMOS circuit design", *Proceedings of SPIE vol. 5113 Noise in Devices and Circuits, edited by M. J. Deen, Z. Çelik-Butler and M. E. Levinshtein, (SPIE, Bellingham, WA, 2003)*, pp. 93-104.

[94] D. M. Pozar, *Microwave Engineering*. Amherst, MA: Wiley, 1998.

[95] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization", *IEEE Trans. Components, Hybrids, and Manufacturing Tech.*, vol. 15, no. 4, pp. 483 - 490, Aug. 1992.

[96] R. van Langevelde, A. J. Scholten and D. B. M. Klaassen, *Physical Background of MOS Model 11, Unclassified Report 2003/00239*, Royal Philips Electronics, April 2003. Available at: http://www.semiconductors.philips.com/Philips_Models/mos_models/model11/index.html.

[97] I. J. Bahl and P. Bhartia eds., *Microwave Solid State Circuit Design*, 2nd ed., Hoboken, N.J. : Wiley-Interscience, 2003.