EFFECTS OF CHANNEL LENGTH FLUCTUATION ON RF OSCILLATORS

EFFECTS OF CHANNEL LENGTH FLUCTUATION ON THE PERFORMANCE OF RF OSCILLATORS

By

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Abstract

As the dimensions of the transistors keep decreasing, the effects of transistors' dimensions fluctuation will become increasingly important for differential radio-frequency (RF) integrated circuits (ICs). In most RFICs, the transistor's channel length is usually much smaller than its channel width. Therefore, small unintentional changes in the channel length due to unavoidable fabrication process variations can cause a large circuit performance deviation, and thus, the effects of channel length fluctuation are extremely important.

This thesis investigates the effects of channel length fluctuation on the performance of RF oscillators. Two fully integrated, cross-coupled, differential LC oscillators have been designed in triple-well 0.18 μm CMOS technology and used as the test circuits. The measured results of the first VCO has a relatively large frequency tuning range of ~25% because two pairs of varactor are used and a power consumption P_{con} less than 1.5 mW with 1.5 V supply voltage. Also, it has an output power P_{out} of -13.3 dBm and a P_{con} of 1.31 mW at an oscillation frequency f_0 of 5.5 GHz, which corresponds to the best phase noise performance of -121.2 dBc/Hz at 1 MHz offset frequency.

The simulated results of the second oscillator has a f_0 of 1.12 GHz, a P_{out} of 1.79 dBm and a P_{con} of 6.479 mW with 1.8 V supply voltage. Both the f_0 and P_{out} are found to be decreased (increased) when the fabricated channel length is larger (smaller) than the one at the design and simulation stages. The maximum variation of f_0 and P_{out} are 2.45 kHz and 0.08 dBm, respectively, with less than 20% of variation in the channel length. Formulae have been derived to predict these variations. Also, the use of body bias on the transistors is proposed as a means to compensate for the changes in the frequency performance characteristics due to the channel length fluctuations. In addition, it is found that the variation of f_0 and P_{out} due to channel length fluctuations is more significant in oscillators with higher f_0. A recommendation is given to designers of how to design an oscillator with high f_0 while minimizing the sensitivity of f_0 and P_{out} to channel length fluctuations. While the phase noise is expected to be affected by the channel length fluctuations, simulation result

does not show a significant dependence of the phase noise on channel length. This discrepancy is believed to be caused by the inaccuracy of the phase noise simulation.

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List of Symbols

A_j	Unit junction area
A_p	Area of one of the plates of MIM capacitor
C	Capacitance
C_{cap}	Value of the capacitor that is used to build LC tank
C_d	Capacitance associated to depletion region of MOS varactor
C_d'	Capacitance associated to depletion region of MOS varactor per unit area
$C_{d,min}$	Minimum C_d
C_{db}	Parasitic drain-body capacitance
C_{device}	Device capacitance
C_{diff}	Diffusion capacitance of pn junction
C_{gd}	Parasitic gate-drain capacitance
C_{gs}	Parasitic gate-source capacitance
C_i	Different capacitors that make up C_{tk}
C_j	Junction capacitance associated to depletion region of pn junction
C_{j0}'	Zero-biased junction capacitance associated to depletion region of pn junction per unit junction area
$C_{L,ox}$	Oxide capacitance of spiral inductor between spiral and substrate
$C_{L,p}$	Equivalent parallel capacitance replaces $C_{L,ox}$, $R_{L,sub}$ and $C_{L,sub}$

$C_{L,s}$	Series capacitance of spiral inductor representing capacitance due to overlap between spiral and center-tap underpass
$C_{L,sub}$	Silicon substrate capacitance of spiral inductor
C_{max}	Maximum capacitance
C_{MIM}	Capacitance value of MIM capacitor
$C_{MIM,ox}$	Oxide capacitance between bottom plate of MIM capacitor and substrate
$C_{MIM,sub}$	Silicon substrate capacitance of MIM capacitor
C_{min}	Minimum capacitance
C_{ox}	Oxide capacitance
C'_{ox}	Oxide capacitance per unit area
C_p	Tunable capacitor represents ideal varactor using parallel equivalent circuit
$C_{parasitic}$	Parasitic capacitance
C_s	Tunable capacitor represents ideal varactor using series equivalent circuit
C_{tk}	Total capacitance in LC tank
D_I	Threshold adjust implant dose
$E_{C,max}$	Maximum stored capacitive energy
E_{dis}	Energy dissipated per cycle
$E_{L,max}$	Maximum stored inductive energy
F_t	Frequency at unity current gain
F_{max}	Maximum frequency at unity power gain
f	Frequency of applied signal
f_0	Oscillation frequency

f_{centre}	Centre frequency that VCOs can achieve
f_{max}	Maximum frequency that VCOs can achieve
f_{min}	Minimum frequency that VCOs can achieve
f_{SR}	Self-resonant frequency
$G(s)$	Feedforward network or open-loop transfer function in s-domain
G_m	Total transconductance
g_m	Transconductance
$H(s)$	Feedback network's transfer function in s-domain
I_{bias}	Bias current controlled by bias current transistor
$I_{C,peak}$	Peak current flowing through a series connection of R_s and C_s causing $V_{C,peak}$ across C_s
I_D	PN diode forward bias current
I_{DS}	Drain-source current
$I_{L,peak}$	Peak current flowing through a series connection of R_s and L_s causing $V_{L,peak}$ across L_s
k	Boltzmann's constant
kf	$1/f$ noise parameter in MOSFET model
L	Inductance
$L\{\Delta\omega\}$	Phase noise
L_1	Length of first segment of spiral inductor
L_2	Length of second segment of spiral inductor
L_3	Length of third segment of spiral inductor
L_g	Gate length

$L_{L,s}$	Inductance of spiral inductor
$L_{MIM,s}$	Parasitic inductance in electrodes of MIM capacitor
L_n	Length of last segment of spiral inductor
L_p	Fixed inductor represents ideal spiral inductor using parallel equivalent circuit
L_s	Fixed inductor represents ideal spiral inductor using series equivalent circuit
L_{tk}	Total inductance in LC tank
m_j	Constant depends on abruptness of pn junction
N_A	Acceptor impurity concentration
N_D	Donor impurity concentration
n	Electron concentration
n_1	non-ideal factor characterizing distributed effect and number of contacts of MOS structure device for R_g
n_2	non-ideal factors characterizing distributed effect and number of contacts of MOS structure device for R_{ch}
n_f	Number of gate fingers
n_i	Intrinsic carrier concentration
O_{ssf}	Oscillation startup safety factor
P_{con}	Power consumption
P_{out}	Output power
P_s	Average power dissipated in resonator
p	Hole concentration
Q_B'	Depletion region charge per unit area

Q_C	Quality factor of varactor
Q_{C_i}	Quality factors of different capacitors C_i
$Q_{C,comb}$	Quality factor of varactor using an equivalent circuit with a resistor connected in series with a parallel connection of resistor and tunable capacitor
$Q_{C,min}$	Minimum quality factor of varactor
$Q_{C,p}$	Quality factor of varactor using parallel equivalent circuit
$Q_{C,s}$	Quality factor of varactor using series equivalent circuit
Q_L	Quality factor of inductor
$Q_{L,max}$	Maximum quality factor of inductor
$Q_{L,p}$	Quality factor of inductor using parallel equivalent circuit
$Q_{L,s}$	Quality factor of inductor using series equivalent circuit
$Q_o^{'}$	Fixed oxide charge per unit area
Q_{tk}	Quality factor of LC tank
q	Magnitude of electronic charge
R	Resistance
R_{acc}	Parasitic resistance associated to accumulation layer of MOS varactor operates in accumulation mode
R_{active}	Negative resistance of active circuit network
R_{ch}	Channel resistance
R_{comb}	Resistance of Z_{comb}
R_d	Parasitic resistance associated to n-well (between edge of depletion region and edge of n^+ implantations) of MOS varactor operates in depletion mode
R_{diff}	Diffusion resistance of pn junction

R_{eff}	Effective parallel resistance in resonator network
R_g	Gate resistance
R_{inv}	Parasitic resistance associated to inversion layer of MOS varactor operates in weak inversion mode
$R_{j,p}$	Inherent parallel losses of reverse-biased pn junction
$R_{j,s}$	Inherent series losses of reverse-biased pn junction
$R_{L,p}$	Equivalent parallel resistance replaces $C_{L,ox}$, $R_{L,sub}$ and $C_{L,sub}$
$R_{L,s}$	Metal series resistance of spiral inductor representing energy losses due to skin effect in spiral interconnect structure and induced eddy current in any conductive media close to the inductor
$R_{L,sub}$	Silicon substrate resistance of spiral inductor
$R_{MIM,s}$	Parasitic resistance in electrodes of MIM capacitor
$R_{MIM,sub}$	Silicon substrate resistance of MIM capacitor
R_p	Resistor represents inherent parallel losses
R_s	Resistor represents inherent series losses
R_{sq}	Sheet resistance
S_L	Spacing between two adjacent segments of spiral inductor
T	Temperature in degrees Kelvin
T_{period}	Time for one period of applied signal
t_i	Thickness of dielectric of MIM capacitor
V_{ctrl}	Control voltage
$V_{C,peak}$	Peak voltage across tunable capacitor
V_{dd}	Highest available DC bias voltage on the whole chip

V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
$V_{L,peak}$	Peak voltage across fixed inductor
V_{osc}	Amplitude of oscillation
V_R	Variable reverse bias voltage
V_T	Threshold voltage
V_{T0}	Zero-substrate-bias value of V_T
V_{TN}	Threshold voltage of nMOSFETs
V_{TP}	Threshold voltage of pMOSFETs
$V_{thermal}$	Thermal voltage
W_g	Gate width
W_L	Conductor width of spiral inductor
$X(s)$	Input signal which is noise from circuit components in s-domain
X_{comb}	Reactance of Z_{comb}
$Y(s)$	Output signal in s-domain
Y_{in}	Input admittance
Z_{comb}	Input impedance of varactor using an equivalent circuit with a resistor connected in series with a parallel connection of resistor and tunable capacitor
Z_{in}	Input impedance
Z_{tk}	Equivalent parallel impedance of LC tank at resonance node
β	Current factor
$\Delta\omega$	Offset frequency from ω_0 at which phase noise is characterized

$\Delta\omega_{1/f^3}$	Corner frequency between $1/f^3$ and $1/f^2$ regions on phase noise plot
ε_0	Permittivity in vacuum
ε_i	Relative permittivity of dielectric
λ	Channel-length modulation parameter
μ_n	Electron mobility
μ_p	Hole mobility
ω	Angular frequency of applied signal
ω_0	Fundamental angular oscillation frequency
ϕ_B	Fermi potential in substrate
ϕ_{MS}	Contact potential of body material to gate material
ϕ_{bi}	Built-in voltage of open-circuit pn junction
ϕ_t	Thermal voltage
ρ	Electrical resistivity
σ	Electrical conductivity
τ_T	Diode transit time

List of Acronyms

AC	Alternating current
ADC	Analog-to-digital converter
BJT	Bipolar junction transistor
CMOS	Complementary metal-oxide-semiconductor

DAC	Digital-to-analog converter
DC	Direct current
DRAM	Dynamic random access memory
FET	Field-effect transistor
FoM	Figure-of-Merit
GSM	Global system for mobile communications
GV	Global variation
IC	Integrated circuit
ITRS	International technology roadmap for semiconductors
LNA	Low-noise amplifier
Li^+	Lithium ion
LO	Local oscillator
LTI	Linear time invariant
LTV	Linear time variant
LV	Local variation
MIM	Metal-insulator-metal
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
nAMOS	n-type accumulation mode MOS
nIMOS	n-channel inversion mode MOS
nMOS	n-channel MOS
nMOSFET	n-channel MOSFET

PA	Power amplifier
pAMOS	p-type accumulation mode MOS
pIMOS	p-channel inversion mode MOS
pMOS	p-channel MOS
pMOSFET	p-channel MOSFET
RF	Radio-frequency
TSMC	Taiwan Semiconductor Manufacturing Co., LTD
VCO	Voltage-controlled oscillator

Chapter 1

Introduction

1.1 MOTIVATION OF THE THESIS

1.1.1 Silicon Complementary Metal-Oxide-Semiconductor Technology

The integrated circuit (IC) technology market share presented in percent of total dollars for 1982 to 2002 is shown in Figure 1.1. It can be seen clearly from this figure that no technology in the past has dominated the IC market like the complementary metal-oxide-semiconductor (CMOS) technology does today. Although the market share of CMOS ICs dropped from its previous year value in 1997, it is not an indication of declining CMOS applications. This is, in fact, due to the continuous lowering of prices of metal-oxide-semiconductor (MOS) memories, particularly the dynamic random access memories (DRAMs) [1]. Also, due to the growth of bipolar complementary metal-oxide-semiconductor (BiCMOS) IC market prior to Intel's switch from BiCMOS-based Pentium microprocessors to CMOS-based ones [1]. Thereafter, the dominance of CMOS ICs turned its market share up again in 1998 and increased to 86% in 2002.

The widespread use of CMOS technology [1] is mainly due to the combination of the following factors.

- Lowest price per function compared to other technologies at the same geometry.
- Low power dissipation.
- High density (i.e. deep submicron features) and scalability.
- Capability for analog and digital circuitry on the same chip (i.e. system-on-chip).

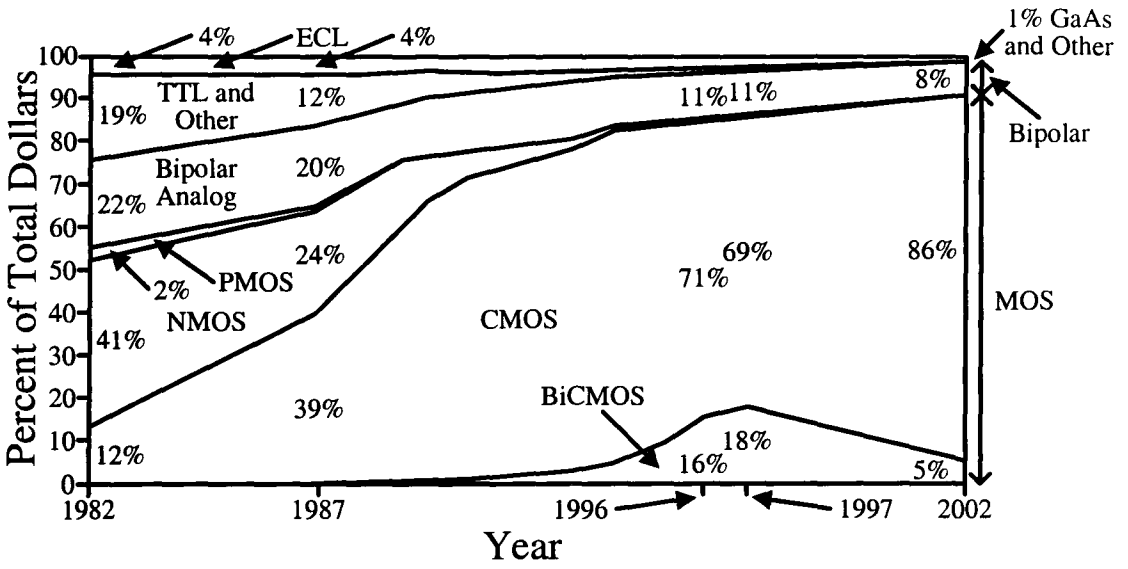


Figure 1.1 1982 to 2002 IC technology market share [1].

The trends with CMOS supply voltage and gate length are good illustrations of low power dissipation and high density, respectively, which is shown in Figure 1.2. From this figure, it can be observed that both supply voltage and gate length will be scaled down continuously, suggesting that the power dissipation and density will be further reduced and increased, respectively.

The interaction among commercial wireless communication applications, available spectrum, and the types of elemental and compound semiconductors likely to be used is schematically shown in Figure 1.3. The consumer portions of wireless communications markets are very sensitive to cost, which is one of the key factors determining the location of boundaries between the types of radio-frequency (RF) semiconductors shown in the top part of Figure 1.3 [2]. In fact, the boundary between the group IV semiconductors silicon Si and silicon germanium SiGe has been moving to higher frequencies with time [2]. This is because of the continuous increase of the peak frequency at unity current gain F_t and peak maximum frequency at unity power gain F_{max} with the continued down-scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) in Si CMOS technology, which is shown in Figure 1.4.

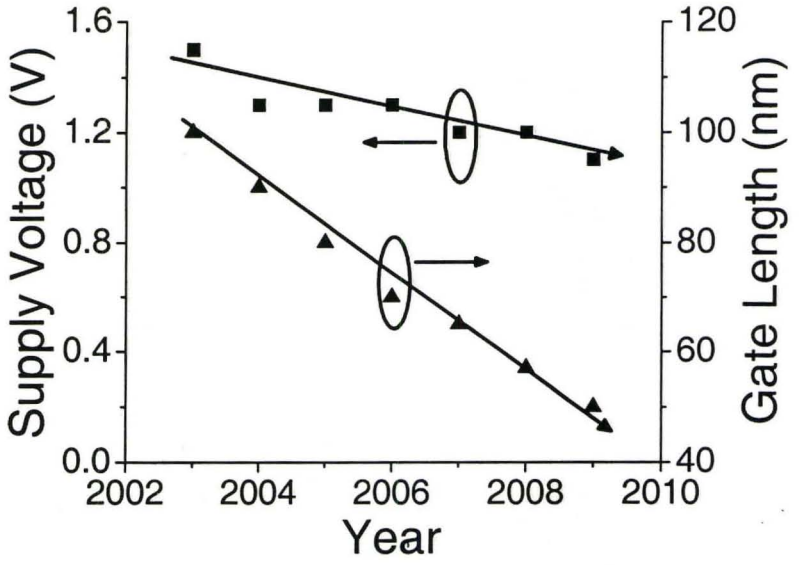


Figure 1.2 Trend of supply voltage and gate length for CMOS [2].

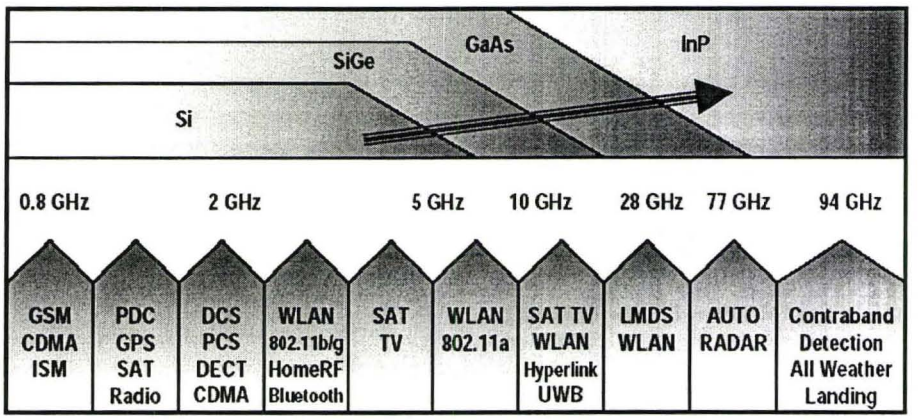


Figure 1.3 Schematic plot of the interaction among commercial wireless communication applications, available spectrum, and the types of semiconductors likely to be [2].

In consequence of the advantages and trends discussed above, RF transceivers implemented in Si CMOS technology for commercial wireless communication applications is a very active and popular research area in nowadays.

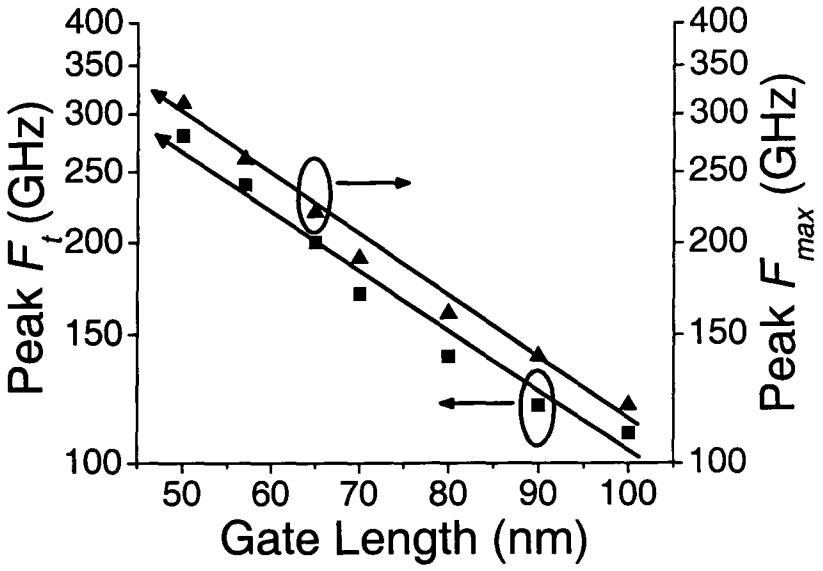


Figure 1.4 Trend of peak F_t and peak F_{max} with gate length for CMOS [2].

1.1.2 Voltage-Controlled Oscillators in Wireless Transceivers

Oscillators have been essential components since the time Edwin Howard Armstrong discovered the heterodyne principle in 1912, which defines the multiplication of two signals in the time domain in order to produce a frequency shift in the frequency domain [3], [4]. However, mobile telephony was not available until the emergence of voltage-controlled oscillator (VCO) modules in the 1980's [3]. A VCO module is basically a miniature version of a discrete-component oscillator constructed on a substrate; it is self-contained and requires only connections to the ground, supply voltage, tuning voltage, and output load [3]. Initially, such modules were fairly large and relatively expensive [3]. However, demand increased for miniaturized VCO modules with the growing sales of mobile telephones in the late 1980's and early 1990's [3]. Therefore, new, smaller and lower cost VCO modules were developed and the size of reduction over time of the state-of-the-art commercial VCO modules is shown in Figure 1.5. Although it can be seen from this figure that the size of VCO modules has been reduced significantly and satisfied the tough space constraints imposed by the new mobile wireless devices such as cellular phones, an even small-

er and more cost-effective VCO technology arose by the end of the 1990's: monolithic IC VCO technology [3].

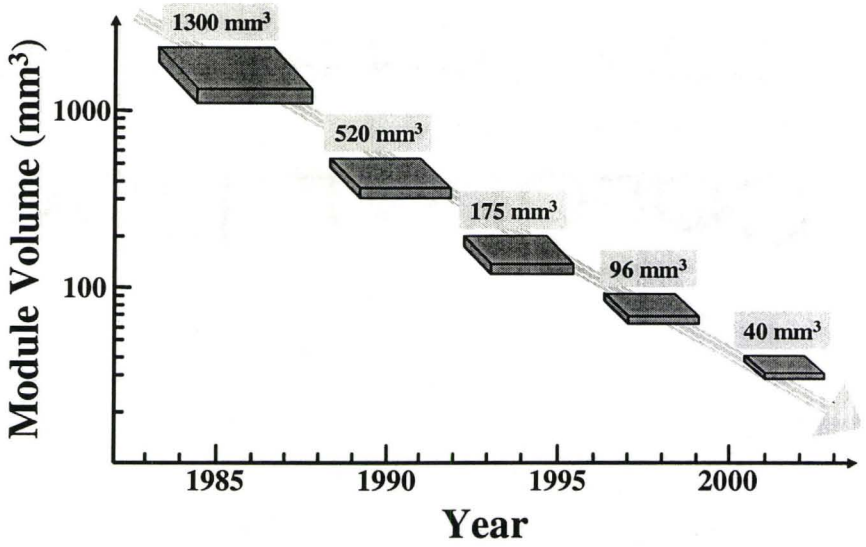


Figure 1.5 The size of reduction over time of the state-of-the-art commercial VCO module [3].

Monolithic IC VCO technology is defined as a VCO implementation in which all the circuit elements of an inductance-capacitance (LC) VCO are integrated on one chip [3]. In general, the overall performance of the early monolithic VCOs was poorer than the VCO modules, especially the phase noise and tuning characteristics [3]. However, monolithic VCOs are extremely small, cost-effective and available in the same process in which RF transceiver functions were being implemented, which implies that the VCO could be integrated with other RF functions [3] and it is illustrated by a simplified block diagram of a RF transceiver in Figure 1.6. It should be noted that only the important RF circuit blocks, starting from the low-noise amplifier (LNA) or power amplifier (PA) at the antenna end to the analog-to-digital converter (ADC) or digital-to-analog converter (DAC) at the base-band end, are shown in Figure 1.6. Therefore, research on monolithic IC VCO technology continues so that better VCOs with improved performance characteristics at increasingly higher frequencies can be obtained. However, the design of a VCO that generates the local

oscillator (LO) carrier signal is still a challenge in the design of single-chip transceivers in CMOS technology in today's wireless communication systems.

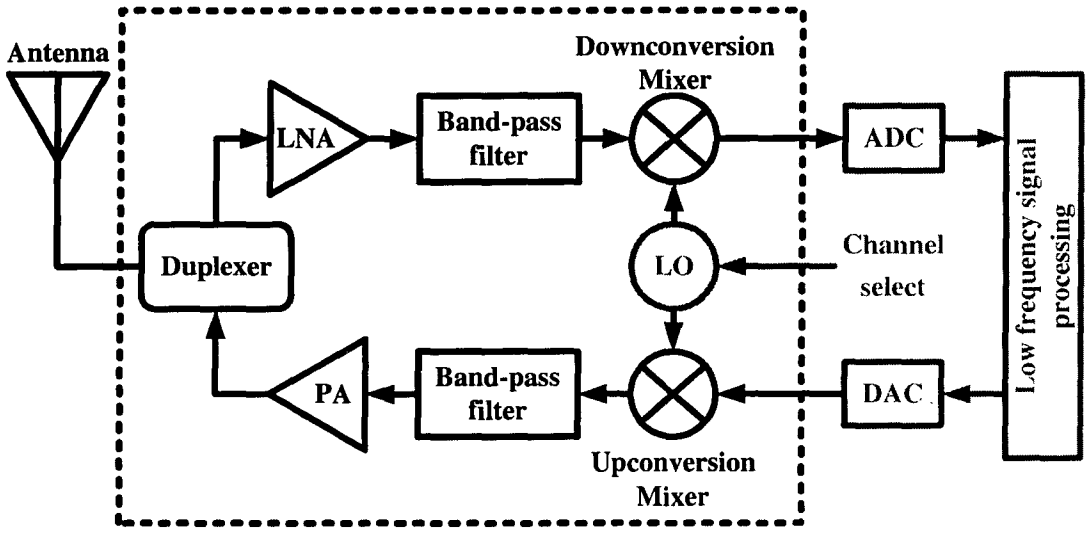


Figure 1.6 Simplified block diagram of a RF transceiver [5].

1.1.3 Device Mismatch

According to the international technology roadmap for semiconductors (ITRS), which is an assessment of the semiconductor technology requirements as a result of a co-operative effort of the global industry manufacturers and suppliers, government organizations, consortia, and universities, one of the difficult challenges in optimizing RF/analog CMOS devices with scaled technology is mismatch [2]. Device mismatch occurs due to unavoidable fabrication process variations such as over- and under-etching, varying doping concentration gradients and unequal oxide thicknesses. As the minimum feature size in the microelectronics devices are reduced to deep submicron values, the control of the variation in the fabrication steps becomes increasingly difficult [6]. For example, it was reported in ITRS 2003 that the variation of etching in modern and future technologies is approximately 20% [2]. This makes the variation of the device parameters in the modern technologies larger than the one in the older technologies, and thus, the circuit yield is requiring more attention than before [7].

As previously discussed, CMOS technology has become a viable choice for implementation of RFICs building blocks as the technology is scaled down. Also, for many RFICs, differential circuit configurations are used. Therefore, the effects of mismatch in the device parameters due to processing will become increasingly important, especially the effects of mismatch in the transistor's parameters since MOSFETs are the most complicated devices in CMOS technologies. However, interestingly, almost no published research can be found in this subject. This is in contrast to the large amount of published research that exist on mismatch effects at lower frequencies.

1.2 OBJECTIVES OF THE THESIS

The accuracy of a circuit's performance depends on the exact values of the transistors' dimensions. This is especially true for differential RFICs. Unfortunately, because of inevitable fabrication process variations such as over- and under-etching, non-uniform doping concentration gradients and uneven oxide thicknesses, the dimensions of the transistors at the design and simulation stages are different from the one after fabrication. Therefore, the effects of transistors' dimensions fluctuation will become increasingly important with the continued down-scaling of MOSFETs' dimensions. In most RF circuits, the transistor's channel length is typically much smaller than its channel width. Therefore, the effects of channel length fluctuation are crucial since small non-deliberate changes in the channel length can lead to a large performance deviation.

The objective of this thesis is to investigate the effects of channel length fluctuation on the performance of RF oscillators. To investigate this problem, two fully integrated, cross-coupled, differential LC oscillators will be designed in TSMC triple-well 0.18 μm standard CMOS technology [8] and used as the test circuits. Also, a possible solution to compensate for the changes in the frequency performance characteristics due to these fluctuations will be sorted. In addition, a recommendation of how to design an oscillator with high oscillation frequency f_0 while minimizing the sensitivity of f_0 and output power P_{out} to channel length fluctuations will be given to designers. It should be noted that the fluc-

tuation of the channel length is assumed to be dominated by the variation of etching in this research since the reported variation of etching in modern and future technologies is approximately 20% in the ITRS 2003 [2], which is a very large variation.

1.3 ORGANIZATION OF THE THESIS

Chapter 2 begins with a discussion of the properties and structures of two passive devices: capacitor and inductor. It will first present the performance parameters that are used to determine the properties of varactors followed by a review of the eight available options of varactors in standard CMOS technology. The principle of operation and the qualitative analysis of the performance parameters for two types of varactors – p^+–to–n-well junction varactor and n-type accumulation mode metal-oxide-semiconductor (MOS) varactor – will then be presented. A performance comparison will be also given for different types of varactors in recent technology generations. Following this, the model of the metal-insulator-metal capacitor used for simulation in Spectre will be reviewed. Finally, the performance parameter and the equivalent circuit model for a spiral inductor will be presented with a performance comparison of recently reported state-of-the-art inductors.

In Chapter 3, the theory of LC oscillators will be reviewed using a two-port model and a two one-port model. The performance parameters used to evaluate LC oscillators will then be presented. These performance parameters are oscillation frequency f_0, frequency tuning range, power consumption P_{con}, amplitude of oscillation V_{osc} / output power P_{out}, and phase noise $L\{\Delta\omega\}$. A Figure-of-Merit (FoM) will also be defined to compare different designs of LC oscillators using these performance parameters. This chapter will then be concluded by a discussion and comparison of two cross-coupled differential LC oscillator topologies: n-channel MOSFET (nMOSFET) cross-coupled differential topology and complementary cross-coupled differential topology.

The process variation and device mismatch will be presented in Chapter 4. This chapter will first define the difference between global variation (GV) and local variation (LV). The influence of LV on resistors, capacitors and MOSFETs will then be reviewed

with the emphasis on MOSFETs, since this is the device that is of interest in this research. Following this, the influence of LV on MOSFETs from deep submicron and RF perspectives will be discussed.

Chapter 5 will present the circuit design and the results of the two fully integrated, cross-coupled, differential LC oscillators used for the analysis of the effects of channel length fluctuations on the performance of LC oscillators. The results of each oscillator will be discussed and analyzed using the performance parameters for LC oscillators that will be presented in Chapter 3. Also, the use of body bias on the MOSFETs will be proposed as a means to compensate for the changes in the frequency performance characteristics due to the channel length fluctuations. In addition, a recommendation of how to design an oscillator with high f_0 while minimizing the sensitivity of f_0 and P_{out} to channel length fluctuations will be given.

Finally, Chapter 6 will conclude the thesis with a summary of the research followed by some discussions on the future research work.

Chapter 2

Passive Devices – Capacitor and Inductor

Analog and radio-frequency (RF) integrated circuits (ICs) are built with active and passive devices. Typical active devices in mainstream silicon technology are metal-oxide-semiconductor (MOS) field-effect transistors (FETs), bipolar junction transistors (BJTs) and diodes, while passive devices are resistors, capacitors and inductors. Passive devices, especially capacitors and inductors, find wide usage in RFICs. For instance, they determine the oscillation frequency of resonators, allow simultaneous power and noise matching for low-noise amplifiers (LNAs), and increase efficiency by maximizing the voltage swing for power amplifiers (PAs) [9]. In this chapter, therefore, the properties and structures of different capacitors (varactor and metal-insulator-metal capacitor) and inductors will be discussed.

2.1 VARACTOR

Varactor is a shortened form of variable reactor, referring to the voltage controlled variable capacitance of a biased pn junction [10]. To understand the properties of varactor, it is essential to know what performance parameters are used to determine its properties.

2.1.1 Performance Parameters

Varactors can be characterized by several performance parameters such as capacitance tuning ratio, quality factor and capacitance-voltage characteristic. Among these parameters, the capacitance tuning ratio and quality factor are the most important [11], [12] and they are presented and discussed in the following two subsections.

2.1.1.1 Capacitance Tuning Ratio

Capacitance tuning ratio is defined as

$$\text{Capacitance Tuning Ratio} \equiv \frac{C_{max}}{C_{min}}, \tag{2.1}$$

where C_{max} and C_{min} are the maximum and minimum capacitance values that the varactor can achieve, respectively. Also, C_{max} and C_{min} are usually measured at the lower and upper limit of the tuning voltage, respectively. It is desired to have a large capacitance tuning ratio as it enables a large frequency tuning range for a voltage-controlled oscillator (VCO), which can compensate the variations of capacitance and inductance with respect to their nominal values due to process variations and make wide-band or even multiband applications possible [13]. In fact, the capacitance tuning ratio is also known as C_{max}/C_{min} *ratio* due to the simple definition in Equation (2.1).

2.1.1.2 Quality Factor

The quality factor of a varactor Q_C is defined as

$$Q_C \equiv 2\pi \frac{|\text{maximum stored capacitive energy} - \text{maximum stored inductive energy}|}{\text{energy dissipated per cycle}}, \tag{2.2}$$

where a sinusoidal voltage excitation is applied to the varactor [14]. Intuitively, from Equation (2.2), Q_C is a relative measure of the inherent losses of the varactor, which should be as small as possible. As a consequence, a good performance varactor should have Q_C as high as possible since the inherent losses are presented in the denominator in Equation (2.2).

An approximate analytical expression of Q_C can be obtained from a simplified equivalent circuit for a varactor using resistor and tunable capacitor as the inherent losses and ideal varactor, respectively, as shown in Figure 2.1. It can be seen from Figure 2.1 that the resistor and tunable capacitor can be connected to each other in either series, parallel or a combination of both [14].

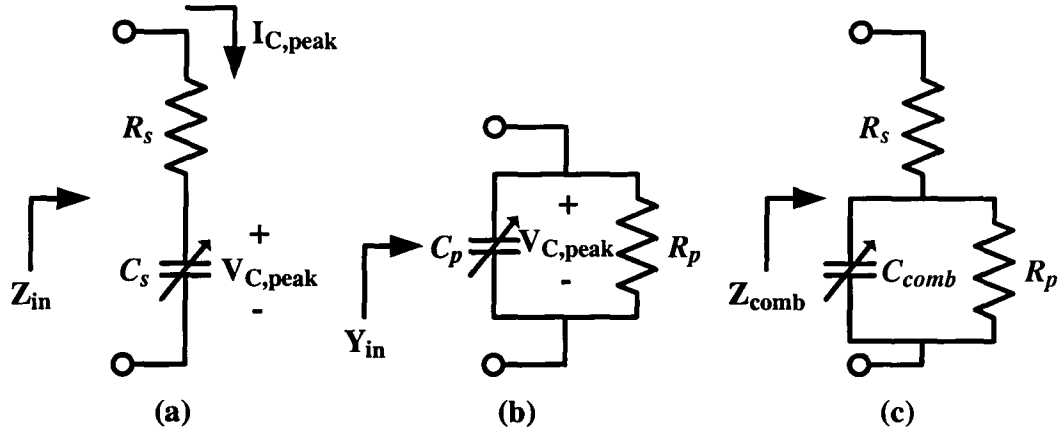


Figure 2.1 Simplified equivalent circuit for a varactor with resistor and tunable capacitor representing the inherent losses and ideal varactor, respectively, connected in either (a) series, (b) parallel or (c) combination of both [14].

Regardless of which simplified equivalent circuit is used, a varactor should be designed to operate far below its self-resonant frequency f_{SR} so that it will not affect the operation of the inductance-capacitance (LC) oscillator. When a varactor is operating far below the f_{SR}, the stored inductive energy is negligible, and thus, Equation (2.2) becomes

$$Q_C \approx 2\pi \frac{|\text{maximum stored capacitive energy}|}{\text{energy dissipated per cycle}} = 2\pi \frac{|E_{C,max}|}{E_{dis}}, \tag{2.3}$$

where

$$E_{C,max} = \frac{1}{2} C V_{C,peak}^2 \tag{2.4}$$

is the maximum stored capacitive energy in which $V_{C,peak}$ is the peak voltage across the tunable capacitor and E_{dis} is the energy dissipated per cycle [14].

For the equivalent circuit connected in series as shown in Figure 2.1(a),

$$E_{C,max} = \frac{1}{2} C_s V_{C,peak}^2 = \frac{1}{2} C_s \left(\frac{I_{C,peak}}{j\omega C_s} \right)^2 \tag{2.5}$$

and

$$E_{dis} = \frac{I_{C,peak}^2 R_s}{2} T_{period} = \frac{I_{C,peak}^2 R_s}{2} \frac{1}{f}, \tag{2.6}$$

where C_s is the tunable capacitor representing the ideal varactor using series equivalent circuit, $I_{C,peak}$ is the peak current flowing through the whole series connection causing $V_{C,peak}$ across the tunable capacitor, R_s is the resistor representing the inherent series losses, T_{period} is the time for one period of the applied signal, $f = 1/T_{period}$ is the frequency of the applied signal and $\omega = 2\pi f$ is its angular frequency. By substituting Equations (2.5) and (2.6) into Equation (2.3), the quality factor of a varactor using the series equivalent circuit $Q_{C,s}$ is

$$Q_{C,s} \approx 2\pi \frac{\left| \frac{1}{2} C_s \left(\frac{I_{C,peak}}{j\omega C_s} \right)^2 \right|}{\frac{I_{C,peak}^2 R_s}{2} \frac{1}{f}} = \frac{1}{\omega C_s R_s}. \tag{2.7}$$

In fact, $Q_{C,s}$ can also be derived directly from the input impedance Z_{in} of the series equivalent circuit as shown in Figure 2.1(a) as follows:

$$Q_{C,s} = \frac{|Im(Z_{in})|}{Re(Z_{in})} = \frac{|-1/(\omega C_s)|}{R_s} = \frac{1}{\omega C_s R_s}, \tag{2.8}$$

which gives the same expression as in Equation (2.7) [14].

Similarly, for the equivalent circuit connected in parallel as shown in Figure 2.1(b), the $E_{C,max}$ is given by Equation (2.4) and

$$E_{dis} = \frac{V_{C,peak}^2}{2R_p} T_{period} = \frac{V_{C,peak}^2}{2R_p} \frac{1}{f}, \tag{2.9}$$

where R_p is the resistor representing the inherent parallel losses. Therefore, the quality factor of a varactor using the parallel equivalent circuit $Q_{C,p}$ can be found by substituting

Equations (2.4) and (2.9) into Equation (2.3) with C replaced by the tunable capacitor representing the ideal varactor in a parallel equivalent circuit C_p, which gives

$$Q_{C,p} \approx 2\pi \frac{\left|\frac{1}{2} C_p V_{C,peak}^2\right|}{\frac{V_{C,peak}^2}{2R_p}\frac{1}{f}} = \omega C_p R_p . \tag{2.10}$$

Also, similar to the series equivalent circuit, $Q_{C,p}$ can be obtained directly from the input admittance Y_{in} of the parallel equivalent circuit as shown in Figure 2.1(b) as follows:

$$Q_{C,p} = \frac{|Im(Y_{in})|}{Re(Y_{in})} = \frac{|\omega C_p|}{1/R_p} = \omega C_p R_p , \tag{2.11}$$

which gives the same expression as in Equation (2.10) [14].

In reality, however, the measured loss of a varactor consists of both series losses and parallel losses. The series losses correspond to the substrate losses and losses in the interconnecting metal layers, whereas the parallel losses represent the dielectric losses [14]. Therefore, a resistor connected in series with a parallel connection of resistor and tunable capacitor, as shown in Figure 2.1(c), is a better model of a real varactor. To determine the quality factor of a varactor using this equivalent circuit with the combination of both series losses and parallel losses $Q_{C,comb}$, its input impedance Z_{comb} is used and it is given by

$$Z_{comb} = R_{comb} + jX_{comb} = \frac{R_s[1 + (\omega C_{comb} R_p)^2] + R_p}{1 + (\omega C_{comb} R_p)^2} - j\frac{(\omega C_{comb} R_p)R_p}{1 + (\omega C_{comb} R_p)^2}, \tag{2.12}$$

where R_{comb} and X_{comb} are the resistance and reactance of Z_{comb}, respectively. By substituting R_{comb} and X_{comb} into Equation (2.8), $Q_{C,comb}$ can be derived as

$$Q_{C,comb} = \frac{|Im(Z_{in})|}{Re(Z_{in})} = \frac{(\omega C_{comb} R_p)R_p}{R_s[1 + (\omega C_{comb} R_p)^2] + R_p} . \tag{2.13}$$

Now, invert both sides of Equation (2.13) and divide both the numerator and denominator by R_p with the assumption of $Q_{C,p} = \omega C_{comb} R_p \gg 1$, then Equation (2.13) simplifies to

$$\frac{1}{Q_{C,comb}} \approx \frac{R_s R_p (\omega C_{comb})^2 + 1}{\omega C_{comb} R_p} = \omega C_{comb} R_s + \frac{1}{\omega C_{comb} R_p} = \frac{1}{Q_{C,s}} + \frac{1}{Q_{C,p}}. \quad (2.14)$$

Two important observations can be made from Equation (2.14):

1. If $Q_{C,s}$ or $Q_{C,p}$ is much smaller than the other one, it dominates $Q_{C,comb}$.
2. The series losses must be considered carefully with the parallel losses in the design of a varactor.

2.1.2 Available Options in Standard CMOS Technology

Integrated varactors can be categorized into two families in standard complementary metal-oxide-semiconductor (CMOS) technology: pn junction varactors and MOS varactors. In each family, there are four types of varactors and they are described and compared in the following two subsections. This comparison is used to determine which type of varactor in each family will be discussed and analyzed in detail later in this chapter. The main criterion used for the comparison is the expected relative quality factor for each type of varactor. Another criterion used is the process and/or terminal constraints that each type of varactor has. These two criteria are used because they are the only characteristics which are predictable without actually building, testing and measuring all types of varactors.

The inherent losses is mainly contributed by the portion of the signal path that is inside the substrate or the well for all eight types of varactors. Therefore, the sheet resistance R_{sq} of different materials can be used to perform a simple and quick comparison for Q_C [14]. The R_{sq} of a given material is defined as the resistance per square [15]. It is proportional to the electrical resistivity ρ of the material, which is equal to the reciprocal of the electrical conductivity σ of the material [15]–[17], i.e.

$$R_{sh} \propto \rho = \frac{1}{\sigma}. \quad (2.15)$$

The σ of an intrinsic silicon is defined as

$$\sigma = q(n\mu_n + p\mu_p), \tag{2.16}$$

where q is the magnitude of electronic charge, n and p are the electron and hole concentrations, respectively, and μ_n and μ_p are the electron and hole mobilities, respectively [17]. For materials using electrons as majority carriers, i.e. $n \gg p$, Equation (2.16) becomes

$$\sigma \approx qn\mu_n. \tag{2.17}$$

Similarly, for materials using holes as majority carriers, i.e. $p \gg n$, Equation (2.16) simplifies to

$$\sigma \approx qp\mu_p. \tag{2.18}$$

In silicon, μ_n is approximately 2.8 times of μ_p [18]. Therefore, from Equations (2.15), (2.17) and (2.18), devices using electrons as majority carriers to form the signal path are expected to have a higher σ, lower ρ and R_{sh}, and thus, lower inherent losses than those using holes as majority carriers. Consequently, devices using electrons as majority carriers are also expected to have a higher Q_C than those using holes.

2.1.2.1 PN Junction Varactors

PN junction varactors are the most widely used integrated capacitance tuning element in VCOs [11], [19]–[25]. The cross-sections of four different types of pn junction varactors available in standard CMOS technologies are shown in Figure 2.2. The resistor represents the series losses, which are the main inherent losses, associated with the signal path that is inside the substrate or the well. Also, a variable reverse bias voltage V_R is applied between the anode A and cathode C terminals to vary the value of the device capacitance C_{device}. Moreover, the p-substrate is grounded through a p^+ implantation contact that is usually done in practice to provide a common ground on the same chip.

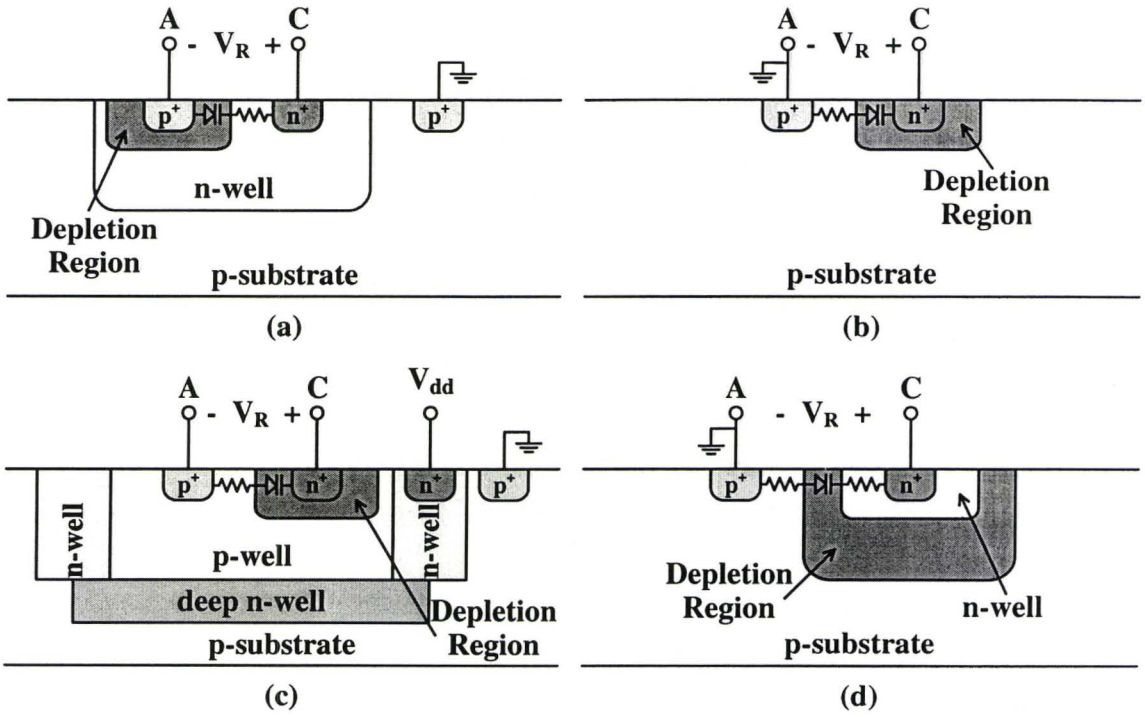


Figure 2.2 Illustration of cross-sections for four different types of pn junction varactors available in standard CMOS technologies: (a) p^+–to–n-well, (b) n^+–to–p-substrate, (c) n^+–to–p-well and (d) n-well–to–p-substrate [14].

The first type of pn junction varactor is the p^+–to–n-well junction varactor, which is shown in Figure 2.2(a). It utilizes the junction capacitance associated with the depletion region between the p^+ implantation and the n-well. Notice that no depletion region is formed surrounding the n^+ implantation because the n^+ implantation is only a contact for the n-well. The main inherent losses in this type of pn junction varactor are associated with the signal path inside the n-well, where electrons are the majority carriers. Therefore, it is expected to have a relatively high Q_C. This type of pn junction varactor does not have any process constraints since all components used to create it are available in standard CMOS technologies. Also, it has no terminal constraints since bias voltages can be applied to both the *A* and *C* terminals [14].

The second type of pn junction varactor, as shown in Figure 2.2(b), is the n^+–to–p-substrate junction varactor. It utilizes the junction capacitance associated with the depletion region between the n^+ implantation and the p-substrate. It should be noted that no depletion region is formed surrounding the p^+ implantation because the p^+ implantation is only a contact for the p-substrate. The main inherent losses in this type of pn junction varactor are associated with the signal path inside the p-substrate, where holes are the majority carriers. Therefore, it is expected to have a Q_C which is lower than the first type. Similar to the p^+–to–n-well junction varactor, this type of pn junction varactor does not have any process constraints in standard CMOS technologies. However, it has terminal constraints. Its *A* terminal is grounded since it is formed by the p-substrate. Therefore, all signals, including the bias voltages, must be applied to the *C* terminal [14].

The n^+–to–p-well junction varactor, as shown in Figure 2.2(c), is the third type of pn junction varactor. It can be seen that this type of pn junction varactor is almost same as the n^+–to–p-substrate junction varactor shown in Figure 2.2(b), except p-well is used instead of p-substrate as the p-type material of the pn junction varactor. Therefore, this type of pn junction varactor is expected to have a Q_C similar to the second type, which is lower than the first type. Additionally, since a p-well is used, then the n-well and deep n-well must be used to isolate the p-well from the p-substrate, i.e. a triple-well process is required. To use the n-well and deep n-well for isolation, the highest available direct current (DC) bias voltage on the whole chip V_{dd} must be applied to the n-well through an n^+ implantation. By doing this, with the p-substrate grounded, the pn junctions between the p-well and n-well/deep n-well, and p-substrate and n-well/deep n-well will be reversely biased. Therefore, the junction currents and junction capacitances between these two pn junctions will be minimized, and thus, a good isolation of the p-well from the p-substrate can be achieved by using the n-well and deep n-well. Triple-well process, however, is not available in all standard CMOS technologies. For instance, triple-well process is available in Taiwan Semiconductor Manufacturing Co., LTD (TSMC) 0.18 μm CMOS technology [8] but not in TSMC 0.35 μm CMOS technology [26]. Consequently, this type of pn junction varactor has process constraints. Also, due to the p-well is isolated from the p-substrate, the terminal

constraint that exists in the second type of pn junction varactor is eliminated, and thus, bias voltages can be applied to both the *A* and *C* terminals.

The fourth type of pn junction varactor is the n-well–to–p-substrate junction varactor, which is shown in Figure 2.2(d). This type of pn junction varactor is also almost same as the second type of pn junction varactor shown in Figure 2.2(b), except n-well is used instead of n^+ as the n-type material of the pn junction varactor. Therefore, it has no process constraints but a terminal constraint, which is that the *A* terminal is grounded and all signals must be applied to the *C* terminal. The junction capacitance utilized by this type of pn junction varactor is associated with the depletion region between the n-well and p-substrate. The main inherent losses are associated with the signal path inside both the n-well and the p-substrate, where electrons and holes are the majority carriers, respectively. Therefore, this type of pn junction varactor is expected to have the lowest Q_C among all four types of pn junction varactors because it has two main contributions to its inherent losses instead of one, which are the cases for the other three types of pn junction varactors described previously [14].

From the comparisons discussed above, it can be concluded that the p^+–to–n-well pn junction varactor is the best among all four types of pn junction varactors that are available in standard CMOS technologies. It has the highest expected Q_C. Also, it has no process or terminal constraints in standard CMOS technologies. Therefore, the p^+–to–n-well pn junction varactor is selected to be discussed and analyzed in detail later in this chapter.

2.1.2.2 MOS Varactors

MOS varactors have been studied intensively in the last few years [11], [13], [14], [19]–[25], [27]–[44]. The cross-sections of four different types of MOS varactors available in standard CMOS technologies are shown in Figure 2.3. The resistor represents the series losses, which are the main inherent losses, associated with the signal path that is inside the substrate or the well. Also, a variable bias voltage is applied between the gate *G* terminal and the connected drain-source *S* terminal to vary the value of C_{device}, which is the capac-

itance between the *G* and *S* terminals looking from the gate. Moreover, the p-substrate is grounded through a p^+ implantation contact that is usually done in practice to provide a common ground on the chip. In addition, none of the MOS varactors shown in Figure 2.3 have the *G* and *S* terminals connected to ground. Therefore, all MOS varactors have no terminal constraints with respect to the limitation of the application of bias voltages on the terminals.

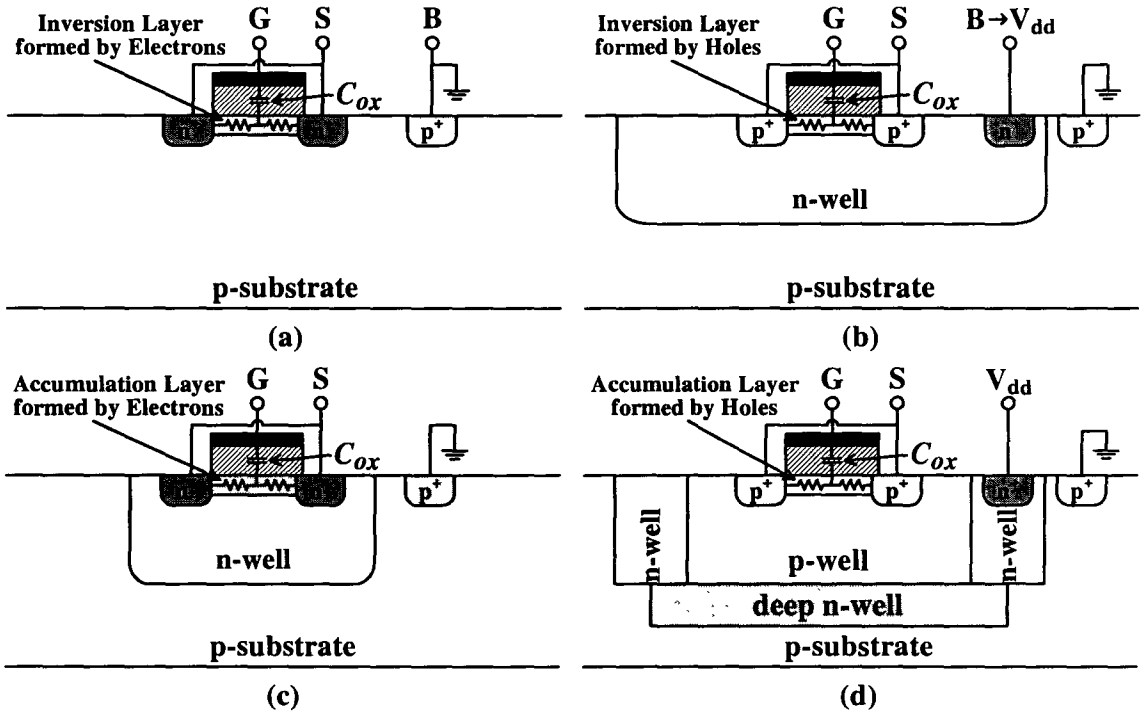


Figure 2.3 Illustration of cross-sections for four different types of MOS varactors available in standard CMOS technologies: (a) nIMOS in strong inversion mode, (b) pIMOS in strong inversion mode, (c) nAMOS in accumulation mode and (d) pAMOS in accumulation mode [14].

Depending on the type of MOS varactor, the operation mode changes between strong inversion and weak inversion or accumulation and weak inversion. In strong inversion and accumulation modes, many free carriers are accumulated at the surface of the semiconductor, whereas very few free carriers are accumulated in weak inversion mode.

Therefore, to compare the MOS varactors by estimating their expected relative Q_C using the relationship between Q_C and majority carriers discussed before, all four types of MOS varactors in Figure 2.3 are illustrated as they are operating in either strong inversion or accumulation mode. The C_{device} of a MOS varactor is approximately equal to the oxide capacitance C_{ox} in these two operation modes [14]. Therefore, only C_{ox} is shown in Figure 2.3 for these types of MOS varactors.

The first type of MOS varactor is the n-channel inversion mode MOS varactor (referred hereafter as the nIMOS varactor), which is shown in Figure 2.3(a) and whose cross-section is identical to a regular n-channel MOS (nMOS) transistor with the body B terminal (i.e. p-substrate) connected to ground. Its C_{device} varies from C_{max} to C_{min} when the operation mode is changed from strong inversion to weak inversion by adjusting the gate-source voltage V_{GS} from positive to negative values. The main inherent losses of an nIMOS varactor operating in the strong inversion mode are associated with the signal path formed by an inversion layer at the surface of the semiconductor, where electrons are the majority carriers. Therefore, nIMOS varactor operating in the strong inversion mode is expected to have a relatively high Q_C. The nIMOS varactor is not subject to any process constraints since all components used to create it, which is a regular nMOS transistor, are available in standard CMOS technologies [14].

The second type of MOS varactor, as shown in Figure 2.3(b), is the p-channel inversion mode MOS varactor (referred hereafter as the pIMOS varactor), whose cross-section is identical to a regular p-channel MOS (pMOS) transistor with the B terminal connected to V_{dd}. Its C_{device} changes from C_{min} to C_{max} when the operation mode is changed from weak inversion to strong inversion by adjusting the V_{GS} from positive to negative values. The main inherent losses of a pIMOS varactor operating in the strong inversion mode are associated with the signal path formed by an inversion layer at the surface of the semiconductor, where holes are the majority carriers. Therefore, pIMOS varactor is expected to have a Q_C lower than its n-channel counterpart, i.e. nIMOS varactor, when both of them are operating in strong inversion mode. The pIMOS varactor does not have any

process constraints since all components used to create a regular pMOS transistor are available in standard CMOS technologies [14].

The n-type accumulation mode MOS varactor (referred hereafter as the nAMOS varactor), as shown in Figure 2.3(c), is the third type of MOS varactor. Its C_{device} changes from C_{max} to C_{min} when the operation mode is changed from accumulation to weak inversion by adjusting the V_{GS} from positive to negative values. The main inherent losses of an nAMOS varactor operating in the accumulation mode are associated with the signal path formed by an accumulation layer at the surface of the semiconductor, where electrons are the majority carriers. Therefore, nAMOS varactor operating in the accumulation mode is expected to have a Q_C similar to an nIMOS varactor operating in the strong inversion mode, which is a relatively high Q_C. The nAMOS varactor is not subject to any process constraints since all components used to create it are available in standard CMOS technologies [14].

The fourth type of MOS varactor is the p-type accumulation mode MOS varactor (referred hereafter as the pAMOS varactor), which is shown in Figure 2.3(d). Its C_{device} changes from C_{min} to C_{max} when the operation mode is changed from weak inversion to accumulation by adjusting the V_{GS} from positive to negative values. The main inherent losses of a pAMOS varactor operating in the accumulation mode are associated with the signal path formed by an accumulation layer at the surface of the semiconductor, where holes are the majority carriers. Therefore, pAMOS varactor operating in the accumulation mode is expected to have a Q_C lower than its n-channel counterpart, i.e. nAMOS varactor, when both of them are operating in accumulation mode [24]. It should be noted that, similar to the n^+–to–p-well junction varactor, pAMOS varactor requires a triple-well process so that the p-well can be isolated from the p-substrate. Consequently, it has process constraints since triple-well process is not available in all standard CMOS technologies [14].

From the comparison discussed above, it can be concluded that both the nIMOS and nAMOS varactors are the best among all four types of MOS varactors that are available in standard CMOS technologies. They have the highest expected Q_C. Also, they have no

process or terminal constraints in standard CMOS technologies. However, previous experimental work [14], [39], [44] have shown that nAMOS varactors, in fact, have a Q_C higher than nIMOS varactors. As a result, nAMOS varactor is selected to be discussed and analyzed in detail later in this chapter.

2.1.3 p^+–to–n-well Junction Varactor

2.1.3.1 Cross-Section and Principle of Operation

The cross-section of a p^+–to–n-well junction varactor is shown in Figure 2.4, which is, in fact, the typical structure of pn junction varactor used in standard CMOS technologies [11], [12], [25]. It is implemented by putting a p^+ implantation in an n-well using an n^+ implantation as a contact with the p-substrate connected to ground through another p^+ implantation. For simplicity, the cross-section only shows the most important equivalent circuit elements – junction capacitance C_j, inherent series losses $R_{j,s}$ and inherent parallel losses $R_{j,p}$ – that are needed to describe its principle of operation.

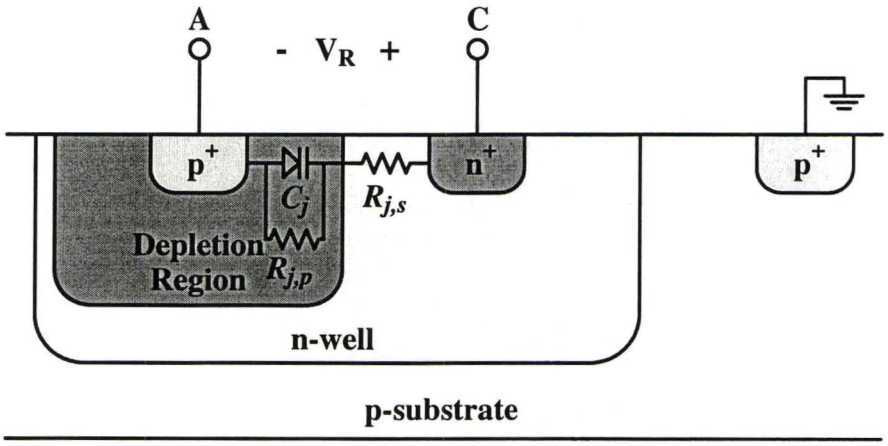


Figure 2.4 Illustration of cross-section for p^+–to–n-well junction varactor only showing junction capacitance C_j, inherent series losses $R_{j,s}$ and inherent parallel losses $R_{j,p}$ for describing the principle of operation [14].

A pn junction under reverse biasing is used as a varactor in integrated VCOs [11], [19], [21]–[24] since forward-biased pn junction has a non-desirable severe degradation of Q_C [14], [19], [36], [37], which will be discussed later in this chapter. Therefore, the operation of a p^+–to–n-well junction varactor is mainly based on the C_j associated with the depletion region between the p^+ implantation and the n-well. It should be noted that, as mentioned before, no depletion region is formed surrounding the n^+ implantation because the n^+ implantation is only a contact for the n-well. In principle, the C_j operates as a parallel plate capacitor. The depletion region is depleted of free carriers, and thus, behaves as an insulator, which forms the dielectric between the parallel plates. As a result, the C_j is a function of the width of the depletion region, which is controlled by the variable reverse bias voltage V_R that is applied between the anode A and cathode C terminals. If V_R increases (i.e. the pn junction is more reversely biased), more majority carrier holes and electrons are depleted in the p-region and n-region, respectively, which increases the width of the depletion region, and thus, decreases C_j. On the contrary, if V_R decreases, C_j increases as a consequence of decreasing the width of the depletion region [10], [15], [17], [45]–[47].

2.1.3.2 Qualitative Analysis of Capacitance Tuning Ratio

The dependence of C_j on V_R at a specific frequency is illustrated qualitatively in Figure 2.5. As mentioned in the previous subsection, C_j is a function of V_R and is given by

$$C_j(V_R) = \frac{C'_{j0}A_j}{\left(1+\frac{V_R}{\phi_{bi}}\right)^{m_j}}, \tag{2.19}$$

where C'_{j0} is the zero-biased junction capacitance per unit junction area A_j when $V_R = 0$ V, $\phi_{bi} = \phi_t \ln[(N_A N_D)/n_i^2]$ is the built-in voltage of an open-circuit pn junction, $\phi_t = (kT)/q$ is the thermal voltage, k is the Boltzmann's constant (1.38×10^{-23} JK^{-1}), T is the temperature in degrees Kelvin, N_A is the acceptor impurity concentration, N_D is the donor impurity concentration, n_i is the intrinsic carrier concentration and m_j is a constant depends on the abruptness of the junction [10], [15], [17], [45]–[47]. The typical values of m_j

for a linearly graded junction, an abrupt junction and a hyper-abrupt junction are 1/3, 1/2 and 2, respectively [10], [15], [45], [47]. Substituting Equation (2.19) into Equation (2.1), the capacitance tuning ratio for a pn junction varactor is

$$\frac{C_{max}}{C_{min}} = \frac{C_j(V_{R,min})}{C_j(V_{R,max})} = \left(\frac{\phi_{bi} + V_{R,max}}{\phi_{bi} + V_{R,min}}\right)^{m_j}. \tag{2.20}$$

It can be observed from Equation (2.20) that a large value of m_j is desired since it provides a larger capacitance tuning ratio. Therefore, the hyper-abrupt junction has the largest capacitance tuning ratio and the linearly graded junction has the smallest. In practice, however, the abruptness of the junction is usually unknown [10], [15], [45], [47]. Also, the capacitance tuning ratio in Equation (2.20) is only a theoretical value and the actual capacitance tuning ratio for a real pn junction varactor is smaller than the theoretical value due to fixed parasitic capacitances [14].

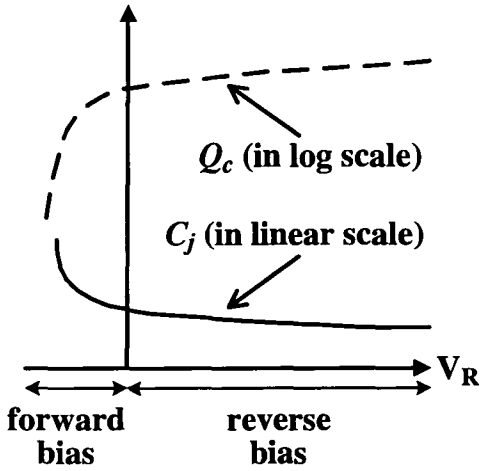


Figure 2.5 Qualitative behaviour of C_j and Q_C versus V_R of a p^+–to–n-well junction varactor at a specific frequency [37].

2.1.3.3 Qualitative Analysis of Quality Factor

The relationship between Q_C and V_R of a p^+–to–n-well junction varactor at a specific frequency is illustrated qualitatively in Figure 2.5. When the pn junction varactor is

reverse biased, the $R_{j,p}$ shown in Figure 2.4 is negligible and the main contribution to the inherent losses is $R_{j,s}$, which can be assumed to be voltage independent [14], [36], [37]. Therefore, the corresponding Q_C can be computed from Equation (2.7) and it only increases a little when V_R increases (i.e. the pn junction is more reversely biased) since C_j does not decrease much for a pn junction [36], [37], [47], as illustrated in Figure 2.5. However, the Q_C of a forward-biased pn junction varactor (i.e. when V_R is negative) is degraded severely due to the increased relative importance of the diffusion capacitance C_{diff} and its associated parallel diffusion resistance R_{diff} [14], [36], [37].

The C_{diff} is in parallel with the C_j when the pn junction is forwardly biased, which is given by

$$C_{diff} = \frac{\tau_T}{R_{diff}}, \tag{2.21}$$

where τ_T is the diode transit time and $R_{diff} = V_{thermal}/I_D$ in which $V_{thermal}$ is the thermal voltage and I_D is the pn diode forward bias current [14], [17], [45], [47]. Also, typically, C_{diff} and R_{diff} are much larger and smaller than C_j and $R_{j,p}$, respectively [45], [46]. Therefore, the total capacitance and total parallel resistance are approximately equal to C_{diff} and R_{diff}. In addition, the inherent series losses are negligible and the main contribution to the losses is the inherent parallel losses for a forward-biased pn junction [14], [36], [37]. As a result, the Q_C for a forward-biased pn junction varactor can be computed from Equation (2.10) as follows

$$Q_C \approx \omega C_{diff} R_{diff} = \omega \tau_T. \tag{2.22}$$

As an example, with a typical value of $\tau_T = 100$ ps [45], $Q_C \approx 1.26$ at 2 GHz. This confirms that forward biasing a pn junction varactor degrades the Q_C severely, which is illustrated in Figure 2.5.

2.1.4 n-type Accumulation Mode MOS Varactor

2.1.4.1 Cross-Section and Principle of Operation

An n-type accumulation mode MOS (nAMOS) varactor is, in fact, a modification of a regular pMOS transistor and only operates in the accumulation and depletion modes theoretically [14], [20], [24], [29], [42], [44]. To ensure its operation in strong, moderate and weak inversion modes is forbidden, any injection of holes in the channel must be inhibited [42]. This is achieved by replacing the two p^+ implantations (i.e. the source and drain) of a regular pMOS transistor with two n^+ implantations to obtain the contacts to the n-well, as shown in Figure 2.6.

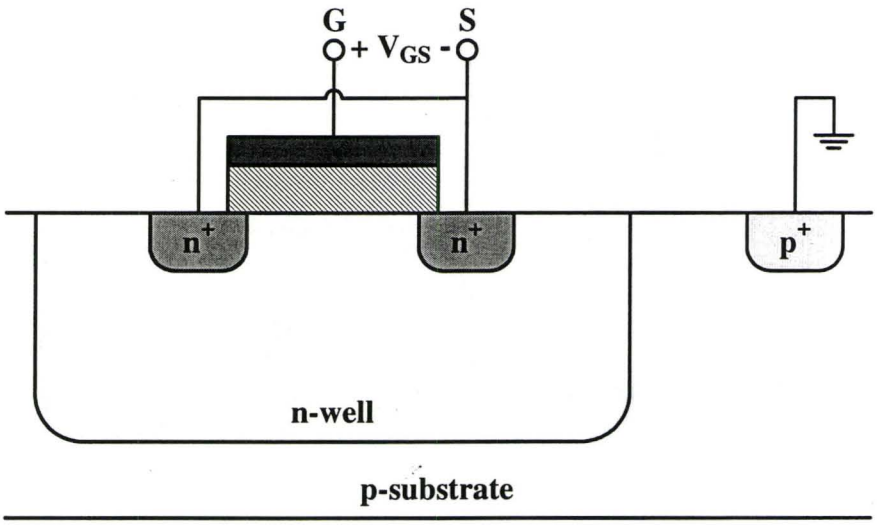


Figure 2.6 Illustration of cross-section for nAMOS varactor.

It is noteworthy that implementing a nAMOS varactor does not require any special or additional fabrication processes in a standard CMOS technology. Also, a variable bias voltage is applied between the gate *G* terminal and the connected drain-source *S* terminal to vary the value of C_{device}, which is the capacitance between the *G* and *S* terminals looking from the gate in this case. That is, a nAMOS varactor is a two terminal device whose operation mode, and thus, C_{device} can be changed by applying different gate-source voltage

V_{GS}. Moreover, the p-substrate is grounded through a p^+ implantation contact that is usually done in practice to provide a common ground on the chip.

Ideally, replacing the p^+ implantations with n^+ implantations in the source and drain of a regular pMOS transistor should suppress any injection of holes in the channel so that a nAMOS varactor only operates in the accumulation and depletion modes. However, in reality, nAMOS varactor does also work in the weak inversion mode, which will be discussed at the end of this subsection. Therefore, nAMOS varactor actually has three operation modes – accumulation, depletion and weak inversion – and their cross-sections are shown in Figure 2.7. For simplicity, the cross-sections in Figure 2.7 only show the most important equivalent circuit elements that are needed to describe the principle of operation.

Figure 2.7(a) shows a nAMOS varactor operating in the accumulation mode when the *G* terminal is biased positively with respect to the *S* terminal. Under this biasing condition, electrons are accumulated at the surface of the semiconductor and an accumulation layer is formed. This accumulation layer acts like a conduction plane at the bottom of the oxide since it is built by free carriers. Therefore, for a nAMOS varactor operating in the accumulation mode, this accumulation layer dominates the inherent losses and can be represented by parasitic resistance in accumulation mode R_{acc}. Also, the C_{device} is simply the oxide capacitance C_{ox}, which is equivalent to the C_{max} that a nAMOS varactor can achieve [44].

When the *G* terminal becomes negatively biased with respect to the *S* terminal, the nAMOS varactor operates in the depletion mode, which is shown in Figure 2.7(b). Electrons are pushed away from the surface of the semiconductor, and thus, a depletion region is formed at the surface of the semiconductor. This depletion region gets wider as the voltage applied to the *G* terminal becomes more negative [44]. Therefore, for a nAMOS varactor operating in the depletion mode, the parasitic resistance associated to the n-well in depletion mode R_d (between the edge of the depletion region and the edge of the n^+ implantations) represents the main inherent losses in the n-well. Also, the C_{device} is the C_{ox} in series with the voltage-dependent capacitance formed by the depletion region C_d [44].

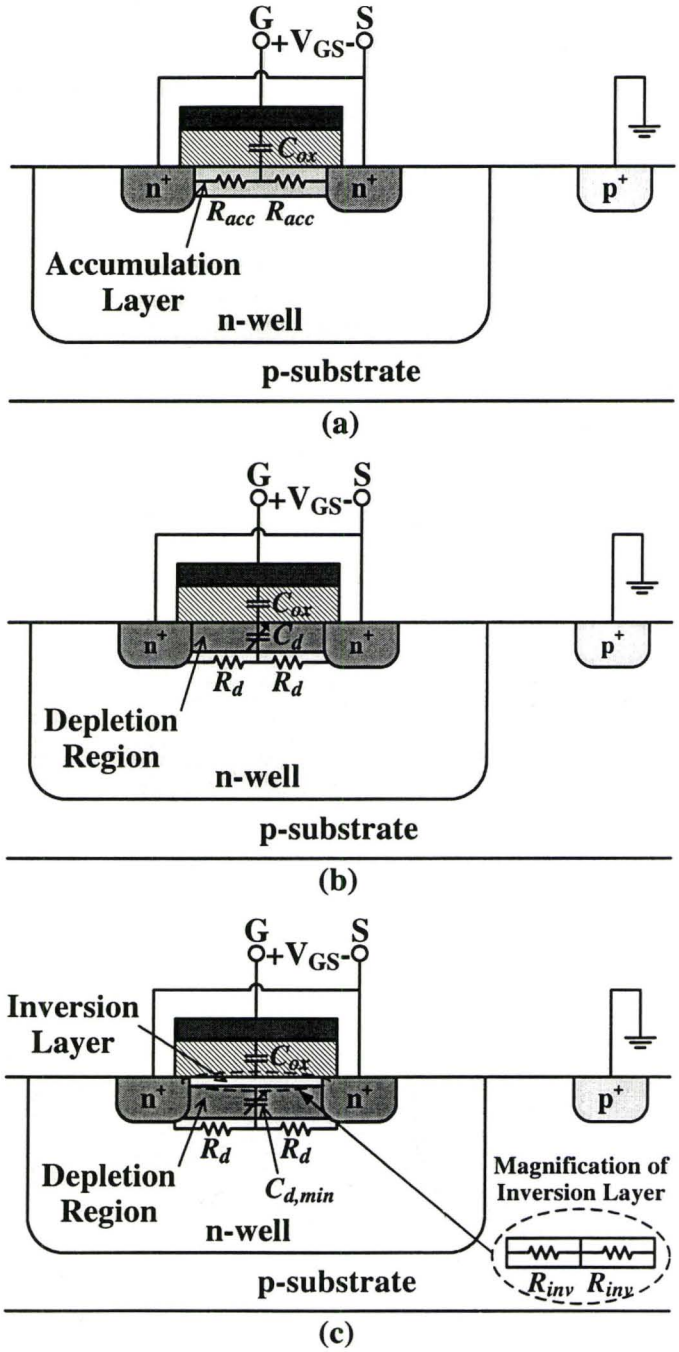


Figure 2.7 Illustration of cross-section for nAMOS varactor operates in (a) accumulation mode, (b) depletion mode and (c) weak inversion mode [13], [14].

As the voltage applied to the G terminal becomes further negative with respect to the S terminal such that $|-V_{GS}| \geq |V_T|$, where V_T is the threshold voltage of the device, the nAMOS varactor starts to operate in the weak inversion mode [44], which is shown in Figure 2.7(c). This is not expected since the idea of replacing the p^+ implantations of a regular pMOS transistor by n^+ implantations should able to inhibit the injection of holes from the p^+ implantations, which implies no abundance of holes can be accumulated at the surface of the semiconductor, and thus, no inversion layer should be formed. Consequently, nAMOS varactor should only operate in accumulation and depletion modes. In fact, this concept is correct. However, replacing the p^+ implantations by n^+ implantations and having the C_{device} adjustable by V_{GS} with the drain and source terminals connected together, the nAMOS varactor is essentially same as the two terminal MOS structure described in [15]. Therefore, at high frequencies, where the nAMOS varactor is supposed to be operated at, very few holes are generated by thermal generation at the surface of the semiconductor to fulfill the required charge changes due to the $-V_{GS}$ [15]. This is because thermal generation is a very slow process and there is no external provider, i.e. p^+ implantations in this case, to provide the required positive charge [15]. As a consequence, most of the required positive charges are generated by ionizing the donor atoms at the bottom of the depletion region to fulfill the required charge changes [15]. This phenomenon takes effect until enough holes are generated to form an inversion layer at the surface of the semiconductor by thermal generation, which shields the depletion region from getting wider since all electric fields are terminated on the inversion layer [13], [33]. When this happens, the C_d reaches its minimum value $C_{d,min}$, and thus, the nAMOS varactor reaches the C_{min} that it can achieve. Therefore, for a nAMOS varactor operating in the weak inversion mode at high frequencies, the parasitic resistances associated to the inversion layer R_{inv} and R_d represent the main inherent losses. Also, the C_{device} is the C_{ox} in series with the $C_{d,min}$ [13].

2.1.4.2 Qualitative Analysis of Capacitance Tuning Ratio

The capacitance tuning ratio for the nAMOS varactor is evaluated qualitatively in this subsection using the simplified equivalent circuit with only the capacitances including

the capacitance $C_{parasitic}$, which represents all extrinsic parasitic capacitances such as gate overlap capacitance, gate fringing capacitance and capacitances formed between the inter-connecting metal layers [29], [37]. As discussed in the previous subsection, the nAMOS varactor has three operation modes – accumulation, depletion and weak inversion – and its capacitance depends on the mode of operation, which is illustrated in Figure 2.8 at a specific frequency. Their simplified equivalent circuits are shown in Figure 2.9. It should be noted that the simplified equivalent circuit for the weak inversion mode operation is for high frequencies purpose since the nAMOS varactor is assumed to be used for high frequencies applications.

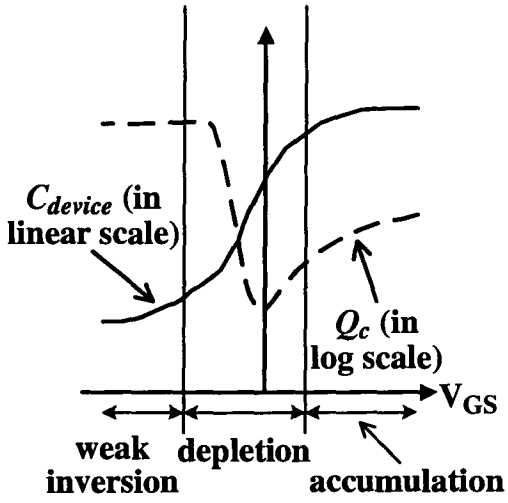


Figure 2.8 Qualitative behaviour of C_{device} and Q_C versus V_{GS} of nAMOS varactor at a specific frequency [37].

It can be seen from Figure 2.9 that the C_{max} and C_{min} are obtained when the nAMOS varactor is operating in the accumulation mode and weak inversion mode, respectively. In accumulation mode, C_{max} is derived from Figure 2.9(a) as [14]

$$C_{max} = C_{parasitic} + C_{ox}. \tag{2.23}$$

To derive C_{min}, the simplified equivalent circuit in Figure 2.9(c) is used and gives [14]

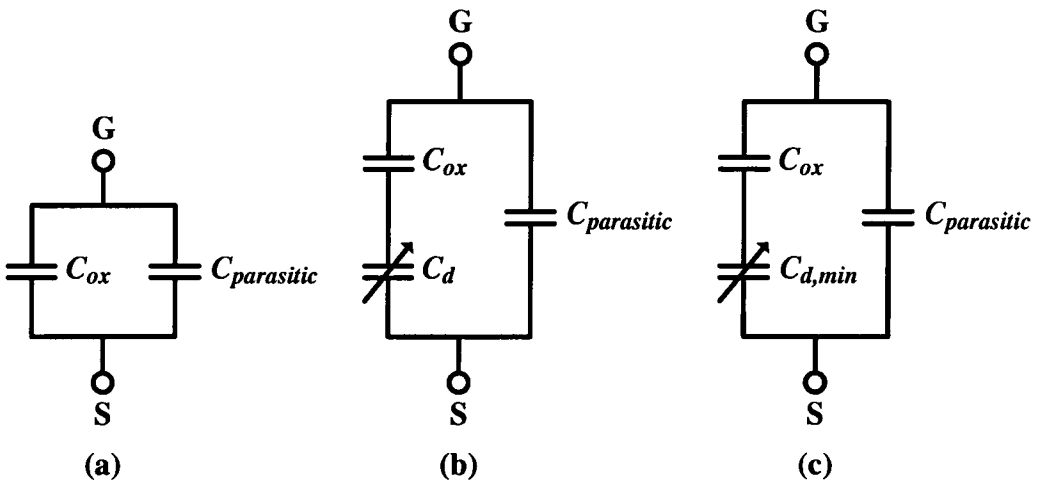


Figure 2.9 Simplified equivalent circuit showing only capacitances for nAMOS varactor operates in (a) accumulation mode, (b) depletion mode and (c) weak inversion mode at high frequencies [13].

$$C_{min} = C_{parasitic} + \frac{C_{ox}C_{d,min}}{C_{ox} + C_{d,min}}. \tag{2.24}$$

Therefore, the capacitance tuning ratio for a nAMOS varactor approaches one as $C_{parasitic}$ becomes infinite by inspecting Equations (2.23) and (2.24), which is not desired. As a result, to obtain the maximum capacitance tuning ratio for a nAMOS varactor, $C_{parasitic}$ must be minimized, or equivalently, the ratio of device intrinsic capacitance and extrinsic parasitic capacitances must be maximized. To maximize this ratio for a specified nominal capacitance value, the nAMOS varactor should be implemented by a long, wide and single-fingered gate so that the extrinsic parasitic capacitances formed between the interconnecting metal layers can be minimized [27], [33], [41].

2.1.4.3 Qualitative Analysis of Quality Factor

From Figure 2.7, it can be seen that all the parasitic components between the *G* and *S* terminals are in series connection. Therefore, the Q_C of a nAMOS varactor can be computed by Equation (2.7), which is repeated here for convenience:

$$Q_{C,s} \approx \frac{1}{\omega C_s R_s}. \tag{2.25}$$

C_s, in this case, is the series parasitic capacitance including the C_{ox} and C_d and can be expressed as

$$C_s(V_{GS}) \propto L_g W_g n_f (C'_{ox} \parallel C'_d(V_{GS})), \tag{2.26}$$

where L_g is the gate length, W_g is the gate width, n_f is the number of gate fingers, C'_{ox} is the oxide capacitance per unit area and C'_d is the depletion capacitance per unit area. As for R_s, it is the series parasitic resistance mainly contributed by the gate resistance R_g in series with the channel resistance R_{ch} given by

$$R_s(V_{GS}) = \frac{1}{n_f}\left(\frac{R_g}{n_1}\frac{W_g}{L_g} + \frac{R_{ch}(V_{GS})}{n_2}\frac{L_g}{W_g}\right), \tag{2.27}$$

where n_1 and n_2 are the non-ideal factors characterizing the distributed effect and the number of contacts of a MOS structure device for R_g and R_{ch}, respectively [13], [15], [48]. It should be noted that, in fact, C'_d and R_{ch} and thus correspondingly C_s and R_s are functions of V_{GS} since they are different in each operation mode. Also, if the gate is contacted on both sides and multifingers are utilized on the layout, which is an usual practice in radio-frequency (RF) designs, R_g is negligible and R_{ch} dominates R_s [13], [33]. Therefore, solving Equations (2.25), (2.26) and (2.27) gives the relationship [13]

$$Q_C \propto L_g^{-2}. \tag{2.28}$$

Consequently, minimizing L_g for a nAMOS varactor will maximize Q_C. However, this contradicts the condition required for maximizing the capacitance tuning ratio as discussed in the previous subsection. Therefore, there is a direct trade-off between the capacitance tuning ratio and Q_C for nAMOS varactor.

The dependence of Q_C on V_{GS} of a nAMOS varactor at a specific frequency is illustrated qualitatively in Figure 2.8. When a nAMOS varactor operates in the accumulation

mode, the R_{ch} is represented by R_{acc}, which is highly conductive, and thus, the Q_C is high [13]. As the operation shifts from accumulation to depletion, the accumulation layer is vanishing and the bottom plate of the C_{device} is formed in the n-well, whose resistance is relatively high. Therefore, the R_{ch}, represented by R_d, increases and thus Q_C drops [13], [36], [37]. When the operation of nAMOS varactor shifts from depletion to weak inversion, Q_C increases instead of decreases despite the continuous increase in R_{ch} until an inversion layer is formed at the surface of the semiconductor, which shields the depletion region from getting wider. This unexpected phenomenon happens because the C_{device} decreases at a faster rate than the increase in R_{ch} due to the high varactor sensitivity (i.e. the rate of changes of C_{device} to the rate of changes of V_{GS}) and thus the overall Q_C increases, which produces a dip in the Q_C curve in Figure 2.8 [13], [36], [37]. In addition, C_{device} is small enough in the weak inversion mode such that Q_C in the weak inversion mode is higher than in the accumulation mode [13]. Also, Q_C is approximately constant in the weak inversion mode since both C_{device} and R_{ch} approach a constant value in this operation mode [28], [34].

2.1.5 Performance Comparison

The capacitance tuning ratio and Q_C of different types of CMOS varactors from the published literature are listed and compared in Table 2.1 to provide an idea of the values of these two performance parameters in recent technology generations. These varactors were originally implemented in different standard CMOS technologies and measured at different frequencies ranging from 1 GHz to 2.5 GHz and different tuning voltage ranges. Therefore, to have a fair comparison, first, all related information are converted to 2 GHz, which is a frequency between two important wireless communication systems: 1.9 GHz Global System for Mobile Communications (GSM) in Canada [49] and 2.4 GHz Bluetooth [50]. The C_{max} and C_{min} that are used to compute the capacitance tuning ratio, in fact, are assumed to be constant over the frequency ranging from 1 GHz to 2.5 GHz, i.e. the capacitance tuning ratio values listed in Table 2.1 are collected from the references directly without any modification. However, the Q_C has to be adjusted since it is strongly frequency dependent and Equation (2.25) can be used for the conversion. For example, converting a published

Q_C at 1 GHz to 2 GHz can be simply achieved by dividing the published Q_C by a factor of two. In addition, the minimum quality factor of varactor $Q_{C,min}$ is listed in Table 2.1 but not other values of Q_C because $Q_{C,min}$ is the worst Q_C that the varactor can have, which is the best Q_C value used as a limiting factor and starting point for circuit design or to indicate if the varactor is able to fulfill the minimum requirement of a circuit for design specifications.

Table 2.1 Comparison of capacitance tuning ratio and $Q_{C,min}$ for different types of CMOS varactors.

Reference	Varactor Type	CMOS Technology (μm)	Tuning Voltage (V)	C_{max}/C_{min} Ratio	$Q_{C,min}$
[37] 2000	p^+–to–n-well junction	0.5	V_R = [0, 1.8]	1.31	110
[37] 2000	pIMOS	0.5 (L_g = 0.5 μm)	V_{GS} = [-1.6, 0.2]	1.74	19
[37] 2000		0.5 (L_g = 1 μm)	V_{GS} = [-1.6, 0.2]	2.01	3.4
[44] 2000	nIMOS	0.5	V_{GS} = [0.5, 2.3]	2.15	25.8
[37] 2000	nAMOS	0.5 (L_g = 0.5 μm)	V_{GS} = [-1, 0.8]	2.07	51
[37] 2000		0.5 (L_g = 1 μm)	V_{GS} = [-1, 0.8]	2.76	10.5
[44] 2000		0.5	V_{GS} = [0.5, 2.3]	1.69	33.2

Second, a common tuning voltage range of 1.8 V is used to obtain the C_{max} and C_{min} values to compute the capacitance tuning ratio for each varactor. This 1.8 V is based on Lithium ion (Li^+) batteries that are the most common power supply for wireless applications nowadays and the common minimum operating voltage for Li^+ batteries are 3 V [14]. In fact, only 2.8 V of this 3 V is used as power supply since there is a 0.2 V voltage drop for the voltage regulator [14]. Also, with a typical tuning voltage margin of 0.5 V for both the power supply and ground, the actual usable tuning voltage range is from 0.5 V to 2.3 V, i.e a tuning voltage range of 1.8 V [14]. The absolute voltages used for the 1.8 V tuning voltage range, however, depend on the type of varactor and they are also shown in Table 2.1.

Most of the capacitance tuning ratio and $Q_{C,min}$ values listed in Table 2.1 are determined from plots reported in the corresponding literature. Some of the values, therefore,

may be reproduced with small error. However, again, the main purpose of presenting Table 2.1 is to give a general idea of the values of these two performance parameters in recent technology generations, and thus, small inaccuracy is acceptable.

Several observations can be made from Table 2.1:

1. p^+–to–n-well junction varactor has smaller capacitance tuning ratio but much larger $Q_{C,min}$ than MOS varactors.
2. pIMOS varactor has smaller $Q_{C,min}$ than nAMOS as estimated in Section 2.1.2.2 by comparing rows 2 and 3 with rows 5 and 6, respectively, in Table 2.1.
3. nIMOS varactor has smaller $Q_{C,min}$ than nAMOS as mentioned in Section 2.1.2.2 by comparing row 4 with row 7 in Table 2.1.

2.2 METAL-INSULATOR-METAL CAPACITOR

Capacitors can also be realized in ICs using the traditional structure, i.e. parallel-plate capacitors with an insulating material called the dielectric between these two conductive plates [6]. This type of capacitor is called metal-insulator-metal capacitor or commonly known as MIM capacitor. The MIM capacitor is usually implemented using one of the conventional metal layers as the bottom plate and a special thin metal layer placed between two conventional metal layers as the top plate with a thin oxide of approximately 40 nm thick [51] between them as the dielectric [6].

The capacitance value of a MIM capacitor C_{MIM} can be computed by

$$C_{MIM} = \frac{A_p \varepsilon_0 \varepsilon_i}{t_i}, \tag{2.29}$$

where A_p is the area of one of the plates, ε_0 is the permittivity in vacuum, ε_i and t_i are the relative permittivity and thickness of the dielectric, respectively [6]. It can be observed from Equation (2.29) that the smaller the t_i, the larger the C_{MIM} and thus a thin oxide is used as the dielectric for MIM capacitor to increase the capacitance value per area, which saves

chip space [9]. In reality, however, the C_{MIM} is underestimated by Equation (2.29) since some of the electric fields called the fringing field go through the air instead of the dielectric, which increases the apparent area of the plates and this problem is proportional to the thickness of the dielectric [6]. Fortunately, for a MIM capacitor, a thin oxide is used as its dielectric and the dimensions of its plates are usually much larger than its vertical dimension [6]. Therefore, this problem is usually neglected in ICs design.

Figure 2.10 shows the equivalent circuit model of a MIM capacitor between Port 1 and Port 2 used in the Spectre simulator for the TSMC 0.18 μm CMOS technology [51]. In this model, $R_{MIM,s}$ and $L_{MIM,s}$ are the parasitic resistance and inductance in the electrodes, $C_{MIM,ox}$, is the oxide capacitance between the bottom plate of the MIM capacitor and the substrate, and $R_{MIM,sub}$ and $C_{MIM,sub}$ are the silicon substrate resistance and capacitance, respectively [51].

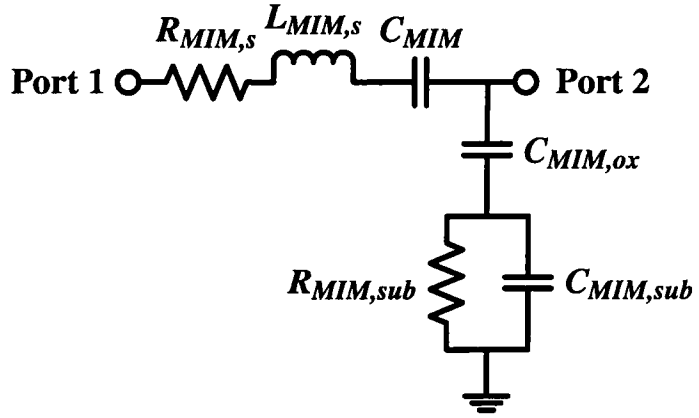


Figure 2.10 Equivalent circuit model of a MIM capacitor between Port 1 and Port 2 used in the Spectre simulator for the TSMC 0.18 μm CMOS technology [51].

The capacitance tuning ratio of a MIM capacitor is, obviously, one since C_{MIM} is voltage independent. Its Q_C is usually larger than 150 at 2 GHz [51], which is even larger than the $Q_{C,min}$ of a p^+–to–n-well junction varactor presented in Table 2.1, using the conversion method discussed in Section 2.1.5.

2.3 INDUCTOR

In standard CMOS technology, spiral inductors are the most widely used integrated on-chip inductors. Spiral inductor, as suggested by the name, is implemented by spiral-shaped planar metal coils using one or more metal layers. An example of a 1.5 turns rectangular planar spiral inductor realized by one metal layer with the key device geometrical parameters is shown in Figure 2.11, where L_1, L_2, L_3 and L_n are the length of the first, second, third and last segments, respectively, W_L is the conductor width and S_L is the spacing between two adjacent segments [52]. The additional segment is realized by a different metal layer, which is required for connecting the inductor at Port 2.

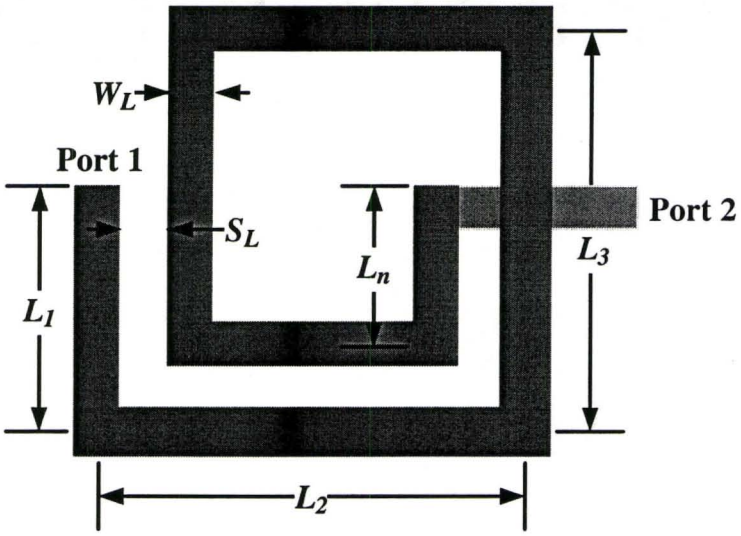


Figure 2.11 Illustration of a 1.5 turns rectangular planar spiral inductor realized by one metal layer with key device geometrical parameters [52]. The additional segment is realized by a different metal layer, which is required for connecting the inductor at Port 2.

The objective of designing the layout of a spiral inductor is to obtain the desired inductance in the smallest area possible. At the same time, the parasitic capacitance must be kept low to ensure the designed frequency band is inside the f_{SR} of the element so that it will not affect the operation of the LC oscillator [52]. Another objective in the design of a spiral inductor is to maximize its quality factor Q_L, which is the most important perform-

ance parameter of spiral inductor, for the frequency range at which the inductor will operate [52]. These objectives can be achieved by adjusting the geometrical parameters and the number of turns to implement the spiral inductor [52]. Further discussion regarding the optimization of the Q_L and the corresponding changes of the inductance with respect to the geometrical parameters and the number of turns can be found in [53], [54].

Q_L is defined as [53]

$$Q_L \equiv 2\pi \frac{|\text{maximum stored inductive energy} - \text{maximum stored capacitive energy}|}{\text{energy dissipated per cycle}} . \quad (2.30)$$

Similar to Q_C, from Equation (2.30), Q_L is a relative measure of the inherent losses of the inductor, which should be as small as possible. As a consequence, a good performance inductor should have Q_L as high as possible since the inherent losses are presented in the denominator in Equation (2.30).

Physically, an on-chip inductor is a two-port element, which is shown in Figure 2.12(a). In this model, $L_{L,s}$ is the inductance of the spiral inductor, $R_{L,s}$ is the metal series resistance representing the energy losses due to skin effect in the spiral interconnect structure and the induced eddy current in any conductive media close to the inductor, $C_{L,s}$ is the series capacitance representing the capacitance due to the overlap between the spiral and the center-tap underpass, $C_{L,ox}$ is the oxide capacitance between the spiral and the substrate, and $R_{L,sub}$ and $C_{L,sub}$ are the silicon substrate resistance and capacitance, respectively [52], [53]. However, to simplify the analysis without sacrificing the inductor characteristics, a one-port physical model is used. This lumped one-port physical model is derived from the two-port model by connecting the Port 2 to ground [53], which is shown in Figure 2.12(b). To further simplify this one-port model, the impedance $C_{L,ox}$, $R_{L,sub}$ and $C_{L,sub}$ can be replaced by a resistance-capacitance (RC) parallel network [53], which is shown in Figure 2.12(c), where

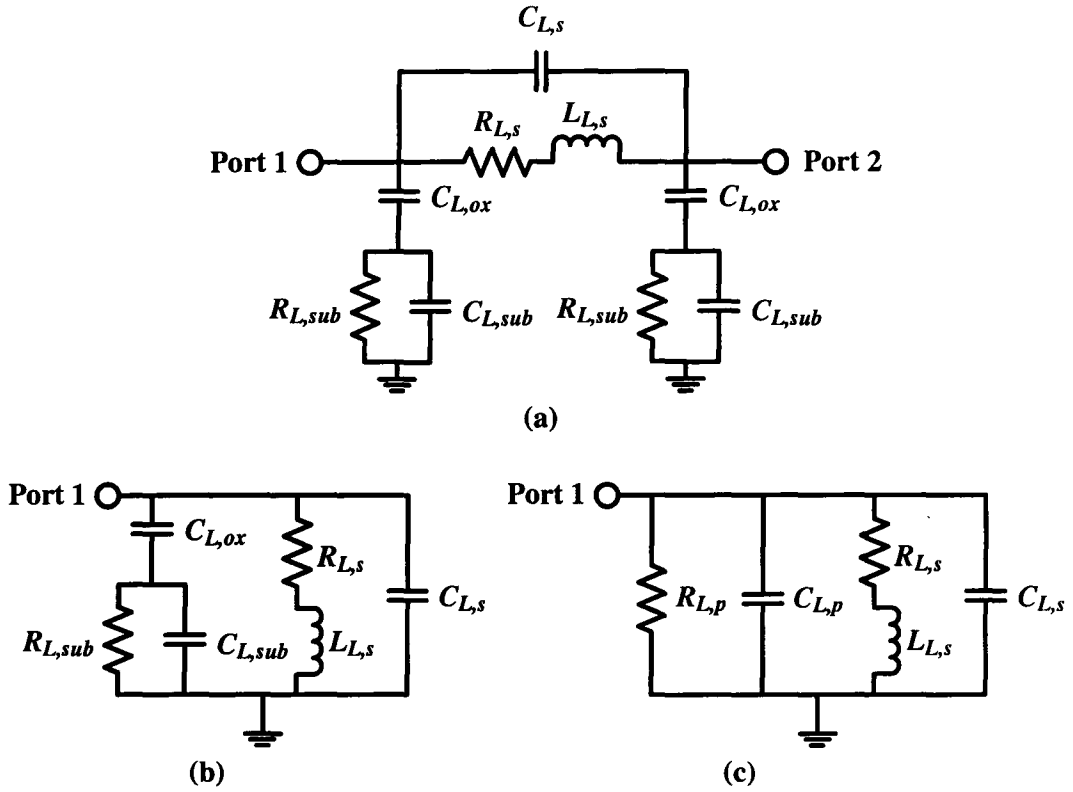


Figure 2.12 Lumped physical model of a spiral inductor: (a) two-port [52], (b) one-port full version [53] and (c) one-port simplified substrate version [53].

$$R_{L,p} = \frac{1}{\omega^2 C_{L,ox}^2 R_{L,sub}} + \frac{R_{L,sub}(C_{L,ox} + C_{L,sub})^2}{C_{L,ox}^2} \tag{2.31}$$

and

$$C_{L,p} = C_{L,ox}\frac{1 + \omega^2(C_{L,ox} + C_{L,sub})C_{L,sub}R_{L,sub}^2}{1 + \omega^2(C_{L,ox} + C_{L,sub})^2 R_{L,sub}^2}. \tag{2.32}$$

Using the circuit element in Figure 2.12(c), the maximum stored inductive energy $E_{L,max}$, maximum stored capacitive energy $E_{C,max}$ and energy dissipated per cycle E_{dis} are

$$E_{L,max} = \frac{V_{L,peak}^2 L_{L,s}}{2[(\omega L_{L,s})^2 + R_{L,s}^2]}, \tag{2.33}$$

$$E_{C,max} = \frac{V_{L,peak}^2 (C_{L,s} + C_{L,p})}{2}, \tag{2.34}$$

and

$$E_{dis} = \frac{2\pi}{\omega} \frac{V_{L,peak}^2}{2} \left[\frac{1}{R_{L,p}} + \frac{R_{L,s}}{(\omega L_{L,s})^2 + R_{L,s}^2} \right], \tag{2.35}$$

respectively, where $V_{L,peak}$ is the peak voltage across the spiral inductor [53]. The analytic expression of Q_L can be obtained by substituting Equations (2.33) to (2.35) into Equation (2.30), which yields

$$Q_L = \frac{\omega L_{L,s}}{R_{L,s}} \cdot \frac{R_{L,p}}{R_{L,p} + [(\omega L_{L,s}/R_{L,s})^2 + 1] R_{L,s}} \cdot \left[1 - \frac{R_{L,s}^2 (C_{L,s} + C_{L,p})}{L_{L,s}} - \omega^2 L_{L,s} (C_{L,s} + C_{L,p}) \right], \tag{2.36}$$

where the first term is the magnetic energy stored and the ohmic loss in the spiral inductor, the second term is the substrate loss factor representing the energy dissipated in the substrate, and the last term is the self-resonance factor describing the reduction in Q_L due to the increase in the peak electric energy with frequency and the vanishing of Q_L at the f_{SR} [53].

In practice, for quick circuit design and analysis, an approximate analytical expression of Q_L is preferred rather than the accurate but complicate analytical expression shown in Equation (2.36). Similar to the varactor, an approximate analytical expression of Q_L can be obtained from a simplified equivalent circuit using resistor and fixed inductor as the inherent losses and ideal spiral inductor, respectively, as shown in Figure 2.13. It can be seen

from Figure 2.13 that the resistor and fixed inductor can be connected to each other in either series or parallel.

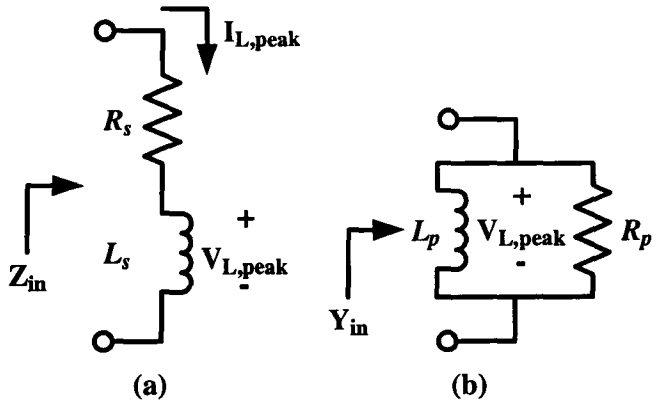


Figure 2.13 Simplified equivalent circuit for a spiral inductor with resistor and fixed inductor representing the inherent losses and ideal spiral inductor, respectively, connected in either (a) series or (b) parallel.

As mentioned earlier, one objective of designing the layout of a spiral inductor is to ensure the designed frequency band is inside the f_{SR} of the element [52]. When a spiral inductor is operating far below the f_{SR}, the stored capacitive energy is negligible, and thus, Equation (2.30) becomes

$$Q_L \approx 2\pi \frac{|\text{maximum stored inductive energy}|}{\text{energy dissipated per cycle}} = 2\pi \frac{|E_{L,max}|}{E_{dis}}, \tag{2.37}$$

where

$$E_{L,max} = \frac{1}{2} L I_{L,peak}^2 \tag{2.38}$$

in which $I_{L,peak}$ is the peak current flowing through the whole series connection causing $V_{L,peak}$ across the fixed inductor.

For the equivalent circuit connected in series as shown in Figure 2.13(a), the $E_{L,max}$ is given by Equation (2.38) and

$$E_{dis} = \frac{I_{L,peak}^2 R_s}{2} T_{period} = \frac{I_{L,peak}^2 R_s}{2} \frac{1}{f}. \tag{2.39}$$

Therefore, the quality factor of an inductor using the series equivalent circuit $Q_{L,s}$ can be found by substituting Equations (2.38) and (2.39) into Equation (2.37) with L replaced by the fixed inductor representing the ideal spiral inductor in a series equivalent circuit L_s, which gives

$$Q_{L,s} \approx 2\pi \frac{\left|\frac{1}{2} L_s I_{L,peak}^2\right|}{\frac{I_{L,peak}^2 R_s}{2} \frac{1}{f}} = \frac{\omega L_s}{R_s}. \tag{2.40}$$

In fact, $Q_{L,s}$ can also be derived directly from the input impedance Z_{in} of the series equivalent circuit as shown in Figure 2.13(a) as follows:

$$Q_{L,s} = \frac{|Im(Z_{in})|}{Re(Z_{in})} = \frac{\omega L_s}{R_s}, \tag{2.41}$$

which gives the same expression as in Equation (2.40).

Similarly, for the equivalent circuit connected in parallel as shown in Figure 2.13(b),

$$E_{L,max} = \frac{1}{2} L_p I_{L,peak}^2 = \frac{1}{2} L_p \left(\frac{V_{L,peak}}{j\omega L_p}\right)^2 \tag{2.42}$$

and

$$E_{dis} = \frac{V_{L,peak}^2}{2R_p} T_{period} = \frac{V_{L,peak}^2}{2R_p} \frac{1}{f}, \tag{2.43}$$

where L_p is fixed inductor representing the ideal spiral inductor using parallel equivalent circuit. By substituting Equations (2.42) and (2.43) into Equation (2.37), the quality factor of an inductor using the parallel equivalent circuit $Q_{L,p}$ is

$$Q_{L,p} \approx 2\pi \frac{\left|\frac{1}{2}L_p\left(\frac{V_{L,peak}}{j\omega L_p}\right)^2\right|}{\frac{V_{L,peak}^2}{2R_p}\frac{1}{f}} = \frac{R_p}{\omega L_p}. \tag{2.44}$$

Also, similar to the series equivalent circuit, $Q_{L,p}$ can be obtained directly from the input admittance Y_{in} of the parallel equivalent circuit as shown in Figure 2.13(b) as follows:

$$Q_{L,p} = \frac{|Im(Y_{in})|}{Re(Y_{in})} = \frac{|-1/(\omega L_p)|}{1/R_p} = \frac{R_p}{\omega L_p}, \tag{2.45}$$

which gives the same expression as in Equation (2.44).

The inductance, maximum quality factor of inductor $Q_{L,max}$ and f_{SR} of different spiral inductors from the published literature are listed and compared in Table 2.2 to provide an idea of the values of these performance parameters in recent technology generations. It should be noted that the $Q_{L,max}$ is usually reported in literature, which is in contrast to Q_C where $Q_{C,min}$ is reported. This is because $Q_{L,max}$ is ranging from approximately 3.7 [55] to 15 [56] at 2 GHz, which is much smaller than the quality factor of other passive devices, and thus, it is usually used as a constraint and starting point for circuit design in practice [57]–[59]. Also, some of the $Q_{L,max}$ and f_{SR} values listed in Table 2.2 are determined from plots reported in the corresponding literature. In the cases which f_{SR} is not shown on the plots, the Q_L versus frequency plot is used to determine the f_{SR}. This is achieved by extrapolating the Q_L curve and the f_{SR} is the frequency at which the Q_L is zero. The values, therefore, may be reproduced with small error. However, again, the main purpose of presenting Table 2.2 is to give a general idea of the values of these two performance parameters in recent technology generations, and thus, small inaccuracy is acceptable.

Table 2.2 Comparison of inductance, $Q_{L,max}$ and f_{SR} for different spiral inductors.

Reference	Structure of Spiral Inductor	CMOS Technology (μm)	Inductance (nH)	$Q_{L,max}$	f_{SR} (GHz)
[55] 2000	rectangular shape using only top metal layer	0.35	not reported	3.5 @ 2.5 GHz	4.2
[55] 2000	rectangular shape using top metal layer with bottom metal patterned ground shield	0.35	not reported	3.7 @ 2 GHz	4.7
[53] 1998	rectangular shape using 2 μm-thick aluminum and silicon substrate of 11 Ωcm	not reported	7.5 @ 1.3 GHz	6 @ 1.3 GHz	6.8
[53] 1998	rectangular shape using 2 μm-thick aluminum and silicon substrate of 11 Ωcm with polysilicon patterned ground shield	not reported	7.4 @ 1.5 GHz	7.2 @ 1.5 GHz	3.6
[60] 2001	circular shape using top two metal layers with special passivation scheme	0.25	2.42 @ 3 GHz	9.6 @ 3 GHz	12.7
[61] 2002	circular shape using top two metal layers with polysilicon patterned ground shield	0.18	6.05 @ 3 GHz	13 @ 3 GHz	7
[56] 2001	circular shape using four parallel current paths with polysilicon patterned ground shield	0.18	5 @ 2 GHz	15 @ 2 GHz	4.2

Chapter 3

LC Oscillator

A major challenge in the design of single-chip transceivers in CMOS technology for today's wireless communication systems is the design of a VCO that generates the local oscillator (LO) carrier signal. Cross-coupled differential LC oscillators are the most popular choice due to their relatively low phase noise, ease of implementation and differential operation [62]. Therefore, in this chapter, the theory of LC oscillators will be reviewed, and the performance parameters used to evaluate VCOs will be presented. Finally, different cross-coupled differential LC oscillator topologies will be discussed and compared.

3.1 LC OSCILLATOR THEORY

All resonator-based LC oscillators can be represented by a simple two-port positive feedback linear time invariant (LTI) circuit in the s-domain as shown in Figure 3.1(a) [63]. This positive feedback LTI circuit can be described by the transfer function

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 - G(s)H(s)}, \tag{3.1}$$

where $G(s)$ is the feedforward network or open-loop transfer function, $H(s)$ is the feedback network's transfer function, $X(s)$ is the input signal which is the noise from the circuit components, $Y(s)$ is the output signal and $Y(s)/X(s)$ is the closed-loop transfer function [64], [65]. If a positive feedback LTI circuit satisfies the Barkhausen criteria:

$$G(s)H(s) = 1 \tag{3.2}$$

and

$$\angle G(s)H(s) = n \cdot 360°, \tag{3.3}$$

where n is an integer, then the circuit may oscillate at the fundamental angular oscillation frequency ω_0 [65]. To ensure oscillation in the presence of temperature and process variations, the oscillator is typically designed to have a loop gain, i.e. $G(s)H(s)$, greater than one and the nonlinearities in the circuit are amplified to reduce the loop gain to exactly one in steady-state operation [65].

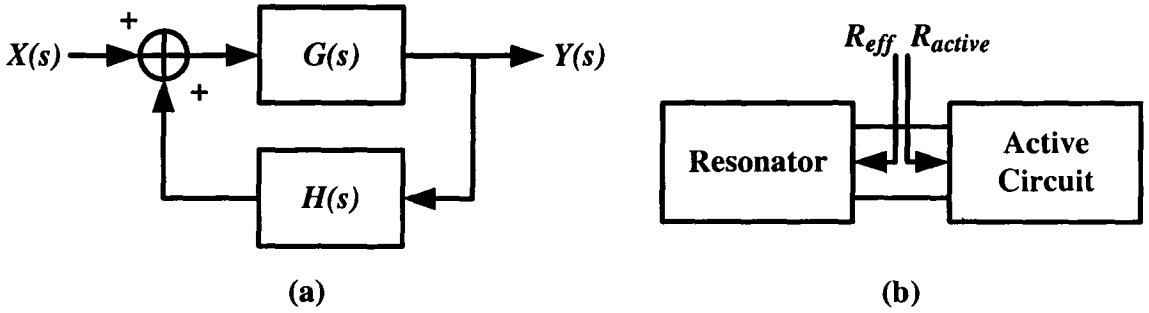


Figure 3.1 Representation of resonator-based LC oscillators using (a) two-port model and (b) two one-port model [63], [65], [66].

An alternate way to represent LC oscillators is to use two one-port networks: an active circuit and a resonator as shown in Figure 3.1(b) [65], [66]. The resonator network, for LC oscillators, is made up of a parallel resistance-inductance-capacitance (RLC) network or commonly known as LC tank [65], [67]. The active circuit network is a simple transconductance g_m amplifier that implements gain or negative resistance R_{active} to compensate for the losses of the effective parallel resistance in the resonator network R_{eff} [67]. To ensure oscillation in steady-state operation, R_{active} must exactly cancel R_{eff}. When this happens, the circuit becomes lossless, which results in oscillation [66]. Due to this representation, LC oscillators are also known as negative resistance oscillators and this representation will be utilized for the oscillator analysis and design in this research.

3.2 PERFORMANCE PARAMETERS

To understand the properties of different cross-coupled differential LC oscillators, it is essential to know what performance parameters are used to determine their properties.

The most important performance parameters used for evaluating LC oscillators are oscillation frequency f_0, frequency tuning range, power consumption P_{con}, amplitude of oscillation V_{osc} or output power P_{out}, and phase noise $L\{\Delta\omega\}$, which are presented and discussed in the following subsections.

3.2.1 Oscillation Frequency

The oscillation frequency f_0 of resonator-based LC oscillators is determined by the resonant frequency of the resonator, i.e. the LC tank:

$$f_0 = \frac{1}{2\pi\sqrt{L_{tk}C_{tk}}}, \tag{3.4}$$

where L_{tk} and C_{tk} are the total inductance and total capacitance in the LC tank, respectively. Ideally, the C_{tk} is same as the value of the capacitor that is used to build the LC tank. However, there are some parasitic capacitances from the inductor, metal interconnections in the circuit and active circuit network, which also contribute to the C_{tk}. The parasitic capacitances from the active circuit network are the parasitic gate-source capacitance C_{gs} and parasitic gate-drain capacitance C_{gd} of the MOSFETs that are used to form the active circuit network. Therefore, a more precise expression of Equation (3.4) is

$$f_0 = \frac{1}{2\pi\sqrt{L_{tk}(C_{cap} + C_{parasitic})}}, \tag{3.5}$$

where C_{cap} is the value of the capacitor that is used to build the LC tank and $C_{parasitic}$ is the equivalent parallel capacitance formed by all parasitic capacitances.

3.2.2 Frequency Tuning Range

The actual values of the L_{tk} and C_{tk}, in practice, are usually different from their nominal values due to process variation. As a consequence, from Equation (3.5), the actual f_0 is different from the nominal f_0. Therefore, the spread in the L_{tk} and C_{tk} must be compensated electronically to ensure the nominal f_0 can be achieved. As discussed in Section

2.3, spiral inductors are the most widely used integrated on-chip inductors, which are also the inductors used in this research, and their inductance values are fixed after fabrication. Therefore, varactors are used to provide an electronically tunable C_{cap} to ensure the nominal f_0 can be achieved, and thus, LC oscillators are also known as VCOs when varactors are utilized in the LC tank since the circuit performance, including the f_0, is adjusted only by the voltage sources that are used to bias the circuit.

The frequency tuning range of VCOs is a range of frequencies that they can cover and often is defined as

$$\text{Frequency Tuning Range} \equiv \frac{f_{max} - f_{min}}{f_{centre}} = 2\left(\frac{f_{max} - f_{min}}{f_{max} + f_{min}}\right), \tag{3.6}$$

where f_{max}, f_{min} and f_{centre} are the maximum, minimum and centre frequencies that the VCOs can achieve, respectively. Recall that varactors can vary their capacitance values from C_{min} to C_{max}. Therefore, by substituting Equation (3.5) into Equation (3.6), the frequency tuning range of VCOs can also be expressed as

$$\text{Frequency Tuning Range} = 2\left(\frac{\sqrt{C_{max} + C_{parasitic}} - \sqrt{C_{min} + C_{parasitic}}}{\sqrt{C_{max} + C_{parasitic}} + \sqrt{C_{min} + C_{parasitic}}}\right). \tag{3.7}$$

It can be observed from Equation (3.7) that the $C_{parasitic}$ decreases the frequency tuning range since it leaves a smaller portion of the C_{tk} for frequency tuning, which indicates that the largest frequency tuning range can be obtained when the $C_{parasitic}$ is minimized. However, the $C_{parasitic}$ caused by the inductor is fixed when it is designed. Also, the practical value of the $C_{parasitic}$ caused by the metal interconnections in the circuit would not be known until the layout of the whole circuit is completed. Therefore, minimization of $C_{parasitic}$ at the design stage can only be achieved by minimizing the size of the MOSFETs that are used to form the active circuit network since the C_{gs} and C_{gd} are proportional to the size of the MOSFETs [15], [17].

3.2.3 Power Consumption

The power consumption P_{con} of cross-coupled differential LC oscillators is determined by

$$P_{con} = V_{dd} I_{bias}, \tag{3.8}$$

where V_{dd} is the supply voltage of the circuit and I_{bias} is the bias current controlled by the bias current transistor (this transistor will be described later in Section 3.3) in the circuit. Also, the P_{con} is usually expressed in mW. It is obvious that the less power the circuit consumes, the better the performance it has because it can operate for a longer time with a given power supply.

3.2.4 Amplitude of Oscillation / Output Power

The amplitude of oscillation V_{osc} of LC oscillators is determined by

$$V_{osc} = Z_{tk} I_{bias} = \omega_0 L_{tk} Q_{tk} I_{bias} = \sqrt{\frac{L_{tk}}{C_{tk}}} Q_{tk} I_{bias}, \tag{3.9}$$

where Z_{tk} is the equivalent parallel impedance of the LC tank at the resonance node and

$$Q_{tk} = \left\{ \frac{1}{Q_L} + \left[\sum_i \left(\frac{1}{Q_{C_i}} \right) \left(\frac{C_i}{C_{tk}} \right) \right] \right\}^{-1}, \tag{3.10}$$

is the quality factor of the LC tank in which Q_{C_i} are the quality factors of different capacitors C_i that make up the C_{tk} [58], [68]. In practice, the Q_{C_i} are usually relatively large compared to Q_L when a spiral inductor is used in the LC tank. Therefore, Q_{tk} is usually limited by $Q_{L,s}$ and is given by

$$Q_{tk} \cong Q_{L,s} \approx \frac{\omega_0 L_s}{R_s}, \tag{3.11}$$

in common design practice [57], [58], [69], [70] when the spiral inductor is approximated by a series equivalent circuit previously discussed in Section 2.3. This also implies that the effective series resistance and L_{tk} in the resonator network can be approximated by the R_s and L_s of the spiral inductor, respectively. As a consequence, by applying series-parallel transformation (series-parallel transformations for both RC and RL networks can be found in Appendix A), R_{eff} and L_{tk} can be expressed as

$$R_{eff} \approx Q_{tk}^2 R_s \approx Q_{L,s}^2 R_s \tag{3.12}$$

and

$$L_{tk} \approx L_s, \tag{3.13}$$

respectively.

It is desirable to have a large V_{osc} so that the oscillator waveform is less sensitive to noise. From Equations (3.9) and (3.11), this can be achieved by either increasing the L_{tk} with the I_{bias} fixed or vice versa. However, the use of a larger inductor to increase the L_{tk} with the I_{bias} fixed would require a smaller C_{tk} to maintain the same nominal f_0, which results in the use of a smaller C_{cap} since it is very difficult to reduce $C_{parasitic}$ in practice. Consequently, the frequency tuning range would be decreased. On the other hand, it can be seen from Equation (3.8) that the use of a larger I_{bias} with the L_{tk} fixed would increase the P_{con}, which is non-desirable. Therefore, there is a direct trade-off among V_{osc}, frequency tuning range and P_{con}.

The V_{osc}, in practice, is usually reported in literature as output power P_{out}, which is the amount of RF power available for driving a load that is typically 50 Ω [71]. Also, it is usually expressed in dBm, which is the number of milliwatts in dB [71].

3.2.5 Phase Noise

Phase noise $L\{\Delta\omega\}$ is an indication of the spectral purity of oscillator's output. The output of an oscillator, ideally, is a single frequency represented by a single vertical line in

the frequency spectrum [71], as shown in Figure 3.2(a). In reality, however, there are noises in the oscillator such that the output is not a single vertical line but a skirt of noises near the f_0 [71], as shown in Figure 3.2(b), and these noises are called the phase noise. $L\{\Delta\omega\}$ is usually specified as the ratio of the noise power in 1 Hz bandwidth at an offset frequency away from the f_0 to the carrier power [71]. Also, it is usually expressed in dBc/Hz at an offset frequency in practice, so it is a negative number, and thus, the more the negative it is, the better is the performance of the circuit.

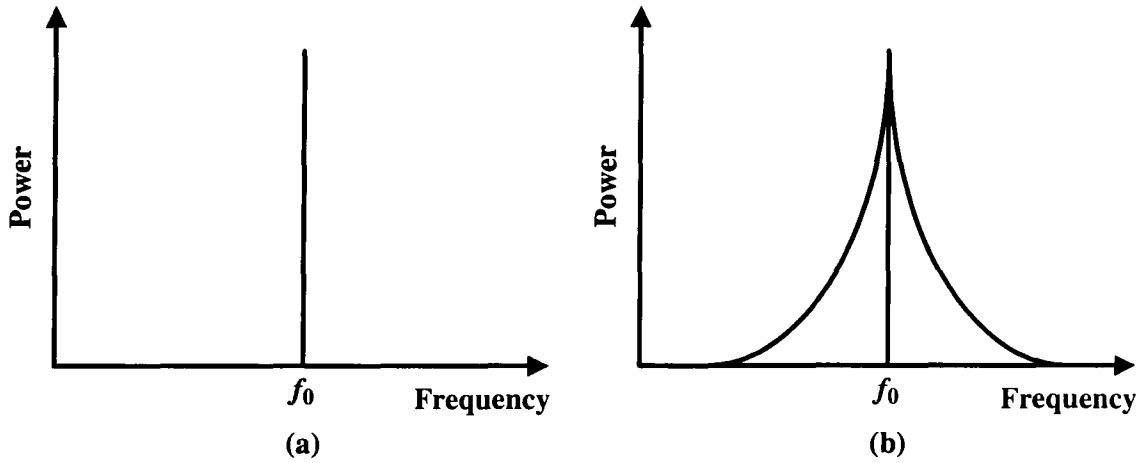


Figure 3.2 Illustration of the output spectrum of (a) an ideal oscillator and (b) a practical oscillator with a skirt of noises due to the phase noise [71].

A well known phase noise model of oscillators, Leeson's model [72], is a LTI model and it was expanded upon in [73], which predicts the $L\{\Delta\omega\}$ to be:

$$L\{\Delta\omega\} = 10 \cdot \log\left\{\frac{2FkT}{P_s}\left[1+\left(\frac{\omega_0}{2Q_{tk}\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}, \tag{3.14}$$

where F is an empirical parameter, k is the Boltzmann's constant, T is the temperature in degrees Kelvin, P_s is the average power dissipated in the resonator, ω_0 is the fundamental angular oscillation frequency, $\Delta\omega$ is the offset frequency from ω_0 at which the $L\{\Delta\omega\}$ is characterized, and $\Delta\omega_{1/f^3}$ is the corner frequency between the $1/f^3$ and $1/f^2$ regions as

shown in Figure 3.3 [73]. This equation can model all three regions of the typical phase noise characteristics shown in Figure 3.3 correctly if both F and $\Delta\omega_{1/f^3}$ are known accurately. However, F is the device excess noise factor, which represents the noise contributed by the active devices in the oscillators and does not include the nonlinear frequency conversion effects [73]. Also, $\Delta\omega_{1/f^3}$ is not same as the device $1/f$ noise corner [73], [74]. Therefore, both F and $\Delta\omega_{1/f^3}$ are empirical parameters at the design stage and they are usually unknown. Another problem with Leeson's model is that it is derived using a LTI system although oscillators are not LTI systems in practice [73].

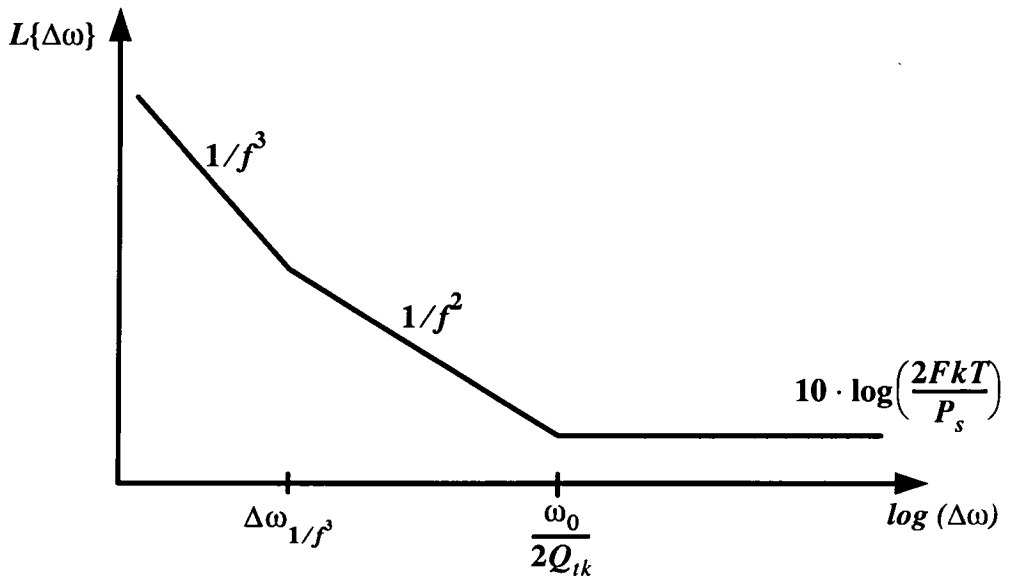


Figure 3.3 Qualitative behaviour of phase noise versus offset frequency from the fundamental oscillation frequency [73].

Hajimiri and Lee proposed a more accurate phase noise model using a linear time variant (LTV) system in [73]. This model explains all the processes involved in converting device noise into phase noise, in particular, the upconversion of $1/f$ device noise into low offset frequency phase noise [73]. It also accommodates the noise folding mechanism, which translates noise at harmonics of the oscillation frequency into the phase noise skirt of ω_0 [73]. The conclusion drawn in [73] is that the upconversion of the $1/f$ device noise depends on the symmetry of the oscillator waveform. Also, proper design of a LC oscilla-

tor using a complementary cross-coupled differential topology can create a more symmetrical oscillator waveform than a non-complementary cross-coupled differential topology, and thus, can suppress the upconversion of the $1/f$ device noise which improves the low offset frequency phase noise [73]. However, this model is not easy to implement in practice since calculations must be performed for each node of the circuit. Moreover, later in [74], [75], it was found that the upconversion of the $1/f$ device noise from the bias current transistor is the main contributor to the low offset frequency phase noise, whereas those contributed from the MOSFETs that are used to form the active circuit network are small and can be neglected.

In this research, to overcome the difficulties of using these two phase noise models to predict the $L\{\Delta\omega\}$ at the design stage, a simple expression

$$L\{\Delta\omega\} = \frac{kTR_{eff}(1 + O_{ssf})\left(\frac{\omega_0}{\Delta\omega}\right)^2}{V_{osc}^2/2} \tag{3.15}$$

is used [58], [76], [77]. In this expression, O_{ssf} is the noise factor safety margin necessary to ensure proper startup of the oscillation, i.e. the ratio of the R_{eff} to the magnitude of the R_{active} (referred hereafter as oscillation startup safety factor). This expression provides straightforward insight into designing oscillators with low phase noise since the values for all the parameters in the expression are known at the design stage. As an example, it can be observed from Equation (3.15) that the $L\{\Delta\omega\}$ can be improved by increasing V_{osc}. However, as discussed in Section 3.2.4, an increase of V_{osc} by increasing the L_{tk} with the I_{bias} fixed would reduce the frequency tuning range. On the other hand, an increase of V_{osc} by increasing the I_{bias} with the L_{tk} fixed would increase the P_{con}. Therefore, there is a trade-off among $L\{\Delta\omega\}$, frequency tuning range and P_{con}.

3.2.6 Figure-of-Merit

Comparing different LC oscillators using the performance parameters one by one that are discussed above is not an easy task. This is especially true since different designs

might sacrifice some performance parameters in order to improve others, but all parameters should still meet the design specifications. Therefore, a Figure-of-Merit (FoM), which is a value of an expression that attempts to incorporate all the important performance parameter values that describe the performance of a circuit, is used to readily compare different designs. The FoM for LC oscillators is [78]

$$FoM = 20\log\left(\frac{\omega_0}{\Delta\omega}\right) - L\{\Delta\omega\} - 10\log\left(\frac{P_{con}}{1\text{ mW}}\right) - 20\log Q_{tk}. \tag{3.16}$$

It can be seen from Equation (3.16) that all performance parameters for which higher values indicate better performance are added to the FoM, whereas those for which lower values mean better performance are subtracted. Therefore, a larger FoM would show an overall better performance of a circuit.

3.3 CROSS-COUPLED DIFFERENTIAL LC OSCILLATOR TOPOLOGIES

Cross-coupled differential LC oscillator topologies can be categorized into two families in standard CMOS technology: n-channel MOSFET (nMOSFET) cross-coupled differential topology (referred hereafter as the nMOS topology) and complementary cross-coupled differential topology (referred hereafter as the CMOS topology). In fact, there is one more family: p-channel MOSFET (pMOSFET) cross-coupled differential topology (referred hereafter as the pMOS topology), which is the counterpart of the nMOS topology. Because the operation and analysis of the pMOS topology is very similar to the nMOS topology, then only the nMOS and CMOS topologies will be discussed and compared.

3.3.1 nMOSFET Cross-Coupled Differential Topology

Figure 3.4 shows the schematic diagram of the simple nMOSFET cross-coupled differential LC oscillator composed of the inductors L1 and L2 with inductances L_{s1} and L_{s2} and parasitic series resistances R_{s1} and R_{s2}, respectively, the capacitors C1 and C2 with

capacitances C_1 and C_2, respectively, and the nMOSFETs M1 and M2 with parasitic gate-source capacitances C_{gs1} and C_{gs2} and parasitic gate-drain capacitances C_{gd1} and C_{gd2}, respectively. Note that since it is a symmetric differential topology, L1 = L2, C1 = C2 and M1 = M2, and thus, $L_{s1} = L_{s2}$, $R_{s1} = R_{s2}$, $C_1 = C_2$, $C_{gs1} = C_{gs2}$ and $C_{gd1} = C_{gd2}$.

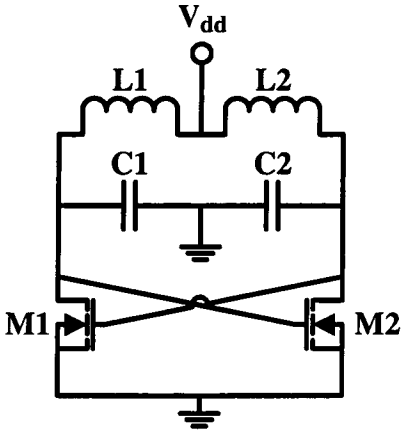


Figure 3.4 Schematic diagram of the simple nMOSFET cross-coupled differential LC oscillator.

3.3.1.1 Resonator Network / LC Tank

The LC tank of this topology, which is shown in Figure 3.5, is built by the series-connected inductors L1 and L2 in parallel with the C_{tk} composed of the capacitances C_1, C_2, C_{gs1}, C_{gs2}, C_{gd1} and C_{gd2}. It can be simplified into a simple parallel RLC network, as shown in Figure 3.5, where

$$R_{eff} \approx Q_{L,s}^2 (R_{s1} + R_{s2}) = 2Q_{L,s}^2 R_{s1}, \tag{3.17}$$

$$L_{tk} = L_{s1} + L_{s2} = 2L_{s1} \tag{3.18}$$

and

$$C_{tk} = \frac{C_1 C_2}{C_1 + C_2} + \frac{C_{gs1} C_{gs2}}{C_{gs1} + C_{gs2}} + (C_{gd1} + C_{gd2}) = \frac{C_1}{2} + \frac{C_{gs1}}{2} + 2C_{gd1}. \tag{3.19}$$

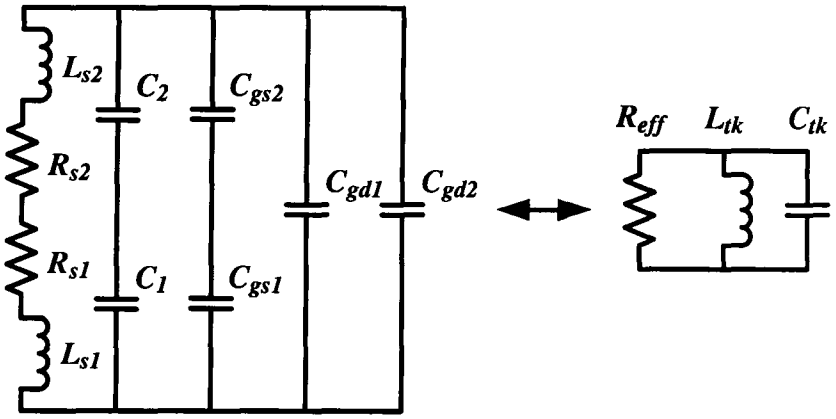


Figure 3.5 LC tank of the simple nMOSFET cross-coupled differential LC oscillator shown in Figure 3.4.

3.3.1.2 Active Circuit Network

The active circuit network is built by the nMOSFETs M1 and M2 connected in a cross-coupled fashion. It works as a cross-coupled differential amplifiers and provides the R_{active} to replenish the energy lost per cycle through the R_{eff} of the LC tank. The R_{active} seen looking into the cross-coupled nMOSFETs is

$$R_{active} = -\frac{2}{G_m}, \tag{3.20}$$

as shown in Figure 3.6, where

$$G_m = g_{m1} = g_{m2} \tag{3.21}$$

is the total transconductance, and g_{m1} and g_{m2} are the transconductance of M1 and M2, respectively. Therefore, to ensure the circuit produces stable oscillation, the magnitude of the R_{active} must be smaller than the R_{eff}, i.e.

$$G_m \geq \frac{2}{2Q_{L,s}^2 R_{s1}} = \frac{R_{s1}}{(\omega_0 L_{s1})^2}, \tag{3.22}$$

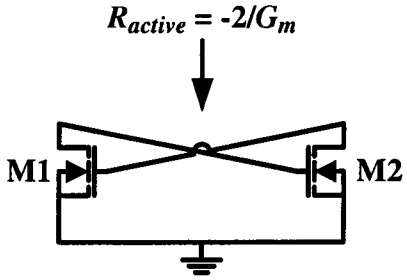


Figure 3.6 The R_{active} seen looking into the active circuit network of the simple nMOSFET cross-coupled differential LC oscillator [58].

by utilizing Equation (3.17). It should be noted that an O_{ssf} of two to three is usually implemented to ensure the startup of the oscillation [58], [79], i.e.

$$G_m \geq \frac{2O_{ssf}}{2Q_{L,s}^2 R_{s1}} = \frac{O_{ssf} R_{s1}}{(\omega_0 L_{s1})^2}. \tag{3.23}$$

The circuit performance of this simple nMOS topology, unfortunately, is very sensitive to the V_{dd} and can be seen from a DC analysis of this circuit. Its DC equivalent circuit is simple since the inductors and capacitors can be replaced by the short and open circuits, respectively, leaving only the M1 and M2 connected to the V_{dd} and the ground directly, which is shown in Figure 3.7. It can be observed from Figure 3.7 that the DC drain-source bias voltage V_{DS} and the DC gate-source bias voltage V_{GS} for both M1 and M2 are V_{DS} = V_{dd} and $V_{GS} = V_{dd}$. Therefore, neglecting the body effect and assuming the M1 and M2 are operating in the saturation region, the DC drain-source current I_{DS} for both M1 and M2 is

$$I_{DS} = \frac{\mu_n C'_{ox}}{2}\left(\frac{W_g}{L_g}\right)(V_{dd} - V_{TN})^2(1 + \lambda V_{dd}) \tag{3.24}$$

and the corresponding g_m is

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C'_{ox}\left(\frac{W_g}{L_g}\right)(V_{dd} - V_{TN})(1 + \lambda V_{dd}), \tag{3.25}$$

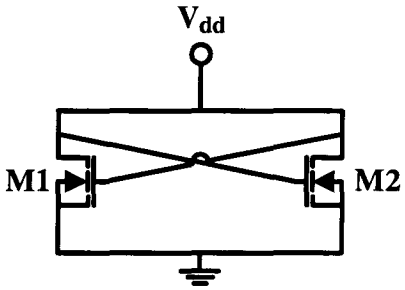


Figure 3.7 DC equivalent circuit of the simple nMOSFET cross-coupled differential LC oscillator.

where V_{TN} is the threshold voltage of the nMOSFETs and λ is the channel-length modulation parameter. It can be clearly seen from Equations (3.24) and (3.25) that both I_{DS} and g_m are directly affected by the V_{dd}, which is not desirable in practice since there is always supply voltage variation.

To make the I_{DS}, and thus, the g_m immune to the supply voltage variation, a bias current transistor, which controls the I_{bias}, can be added to the circuit to set the bias of the nMOSFETs. The bias current transistor is biased with a proper DC gate voltage V_g to operate in the saturation region so that it works as a constant current source, and thus, the I_{bias} is less sensitive to the supply voltage variation. It can be implemented by placing either a pMOSFET at the top of the circuit or an nMOSFET at the bottom of the circuit, as shown in Figures 3.8(a) and (b), respectively. In practice, the pMOSFET bias current transistor is better than its nMOSFET counterpart with respect to the nMOS topology because it taps the LC tank common mode point, which has less variation from the alternating current (AC) perspective in comparison to the common source point tapped by the nMOSFET bias current transistor [81]. Also, the pMOSFETs has lower $1/f$ device noise than the nMOSFETs [80], [81]. However, the bias current transistor adds noise to the overall $L\{\Delta\omega\}$ of the oscillator regardless of whether a pMOSFET or a nMOSFET is used.

Another advantage of having a bias current transistor is to increase the flexibility of the circuit. For example, as discussed in Section 3.2.5, increase the I_{bias} with the L_{tank} fixed would increase the V_{osc}, and thus, improve the $L\{\Delta\omega\}$ with a tradeoff of increasing the

P_{con}. Also, since the V_{osc} can be enlarged by increasing the I_{bias} without changing the V_{dd}, a low voltage circuit implementation with a high P_{out} is possible by employing this topology.

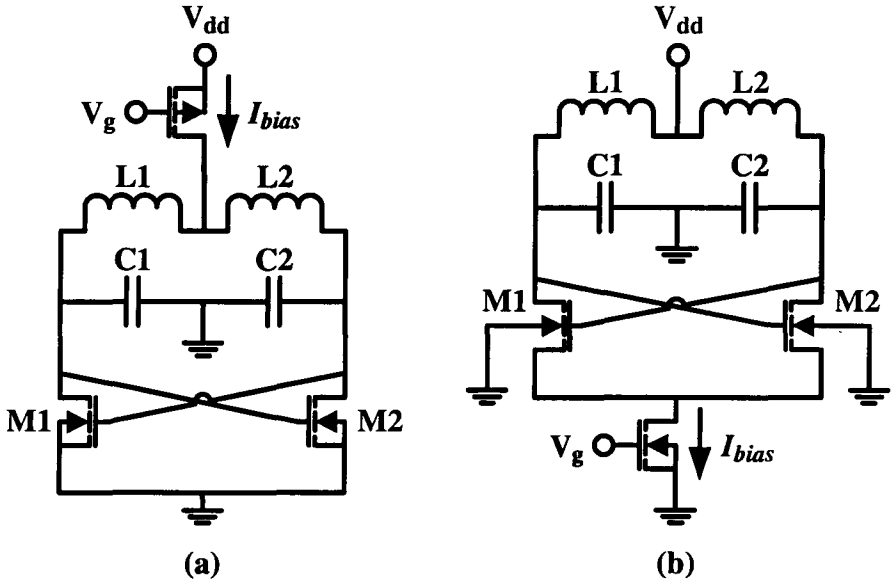


Figure 3.8 Schematic diagram of the simple nMOSFET cross-coupled differential LC oscillator with a bias current transistor implemented by placing (a) a pMOSFET at the top of the circuit or (b) an nMOSFET at the bottom of the circuit to control I_{bias}.

3.3.2 Complementary Cross-Coupled Differential Topology

The schematic diagram of the simple complementary cross-coupled differential LC oscillator is shown in Figure 3.9. It is composed of the inductor L1 with inductance L_{s1} and parasitic series resistance R_{s1}, the capacitor C1 with capacitance C_1, the nMOSFETs M1 and M2 with parasitic gate-source capacitances C_{gs1} and C_{gs2} and parasitic gate-drain capacitances C_{gd1} and C_{gd2}, respectively, and the pMOSFETs M3 and M4 with parasitic gate-source capacitances C_{gs3} and C_{gs4} and parasitic gate-drain capacitances C_{gd3} and C_{gd4}, respectively. It should be noted that M1 = M2 and M3 = M4 since it is a symmetric differential topology, and thus, $C_{gs1} = C_{gs2}$, $C_{gd1} = C_{gd2}$, $C_{gs3} = C_{gs4}$ and $C_{gd3} = C_{gd4}$. Also, from the AC perspective, a connection to the common mode point of the inductor is not

necessary in this CMOS topology compared to the nMOS topology. Therefore, oscillators in a CMOS topology can be implemented with only one symmetrical inductor, which saves much chip space.

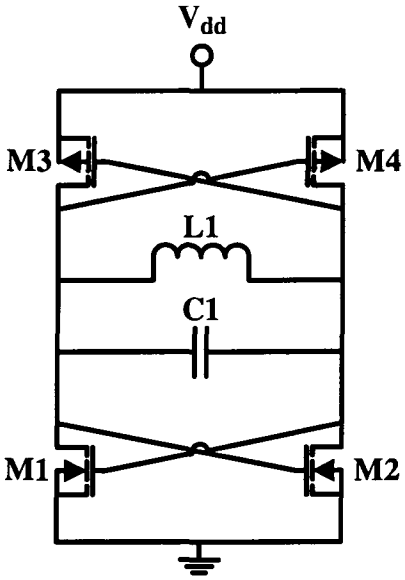


Figure 3.9 Schematic diagram of the simple complementary cross-coupled differential LC oscillator.

3.3.2.1 Resonator Network / LC Tank

Figure 3.10 shows the LC tank of this topology, which is built by the inductor L1 in parallel with the C_{tk} composed of the capacitances C_1, and the C_{gs} and C_{gd} of the M1, M2, M3 and M4. Similar to the nMOS topology, it can be simplified into a simple parallel RLC network, as shown in Figure 3.10, where

$$R_{eff} \approx Q_{L,s}^2 R_{s1}, \tag{3.26}$$

$$L_{tk} = L_{s1} \tag{3.27}$$

and

$$C_{tk} = C_1 + \frac{C_{gs1}}{2} + 2C_{gd1} + \frac{C_{gs3}}{2} + 2C_{gd3}. \tag{3.28}$$

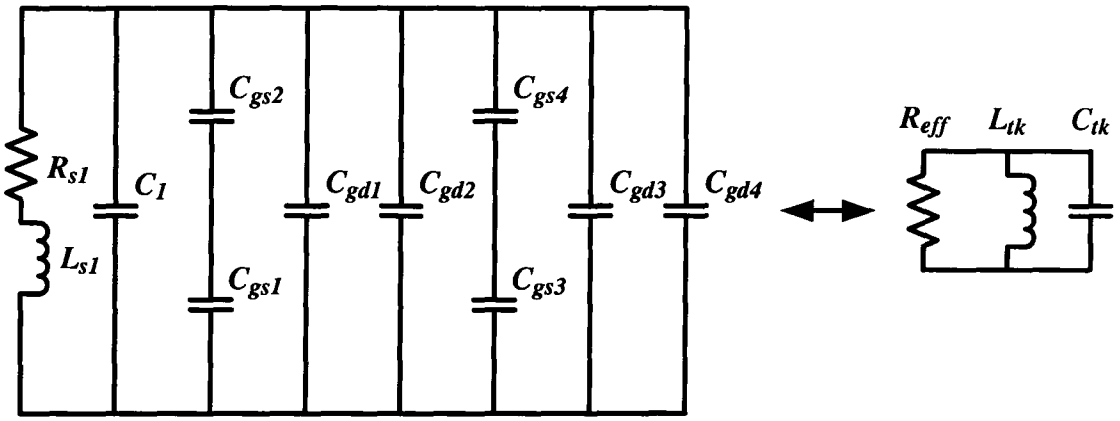


Figure 3.10 LC tank of the simple complementary cross-coupled differential LC oscillator shown in Figure 3.9.

3.3.2.2 Active Circuit Network

The active circuit network of the CMOS topology is, in fact, a modification of the one for the nMOS topology. The cross-coupled pMOSFETs M3 and M4 are connected in parallel to the cross-coupled nMOSFETs M1 and M2 in order to provide the R_{active} together. Therefore, the analyzes and discussions of this topology are nearly identical to those for the nMOS topology that are presented in Section 3.3.1.2, except for the following.

1. Two pairs of cross-coupled of transistors instead of one should be considered.
2. The LC tank is composed of one inductor, one capacitor, and the C_{gs} and C_{gd} of the M1, M2, M3 and M4 instead of two inductors, two capacitors, and the C_{gs} and C_{gd} of the M1 and M2 should be considered.

Consequently, Equations (3.21) to (3.23) should be modified to:

$$G_m = g_{m1} + g_{m4} = g_{m2} + g_{m3}, \tag{3.29}$$

$$G_m \geq \frac{2}{Q_{L,s}^2 R_{s1}} = \frac{2R_{s1}}{(\omega_0 L_{s1})^2} \tag{3.30}$$

and

$$G_m \geq \frac{2O_{ssf}}{Q_{L,s}^2 R_{s1}} = \frac{2O_{ssf} R_{s1}}{(\omega_0 L_{s1})^2}, \tag{3.31}$$

respectively, where g_{m3} and g_{m4} are the transconductance of M3 and M4, respectively. Also, the CMOS topology version of Figures 3.8(a) and (b) are shown in Figures 3.11(a) and (b), respectively. Note that the sizes of the M1, M2, M3 and M4 are designed to have g_{m1} = g_{m2} = g_{m3} = g_{m4} in practice, which enhances the symmetry of the oscillator waveform, and thus, improves the $L\{\Delta\omega\}$ performance [73].

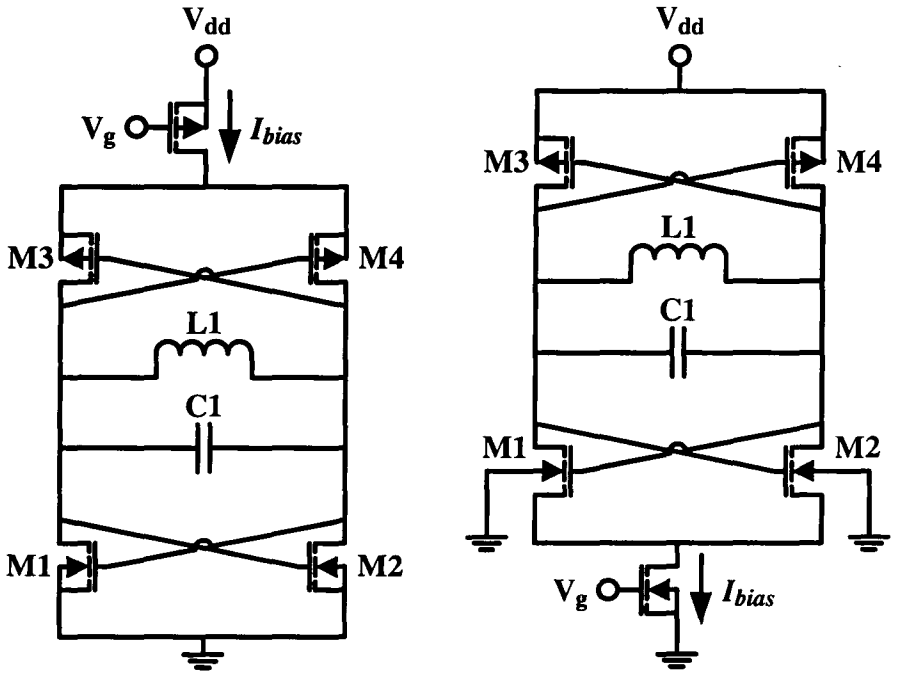


Figure 3.11 Schematic diagram of the simple complementary cross-coupled differential LC oscillator with a bias current transistor implemented by placing (a) a pMOSFET at the top of the circuit or (b) an nMOSFET at the bottom of the circuit to control I_{bias}.

3.3.3 Performance Comparison

3.3.3.1 Oscillation Frequency

The f_0 of the nMOS and CMOS topologies can be derived by substituting Equations (3.18) and (3.19), and Equations (3.27) and (3.28) into (3.4), respectively, which yields

$$f_0 = \frac{1}{2\pi\sqrt{2L_{s1}\left(\frac{C_1}{2}+\frac{C_{gs1}}{2}+2C_{gd1}\right)}} = \frac{1}{2\pi\sqrt{L_{s1}(C_1+C_{gs1}+4C_{gd1})}} \tag{3.32}$$

and

$$f_0 = \frac{1}{2\pi\sqrt{L_{s1}\left(C_1+\frac{C_{gs1}}{2}+2C_{gd1}+\frac{C_{gs3}}{2}+2C_{gd3}\right)}}. \tag{3.33}$$

As discussed in Section 3.3.2.2, the active circuit network of the CMOS topology is usually designed to have $g_{m1} = g_{m2} = g_{m3} = g_{m4}$ in practice. To achieve $g_{m1} = g_{m2} = g_{m3} = g_{m4}$, the aspect ratio of the pMOSFETs must be larger than the one for the nMOSFETs because μ_n is approximately 2.8 times μ_p in silicon [18] and the threshold voltage of the pMOSFETs V_{TP} is larger than the V_{TN} when their absolute values are compared [82]. This implies that $C_{gs1} < C_{gs3}$ and $C_{gd1} < C_{gd3}$ since both C_{gs} and C_{gd} are proportional to the W_g [17]. Therefore, to have the same f_0, it can be observed from Equations (3.32) and (3.33) that the C_1 used in the CMOS topology must be smaller than the one for the nMOS topology.

3.3.3.2 Frequency Tuning Range

From the discussion in the previous subsection, the $C_{parasitic}$ of the CMOS topology is larger than the one for the nMOS topology. Also, recall from Section 3.2.2 that the largest frequency tuning range can be obtained when the $C_{parasitic}$ is minimized. Therefore, the CMOS topology has a smaller frequency tuning range than the nMOS topology.

3.3.3.3 Power Consumption

For a given $L\{\Delta\omega\}$ performance, the CMOS topology consumes less power than the nMOS topology. This is because the entire I_{bias} is useful for the oscillation in the CMOS topology since both pMOSFETs and nMOSFETS are employed at the same time instead of only the nMOSFETs in the nMOS topology. That is, the CMOS topology only needs approximately half of the I_{bias}, and thus, approximately half of the P_{con} that is required by the nMOS topology to generate the same V_{osc}, which gives the same $L\{\Delta\omega\}$ performance.

3.3.3.4 Amplitude of Oscillation / Output Power

The CMOS topology generates a larger V_{osc} than the nMOS topology for a given I_{bias}. In the CMOS topology, the advantage of having the I_{bias} used by both pMOSFETs and nMOSFETs is taken rather than only by the nMOSFETs in the nMOS topology. Therefore, the V_{osc} generated by the CMOS topology for a given I_{bias} is approximately twice of the one produced by the nMOS topology.

3.3.3.5 Phase Noise

As discussed in Section 3.2.5, the $L\{\Delta\omega\}$ can be improved by increasing the V_{osc}. Also, from the previous subsection, the CMOS topology generates a larger V_{osc} than the nMOS topology for a given I_{bias}. Therefore, the CMOS topology has a better $L\{\Delta\omega\}$ performance than the nMOS topology for a given I_{bias}.

Chapter 4

Process Variation and Device Mismatch

Designers are currently utilizing the advanced deep submicron CMOS technologies to achieve the goal of implementing and integrating of low-voltage, low-power, low-cost and high performance analog, RF and mixed-signal circuits for diverse applications. Unfortunately, however, as the technology is scaled down continuously, the control of the variation in the fabrication steps such as etching, channel and source/drain implants, and gate oxide growth becomes more and more difficult [6]. This makes the variation of the device parameters in the modern technologies larger than the one in the older technologies, and thus, the circuit yield loss is more pronounced than before [7]. As a consequence, the control of the process variation and manufacturing uncertainty becomes more critical. Also, physical, predictive and accurate statistical models describing the device, and thus, the circuit parameters variation caused by the process variation become more indispensable for designers. Therefore, in this chapter, the global and local variations will be reviewed and followed by the influence of local variation on different devices. Finally, some considerations for the influence of the local variation on MOSFETs will be discussed from the deep submicron CMOS technologies and RF perspectives.

4.1 PROCESS VARIATION – GLOBAL AND LOCAL

The variation of device characteristics can be categorized into two families: global variation (GV) and local variation (LV). The GV describes the lot-to-lot, wafer-to-wafer, and die-to-die process variability [6]. That is, it accounts for the total variation in the value of a component over a wafer or a lot [83]. Therefore, it is also known as the interdie variation [6] or distance effects [84]. For example, since the same variation is assumed for the devices in the same circuit, the GV has little influence on the circuit behaviour of some an-

alog circuits such as a current mirror with a constant current bias as long as all transistors can still be biased in the saturation region. The LV describes the process variability caused by the variation of some process parameters such as oxide thickness and doping profile across the die [6]. That is, it reflects the variation in a device value with reference to an adjacent device on the same die [83]. Therefore, it is also known as intradie variation [6] or local mismatch [83]. As an example, devices with the same geometry placed side by side and close to each other may have different electrical parameters due to the LV.

In reality, most circuit simulators with statistical modelling capability for digital applications ignore the LV when simulating the circuit behaviour [6]. This is not a problem because the influence of the GV but not the LV on the circuit performance is important for digital circuits. Also, the device variation caused by the GV is much larger than that caused by the LV [6]. For analog circuits, however, both of the GV and LV influence significantly the variation of the circuit behaviour [85]–[87]. Therefore, modelling of devices with the LV is needed in designing analog circuits to simulate and predict the analog circuit performance statistically and accurately. In analog circuits, resistors, capacitors and MOSFETs are the most common devices used and sensitive to the LV. As a result, the influence of LV on resistors, capacitors and MOSFETs will be discussed in the following section. However, since MOSFETs are the devices focused on in this research, the influence of LV on MOSFETs will be examined in more detail.

It should be noted that terms such as mismatch, parametric matching, stochastic fluctuations and offsets are all commonly used to refer the electrical device parameters of IC components and they can vary substantially due to process variation. Therefore, these terms will be used interchangeably.

4.2 INFLUENCE OF LOCAL VARIATION ON DEVICES

Two parameters are used to describe the matching characteristics of devices. They are the mean μ and the bias-corrected standard deviation σ, which are defined as

$$\mu = \frac{\sum_{k=1}^{N} x_k}{N} \tag{4.1}$$

and

$$\sigma = \sqrt{\frac{\sum_{k=1}^{N} (x_k - \mu)^2}{N-1}}, \tag{4.2}$$

respectively, where x_k is the parameter value of the kth sample and N is the total number of samples for the experiment [88]. The μ describes the systematic mismatch between the matched devices, which is caused by mechanisms that influence all of the samples in the same manner [6]. The σ is a measure of the random mismatch caused by stochastic fluctuations in process parameters or material properties [6]. The μ is important because the absolute value of the devices affects the circuit performance directly. In the case of symmetric differential circuits, the matching property of the devices is as important as or even more important than the variation of the absolute value of the devices, and thus, the σ is also critical.

4.2.1 Influence of Local Variation on Resistors

Current CMOS technology provides various resistance options: n^+ or p^+ poly resistors, n^+ or p^+ diffusion resistors and n-well resistor [82]. The effects of process variation are not the same for different types of resistor since different materials have different electrical characteristics and temperature dependencies. However, the process variations that cause the device mismatch of different types of resistor are very similar and they can be categorized into two groups: area fluctuations and peripheral fluctuations [6]. The area fluctuations are those fluctuations that occur in the whole device and scale with the device area such as the fluctuations of the film thickness, the doping concentration, the doping pro-

file and the annealing conditions [6]. The peripheral fluctuations are those fluctuations only take place along the edges of the device and scale with the device periphery. An example of the peripheral fluctuations is the dimensional variation caused by the photolithographic inaccuracies and nonuniform etching [6]. Therefore, for a pair of matched resistors with width W_R and resistance R, the standard deviation of the random mismatch between the resistors σ_R is

$$\sigma_R = \frac{\sqrt{A_{R,a} + \frac{A_{R,p}}{W_R}}}{W_R\sqrt{R}}, \tag{4.3}$$

where $A_{R,a}$ and $A_{R,p}$ are the mismatch coefficients describing the influence of the area and peripheral fluctuations for resistors, respectively [89]. It can be observed from Equation (4.3) that resistors with narrow widths have poorer matching characteristics than those with wide widths. That is, to improve the matching, resistors implemented with wide widths are preferred to narrow widths.

4.2.2 Influence of Local Variation on Capacitors

In CMOS technologies, several different types of capacitor are available: MIM capacitors, pn junction capacitors and MOS capacitors. The capacitance value and matching property of a MIM capacitor are sensitive to the variations of the thickness of the dielectric and the geometry of the metal plates [6]. For a pn junction capacitor, the process variations that cause the device mismatch are the fluctuations of the doping concentration and the doping profile. In the case of a MOS capacitor, the capacitance value is dependent on the variations of the oxide thickness, the geometry and the doping profile [6]. Similar to the resistors, the process variations that cause the device mismatch of different types of capacitor can be categorized into the area fluctuations and the peripheral fluctuations (excluding the fluctuation of the oxide thickness) [89]. For a pair of matched capacitors with capacitance C, the standard deviation of the random mismatch between the capacitors σ_C is

$$\sigma_C = \frac{\sqrt{A_{C,a} + \frac{A_{C,p}}{C}}}{\sqrt{C}}, \tag{4.4}$$

where $A_{C,a}$ and $A_{C,p}$ are the mismatch coefficients describing the contribution of the area and peripheral fluctuations for capacitors, respectively [89]. It can be observed from Equation (4.4) that as the C increases, the contribution of the peripheral fluctuation decreases. Also, for large capacitors, the area fluctuations dominate the random mismatch such that

$$\sigma_C \approx \frac{\sqrt{A_{C,a}}}{\sqrt{C}}. \tag{4.5}$$

4.2.3 Influence of Local Variation on MOSFETs

MOSFETs are the most complicated devices in CMOS technologies and the variations in many process parameters can cause the variations in device characteristics. The subject of MOSFET parameter mismatch fluctuation was originally examined from the analog IC designers' standpoint and based on the characterization of populations of matched pairs with a range of device dimensions. Lakshmikumar et al. [83] were the first researchers to publish insights about MOSFET matching beyond the basic analog circuit designers' concept that large devices match better. They introduced the Poisson statistics for the dopant fluctuations. Also, they derived the theoretical relation between the mismatch standard deviation and the inverse of the square root of the active device area. A generalized description for this relationship is

$$\sigma_{\Delta P} = \frac{A_{\Delta P}}{\sqrt{WL}}, \tag{4.6}$$

where $\sigma_{\Delta P}$ is the standard deviation of the mismatch ΔP of the parameter P, $A_{\Delta P}$ is the mismatch coefficients and WL is the active device area of the population of the matched pairs under investigation [7], [83]. In addition, Lakshmikumar et al. aimed to use the DC drain-source current mismatch ΔI_{DS} as a measure of the device mismatch, where I_{DS} is given by

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{4.7}$$

in which

$$\beta = \mu C'_{ox}\frac{W_g}{L_g} \tag{4.8}$$

is the current factor, since MOSFETs are generally operating in saturation region in analog circuits and the channel length modulation effect is neglected because of old CMOS technology (3 μm CMOS process), and thus, only large devices were available for the experiment at the time the research was taken place. Typically, the device factor $\Delta I_{DS}/I_{DS}$, which is the variation of the DC drain-source current normalized to the DC drain-source current, is used to describe the mismatch behaviour of MOSFETs [6], [85], [90], [91]. It includes two portions – the threshold voltage mismatch and the current factor mismatch – and is expressed as [6], [85], [90], [91]

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{1}{I_{DS}}\left[\left(\frac{\partial I_{DS}}{\partial V_T}\right)\Delta V_T + \left(\frac{\partial I_{DS}}{\partial \beta}\right)\Delta\beta\right] = -\frac{g_m}{I_{DS}}\Delta V_T - \beta\Delta\frac{1}{\beta}. \tag{4.9}$$

4.2.3.1 Threshold Voltage Mismatch

The V_T of a MOSFET can be expressed as

$$V_T = \phi_{MS} + 2\phi_B + \frac{Q'_B}{C'_{ox}} - \frac{Q'_o}{C'_{ox}} + \frac{qD_I}{C'_{ox}}, \tag{4.10}$$

where ϕ_{MS} is the contact potential of the body material to the gate material (i.e. the gate-body work function difference), ϕ_B is the Fermi potential in the substrate, Q'_B is the depletion region charge per unit area, Q'_o is the fixed oxide charge per unit area, q is the magnitude of electronic charge and D_I is the threshold adjust implant dose, with the assumption that the implanted ions have a delta function profile at the silicon-silicon dioxide interface [18], [83]. Notice that the last term in this expression accounts for an ion implantation step

in the fabrication process, which allows to adjust the V_T to a desired value and is known as the threshold adjust implant [92]. The σ of V_T can be determined if the standard deviations of the various terms on the right hand side of Equation (4.10) can be found. The conclusion drawn in [83] is that the standard deviation of threshold voltage mismatch is inversely proportional to the square root of the channel area. Also, the major contributor to the threshold voltage mismatch is the nonuniform distribution of the dopant atoms in the substrate. However, in a well-controlled process, the effect of the nonuniform distribution of fixed oxide charges on threshold voltage mismatch is negligible. In addition, the gate oxide capacitance has little influence on the threshold voltage mismatch since it is quite uniform. Moreover, the ϕ_B has a logarithmic dependence on the substrate doping and the ϕ_{MS} has a similar dependence on the substrate and polysilicon gate dopings. Therefore, these two slow varying terms can be regarded as constants, and thus, not contributing to any threshold voltage mismatch.

4.2.3.2 Current Factor Mismatch

The β, as previously mentioned in Equation (4.8), is given by

$$\beta = \mu C'_{ox} \frac{W_g}{L_g} \tag{4.11}$$

and is repeated here for convenience. In all fabrication processes, there are edge variations. Edge variation happens because the edges of the interconnection lines and devices of an integrated pattern cannot be exactly located due to the uncertainty in the locations of the particle beams and mask dimensions [93]. Therefore, the edges of ideally straight edges are never exactly straight. Also, the physical dimensions are not exactly same as those drawn on the layout because of the photomask offsets and the photomask raggedness [84]. As a consequence, the W_g and L_g at the design and simulation stages are always different from those after fabrication. This was confirmed from the conclusion in [83], which stated that the mismatch in β due to the edge variations is proportional to $(1/L_g^2 + 1/W_g^2)^{1/2}$. It was

also concluded that the variation of the gate oxide capacitance is a common contributing factor to the threshold voltage mismatch and the current factor mismatch.

4.3 INFLUENCE OF LOCAL VARIATION ON MOSFETS FROM DEEP SUBMICRON AND RF PERSPECTIVES

The threshold voltage mismatch and the current factor mismatch have been studied by many researchers such as Lakshmikumar et al. [83], Shyu et al. [89] and Pelgrom et al. [94]. However, their research was based on old CMOS technologies. For example, the research for Lakshmikumar et al. and Pelgrom et al. were performed on 3 μm [83] and 2.5 μm [94] CMOS processes, respectively. Therefore, their results did not and were not able to consider the influence of the process variation on MOSFETs that only exists in deep submicron CMOS technologies. Fortunately, recent literature [7], [83]–[85], [90], [91], [95] have already studied this subject in deep submicron CMOS technologies and found that some factors that were negligible in influencing the device matching behaviour of MOSFETs are now becoming important. For instance, it was found in [95] that the threshold voltage mismatch is affected by the penetration of the source/drain and halo implants through the gate. This penetration depends on the thickness and crystal orientation fluctuations of the gate of the MOSFET [95].

The previously discussed device mismatch behaviour of MOSFETs is described by the device factor $\Delta I_{DS}/I_{DS}$, which is based on the threshold voltage mismatch and the current factor mismatch. This approach for describing and analyzing the device mismatch behaviour of MOSFETs is widely used by designers because I_{DS} is one of the common parameters that is used to analyze the property of MOSFETs. However, depending on the applications, different device factors should be used. For example, in analog circuit applications, the mismatch of the g_m was introduced in [96] additional to the V_T and the β since g_m is an important parameter in analog circuit designs. As for RF applications, unfortunately, almost no published research can be found in this subject, especially regarding the parasitic capacitances and gate resistance, which is very important for RFICs designs.

Chapter 5

Channel Length Fluctuation Effects on the Performance of RF Oscillators

The accuracy of the transistors' channel length is very important to the circuit performance, especially for differential RFICs. In reality, however, the dimensions of the transistors at the design and simulation stages are different from those after fabrication due to unavoidable fabrication process variations such as over- and under-etching, varying doping concentration gradients and uneven oxide thicknesses. Therefore, as the dimensions of the transistors keep decreasing, the effects of transistors' dimensions fluctuation will become increasingly important.

In most RFICs, the transistor's channel length is usually much smaller than its channel width. Therefore, small unintentional changes in the channel length can cause a large performance deviation. To examine this problem, two fully integrated, cross-coupled, differential LC oscillators are used as the test circuits. Both oscillators are designed in TSMC 0.18 μm having one polysilicon and six metal layers CMOS technology and with a triple-well process available [8]. The first oscillator utilized the CMOS topology with an nMOSFET as the bias current transistor and the second one employed the nMOS topology with a pMOSFET as its bias current transistor. Also, the use of body bias on the MOSFETs is proposed as a means to compensate for the changes in the frequency performance characteristics due to the channel length fluctuations. Therefore, in this chapter, the circuit design and the results of the first and second oscillators, will be presented. It should be noted that the fluctuation of the channel length is assumed to be dominated by the variation of etching in this research since the reported variation of etching in modern and future technologies is very high, it is approximately 20% in the ITRS 2003 [2].

5.1 COMPLEMENTARY CROSS-COUPLED DIFFERENTIAL LC VCO

5.1.1 Circuit Design

The schematic diagram and the layout of the cross-coupled differential LC VCO designed for this research are shown in Figures 5.1 and 5.2, respectively. This VCO utilizes the CMOS topology with an nMOSFET M7 as the bias current transistor to control I_{bias}. The outputs are buffered using source followers (nMOSFETs M5 and M6) for measurement purposes.

The inductor used in the LC tank is a 1.5 turns octagonal planar spiral inductor implemented with only the top metal layer. It can be observed from Figure 5.2 that it is a quasi-symmetrical spiral inductor. Therefore, the two-port lumped physical model shown in Figure 2.12(a), which is for symmetrical spiral inductor, can be used with modification. The modification is simply having the $C_{L,ox}$, $R_{L,sub}$ and $C_{L,sub}$ different instead of having them the same for Ports 1 and 2 to reflect the quasi-symmetrical structure. This modified two-port lumped physical model is shown in Figure 5.3 and it was used for the circuit simulation.

Figure 5.4 shows the simulated and measured Q_L and inductance of the 1.5 turns quasi-symmetrical octagonal planar spiral inductor based on the model shown in Figure 5.3. The details of how to extract the measured Q_L and inductance can be found in [52]. The values of the equivalent circuit model parameters used in the simulation is summarized in Table 5.1. It can be observed from Figure 5.4 that this 1.5 turns quasi-symmetrical octagonal planar spiral inductor has a $Q_{L,max}$ of 8.4 at 5 GHz with a corresponding inductance of 1.28 nH.

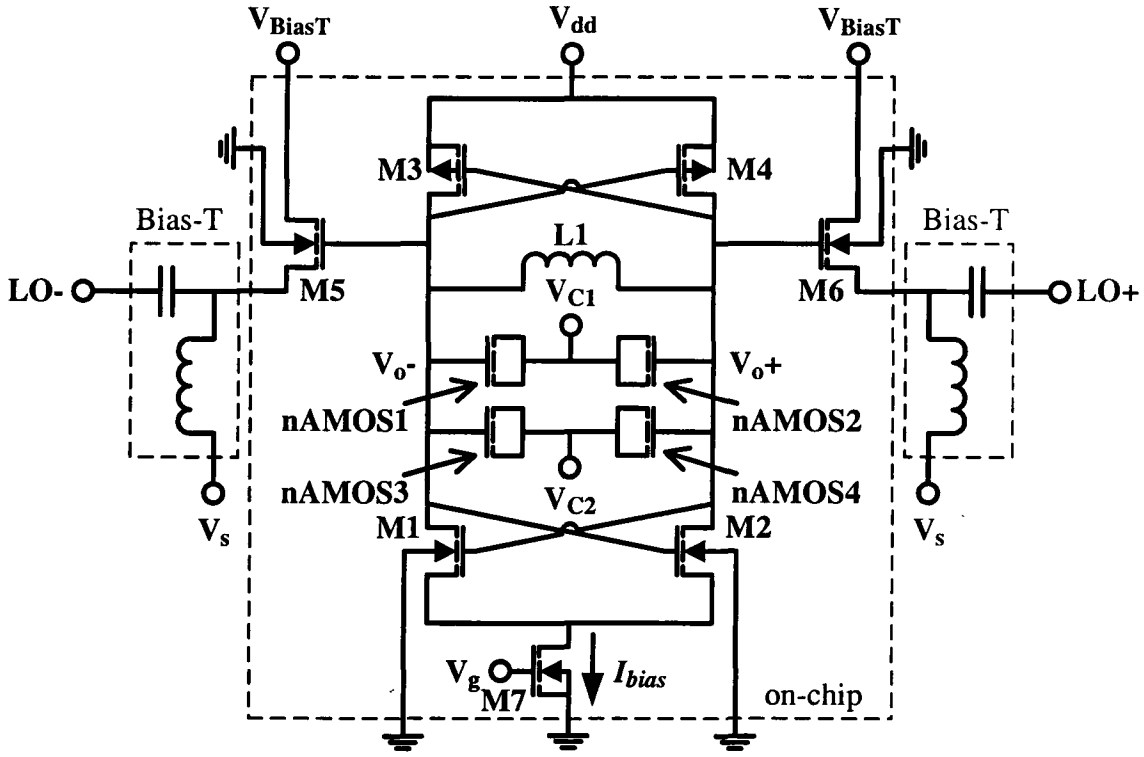


Figure 5.1 Schematic diagram of the complementary cross-coupled differential LC VCO with two pairs of nAMOS varactors for frequency tuning and an nMOSFET as the bias current transistor.

Two pairs of nAMOS varactor are used as the capacitor in the LC tank so that tuning of f_0 is possible and a larger frequency tuning range can be achieved compared to using only one pair of nAMOS varactor [13]. The first and the second pairs of the nAMOS varactor are composed of four nAMOS varactors nAMOS1 and nAMOS2, and nAMOS3 and nAMOS4, respectively. It should be noted that the gate terminals and the connected drain-source terminals of the nAMOS varactors are connected to the hot node of the oscillator (V_o+ or V_o-) and the control voltage V_{ctrl}, respectively. Therefore, the C_{device} of the nAMOS varactors can be changed by adjusting the V_{ctrl}, which implies that the C_{device} of the nAMOS varactors changes from C_{max} to C_{min} when the operation mode is changed from accumulation to weak inversion by adjusting the V_{ctrl} from negative to positive values. Also, two separate control voltages V_{C1} and V_{C2} instead of a single V_{ctrl} are used for the two pairs of nAMOS varactor so that fine tuning of f_0 is possible [13]. Moreover,

different sizes are used for the two pairs of nAMOS varactor so that different frequency tuning range can be obtained from each pair of varactor. However, at the time this circuit was designed and simulated, the model of nAMOS varactor was not available. Therefore, although pIMOS varactor has different properties from nAMOS varactor, it was used for the simulation since its structure is identical to a regular pMOSFET, whose model is already available. Also, as previously discussed in Section 2.1.4, the nAMOS varactor is built by replacing the p^+ implantations with n^+ implantations in the source and drain of a regular pMOSFET, which implies that the structure of the nAMOS varactor is very similar to the pIMOS varactor. More importantly, as compared in Section 2.1.5, the pIMOS varactor has smaller $Q_{C,min}$ than nAMOS varactor. Therefore, if the Q_C of the pIMOS varactor is not high enough and has significant effect on the Q_{tk} of this design but the VCO is still able to oscillate, then this VCO will also oscillate providing that the size of the nAMOS varactors implemented is same as that of the pIMOS varactors used in the simulation, which is what have been done when the layout of this VCO was drawn.

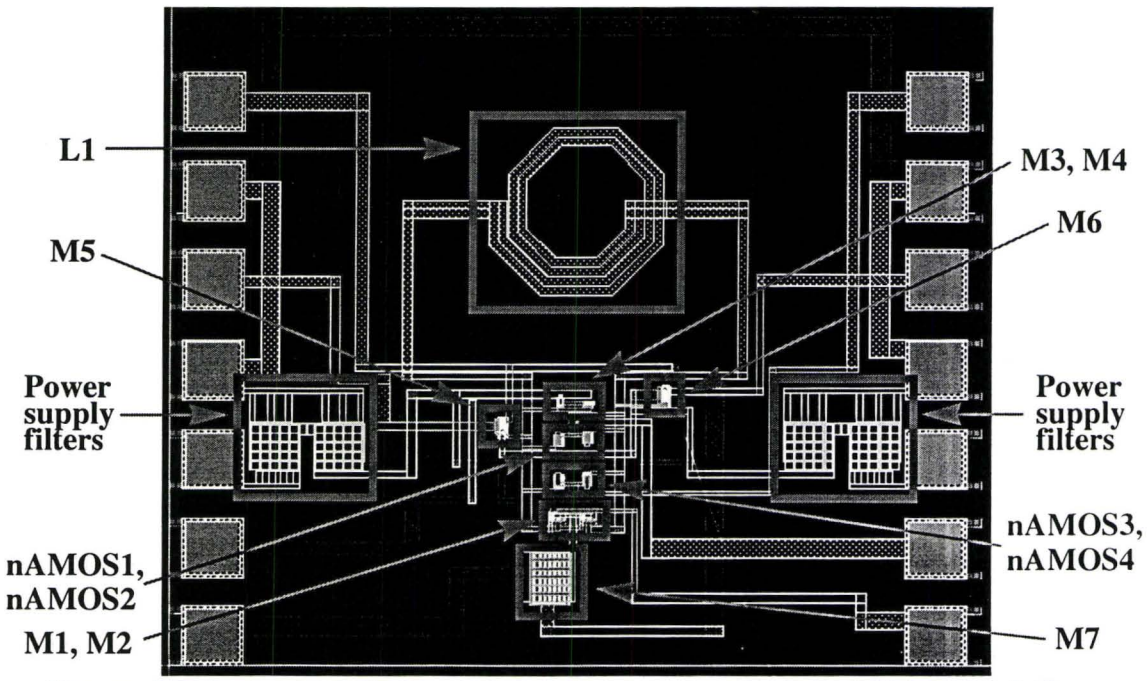


Figure 5.2 Layout of the complementary cross-coupled differential LC VCO shown in Figure 5.1.

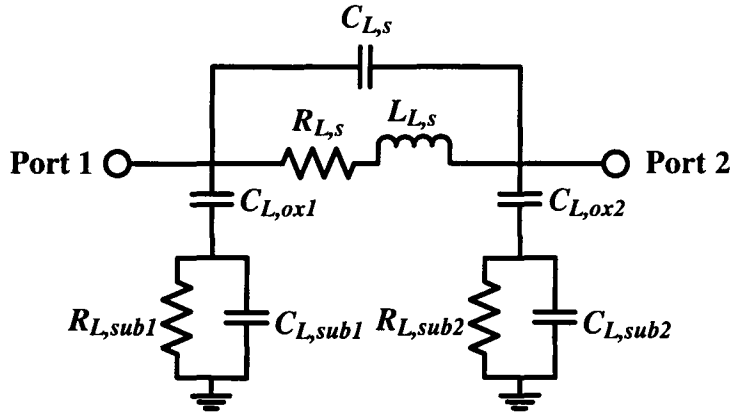


Figure 5.3 Modified two-port lumped physical model for quasi-symmetrical spiral inductor.

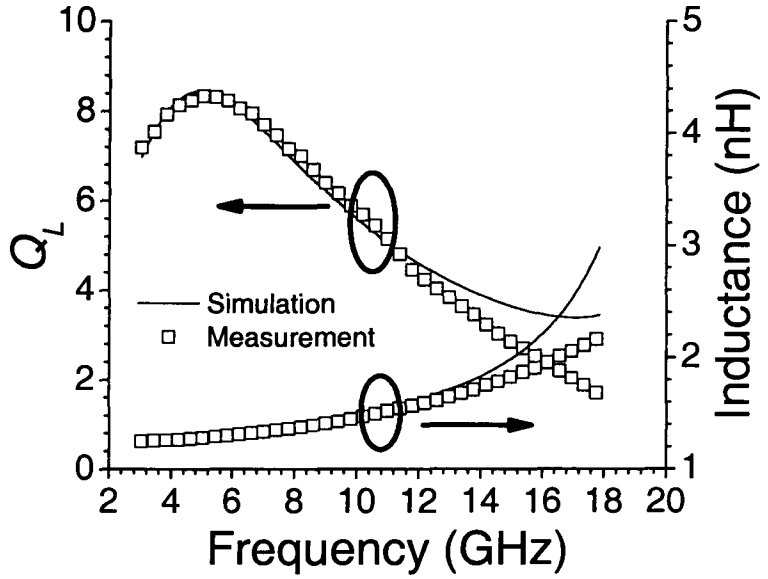


Figure 5.4 Simulated and measured Q_L and inductance of the 1.5 turns quasi-symmetrical octagonal planar spiral inductor.

The design of this VCO followed the analysis, discussion and equations presented in Chapter 3, particularly Section 3.3.2 for the CMOS topology. The circuit was simulated in Spectre and implemented using the devices summarized in Table 5.2.

Table 5.1 Summary of the equivalent circuit model parameter values of the 1.5 turns quasi-symmetrical octagonal planar spiral inductor.

$L_{L,s}$ (nH)	$R_{L,s}$ (Ω)	$C_{L,s}$ (aF)	$C_{L,ox1}$ (fF)	$C_{L,ox2}$ (fF)	$R_{L,sub1}$ (Ω)	$R_{L,sub2}$ (Ω)	$C_{L,sub1}$ (fF)	$C_{L,sub2}$ (fF)
1.239	3.1648	580	118	104	311	222	54.3	98.5

Table 5.2 Summary of the devices used in the complementary cross-coupled differential LC VCO.

Active Device – nMOSFET				
Name	Number of fingers	W_g (μm)	L_g (μm)	
M1, M2	4	20	0.18	
M5, M6	5	50	0.18	
M7	48	480	2	
Active Device – pMOSFET				
Name	Number of fingers	W_g (μm)	L_g (μm)	
M3, M4	8	40	0.18	
Passive Device – Capacitor				
Name	Number of fingers	W_g (μm)	L_g (μm)	
nAMOS1, nAMOS2	4	34	1	
nAMOS3, nASMO4	4	30	1.2	
Passive Device – Inductor				
Name	Type	Inductance (nH)	Series Resistance	Area (μm^2)
L1	Spiral Inductor	1.239	3.1648	91325

5.1.2 Experimental Results

The implemented VCO was measured using wafer probing with Agilent E4440A 26.5 GHz spectrum analyzer and Agilent 4156C semiconductor parameter analyzer. The V_{BiasT} and V_s of the Bias-Ts and V_g of M7 were biased at 1.8 V, 0 V and 0.6 V, respectively, for all measurements. Two different values of V_{dd}, 1.8 V and 1.5 V, were used. For each V_{dd}, three different biasing conditions of V_{ctrl} were measured:

1. V_{C2} = 0 V and V_{C1} was swept from 0 V to 1.8 V with a step size of 0.2 V.
2. V_{C1} = 0 V and V_{C2} was swept from 0 V to 1.8 V with a step size of 0.2 V.
3. $V_{C1} = V_{C2}$ and was swept from 0 V to 1.8 V with a step size of 0.2 V.

The simulated and measured f_0 for V_{dd} = 1.8 V is shown in Figure 5.5. However, since the pIMOS varactor has different properties from the nAMOS varactor, different ranges of V_{ctrl} were used for the pIMOS and nAMOS varactors in order to see the full frequency tuning range. The values of V_{ctrl} used for the simulation and the measurement were 0.5 V to 2.3 V and 0 V to 1.8 V, respectively. It should be noted that 1.8 V should be the maximum voltage that can be applied to V_{ctrl} in practice since 0.18 μm CMOS technology is for V_{dd} = 1.8 V applications [8]. Also, for simplicity, only the results for $V_{C1} = V_{C2}$ are shown in Figure 5.5.

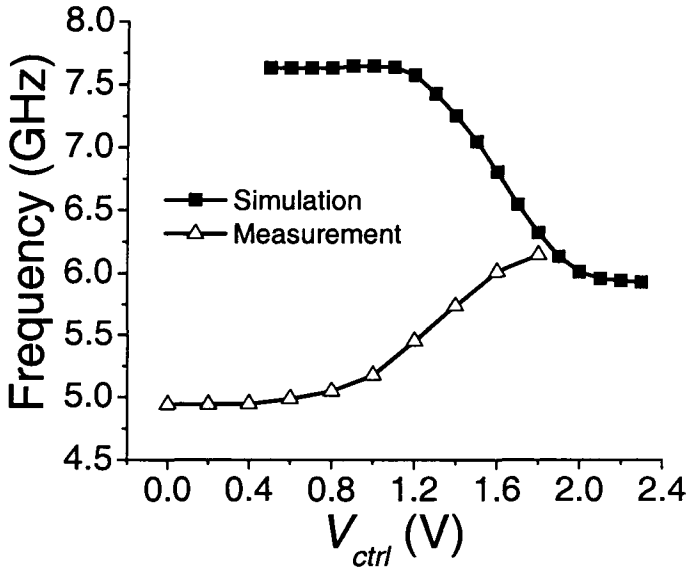


Figure 5.5 Simulated and measured f_0 for $V_{C1} = V_{C2}$ with V_{dd} = 1.8 V.

It can be seen from Figure 5.5 that when the V_{ctrl} increases, the f_0 for the simulated and measured results are decreasing and increasing, respectively. Therefore, on the first glance, there is no valuable comparisons or conclusions that can be made from this plot. However, this is not correct. The f_{min} provides very important information because it oc-

curs when the C_{device} of the varactors reaches C_{max}, which is approximately equals C_{ox} for both pIMOS and nAMOS varactors as discussed in Section 2.1.2.2. Also, since C_{ox} is proportional to the size of the device and the size of the implemented nAMOS varactors is same as the size of the pIMOS varactors used in the simulation, then the C_{ox} should be the same for both pIMOS and nAMOS varactors. Consequently, the simulated f_{min} should be same as the one obtained from measurement. However, it can be observed from Figure 5.5 that the simulated and measured f_{min} are 5.95 GHz and 4.94 GHz, respectively, which corresponds to a relatively large difference of 1.01 GHz, or equivalently, a difference of approximately 0.26 pF in the C_{tk} since the inductance is almost the same at 4.94 GHz and 5.95 GHz, which can be observed from Figure 5.4. This difference can be caused by the inaccuracy of the transistors' model used in the simulation. Another possible cause is the non-deliberate channel length fluctuation of the MOSFETs (M1, M2, M3 and M4) and nAMOS varactors (nAMOS1, nAMOS2, nAMOS3 and nAMOS4), whose C_{gs} and C_{ox}, respectively, are directly related to their channel lengths [15], [17], and thus, affects the C_{tk} and consequently the f_{min}. Although this is a good example of small unintentional changes in the channel length due to fabrication process variations can lead to a large circuit performance deviation, it is not easy to use this design to analyze how the channel length fluctuation affects the performance characteristics of LC oscillator. This is because the properties of the pIMOS and the nAMOS varactors are different, and thus, the simulated and measured circuit performance are different not only with respect to the values but also the tendency and the rate of changes of the values as can be seen in Figure 5.5. As a result, only the measurement results of this design will be presented in the rest of this section and they will not be used for the analysis of the channel length fluctuation effects on the circuit performance of LC oscillator. Also, a second LC oscillator was thereby designed using only devices that have proper model for simulation so that the channel length fluctuation effects on the circuit performance of LC oscillator can be examined. The circuit design and results for the second oscillator will be presented in Section 5.2.

Figures 5.6 and 5.7 show the f_0 for all three different biasing conditions of V_{ctrl} with V_{dd} biased at 1.8 V and 1.5 V, respectively. It can be seen from Figures 5.6 and 5.7 that at

a V_{dd} of 1.8 V and 1.5 V, the f_{min} and f_{max} are 4.94 GHz and 6.14 GHz, and 4.94 GHz and 6.28 GHz, respectively, which corresponds to a frequency tuning range of 21.7% and 23.9%, respectively. It is worth noticing that, from Figure 5.4, the L_{tk} and Q_L, which is approximately same as Q_{tk}, are approximately constant between 4.94 GHz and 6.28 GHz. Therefore, the increases of f_0 when V_{ctrl} increases is due to the decreases of C_{tk}.

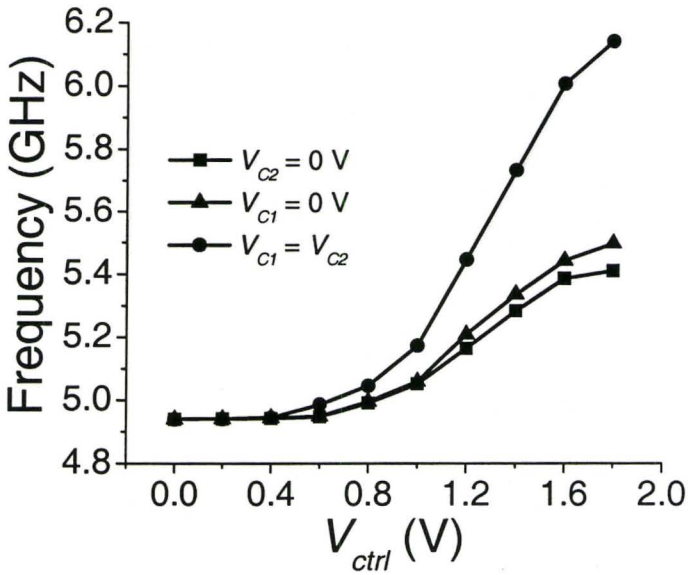


Figure 5.6 f_0 for three different biasing conditions of V_{ctrl} with V_{dd} = 1.8 V.

Two advantages of employing two pairs of varactor instead of one pair and each with its individual V_{ctrl} can also be observed from Figures 5.6 and 5.7. The first advantage is two pairs of varactor has a larger tunable C_{cap}, and thus, frequency tuning range than if only one pair is used. This can be seen if V_{C1} (or V_{C2}) is swept from 0 V to 1.8 V with V_{C2} (or V_{C1}) = 0 V, which is equivalent to having V_{C2} (or V_{C1}) acts as a capacitor with fixed capacitance. Under this condition, the frequency tuning range is approximately half of the actual frequency tuning range, which can be observed from Figures 5.6 and 5.7. The second advantage is fine tuning of f_0 is possible. This can be only achieved if each pair of varactor has its own V_{ctrl}, which is what has been implemented in this design. For example, assuming a voltage supply that can only be adjusted with a step size of 0.2 V is used and it can be seen from Figure 5.6 that a f_0 of 5.6 GHz is not obtainable. However, by increasing

V_{C1} (or V_{C2}) instead of keeping it at 0 V and sweeping V_{C2} (or V_{C1}), this would be same as shifting the curve of V_{C1} = 0 V (or the curve of V_{C2} = 0 V) upwards, and thus, a f_0 of 5.6 GHz can be obtained.

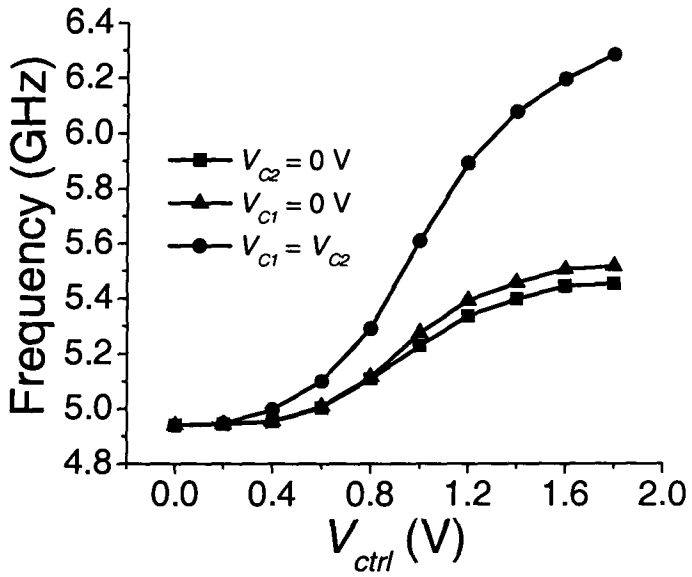


Figure 5.7 f_0 for three different biasing conditions of V_{ctrl} with V_{dd} = 1.5 V.

The current consumption for all three different biasing conditions of V_{ctrl} with V_{dd} biased at 1.8 V and 1.5 V are shown in Figures 5.8 and 5.9, respectively. It can be seen from Figures 5.8 and 5.9 that this design consumes less than 1 mA of current for both V_{dd} of 1.8 V and 1.5 V, which corresponds to a P_{con} of less than 1.8 mW and 1.5 mW, respectively. Also, the current, and thus, the P_{con} is found to be approximately constant since it only varies 0.51% and 1.89% when V_{dd} is 1.8 V and 1.5 V, respectively. In fact, the current, and thus, the P_{con} is expected to be approximately constant since a bias current transistor M7 is used to control the I_{bias} in this design. Also, a relatively large L_g, 2 μm, was used for M7 to minimize the channel-length modulation effect on this MOSFET although a smaller L_g could be used to obtain the same I_{bias} as long as the aspect ratio of this MOSFET is kept, which further enhances the stability of the current consumption, and thus, the P_{con}.

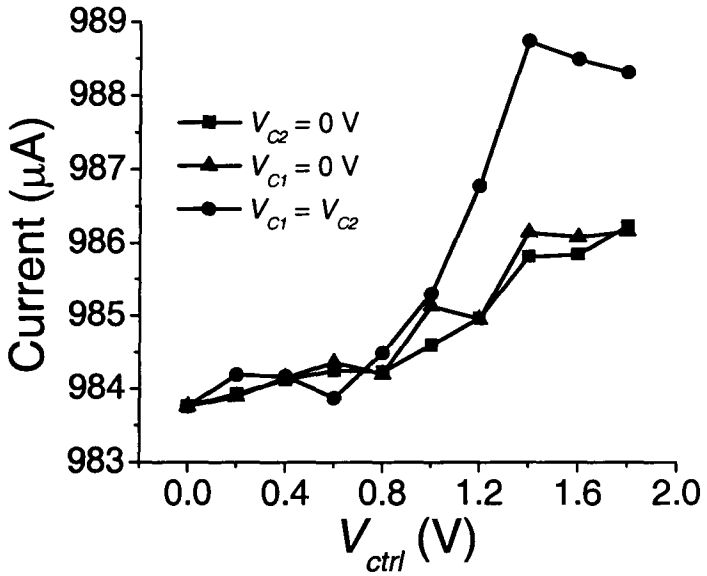


Figure 5.8 Current consumption for three different biasing conditions of V_{ctrl} with V_{dd} = 1.8 V.

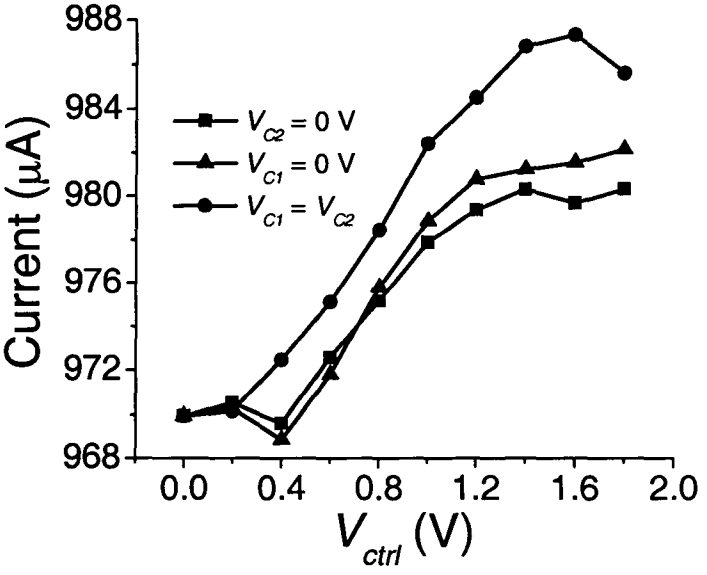


Figure 5.9 Current consumption for three different biasing conditions of V_{ctrl} with V_{dd} = 1.5 V.

Figures 5.10 and 5.11 show the P_{out} for all three different biasing conditions of V_{ctrl} with V_{dd} biased at 1.8 V and 1.5 V, respectively. It can be observed from Figures 5.10 and 5.11 that the P_{out} increases with V_{ctrl}, which is expected. Recall from Equation (3.9), which is repeated here for convenience:

$$V_{osc} = Z_{tk} I_{bias} = \omega_0 L_{tk} Q_{tk} I_{bias} = \sqrt{\frac{L_{tk}}{C_{tk}}} Q_{tk} I_{bias}, \tag{5.1}$$

that the V_{osc}, and thus, the P_{out} of LC oscillators is determined by the L_{tk}, Q_{tk}, I_{bias} and C_{tk}. As previously discussed, the L_{tk}, Q_{tk} and I_{bias} are approximately constant for the whole frequency range and the increases of f_0 when V_{ctrl} increases is due to the decreases of C_{tk}. Therefore, from Equation (5.1), it can be predicted that when V_{ctrl} increase, the C_{tk} would decrease which causes the V_{osc}, and thus, the P_{out} increase.

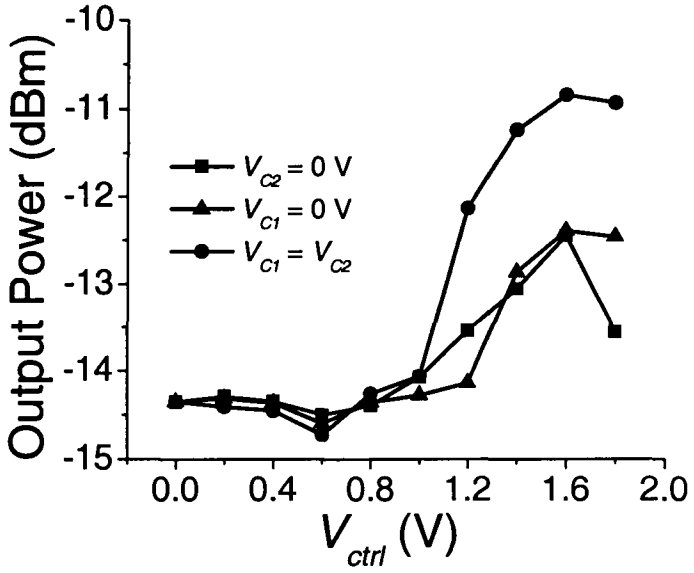


Figure 5.10 P_{out} for three different biasing conditions of V_{ctrl} with V_{dd} = 1.8 V.

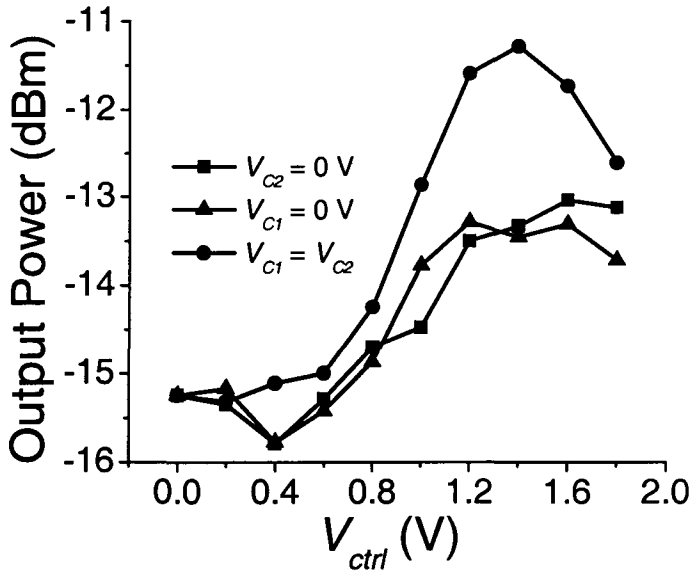


Figure 5.11 P_{out} for three different biasing conditions of V_{ctrl} with V_{dd} = 1.5 V.

The phase noise performance for V_{dd} of 1.8 V and 1.5 V are very similar to each other with V_{dd} = 1.5 V having a better performance in general. Therefore, only the results for V_{dd} = 1.5 V are shown below for discussion. It should be noted that all the $L\{\Delta\omega\}$ values reported below are the ratio of the noise power in a 1 Hz bandwidth at an offset frequency to the carrier power. The $L\{\Delta\omega\}$ for V_{C2} = 0 V at 600 kHz, 1 MHz and 3 MHz offset frequencies is shown in Figure 5.12. It can be seen from this figure that the $L\{\Delta\omega\}$ is almost the same when V_{C1} increases from 0 V to 0.2 V, then increases when V_{C1} increases from 0.2 V to 0.4 V and decreases thereafter, which is expected. Recall that $L\{\Delta\omega\}$ is inversely proportional to P_{out}. Therefore, if P_{out} increases or decreases, $L\{\Delta\omega\}$ should be decreased or increased correspondingly. As a result, by comparing the curve of V_{C2} = 0 V in Figure 5.11 to Figure 5.12, $L\{\Delta\omega\}$ decreases or increases when P_{out} increases or decreases. The same relationship can also be observed between the curves of V_{C1} = 0 V and V_{C1} = V_{C2} in Figure 5.11, and Figures 5.13 and 5.14 for V_{C1} = 0 V and V_{C1} = V_{C2}, respectively.

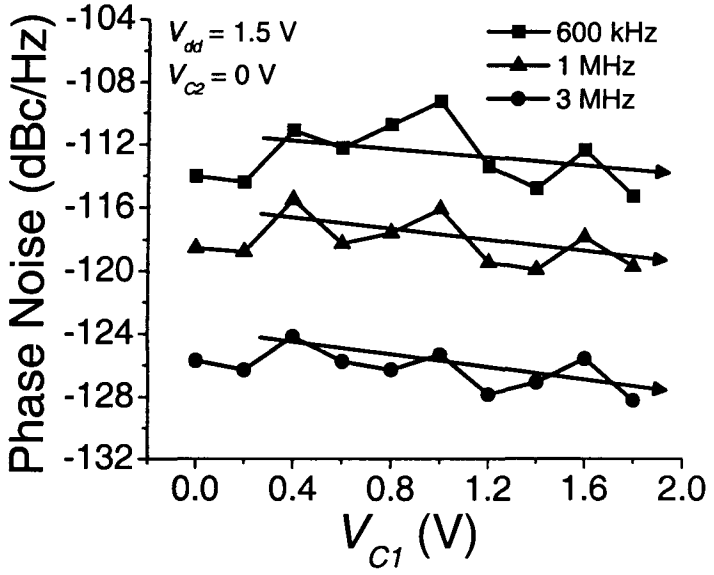


Figure 5.12 Phase noise performance for V_{C2} = 0 V at 600 kHz, 1 MHz and 3 MHz offset frequencies with V_{dd} = 1.5 V.

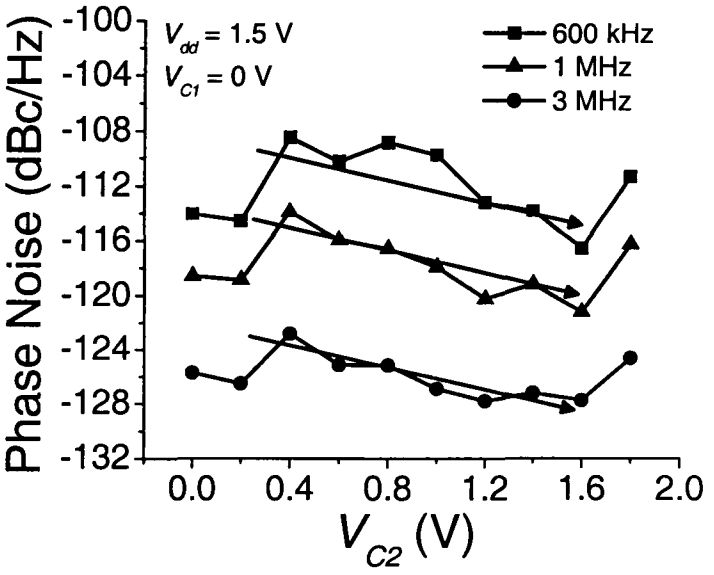


Figure 5.13 Phase noise performance for V_{C1} = 0 V at 600 kHz, 1 MHz and 3 MHz offset frequencies with V_{dd} = 1.5 V.

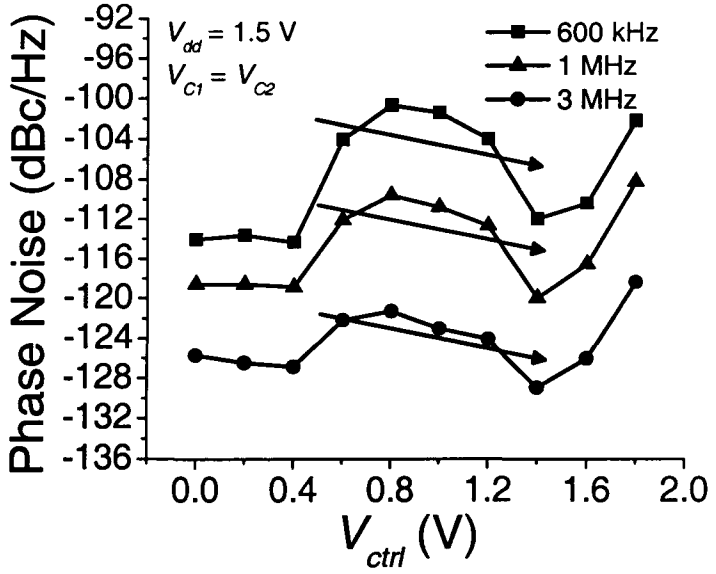


Figure 5.14 Phase noise performance for V_{C1} = V_{C2} at 600 kHz, 1 MHz and 3 MHz offset frequencies with V_{dd} = 1.5 V.

The frequency spectrum for V_{C1} = 0 V and V_{C2} = 1.6 V at V_{dd} = 1.5 V is shown in Figure 5.15. From this figure, it can be observed that the output power is -13.3 dBm at a f_0 of 5.506 GHz. Figure 5.16 shows the phase noise performance for the spectrum of Figure 5.15. The phase noise at 600 kHz, 1 MHz and 3 MHz offset frequencies were measured to be -116.6 dBc/Hz, -121.2 dBc/Hz and -127.8 dBc/Hz, respectively.

Table 5.3 compares the results of this design using the information from the frequency spectrum shown in Figure 5.15 with several previously reported oscillators implemented in CMOS technology using the FoM in Equation (3.16), which is repeated here for convenience:

$$FoM = 20\log\left(\frac{\omega_0}{\Delta\omega}\right) - L\{\Delta\omega\} - 10\log\left(\frac{P_{con}}{1\text{ mW}}\right) - 20\log Q_{tk}. \tag{5.2}$$

The values listed in Table 5.3 are collected from the references directly without any modification. The VCO discussed here is able to achieve a FoM of 176.4 dB, which is higher

compared to the other oscillators. This is achieved mainly by lowering the power consumption considerably, while still maintaining acceptable performance.

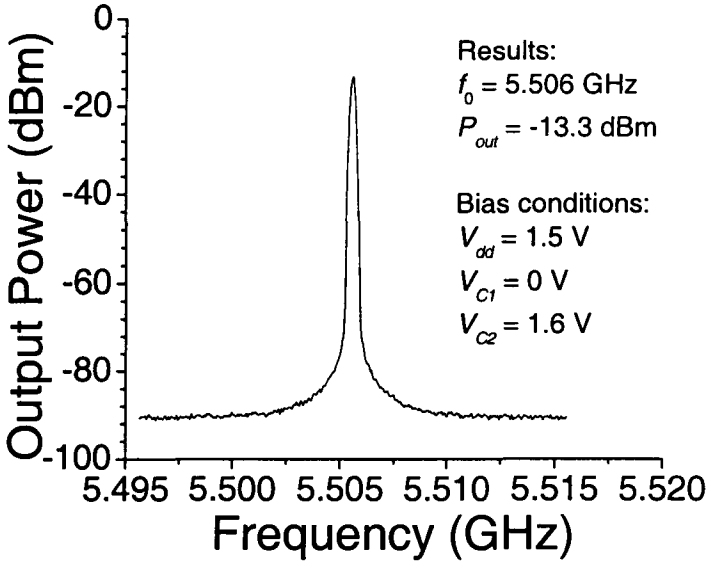


Figure 5.15 Spectrum for V_{C1} = 0 V and V_{C2} = 1.6 V with V_{dd} = 1.5 V.

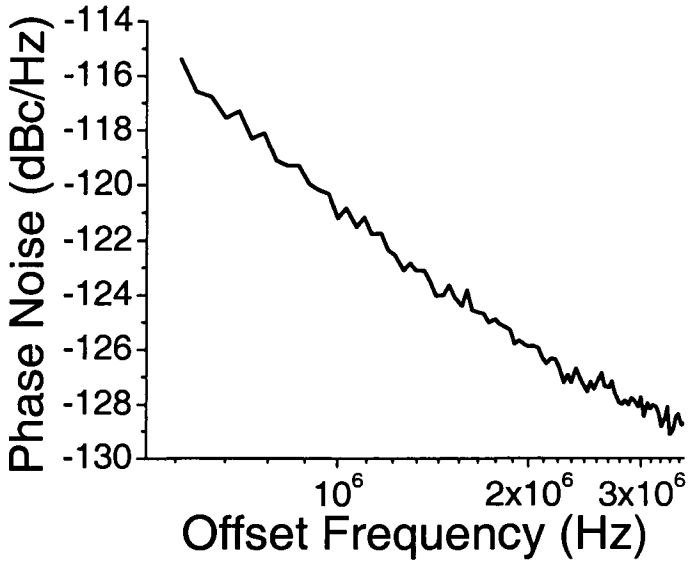


Figure 5.16 Phase noise performance for the spectrum of Figure 5.15.

Table 5.3 FoM for various CMOS oscillators.

Reference	CMOS Technology (μm)	f_0 (GHz)	$L\{\Delta\omega\}$ (dBc/Hz)	P_{con} (mW)	Q_{tk}	FoM (dB)
This Work	0.18	5.506	-121.2 @ 1 MHz	1.31	8.3	176.4
[75] 2002	0.25	5.1	-132 @ 3 MHz	7.25	6	172.4
[97] 2003	0.18	1.82	-125 @ 1 MHz	6.54	5	168.1
[98] 2004	0.18	3.8	-115 @ 1 MHz	7.2	4.2	165.6
[99] 2004	0.18	10.02	-102 @ 1 MHz	3.7	5.5	161.5

5.2 NMOSFET CROSS-COUPLED DIFFERENTIAL LC OSCILLATOR

5.2.1 Circuit Design

Figures 5.17 and 5.18 show the schematic diagram and the layout of the second cross-coupled differential LC oscillator designed for this research, respectively. This oscillator utilizes the nMOS topology with a pMOSFET M5 as the bias current transistor to control I_{bias}. The outputs are buffered using source followers (nMOSFETs M3 and M4) for measurement purposes.

The inductors L1 and L2 used in the LC tank are 2.5 turns rectangular planar spiral inductor implemented with only the top metal layer. It can be observed from Figure 5.18 that they are quasi-symmetrical spiral inductors. Therefore, the modified two-port lumped physical model shown in Figure 5.3 was used for the circuit simulation. Figure 5.19 shows the simulated and measured Q_L and inductance of the 2.5 turns quasi-symmetrical rectangular planar spiral inductor based on the model shown in Figure 5.3. The details of how to extract the measured Q_L and inductance can be found in [52]. The values of the equivalent circuit model parameters used in the simulation is summarized in Table 5.4. It can be observed from Figure 5.19 that this 2.5 turns quasi-symmetrical rectangular planar spiral inductor has a $Q_{L,max}$ of 5.7 at 2.3 GHz with a corresponding inductance of 3.85 nH.

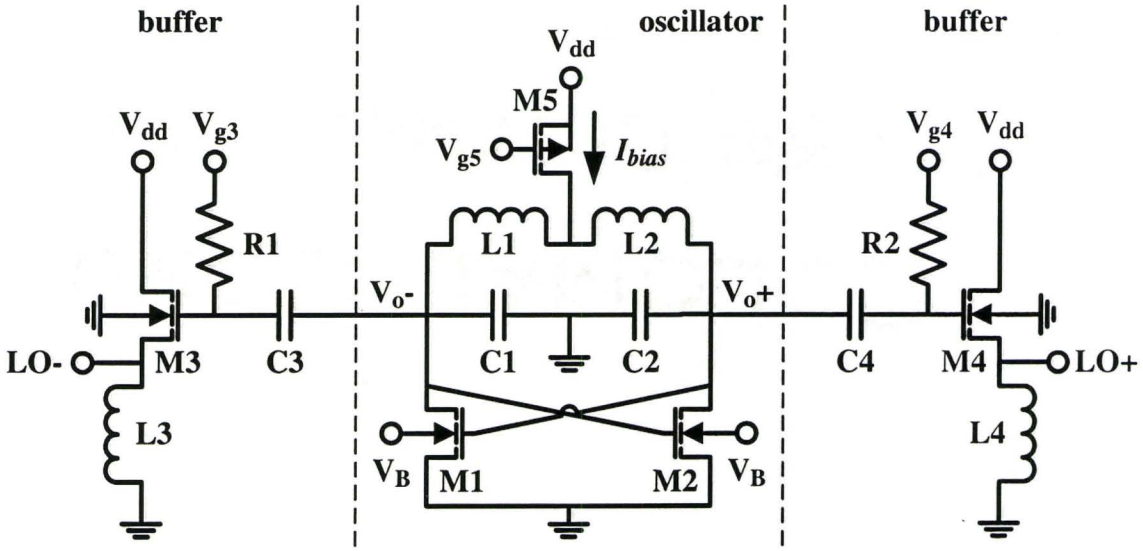


Figure 5.17 Schematic diagram of the nMOSFET cross-coupled differential LC oscillator with a pMOSFET as the bias current transistor.

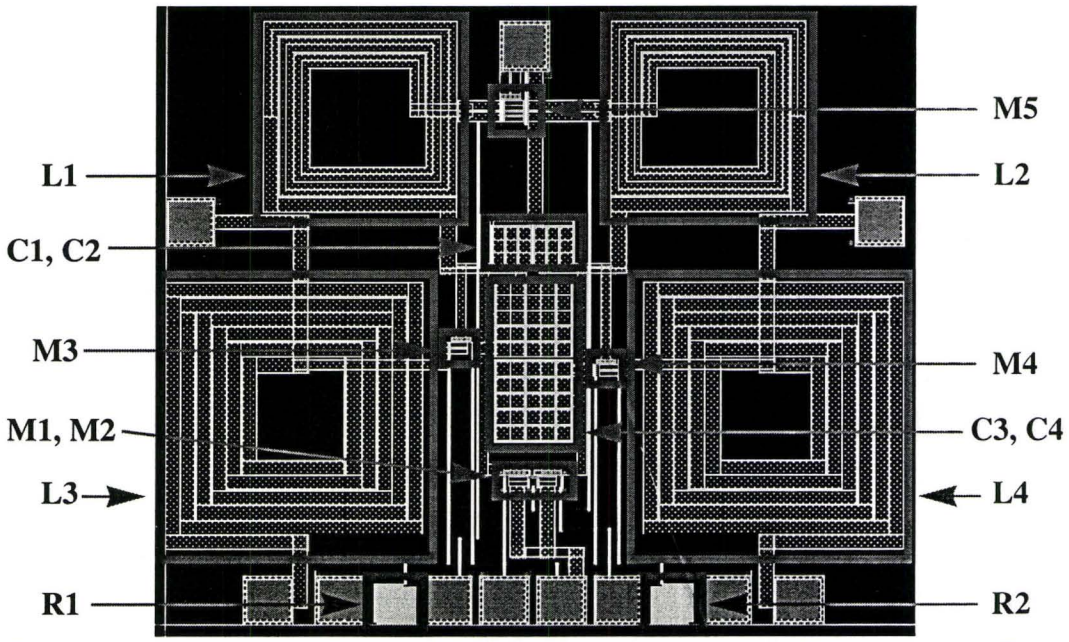


Figure 5.18 Layout of the nMOSFET cross-coupled differential LC oscillator shown in Figure 5.17.

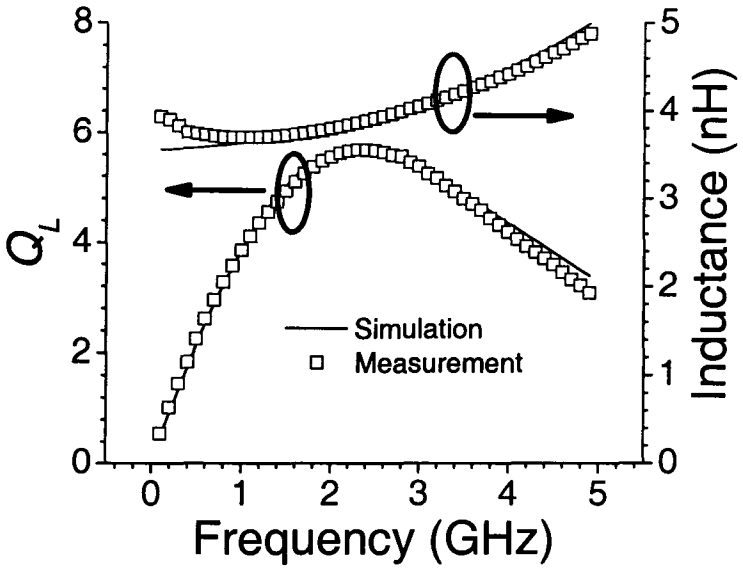


Figure 5.19 Simulated and measured Q_L and inductance of the 2.5 turns quasi-symmetrical rectangular planar spiral inductor.

Table 5.4 Summary of the equivalent circuit model parameter values for the 2.5 turns quasi-symmetrical rectangular planar spiral inductor.

$L_{L,s}$ (nH)	$R_{L,s}$ (Ω)	$C_{L,s}$ (fF)	$C_{L,ox1}$ (fF)	$C_{L,ox2}$ (fF)	$R_{L,sub1}$ (Ω)	$R_{L,sub2}$ (Ω)	$C_{L,sub1}$ (fF)	$C_{L,sub2}$ (fF)
3.036	3.073	5.76	218.1	211	303	265	79.65	62.85

All capacitors used in this design are MIM capacitors, which implies that tuning of f_0 is not possible for this circuit. In addition, as previously discussed in Section 2.2, the $Q_{C,min}$ of MIM capacitors is usually larger than 150 at 2 GHz [51], which is much larger than the $Q_{L,max}$ of the spiral inductors used in this design. Therefore, the Q_{tk} of this design is limited by the Q_L of the spiral inductors. The resistors R1 and R2 are implemented with n-well diffusion in the p-substrate, which are used to provide a DC bias to the gate of the source followers.

The design of this oscillator followed the analysis, discussion and equations presented in Chapter 3, particularly Section 3.3.1 for nMOS topology. The circuit was simu-

lated in Spectre and implemented using the devices summarized in Table 5.5. In fact, this circuit is almost same as the LC oscillator that was designed by Sasan Naseh, another graduate student in our group, which was used to investigate the effects of hot-carrier stress on the performance of the LC tank CMOS oscillators [100]. The only difference is this design does not have the additional capacitors and resistors between the hot nodes of the oscillator (V_o+ and V_o-) and the gate of M1 and M2, which are used to provide hot-carrier stress on M1 and M2 [100]. Therefore, this design has already demonstrated that it worked properly [100]. As a result, to simplify the analysis of this research, the effects of channel length fluctuation on the performance of the LC oscillator will be based on only the simulation results. Consequently, the circuit was simulated without the buffers since they are only for measurement purposes, and thus, the devices summarized in Table 5.5 only includes those that are for the LC oscillator.

Table 5.5 Summary of the devices used in the nMOSFET cross-coupled differential LC oscillator.

Active Device – nMOSFET				
Name	Number of fingers	W_g (μm)	L_g (μm)	
M1, M2	10	100	0.3	
Active Device – pMOSFET				
Name	Number of fingers	W_g (μm)	L_g (μm)	
M5	20	200	1	
Passive Device – Capacitor				
Name	Type	Capacitance (pF)	Area (μm^2)	
C1, C2	MIM Capacitor	5.985	6790	
Passive Device – Inductor				
Name	Type	Inductance (nH)	Series Resistance	Area (μm^2)
L1, L2	Spiral Inductor	3.036	3.073	153000

5.2.2 Simulation Results

The channel length of M_1 and M_2 were set equal to each other as the circuit is a symmetrical differential circuit with the assumption of both M_1 and M_2 were being placed very close to each other so that they have the same amount of channel length fluctuations [101]. With 0.3 μm as the reference channel length at the circuit design and simulation stages, four other values – 0.25 μm, 0.28 μm, 0.32 μm and 0.35 μm – were used as possible fabricated channel lengths.

The circuit was simulated with $V_{dd} = 1.8$ V, $V_{g5} = 0.5$ V and $V_B = 0$ V. Figure 5.20 shows the current consumption of this oscillator for the reference channel length and its variation with different channel lengths. The simulated results, for the reference channel length, show that the current consumption is 3.599 mA, which corresponds to a P_{con} of 6.479 mW. Also, the current and power consumptions are found to be approximately constant since they only vary in the order of μA and μW for all values of tested channel lengths. This is expected since a bias current transistor M5 was used to control the I_{bias} and a relatively large L_g, 1 μm, was used for this bias current transistor to minimize the channel-length modulation effect, which further enhances the stability of the current and power consumptions.

From Chapter 3, the f_0 of this oscillator can be estimated by:

$$f_0 = \frac{1}{2\pi\sqrt{L_{s1}(C_1 + C_{gs1} + 4C_{gd1})}}. \tag{5.3}$$

However, because of the parasitic drain-body capacitance C_{db} of M1 and M2 will be utilized in this design, which will be discussed later. Also, the parasitic drain-body capacitance of M1 C_{db1} is same as the parasitic drain-body capacitance of M2 C_{db2} since M1 and M2 have the same size and this is a symmetrical differential circuit. Therefore, a more precise expression of Equation (5.3) is [101]

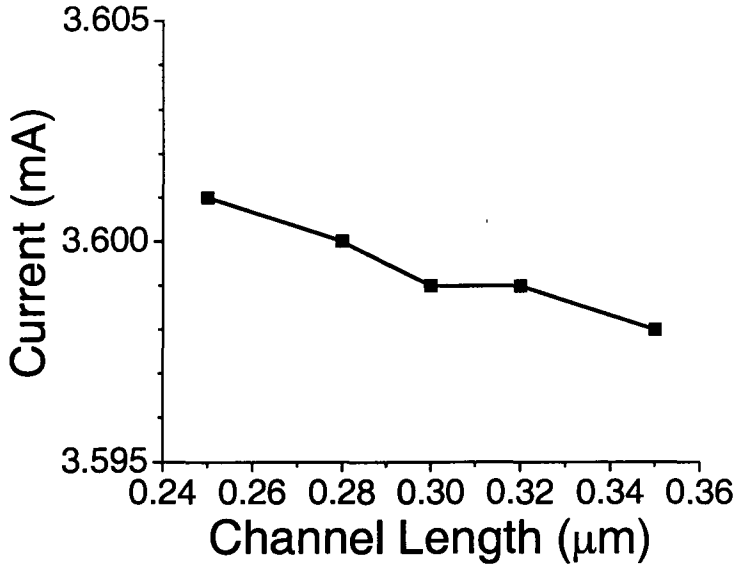


Figure 5.20 Variation of current consumption due to channel length fluctuations.

$$f_0 = \frac{1}{2\pi\sqrt{L_{s1}(C_1 + C_{gs1} + 4C_{gd1} + C_{db1})}}. \tag{5.4}$$

The f_0 of this oscillator is about 1.12 GHz with the reference channel length and its variation with different channel lengths is shown in Figure 5.21. It can be observed from this figure that the maximum variation of f_0 is 2.45 kHz with less than 20% of variation in channel length. Also, from Figure 5.19, the L_{tk} and Q_L, which is approximately same as Q_{tk}, are approximately constant within this amount of f_0 variation at 1.12 GHz. Moreover, the capacitance of the MIM capacitors are fixed. Therefore, the variation of the f_0 is due to the variation of the C_{gs} of M1 and M2 since C_{gs} is the only $C_{parasitic}$ affected by the channel length among C_{gs}, C_{gd} and C_{db} when M1 and M2 are operating in the saturation region [15], [17]. It should be noted that since L_{s1} = 3.036 nH and C_1 = 5.985 pF in this design, which corresponds to a f_0 of 1.18 GHz, the sum of C_{gs1}, $4C_{gd1}$ and C_{db1} must be equal 0.67 pF so that the f_0 is 1.12 GHz instead of 1.18 GHz.

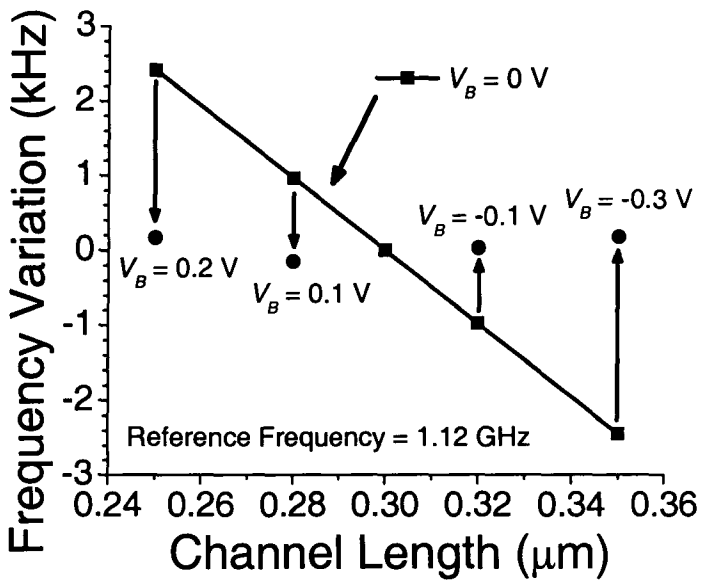


Figure 5.21 Variation of f_0 due to channel length fluctuations with compensation achieved by applying appropriate V_B to the MOSFETs.

From Figure 5.21, it can also be seen that the f_0 decreases with an increase of channel length while the current does not change. This is expected and can be predicted from a modification of Equation (5.4):

$$\Delta f_0 = \frac{1}{2\pi\sqrt{L_{s1}}}\left(\frac{1}{\sqrt{C_t + C_{gs1,fab}}} - \frac{1}{\sqrt{C_t + C_{gs1,design}}}\right), \tag{5.5}$$

where

$$C_{gs1,fab} = C_{gs1,design}\left(\frac{L_{eff,fab}}{L_{eff,design}}\right), \tag{5.6}$$

$C_t = C_l + 4C_{gdl} + C_{dbl}$, $C_{gsl,fab}$ and $L_{eff,fab}$ are the C_{gsl} and effective channel length after fabrication, respectively, and $C_{gsl,design}$ and $L_{eff,design}$ are the C_{gsl} and effective channel length at the design and simulation stages, respectively. When $L_{eff,fab}$ is larger than $L_{eff,design}$, from Equation (5.6), the first term inside the bracket of Equation (5.5) is smaller than the second term which makes Δf_0 become negative, i.e. frequency decreases. Moreover, it can

be observed from Figure 5.21 that the magnitude of f_0 variation is nearly the same when the channel length is increased or decreased by the same amount. These variations of f_0 due to channel length fluctuations, fortunately, can be compensated by applying appropriate bias voltage to the body of the nMOSFETs V_B, which changes C_{db}, while the changes of current consumption is negligible since it only varies in the order of 10 μA. For instance, when channel length is increased from 0.3 μm to 0.32 μm, the decreases of the f_0 can be compensated by applying -0.1 V to V_B, which decreases C_{db} and thus increases the f_0, and this is shown in Figure 5.21. Different values of V_B used to compensate the f_0 for each value of channel length are also shown in Figure 5.21.

Equation (5.5), in fact, contains other important information for designers in addition to predicting the variation of f_0 due to channel length fluctuations. To illustrate this, assume there are two LC oscillators utilizing the topology shown in Figure 5.17, and the L_{tk} and Q_{tk} are constant within the amount of f_0 variation due to channel length fluctuations for both oscillators such that the variation of the f_0 is due to the variation of the C_{gs1}. Consequently, the amount of f_0 variation only depends on C_t and C_{gs1}. Also, assume $C_{gs1,design}$ = 0.1 pF for both oscillators, and C_t = 4 pF and 1 pF for the first and the second oscillators, respectively, such that the first oscillator has a lower f_0 than the second one. Figure 5.22 illustrates the variation of f_0 due to channel length fluctuations for these two oscillators. It can be clearly seen from this figure that the second oscillator, which has C_t = 1 pF and higher f_0, has a larger amount of f_0 variation than the first one when the channel length is increased or decreased by the same amount. This phenomenon is reasonable because decreasing C_t to increase f_0 would make C_{gs1} dominate the terms inside the bracket of Equation (5.5), and thus, the f_0 is more sensitive to the channel length fluctuations. Therefore, to minimize the sensitivity of f_0 to channel length fluctuations, it is recommended that the C_{gs1} should be made as small as possible compared to C_t. Also, if oscillators with high f_0 is desired, it is better to achieve the high f_0 by decreasing L_{s1} instead of C_t.

The P_{out} of this oscillator to a 50 Ω load is 1.79 dBm for the reference channel length and its variation with different channel lengths is shown in Figure 5.23. From this figure, it can be observed that the maximum variation of P_{out} is 0.08 dBm with less than

20% of variation in the channel length. Also, it can be seen from the same figure that the P_{out} decreases with an increase of channel length while the current does not change. This is expected and can be predicted from a modification of Equation (5.1):

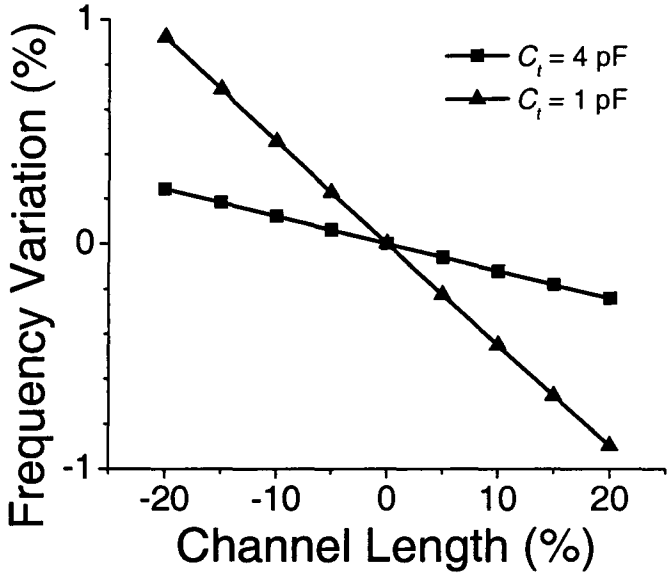


Figure 5.22 Illustration of the variation of f_0 due to channel length fluctuations. The oscillator with smaller C_t, and thus, higher f_0 is more sensitive to channel length fluctuations.

$$\Delta V_{osc} = \sqrt{L_{tk}} Q_{tk} I_{bias} \left(\frac{1}{\sqrt{C_t + C_{gs1,fab}}} - \frac{1}{\sqrt{C_t + C_{gs1,design}}} \right). \tag{5.7}$$

When $L_{eff,fab}$ is larger than $L_{eff,design}$, from Equation (5.6), the first term inside the bracket of Equation (5.7) is smaller than the second term which makes ΔV_{osc} become negative, i.e. V_{osc} and thus P_{out} decreases. It should be noted that this modification of Equation (5.1) is valid because, as previously discussed, the L_{tk}, Q_{tk} and I_{bias} are approximately constant within the range of f_0 variation. Also, the decreases of f_0 when channel length increases is due to the increases of C_{tk}.

It can also be observed from Figure 5.23 that when the channel length is increased or decreased by the same amount, the magnitude of P_{out} variation is approximately the

same. To compensate for these variations of P_{out} due to channel length fluctuations, the same bias voltages that are applied to V_B to compensate for the variations of f_0 of each channel length are used. This is because the main purpose of an oscillator is to generate a signal at a specified frequency. Therefore, an oscillator is not useful if it cannot produce the requested frequency accurately even it has a very large P_{out}. It can be seen from Figure 5.23 that when the channel length is larger than the reference channel length, applying a reverse body bias to the nMOSFETs not only compensates the drop in P_{out} but also provide a gain. However, when the channel length is smaller than the reference channel length, having the body of the nMOSFETs forward biased makes the P_{out} smaller than the reference channel length with $V_B = 0$ V.

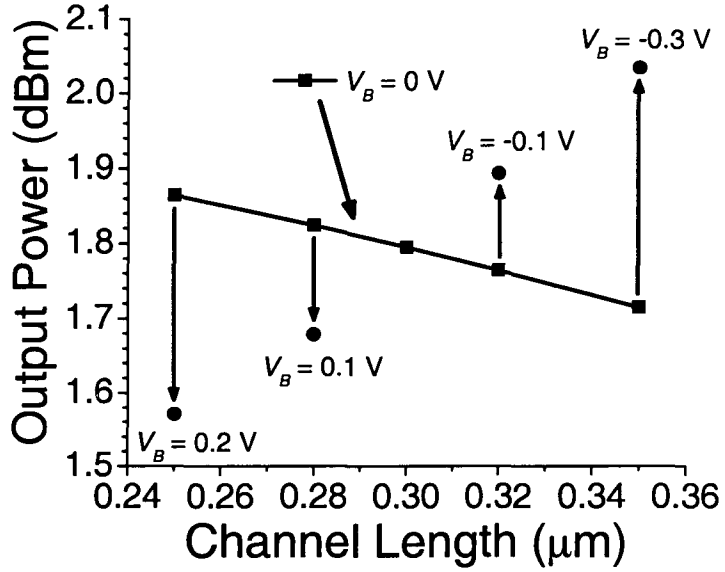


Figure 5.23 Variation of P_{out} due to channel length fluctuations. The effects of applying different V_B to the MOSFETs are also shown.

Similar to the f_0, Equation (5.7) holds other important information for designers despite predicting the variation of P_{out} due to channel length fluctuations. To illustrate this, in addition to the assumptions stated before for the analysis of the sensitivity of f_0 to channel length fluctuations, it is also assumed that the I_{bias} is constant within the amount of f_0 variation due to channel length fluctuations for both oscillators such that the variation of

the P_{out} is due to the variation of the C_{gs1}. Therefore, the amount of P_{out} variation only depends on C_t and C_{gs1}, which is the same condition for the analysis of the sensitivity of f_0 to channel length fluctuations. Consequently, the second oscillator, which has C_t = 1 pF and higher f_0, has a larger amount of P_{out} variation than the first one when the channel length is increased or decreased by the same amount. This is because increasing f_0 by decreasing the C_t would make C_{gs1} dominate the terms inside the bracket of Equation (5.7), and thus, the P_{out} is more sensitive to the channel length fluctuations. Therefore, to minimize the sensitivity of P_{out} to channel length fluctuations, it is recommended to reduce the ratio of the C_{gs1} to the C_t as much as possible. Also, if oscillators with high f_0 is required, it is better to obtain the high f_0 by decreasing L_{s1} instead of C_t. However, from Equation (5.1), decreasing L_{s1} would decrease P_{out}, which is not desirable. Therefore, to compensate for the losses in P_{out} due to the decreases of L_{s1}, either the I_{bias} should be increased or the Q_{tk} should be enhanced. However, increasing the I_{bias} would increase the P_{con}, which is not desirable. As for enhancing the Q_{tk}, it would not adversely affect any performance characteristics of oscillators. As a result, to achieve high f_0 without degrading the P_{out} and at the same time minimizing the sensitivity of P_{out} to channel length fluctuations, it is recommended to decrease the L_{tk}, enhance the Q_{tk}, and reduce the ratio of the C_{gs1} to the C_t.

The variation of $L\{\Delta\omega\}$ with different channel lengths was initially predicted by using Equation (3.15), which is repeated here for convenience:

$$L\{\Delta\omega\} = \frac{kTR_{eff}(1 + O_{ssf})\left(\frac{\omega_0}{\Delta\omega}\right)^2}{V_{osc}^2/2}. \tag{5.8}$$

In this expression, Q_{tk}, and thus, R_{eff} is approximately constant within the range of f_0 variation as previously discussed. Also, k and T are the Boltzmann's constant and temperature in degrees Kelvin, respectively, which are constant. Moreover, O_{ssf} is the oscillation startup safety factor, which is fixed after the sizes of the M1 and M2 are decided. Furthermore, $\Delta\omega$ is the offset frequency at which the $L\{\Delta\omega\}$ is characterized, which is not related to the channel length of the M1 and M2. Therefore, only V_{osc} and f_0, and thus, ω_0 are affected by

channel length fluctuations. Consequently, it should be possible to estimate the variation of $L\{\Delta\omega\}$ due to channel length fluctuations by performing the algebraical derivation similar to those that were done for f_0 and V_{osc}. However, such algebraical derivation, which yields:

$$\Delta L\{\Delta\omega\} = 2kTR_{eff}(1 + O_{ssf})\left(\frac{1}{\Delta\omega L_{tk} Q_{tk} I_{bias}}\right)^2, \tag{5.9}$$

shows that the channel length fluctuations do not affect the $L\{\Delta\omega\}$. This result is not correct because Equation (5.8) is essentially equivalent to the Leeson's model, i.e. the upconversion of $1/f$ device noise into low offset frequency phase noise is not considered [73]. Also, the channel length of MOSFET affects the low frequency $1/f$ current noise of the device with a 1/(channel length)^3 relationship [102], which will therefore affect the low offset frequency phase noise [74], [75]. Therefore, the variation of $L\{\Delta\omega\}$ with different channel lengths was found out by simulation. Unfortunately, simulation result does not show a significant dependence of low offset frequency phase noise on channel length while it should be. This discrepancy is believed to be caused by the inaccuracy of the phase noise simulation.

The accuracy of the phase noise simulation was tested by changing the $1/f$ noise parameter *kf* in the MOSFET model to simulate the $L\{\Delta\omega\}$ of this circuit, which should have significant effects on the low offset frequency phase noise. For example, a phase noise simulation was performed for this circuit using the reference channel length and the original values of *kf* for both the nMOSFET (4.0×10^{-29}) and pMOSFET (6.1×10^{-28}), then the phase noise simulation was performed again with the *kf* of pMOSFET changed from 6.1×10^{-28} to 6.1×10^{-20}. However, the simulation results show that the $L\{\Delta\omega\}$ are -65.610 dBc/Hz and -65.609 dBc/Hz for these two cases, respectively, at an offset frequency of 1 kHz. It can be clearly seen that the simulation results for the $L\{\Delta\omega\}$ at a low offset frequency of 1 kHz did not show significant changes even though the *kf* of pMOSFET has been changed several orders of magnitude with respect to its original value. More testing on the accuracy of the phase noise simulation have been performed. The detail and the results of these testing can be found in Appendix B. However, all the simulation results show that

the there was no significant dependence of $L\{\Delta\omega\}$ on the values of kf. Therefore, it can be concluded that the phase noise simulation is inaccurate for low offset frequency phase noise. Consequently, solutions for the inaccuracy of the phase noise simulation must be sorted in the future.

Chapter 6

Conclusions and Future Work

During the course of this work, much has been learnt about circuit design for RFICs. The experience gained by going through the whole design cycle was invaluable. Learning and understanding new simulation tools, and device and circuit theory were challenging and exciting; design, simulation, optimization and layout of a circuit were time consuming and interesting; measurement of a fabricated design was distressing but satisfying the designs worked properly.

Having this research work focused on the mismatch effects of MOSFETs on RFICs made it become more amazing. This is because identical devices should be obtained by simply "click and copy" during the layout of the design. However, in reality, matching is not that simple due to unavoidable fabrication process variation, which can cause a large deviation of the circuit performance.

6.1 CONCLUSIONS

In this thesis, the effects of channel length fluctuation on the performance of RF oscillators were investigated. Two fully integrated, cross-coupled, differential LC oscillators were designed in TSMC triple-well 0.18 μm standard CMOS technology [8] and used as the test circuits. Although the first VCO could not be used for the analysis of channel length fluctuation effects due to different types of varactor were used in the simulation and fabrication, the difference between the simulated and measured f_{min}, which was 1.01 GHz, providing a good example that the fabrication process variation could lead to a large circuit performance deviation. Nevertheless, this VCO was found to have the following characteristics.

- A frequency tuning range of 21.7% and 23.9% when it was measured at a V_{dd} of 1.8 V and 1.5 V, respectively. This relatively large frequency tuning range was achieved by using two pairs of nAMOS varactor instead of one pair.
- A current consumption of less than 1 mA for both V_{dd} of 1.8 V and 1.5 V, which corresponds to a P_{con} of less than 1.8 mW and 1.5 mW, respectively.
- The current and power consumptions were approximately constant for both V_{dd} of 1.8 V and 1.5 V since a bias current transistor was used to control the I_{bias}. Also, a relatively large L_g was used for this bias current transistor to minimize the channel-length modulation effect, which further enhances the stability of the current and power consumptions.
- A P_{out} of -13.3 dBm and a P_{con} of 1.31 mW with a f_0 of 5.506 GHz when it was measured with $V_{C1} = 0$ V and $V_{C2} = 1.6$ V at $V_{dd} = 1.5$ V, which corresponds to a $L\{\Delta\omega\}$ of -121.2 dBc/Hz at 1 MHz offset frequency.
- A FoM of 176.4 dB, which is higher compared to other oscillators listed in Table 5.3. This higher FoM is achieved mainly by lowering the P_{con} considerably, while still able to maintain acceptable level of performance.

The second oscillator was designed using only devices that have proper model for simulation. The simulated results were used to analyze the effects of channel length fluctuation on the performance of RF oscillators. It was found that:

- The current consumption was 3.599 mA for the reference channel length when simulated at $V_{dd} = 1.8$ V, which corresponds to a P_{con} of 6.479 mW. Also, the current and power consumptions were found to be approximately constant for all values of tested channel lengths, which was expected since a bias current transistor was used to control the I_{bias} and a relatively large L_g was used for this bias current transistor to minimize the channel-length modulation effect, which further enhances the stability of the current and power consumptions.

- The f_0 was 1.12 GHz with the reference channel length and it decreases with an increase of channel length while the current does not change. The maximum variation of f_0 was 2.45 kHz with less than 20% of variation in the channel length. A formula was derived to explain and predict the variation of f_0 due to channel length fluctuations.
- The variation of f_0 due to channel length fluctuations is more significant in oscillators with higher f_0. To minimize the sensitivity of f_0 to channel length fluctuations, it is recommended to reduce the ratio of the C_{gs1} to the C_t. Also, if oscillators with high f_0 is desired, it is better to achieve the high f_0 by decreasing L_{s1} instead of C_t.
- The use of body bias on the MOSFETs was proposed as a means to compensate for the changes in the frequency performance characteristics due to the channel length fluctuations.
- The P_{out} to a 50 Ω load was 1.79 dBm for the reference channel length and its maximum variation was 0.08 dBm with less than 20% variation in the channel length. Also, it decreases with an increase of channel length while the current does not change. The variation of P_{out} due to channel length fluctuations was explained and predicted by a derived new formula.
- The variation of P_{out} due to channel length fluctuations is more significant in oscillators with higher f_0. To achieve high f_0 without degrading the P_{out} and at the same time minimizing the sensitivity of P_{out} to channel length fluctuations, it is recommended to decrease the L_{tk}, enhance the Q_{tk}, and reduce the ratio of the C_{gs1} to the C_t.
- The low offset frequency phase noise was expected to be affected by the channel length fluctuations. This is because the channel length of MOSFET affects the low frequency $1/f$ current noise of the device with a 1/(channel length)^3 relationship [102], which will therefore affect the low offset frequency phase noise [74], [75]. However, simulation result did not show a significant dependence of the low offset frequency

phase noise on channel length. This discrepancy is believed to be caused by the inaccuracy of the phase noise simulation.

6.2 FUTURE WORK

There are two main future works for this research. The most obvious one is to find out the causes and the solutions for the inaccuracy of the phase noise simulation at low offset frequencies. This is not only important for the analysis of the variation of $L\{\Delta\omega\}$ due to channel length fluctuations but also the regular design of oscillators.

The second main future work is to obtain an accurate model for the nAMOS varactor so that simulation of the first VCO can be performed with the proper device model, and thus, comparison between the simulated and measured results is possible. Consequently, the effects of channel length fluctuation on the performance of LC oscillators can be analyzed using the first VCO designed for this research. Also, having the model of nAMOS varactor available will allow the use of nAMOS varactor in future designs easier.

Another possible future work is to improve the accuracy of the nMOSFET model, especially when deep n-well is used to isolate the p-well from the p-substrate so that different potentials can be applied to the body of different nMOSFETs on the same chip. The accuracy of the nMOSFET model with the application of deep n-well is suspected because there are design rules for the layout of the deep n-well regarding only the minimum dimensions but not the maximum [8]. Also, there is no options on the simulation software, which allow designers to specify the dimensions of the deep n-well that are going to be used in their designs. However, the capacitance and current for the pn junctions between the p-well and deep n-well, and p-substrate and deep n-well are directly related to the size of the deep n-well used, and thus, will affect the characteristics of nMOSFETs.

The deviation of performance characteristics for LC oscillators due to channel length fluctuations has been investigated in this research. However, the effects of channel length fluctuation on the performance of other differential RFICs such as mixers and LNAs are still have not been examined. Therefore, more research can be conducted for other dif-

ferential RFICs. Also, the deviation of performance characteristics caused by other process variations such as uneven oxide thicknesses and inconsistent doping concentration will be also valuable.

Appendix A

Series-Parallel Transformations for RC and RL Networks

For a resistance-capacitance (RC) network connected in series, as shown in Figure A.1(a), the impedance $Z_{C,s}$ is

$$Z_{C,s} = R_{C,s} - \frac{j}{\omega C_s}, \tag{A.1}$$

the admittance $Y_{C,s}$ is

$$Y_{C,s} = \frac{1}{R_{C,s}} \| j\omega C_s = \frac{j\omega C_s}{1 + j\omega C_s R_{C,s}} = \frac{(\omega C_s)^2 R_{C,s}}{1 + (\omega C_s R_{C,s})^2} + \frac{j\omega C_s}{1 + (\omega C_s R_{C,s})^2} \tag{A.2}$$

and the quality factor $Q_{C,s}$ is

$$Q_{C,s} = \frac{1}{\omega C_s R_{C,s}}. \tag{A.3}$$

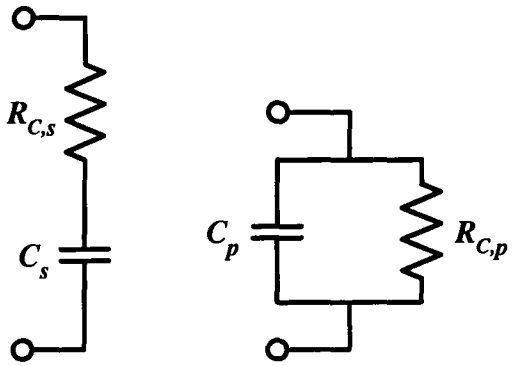


Figure A.1 RC network connected in (a) series and (b) parallel.

For a RC network connected in parallel, as shown in Figure A.1(b), the impedance $Z_{C,p}$ is

$$Z_{C,p} = R_{C,p} \| \frac{1}{j\omega C_p} = \frac{R_{C,p}}{1 + j\omega C_p R_{C,p}} = \frac{R_{C,p}}{1 + (\omega C_p R_{C,p})^2} - \frac{j\omega C_p R_{C,p}^2}{1 + (\omega C_p R_{C,p})^2}, \quad \text{(A.4)}$$

the admittance $Y_{C,p}$ is

$$Y_{C,p} = \frac{1}{R_{C,p}} + j\omega C_p \quad \text{(A.5)}$$

and the quality factor $Q_{C,p}$ is

$$Q_{C,p} = \omega C_p R_{C,p}. \quad \text{(A.6)}$$

Now, assume the values of $R_{C,p}$ and C_p are known and the equivalent RC network connected in series is used. The equivalent series resistance $R_{C,s,eq}$ can be found by equating $Re(Z_{C,s}) = Re(Z_{C,p})$ and solving for $R_{C,s}$ as follows:

$$R_{C,s,eq} = \frac{R_{C,p}}{1 + (\omega C_p R_{C,p})^2} = R_{C,p}\left(\frac{1}{1 + Q_{C,p}^2}\right) \quad \text{(A.7)}$$

and the equivalent series capacitance $C_{s,eq}$ can be found by equating $Im(Z_{C,s}) = Im(Z_{C,p})$ and solving for C_s as follows:

$$-\frac{1}{\omega C_{s,eq}} = -\frac{\omega C_p R_{C,p}^2}{1 + (\omega C_p R_{C,p})^2} \Rightarrow C_{s,eq} = \frac{1 + (\omega C_p R_{C,p})^2}{\omega^2 C_p R_{C,p}^2} = C_p\left(\frac{1 + Q_{C,p}^2}{Q_{C,p}^2}\right). \quad \text{(A.8)}$$

Similarly, if the values of $R_{C,s}$ and C_s are known and the equivalent RC network connected in parallel is used, the equivalent parallel resistance $R_{C,p,eq}$ and capacitance $C_{p,eq}$ can be found by equating $Re(Y_{C,p}) = Re(Y_{C,s})$ and $Im(Y_{C,p}) = Im(Y_{C,s})$ and solving for $R_{C,p}$ and C_p, respectively, as follows:

$$\frac{1}{R_{C,p,eq}} = \frac{(\omega C_s)^2 R_{C,s}}{1+(\omega C_s R_{C,s})^2} \Rightarrow R_{C,p,eq} = \frac{1+(\omega C_s R_{C,s})^2}{(\omega C_s)^2 R_{C,s}} = R_{C,s}(1+Q_{C,s}^2) \quad \text{(A.9)}$$

$$\omega C_{p,eq} = \frac{\omega C_s}{1+(\omega C_s R_{C,s})^2} \Rightarrow C_{p,eq} = \frac{C_s}{1+(\omega C_s R_{C,s})^2} = C_s\left(\frac{Q_{C,s}^2}{1+Q_{C,s}^2}\right). \quad \text{(A.10)}$$

The same method can be applied to a resistance-inductance (RL) network connected in series or parallel to find its equivalent parallel or series resistance and inductance, respectively. For a RL network connected in series, as shown in Figure A.2(a), the impedance $Z_{L,s}$, the admittance $Y_{L,s}$ and the quality factor $Q_{L,s}$ are

$$Z_{L,s} = R_{L,s} + j\omega L_s, \quad \text{(A.11)}$$

$$Y_{L,s} = \frac{1}{R_{L,s}} \| \frac{1}{j\omega L_s} = \frac{1}{R_{L,s}+j\omega L_s} = \frac{R_{L,s}}{R_{L,s}^2+(\omega L_s)^2} - \frac{j\omega L_s}{R_{L,s}^2+(\omega L_s)^2} \quad \text{(A.12)}$$

and

$$Q_{L,s} = \frac{\omega L_s}{R_{L,s}}, \quad \text{(A.13)}$$

respectively.

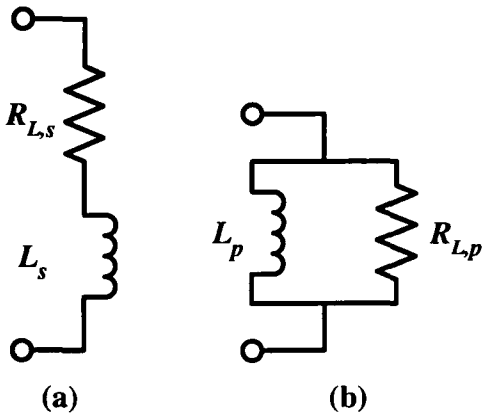


Figure A.2 RL network connected in (a) series and (b) parallel.

For a RL network connected in parallel, as shown in Figure A.2(b), the impedance $Z_{L,p}$, the admittance $Y_{L,p}$ and the quality factor $Q_{L,p}$ are

$$Z_{L,p} = R_{L,p} \| j\omega L_p = \frac{j\omega L_p R_{L,p}}{R_{L,p} + j\omega L_p} = \frac{(\omega L_p)^2 R_{L,p}}{R_{L,p}^2 + (\omega L_p)^2} + \frac{j\omega L_p R_{L,p}^2}{R_{L,p}^2 + (\omega L_p)^2}, \quad \text{(A.14)}$$

$$Y_{L,p} = \frac{1}{R_{L,p}} - \frac{j}{\omega L_p} \quad \text{(A.15)}$$

and

$$Q_{L,p} = \frac{R_{L,p}}{\omega L_p}, \quad \text{(A.16)}$$

respectively.

Therefore, to find the equivalent series resistance $R_{L,s,eq}$ and inductance $L_{s,eq}$, equate $Re(Z_{L,s}) = Re(Z_{L,p})$ and $Im(Z_{L,s}) = Im(Z_{L,p})$ and solve for $R_{L,s}$ and L_s, respectively, as follows:

$$R_{L,s,eq} = \frac{(\omega L_p)^2 R_{L,p}}{R_{L,p}^2 + (\omega L_p)^2} = \frac{R_{L,p}}{1 + (R_{L,p}/\omega L_p)^2} = R_{L,p}\left(\frac{1}{1 + Q_{L,p}^2}\right) \quad \text{(A.17)}$$

$$\omega L_{s,eq} = \frac{\omega L_p R_{L,p}^2}{R_{L,p}^2 + (\omega L_p)^2} \Rightarrow L_{s,eq} = \frac{R_{L,p}^2/\omega^2 L_p}{1 + (R_{L,p}/\omega L_p)^2} = L_p\left(\frac{Q_{L,p}^2}{1 + Q_{L,p}^2}\right). \quad \text{(A.18)}$$

Similarly, to find the equivalent parallel resistance $R_{L,p,eq}$ and inductance $L_{p,eq}$, equate $Re(Y_{L,p}) = Re(Y_{L,s})$ and $Im(Y_{L,p}) = Im(Y_{L,s})$ and solve for $R_{L,p}$ and L_p, respectively, as follows:

$$\frac{1}{R_{L,p,eq}} = \frac{R_{L,s}}{R_{L,s}^2 + (\omega L_s)^2} \Rightarrow R_{L,p,eq} = \frac{1 + (\omega L_s/R_{L,s})^2}{1/R_{L,s}} = R_{L,s}(1 + Q_{L,s}^2) \quad \text{(A.19)}$$

$$-\frac{1}{\omega L_{p,eq}} = -\frac{\omega L_s}{R_{L,s}^2 + (\omega L_s)^2} \quad \Rightarrow \quad L_{p,eq} = \frac{1 + (\omega L_s / R_{L,s})^2}{\omega^2 L_s / R_{L,s}^2} = L_s\left(\frac{1 + Q_{L.s}^2}{Q_{L.s}^2}\right). \quad \text{(A.20)}$$

Appendix B

Testing on Accuracy of Phase Noise Simulation

The details, procedures and results of testing the accuracy of phase noise simulation are reported at below.

1. An LC oscillator was simulated in the schematic level and its schematic diagram is shown in Figure B.1.

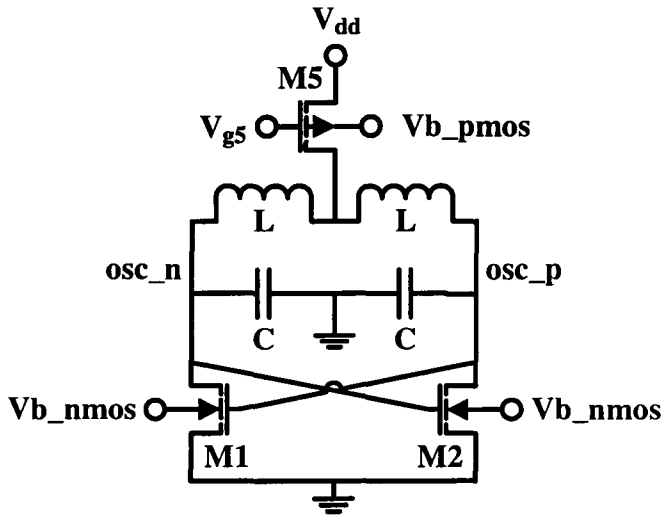


Figure B.1 Schematic diagram of the LC oscillator simulated for testing the accuracy of phase noise simulation.

2. The values used in the oscillator are listed at below:

   - L = 3.036 nH. This is actually a symbol of the modified two-port lumped physical model for quasi-symmetrical spiral inductor shown in Figure 5.3. The equivalent circuit model parameter values listed in Table 5.4 were used.

- C = 5.985 pF and its *Quality type* was set to *ideal.*
- M5 is a pMOSFET with *Multiplier* = 20, *Width* = 10.0 μm and *Length* = 1.000 μm
- M1 and M2 are nMOSFETs with *Multiplier* = 10, *Width* = 10 μm and *Length* = W*1 μm where W was set to 0.3 on the *Analog Environment*, which makes *Length* = 0.3 μm
- V_{dd} = 1.8 V
- V_{g5} = 500 mV
- *Vb_pmos* = 1.8 V
- *Vb_nmos* = 0 V

3. Figures B.2 to B.10 show the settings that were used for the phase noise simulation, including the *Analog Environment*, *dc analysis*, *tran analysis* (i.e. transient analysis), *pss analysis* (i.e. periodic steady state analysis), *pnoise analysis* (i.e. periodic noise analysis), and their corresponding options.

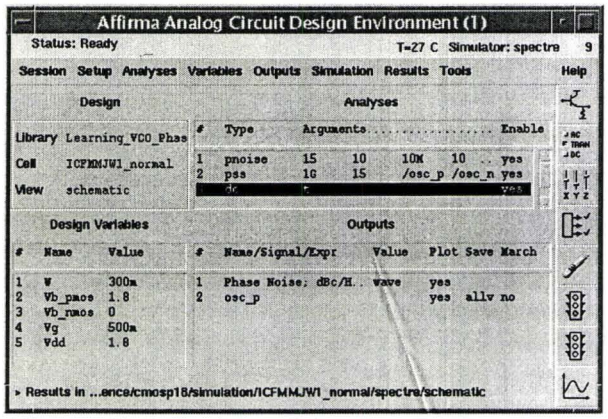


Figure B.2 Setting of *Analog Environment*.

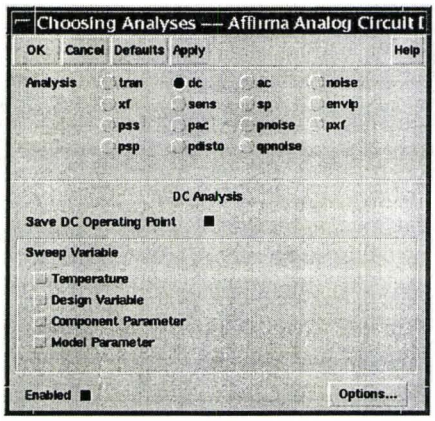


Figure B.3 Setting of *dc analysis*.

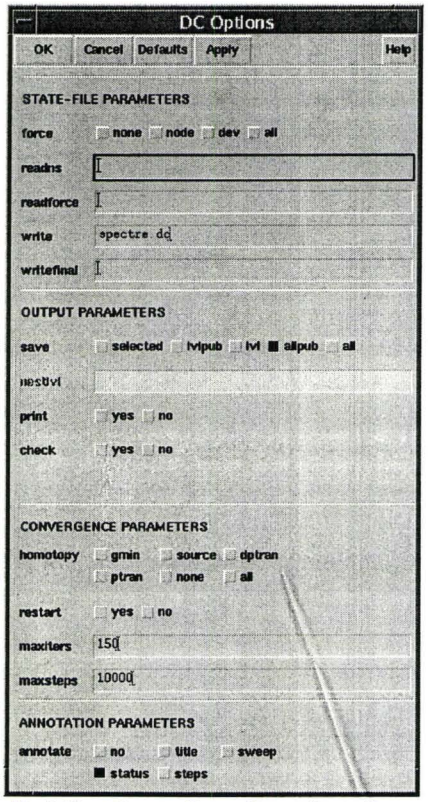


Figure B.4 Setting of *options* for *dc analysis*.

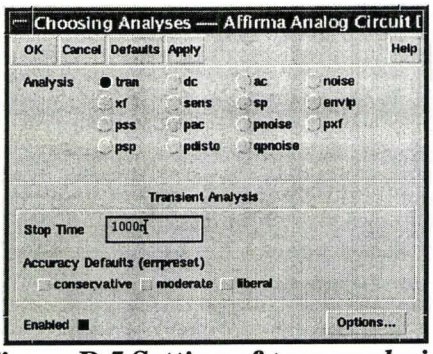
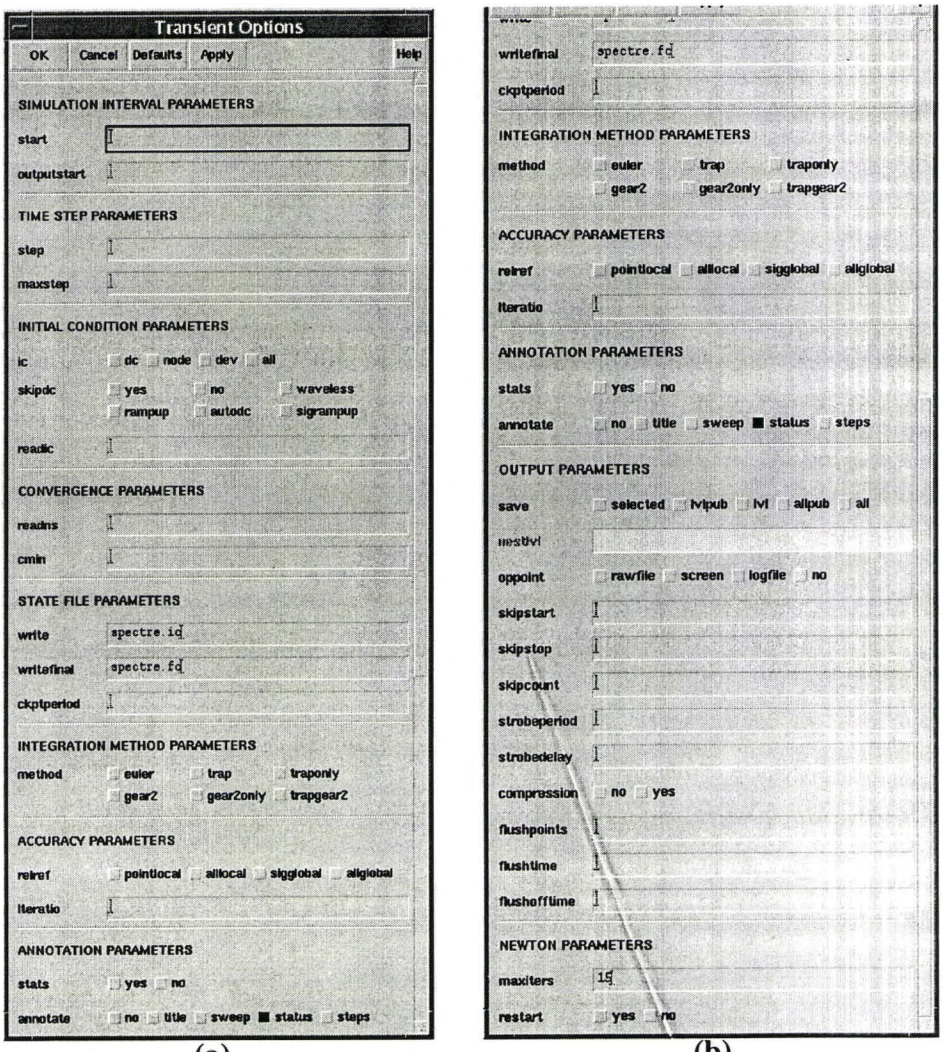


Figure B.5 Setting of *tran analysis*.



(a) (b)

Figure B.6 Setting of *options* for *tran analysis* (a) top half and (b) bottom half.

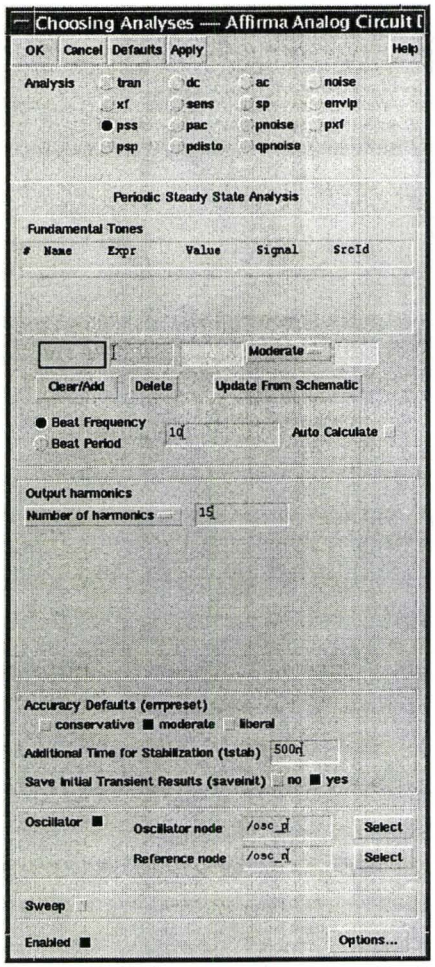


Figure B.7 Setting of *pss analysis*.

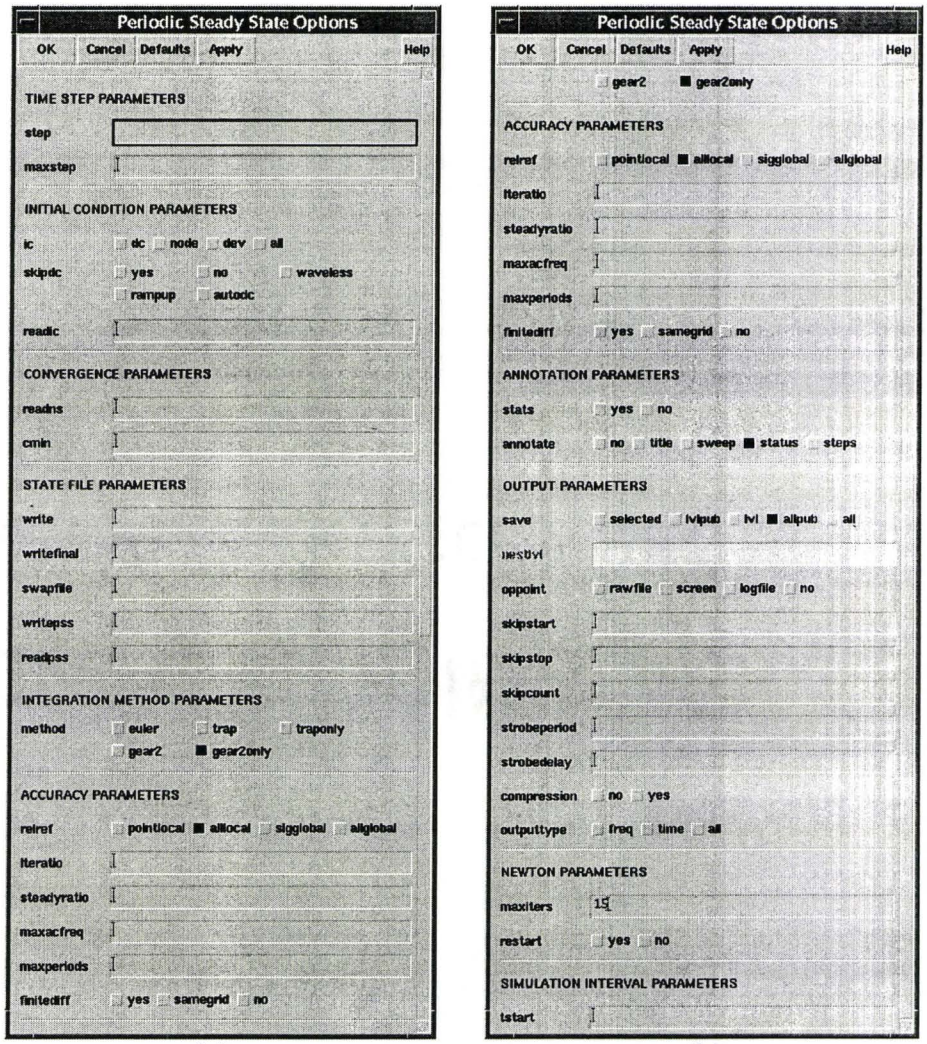


Figure B.8 Setting of *options* for *pss analysis* (a) top half and (b) bottom half.

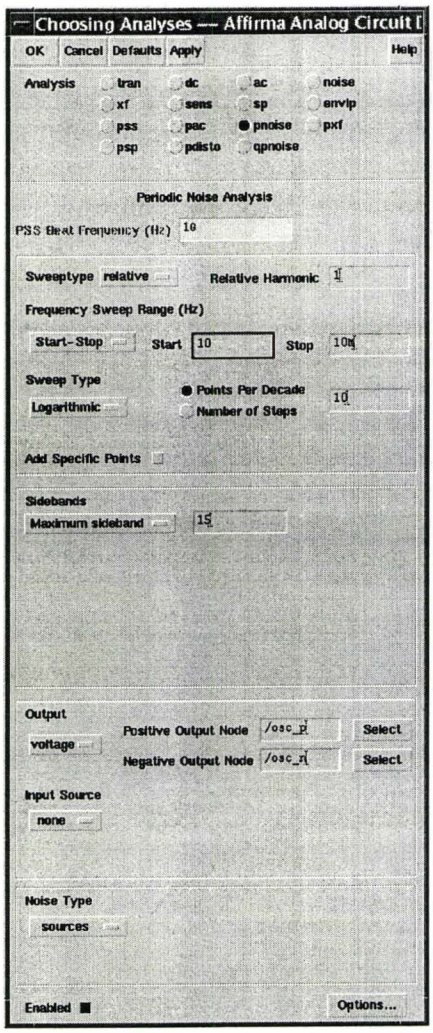


Figure B.9 Setting of *pnoise analysis*.

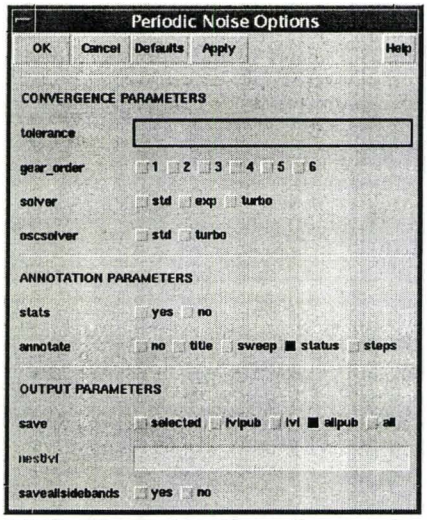


Figure B.10 Setting of *options* for *pnoise analysis*.

4. The procedure of changing the 1/*f* noise parameter *kf* in the MOSFET model are as follow:

   a. The files *icfspectre.init* and *mm018.scs* were copied from the original directory to a new directory.

   b. The values of *kf* in the *mm018.scs* file in the new directory were changed and the file was saved after all the changes were made.

   c. On the *Analog Environment*, the *Model Library File* (opened by choosing *Setup -> Model Libraries...*) was set to the *icfspectre.init* file in the new directory.

5. To look at the effects of the device low frequency noise on the oscillator phase noise, the value of *kf* in the MOSFET model was changed. Three cases were simulated for comparison and these three cases are listed in Table B.1.

Table B.1 Three cases used for testing the accuracy of phase noise simulation.

	nMOSFET *kf*	pMOSFET *kf*
Case Original	4.0×10^{-29}	6.1×10^{-28}
Case 1	4.0×10^{-20}	6.1×10^{-28}
Case 2	4.0×10^{-29}	6.1×10^{-20}

- All cases were simulated using the simulation values and settings showed from Points 2 and 3 presented before.
- For Case Original, the simulation was carried out without changing the values of *kf* for neither nMOSFET nor pMOSFET.
- For Case 1, the procedure in Point 4 was used to change the values of *kf* for only all the 1.8 V nMOSFETs, i.e. 12 bins in total, and pMOSFETs were not changed. The values of *kf* were changed from 4.0×10^{-29} to 4.0×10^{-20}.
- For Case 2, the procedure in Point 4 was used to change the values of *kf* for only all the 1.8 V pMOSFETs, i.e. 12 bins in total, and nMOSFETs were not changed. The values of *kf* were changed from 6.1×10^{-28} to 6.1×10^{-20}.

6. Three *Frequency Sweep Range* – 10 Hz to 100 kHz, 100 kHz to 5 MHz and 10 Hz to 10 MHz – of *pnoise analysis* were simulated for each case and several phase noise values at different offset frequencies were recorded and listed in Tables B.2, B.3 and B.4, respectively.

It can be clearly seen from Tables B.2, B.3 and B.4 that regardless of which *Frequency Sweep Range* was used, the phase noise simulation result does not show significant changes for all three cases at the same offset frequency although the values of *kf* for nMOSFET and pMOSFET have been changed several orders of magnitude in Case 1 and Case 2 with respect to Case Original, which should have significant effects on the low offset fre-

quency phase noise of oscillator. Therefore, it can be concluded that the phase noise simulation does not accurately take the $1/f$ noise component.

Table B.2 Phase noise simulation results for offset frequency of 10 Hz to 100 kHz.

	Phase Noise (dBc/Hz)		
Offset Frequency	**Case Original**	**Case 1**	**Case 2**
10 Hz	-3.834	-3.831	-3.830
100 Hz	-36.041	-36.038	-36.037
1 kHz	-65.610	-65.609	-65.609
10 kHz	-88.352	-88.352	-88.352
100 kHz	-108.591	-108.592	-108.592

Table B.3 Phase noise simulation results for offset frequency of 100 kHz to 5 MHz.

	Phase Noise (dBc/Hz)		
Offset Frequency	**Case Original**	**Case 1**	**Case 2**
100 kHz	-108.591	-108.592	-108.592
600 kHz	-124.129	-124.129	-124.129
1 MHz	-128.606	-128.606	-128.606
3 MHz	-138.102	-138.102	-138.102
5 MHz	-142.573	-142.573	-142.573

Table B.4 Phase noise simulation results for offset frequency of 10 Hz to 100 MHz.

	Phase Noise (dBc/Hz)		
Offset Frequency	**Case Original**	**Case 1**	**Case 2**
10 Hz	-3.834	-3.831	-3.831
100 Hz	-36.041	-36.038	-36.038
1 kHz	-65.610	-65.609	-65.609
10 kHz	-88.352	-88.352	-88.352
100 kHz	-108.591	-108.592	-108.592
600 kHz	-124.129	-124.129	-124.129
1 MHz	-128.606	-128.606	-128.606
3 MHz	-138.102	-138.102	-138.102
5 MHz	-142.570	-142.570	-142.570
10 MHz	-148.562	-148.563	-148.563

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