DESIGN OF LOW-VOLTAGE, MICROPOWER RF VCOs

DESIGN OF LOW-VOLTAGE, MICROPOWER RF VOLTAGE-CONTROLLED OSCILLATOS

By

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Cairo, Egypt, 2000

A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfilment of the Requirements

for the Degree

Master of Applied Science

McMaster University

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MASTER OF APPLIED SCIENCE (2004) McMaster University
(Electrical and Computer Engineering) Hamilton, Ontario

TITLE: The Design of Low-voltage, micro-power Voltage-controlled Oscillators

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NUMBER OF PAGES: xxiii, 151.

Acknowledgements

I would like to start my thanks by thanking Allah, the great, who has given me the strength and the patience to overcome all the difficulties in my life and those that I went through to finish this work. I also thank Allah for his wisdom, which he chose the path of engineering for me to help and contribute to humanity.

I would also like to express my sincere gratitude and deepest appreciation to my research supervisors and mentors, Dr. M. Jamal Deen and Dr. H. deBruin, for their support, guidance and giving me the opportunity for academic advancement. Without their careful supervision, constant encouragement, and fruitful technical and scientific inputs through out the course of this work, this thesis would not have been completed.

Also, I would like to thank the Canadian Microelectronics Corporation (CMC) for arranging the fabrication of the test chips, Gennum for packaging the loose die chips and Coil Craft for providing the free samples of inductors that I used in this research.

Next, I would like to thank several professors in the Electrical and Computer Engineering (ECE) department at McMaster University for their support during my courses and research work, especially Dr. Y. Haddara for his valuable discussions and guidance, and giving me academic and moral support. Dr. C. H. Chen for his precious discussions, especially regarding the designs of analog and radio-frequency (RF) circuits. Also, Dr. M. Bakr for his valuable discussions regarding the spiral inductors and EM simulations.

Special thanks are given to the administrative staffs in the ECE department. In particular, Terry Greenlay and Cosmin Coroiu for providing the technical support to all the fa-

cilities that I needed. Also, Cheryl Gies and Helen Jachna for their love and care. Moreover, Grace Ferracuti, Barb McDonald and Fran Bielby for creating the comfortable research environment for all faculty members and graduate students.

I am also thankful to my colleagues in Dr. M. Jamal Deen's Integrated Microelectronics Research group - Rizwan Murji, Sasan Naseh, Yasser El-Batawy, Farseem Mohamady, Munir El-Desouki, Juan-Carlos Ranuarez and Dr. O. Marinov - for their support, comments and technical assistance during the course of this research. I would also like to thank Nelson Costa for his help in designing the printed circuit board for this research.

I would also like to acknowledge Nabeel Jafferali and Wai Leung Ngan, my two friends and companions throughout this course work, where they shared every tough moment with me in order to conduct the research.

I am also grateful for my family in Canada - my aunt, uncle and cousins. They helped me to put my first step in Canada and overcome the home sickness that I felt to my home country. I would also like to thank my friends, Tarek Sadek, Hossam Sadek and Sherif Abdou for their moral support. Also, Tarek El Esseily for his moral support and technical help.

My acknowledgements would not be completed without expressing my deepest and warmest gratitude to my parents and brother. Within our small family, I have learnt the meaning of love, respect for others, responsibility and sacrifice.

Finally, I would like to express my deepest and warmest gratitude to my great and loving wife Noha. I have really enjoyed every second I spend with her. I would like to thank for her patience, understanding, encouragement and being supportive to me in all the harsh times. Without her in my life, all my work would have been tasteless.

Abstract

With the rapid increase in the market of portable wireless devices, the life time of the battery has become very important, especially in wireless medical telemetry, where it becomes very critical due to the nature of the application. As part of the wireless system, RF circuits are required to have low-power consumption as one of the ways to increase the device life time before the need to charge or change its battery. Meanwhile, the low-power RF circuit should maintain the basic noise and linearity performance required to guarantee an acceptable BER (Bit-Error Rate) at the receiver end. Furthermore, these circuits must be cheap and compatible with digital technologies.

This thesis focuses on the design of CMOS voltage-controlled oscillators (VCO), as one of the building blocks of a wireless transceiver. Power consumption reduction of the VCO is the main objective in the thesis. The first step to achieve the low-power requirement is to optimize the quality factor of the passive devices, such as inductors and capacitors. Therefore, we have introduced a new technique to enhance the quality factor of the monolithic inductors. This technique is based on decreasing the overall parasitic resistance while increasing the mutual inductance between the strips of the inductor. Momentum simulations are performed to compare between the proposed technique and another regular inductor that has the same inductance value. The proposed inductor shows 23% enhancement in its quality factor.

Three ultra low-voltage VCOs are presented. The first two VCOs are designed to operate at frequencies equal to 600 MHz and 2.4 GHz. The novelty in these designs is the

low-supply voltage with a value of 400 mV, which is about 100 mV below the threshold voltage of the transistor. Biasing in sub-threshold, leads to reducing the power consumption performance. These oscillators are the first RF oscillators to be biased in sub-threshold.

The third oscillator was designed to operate at 6 GHz. In this design we have added another contribution, where we forward biased the body contact of the VCO to overcome the high frequency effects that occur in sub-threshold. The three oscillators are designed to operate with supply voltages of 350 mV, 400 mV and 450 mV, respectively. The oscillators have a minimum phase noise of -128 dBc/Hz, -123 dBc/Hz and -113 dBc/Hz at 1 MHz offset, respectively, and power consumption of 36 μW, 41 μW and 90 μW, respectively. These results show the minimum power consumption and supply voltage operation reported in the literature. In the analysis of these oscillators, discussions are given on the large signal performance of the oscillator and the effect of the inductor mismatch on the power consumption and the phase noise performance. From these three VCOs, the 600 MHz oscillator was measured. It operates with a supply of 430 mV, consumes 257 μW and has phase noise of -132.5 dBc/Hz at 600 kHz offset.

To show the effectiveness of the low-power technique used with the above VCOs, another oscillator is designed at 2.4 GHz with a higher supply voltage of 1 V. The oscillator's phase noise is -123.1 dBc/Hz and it consumes 135 μW which is considered very good compared to other oscillators operating with the same supply voltage. Tuning is realized by using body-biasing of the oscillator. Therefore, we have presented a unique discussion on the effect of body-biasing on the performance of the oscillator. Measurments for this oscillator was obtained, however, it does not match the simulations due to the package parastics.

List of Symbols

A	Area of the junction
A_v	Voltage gain
C	Capacitance
C_{bypass}	Bypass capacitor
C_{CS}	Common-source capacitance
C_{ct}	Cross-talk capacitance
C_{dep}	Capacitance of depletion region
$C_{fringing}$	Fringing capacitance between gate, source and drain
C_G	Capacitance at the gate
C_{GD}	Gate-to-drain capacitance
C_{GS}	Source-gate capacitance
C_{inv}	Inversion capacitance
C_j	Reverse-biased depletion capacitance
C'_j	Junction capacitance per unit area
C_{max}/ C_{min}	Capacitance tuning ratio of the varactor
C_{ov}	Overlap capacitance
C_{ox}	Oxide capacitance
C_S	Feed-through capacitance
C_{SB}	Source bulk junction capacitance
C_{sides}	Side walls capacitance
C_{sub}	Substrate capacitance

C_{par}	Parasitic capacitance
d_{min}	Minimum distance
f	Frequency
f_{corner}	$1/f$ corner frequency
f_o	Frequency of oscillation
f_{SR}	Self resonance frequency
g_m	Transconductance
G_{sub}	Substrate conductance
I_{DD}	Supply current
I_{DS}	Drain-to-source current
L	Inductance
L_{CS}	Common-source inductor
$\mathrm{L_{gate}}$	Length of the gate
$\mathrm{l_{min}}$	Minimum length
L_S	Series inductance of inductor
L_{self}	Self inductance
$M+$	Positive mutual inductance
$M-$	Negative mutual inductance
P	Power consumption
P_{sig}	Signal power
Q	Quality factor
Q_C	Quality factor of the capacitor
Q_{dep}	Charge of the depletion layer
Q_G	Charge at the gate
Q_{inv}	Charge of the inversion layer
Q_L	Quality factor of inductor
Q_{tank}	Quality factor of the tank

R_{acc}	Resistance of the accumulation layer
R_{buff}	Resistance of the buffer
R_C	Equivalent parallel resistance of the capacitor
R_{crowd}	Resistance caused by current crowding
R_{DC}	Resistance at DC
R_g	Gate resistance
R_{inv}	Resistance of the inversion layer
R_P	Parasitic parallel resistance of the depletion region
R_{PC}	Equivalent parasitic parallel resistance of capacitor
R_{PL}	Equivalent parasitic parallel resistance of inductor
R_S	Series parasitic resistance
R_{SC}	Equivalent parasitic series resistance of capacitor
R_{sheet}	Sheet resistance
R_{skin}	Metal resistance influenced by the skin effect
R_{SL}	Equivalent parasitic series resistance of inductor
R_{sub}	Equivalent parasitic resistance of substrate
R_{tank}	Equivalent parallel resistance of the LC tank circuit
R_{tail}	Equivalent parallel resistance of the tail LC tank circuit
t	Metal thickness
t_{ox}	Oxide thickness
V_{body}	Potential of the body of the transistor
V_{cont}	Control voltage
V_{DD}	Supply voltage
$V_{DD\text{-}buff}$	Supply voltage of the buffer
V_R	Reverse applied biasing voltage
V_G	Gate Voltage

V_{GB}	Gate-to-bulk Voltage
V_{GS}	The Gate-to-source potential
V_{th}	Threshold voltage
V_{TH}	Threshold Voltage of the MOSFET
W	Width of transistor
W_{gate}	Width of the gate
X_C	Equivalent impedance of capacitor
X_L	Equivalent impedance of inductor
Δf	Offset frequency from f_0
$\Delta\omega$	Offset frequency from ω_o
Φ_o	Built-in potential of the diode
μ_o	Permeability in free space
δ	Skin depth
ε_o	Electrical permittivity of SiO_2
ε_{ox}	Relative permittivity of SiO_2
σ	Metal conductivity
ω	Angular frequency
ω_o	Angular frequency of oscillation

List of Acronyms

A-MOS	Accumulation mode MOS
AC	Alternating Current
B	Bulk/Body
BER	Bit-Error Rate
C-MOS	Complementary Metal Oxide Semiconductor
CM	Common Mode
CMR	Common Mode Rejection
D	Drain terminal of the MOSFET
DC	Direct Current
DNW	Deep *n*-Well
FOM	Figure of Merit
GMD	Geometric Mean Distance
I-MOS	Inversion mode MOS
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LTI	Linear Time-Invariant
LTV	Linear Time-Variant
MOS	Metal Oxide Semiconductor
PCB	Printed Circuit Board
PLL	Phase Locked Loop
pnoise	Periodic Noise

RF	Radio Frequency
S	Source terminal of the MOSFET
SAW	Surface Acoustic Wave
SM	Surface Mount
STI	Shallow Trench Isolations
TL	Transmission Line
VCO	Voltage Controlled Oscillator

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Chapter 1 *Introduction*

1.1 Motivation

Since the invention of the bipolar junction transistor in 1947, the second half of the twentieth century has witnessed great development in the technology and design of analog and radio frequency (RF) circuits for telecommunication purposes. Furthermore, the major advent in the silicon technologies during the past 20 years, especially the wide-spread use of the CMOS technologies had opened the way for more applications and frequency bands to be established, and thus, aided the telecommunication industry to expand more and more. In order to fulfil the high demand of the telecommunication market, RF circuits' designers were faced with many challenges. The core of these challenges is mainly to utilize the available technology to design and fabricate circuits that operate at high frequencies, that are less noisy and require lower power budget.

Unfortunately, other applications such as medical telemetry have not received much attention by RF circuit designers due to its small market. Therefore, RF circuits used for telecommunication have been also used for medical telemetry, where they served the purpose quite well. This is attributed to the more strict performance requirements of the telecommunication circuits. However, in medical telemetry the power consumption requirements are more critical than in telecommunications.

To further understand the reason power consumption is a critical criterion for medical telemetry, consider the case where a severely ill patient needs to be monitored by hospital staff. This patient is connected to wireless sensors which monitor their vital signs and communicates them wirelessly to a base station located where it is easily accessible to the nurse or doctor. In such a device, the RF front end should have extremely low power consumption, since the device should be able to operate on a single battery for long periods of time because of the critical nature of the application. Furthermore, most of the power should be reserved for the primary function of the device, which is sensing.

Another application where power consumption is a very critical issue is Bio-sensors. With the global terror nowadays from any biological warfare [3], it is of great interest for researchers and scientists to develop small bio-sensors that can detect the presence of any biological danger. It is their greatest interest to be able to build-up a bio-sensor that can take a sample from the air, analyze it and transmit this data digitally. The binary data is then sent to a base station, where it can be processed to determine the nature of the air sample taken. This whole process should be fast in order to warn the individuals present in the area in case of any danger.

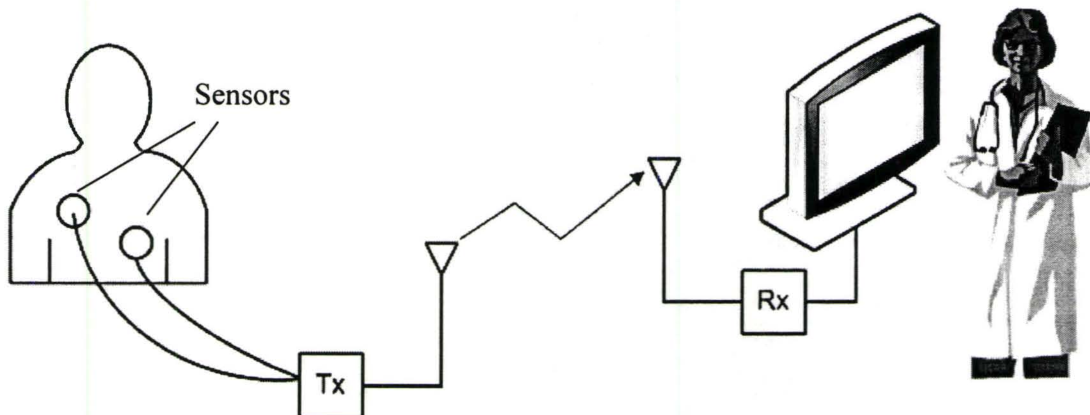


Figure 1.1 Basic schematic for a wireless medical telemetry system.

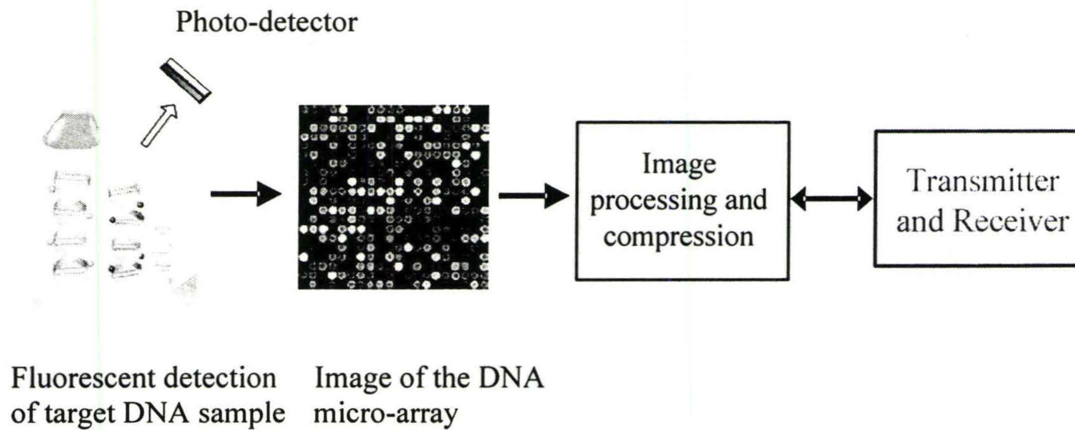


Figure 1.2 A block diagram of a portable, wireless DNA bio-sensor [1].

A block diagram for such a bio-sensor is shown in Figure 1.2. The biological detection is done by detecting the fluorescent signal due to the hybridization that accrues between an immobilized single strand DNA probe on the array and the DNA of the bacteria or virus detected. The florescence emission from the micro-array is then scanned by the image sensors. The image is then filtered from noise and compressed before being transmitted.

These bio-sensors are used in a wireless sensor network environment as shown in Figure 1.3. The bio-sensors are required to be cheap, small and stay functional alone in the field for long periods of time without the need to change its battery or recharge it. It is also required that this bio-sensor operates with a tiny battery or even a solar cell that can guarantee its functionality for a long time. Therefore, the circuits designed for such a system should have very low power consumption and should operate under extremely low voltages and biasing conditions to guarantee its survival in the surrounding environment.

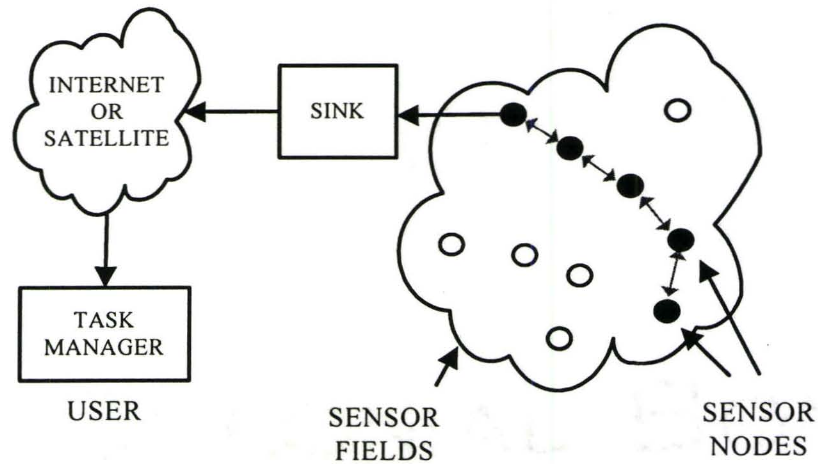


Figure 1.3 Sensor nodes scattered in a sensor field [2].

1.2 Role of Oscillators in Wireless Transceivers

In order to realize the importance of oscillators in RF receivers, assume having an RF signal received at the antenna. The function of the receiver is to demodulate this signal and to extract the information carried on it in the form of base-band data. To achieve this function, the receiver should primarily filter out the desired signal from its neighbouring interferers and boost its power to a level where it can be easily demodulated. These basic tasks are troublesome to be done at such high frequencies as the RF signal. Therefore, super-heterodyne receivers were invented as a way to overcome this problem. In the super-heterodyne receivers, the RF signal is down-converted to a lower frequency band called the intermediate frequency (IF) band, where filtering, boosting the power level and demodulating the signal is a much easier task. In order to perform the down-conversion of the signal in the frequency domain, two circuit blocks have been added to the receiver. These two are the mixer and the local oscillator and they are placed in the receiver path as shown in Figure 1.4.

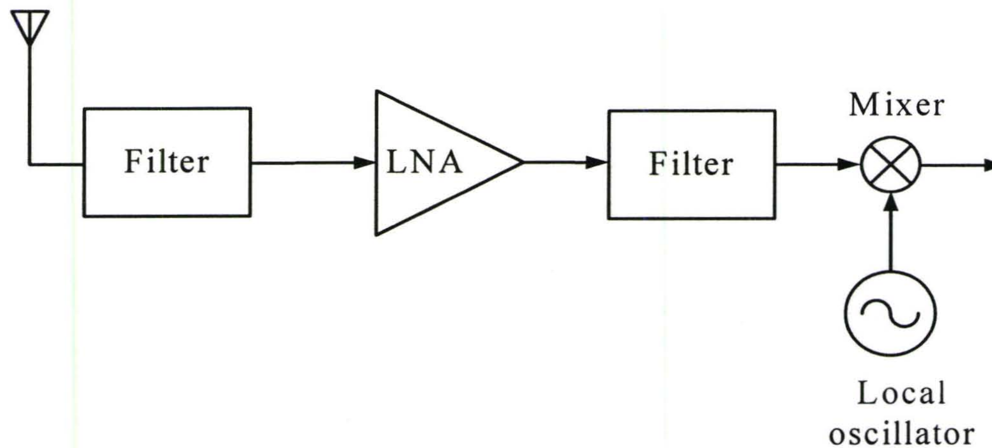


Figure 1.4 Basic schematic for an RF receiver.

The mixer is a non-linear circuit that performs the frequency conversion by multiplying the RF signal with the signal provided by local oscillator, and gives out their product to be at the desired IF and other high frequency components. The mixer is then followed by a filter to remove the high frequency components to prevent them from distorting the wanted IF signal.

Many receiver architectures have been developed, where all of them are based on the down-conversion of the RF signal to IF signal. Some of these architectures used double-conversion method and direct conversion (zero-IF) method [4], [5] and all of the architectures require at least one local-oscillator in the receiver to perform the frequency conversion.

In the case of transmitters, the modulation is usually done at low-frequencies and then up-converted to the RF band by mixing it with the local oscillator signal.

1.3 Voltage-Controlled Oscillator

The frequency at the output of the mixer f_{IF} is a fixed frequency. All the circuits that follow the mixer in the chain of the receiver have an optimized performance for the frequency component that is down-converted to f_{IF}. But in real life, receivers are designed

for the detection of several channels, not only one. Therefore, in order for the receiver to track different channels and down-convert them to f_{IF}, then the receiver should have an oscillator that has the ability to change its frequency, to down-convert the selected channel of interest to f_{IF}. This ability of the oscillator to change its output frequency is called tuning. The tuning is achieved via a control voltage that is applied to the oscillator, in which varying the control voltage, shown in Figure 1.5, varies the frequency of the output signals. The oscillator in this case is called a voltage-controlled oscillator (VCO). The change in the frequency of the output of the VCO must be designed in a way, where it changes linearly with the change in the control voltage. The typical transfer function of the VCO is shown in Figure 1.6. In Figure 1.6(a), the change in the frequency with the control voltage has a positive slope, while in Figure 1.6(b), the change in the frequency with the control voltage has a negative slope.

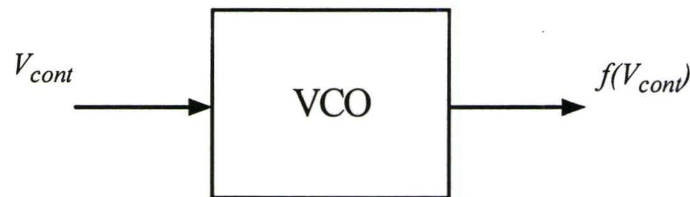


Figure 1.5 Block diagram of a VCO from the system point of view.

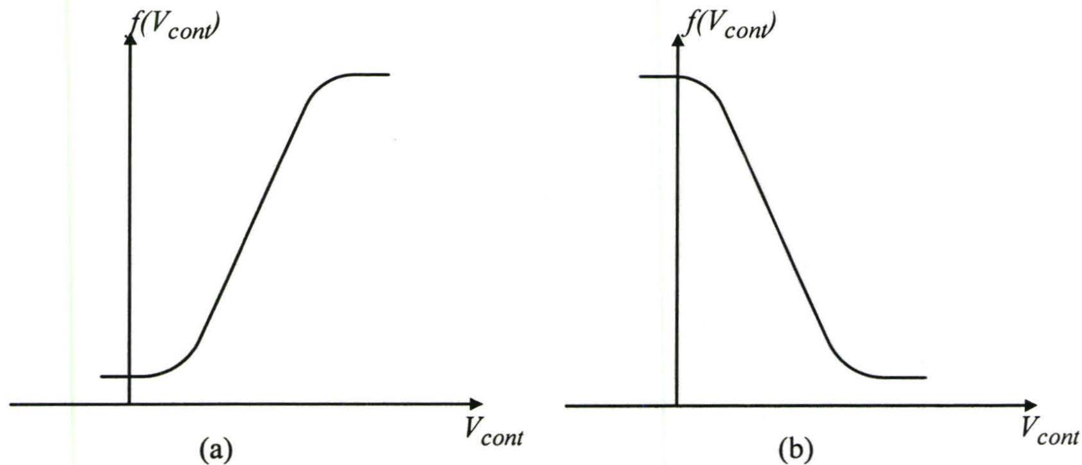


Figure 1.6 Transfer function of a VCO.

1.4 Thesis Objectives and Organization

Based on the above discussion, we can see that the need for low-voltage, low-power RF circuits is inevitable for medical telemetry and bio-sensors. And as the VCO is a basic and essential block in the RF transceiver, this thesis is dedicated to the design of low-power and low-voltage VCOs that can be used for such applications.

In chapter two, the fundamentals of oscillators are discussed. In the chapter, we are more interested in the design of LC tank oscillators, therefore, the basic fundamentals for inductances and capacitances are presented. The performance parameters of oscillators such as power consumption, tuning and phase noise are discussed, as well as the trade-offs between them. The phase noise concept and models are further described as it is a critical criterion for the oscillator performance. Finally, a discussion on the different topologies of the LC oscillators are discussed and their cons and pros.

Chapter three starts with the first passive component that is used in the design of the oscillator, which is the varactor. In this chapter, the basic physical concepts for varactors are explained, followed by their design procedures and design considerations. Finally, a comparison between the different types of varactors is given.

In chapter four, the discussion on the passive components continues, where various types of inductors are presented. However, more emphasis will be given to the physical concept of monolithic spiral inductors. The modeling of the spiral inductor and the means of optimizing its performance will be discussed in detail. Finally, a new type of inductor will be presented. This type of inductor is based on the mutual inductance between parallel microstrips and it can be used for high frequency applications.

In chapter five and six the design of a low-voltage and low-power VCOs is discussed. In each of these chapters, the design, simulations and challenges for each of these VCOs are discussed. Simulations will be presented to prove the theory of operation of each VCO.

In chapter seven, comparison between the measurement and simulation results are given. Finally, in chapter eight, the summary and conclusion of this work is presented as well as the recommended future research work.

Chapter 2 *Fundamentals of Oscillators*

2.1 Introduction

Oscillators are circuits that provide a periodic output waveform without applying any AC input to the circuit. They convert the power provided by their biasing voltages to a power at their frequency of oscillation.

In order for the oscillation to buildup, the oscillator must have a positive feedback loop where a portion of the output signal is added to the input in a manner that reinforces the input signal. The reinforced input signal is then amplified to increase the amplitude at the output. The input signal keeps circulating in the closed-loop, thus building-up the output oscillation amplitude until it saturates.

For the oscillator to start in this scenario, there should be a broadband small-signal, such as noise that perturbs the system. The oscillator then picks the frequency component of the signal that satisfies the condition of oscillation and circulates it within its closed loop to build up the oscillation amplitude. This broadband small-signal is the background noise that is always present and produced by the oscillator's circuit components. A schematic of an oscillator using a positive feedback loop representation is shown in Figure 2.1.

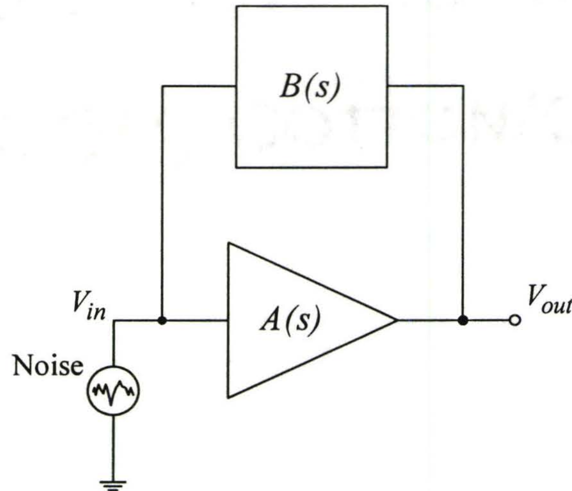


Figure 2.1 Fundamental model of an oscillator using positive feedback loop representation [6], [7].

2.2 Condition of Oscillation

The model of the oscillator shown in Figure 2.1 is described by the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1-[A(s)\cdot B(s)]}, \tag{2.1}$$

where $A(s)$ is the open-loop transfer function of the oscillator and $B(s)$ is the transfer function of the feedback network. V_{out} is the output oscillation amplitude and V_{in} is a noise signal that satisfies the conditions of oscillation, which are given by

$$A(s)\cdot B(s) = 1 \tag{2.2}$$

$$\angle[A(s)\cdot B(s)] = 0. \tag{2.3}$$

These two conditions of eq.(2.2) and eq.(2.3) are called the Barkhausen criteria.

The Barkhausen criteria for oscillation can be described by utilizing a two-port model to describe the oscillator as a positive feedback system; as shown in Figure 2.2(a) However, for microwave engineers, traditionally, the oscillator is described using a one-

port model. By utilizing the one-port model, the two-port oscillator model can be described with two one-port networks as shown in Figure 2.2(b). One of the networks is responsible for providing gain or negative resistance ($-R_{active}$) to the other lossy resonator network that has resistance $R_{resonator}$. In order to ensure oscillation in this case, the condition of oscillation is given by

$$R_{resonator} = -R_{active} \tag{2.4}$$

The two models of the oscillator are identical and either of them can be used for any oscillator topology, except for the Gunn and the tunnel diode oscillators which can only be described by the one-port model [8].

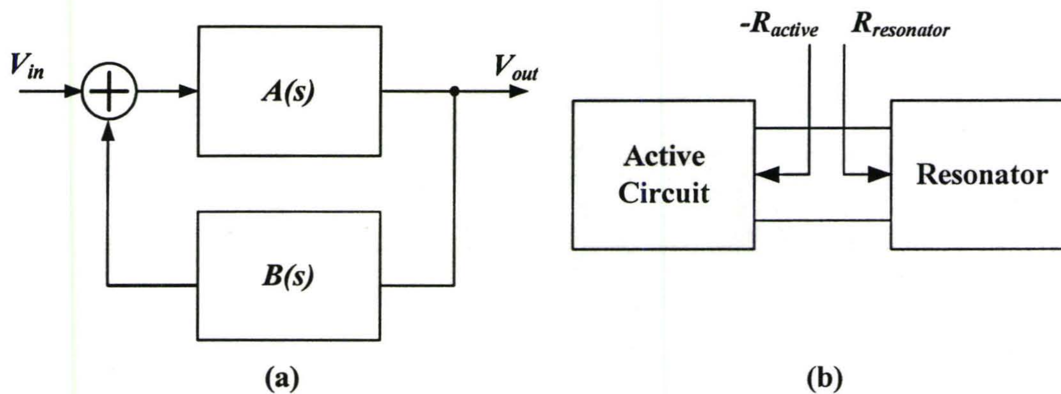


Figure 2.2 Comparison between the (a) two-port model and the (b) one-port model for oscillators.

2.3 Resonator-Based LC Tank Oscillators

Oscillators are classified according to the nature of their feedback network. Some of these oscillators have a resonator in their feedback networks which acquire a frequency selection feature. Therefore, these types of oscillators are called resonator-based oscillators. Other oscillators do not have a frequency selective network in their feedback loop and they are referred to as resonatorless-based oscillators. In this case, oscillation happens when the open-loop gain just exceeds unity at the frequency that has a zero-phase shift

through the loop. Due to the nature of the frequency selective network, the resonator-based oscillators have much higher spectral purity than the resonatorless-based oscillators. Hence, resonator-based oscillators are preferred for wireless applications.

The highest spectral purity resonator-based oscillators can be implemented using a quartz crystal or a surface acoustic wave (SAW) device. These resonators can achieve high spectral purity, are immune from aging and have very low temperature coefficients. However, the quartz crystal and the SAW devices are not compatible with the integrated circuit (IC) fabrication process, and hence, they can not be fabricated on-chip. Furthermore, their relatively large size consumes a lot of the printed circuit board (PCB) area. Due to these disadvantages, LC tank circuits are mostly used in modern RF oscillator designs. A major advantage of the LC tanks is that they can be implemented on-chip; however, the resulting spectral purity is worse than oscillators with a crystal or a SAW device and their power consumption is also higher.

2.3.1 Role and Requirements of the LC circuit

The LC circuit is considered as the passive circuitry of the oscillator. A passive circuit is composed of passive components that either store or dissipate energy but cannot provide gain to any signals that are applied to it. In this section, the general role and requirements of the LC passive circuit for oscillator design are discussed. Further discussion on the fundamental operation and circuit models for each of the passive components will be presented in chapters three and four.

The primary role of the LC tank circuit is frequency selection. The frequency of oscillation f_o for any resonantor-based oscillator is determined by the resonant frequency of the LC circuit. It should be noted that the parallel connection of the inductor and the capacitor of the LC tank circuit is mostly used in the oscillator design rather than the series connection. This is because parallel LC tanks give a high impedance at resonance, which helps to boost the gain of the oscillator above unity at the frequency of resonance in order to start up the oscillation, as will be discussed later in section 2.6. At resonance, the impedance of the capacitor and the inductor are equal and out of phase, so

$$X_L = X_C, \tag{2.5}$$

or equivalently,

$$(2\pi f_o)L = \frac{1}{(2\pi f_o)C}, \tag{2.6}$$

which gives

$$f_o = 1/(2\pi\sqrt{LC}), \tag{2.7}$$

where f_o is the resonance frequency of the LC tank circuit.

The second role of the LC tank circuit is tuning. To have an LC resonator that can change its resonance frequency (f_o), the inductance L and the capacitance C should be variable. Practically, it is easier to implement the variable reactor using the capacitor rather than the inductor. Historically, in the early heterodyne receivers, tuning was done mechanically by using an adjusting knob to align a rotating ganged multi-plate metal with other plates that are fixed, but interleaved with the rotating ones. These plates had air as a dielectric between them, and thus changing their alignment varied the value of the overall capacitance.

In the 1960s, with the advent of commercial semiconductor technologies, the *pn* diode varactor replaced the mechanically adjustable capacitor. The *pn* junction diodes were smaller in size, cheaper, and had the advantage of the electrical adjustment of frequency, which had a tremendous impact on the development of the phase-locked loop (PLL). The reverse *pn* junction diode varactors were used in the discrete design for VCOs up to the 1980s, and then they were implemented with VCO modules and monolithic integrated circuits (ICs) [21].

In the 1990s, with the maturity of the CMOS silicon IC fabrication, varactors were implemented using the MOS capacitor. Introducing the MOS varactors was considered to be another breakthrough in integrated passive varactors on silicon due to its compatibility, easy integration and higher tuning range in comparison to *pn* diode varactors, while maintaining the high quality factor criteria with the advanced CMOS technologies . As a result,

much research has been done since the mid 1990s to enhance the performance and obtain a good model for the MOS varactors.

Ideally, the LC circuit should have an infinite equivalent impedance at parallel resonance. However, due to the parasitic losses that are associated with the inductor and capacitor, the impedance at parallel resonance is finite. A measure of these parasitic losses is given by the quality factor (Q), which is considered the most important requirement of the LC tank circuit. Generally, the Q of an inductor or a capacitor is given by

$$Q = 2\pi\frac{|\text{Total magnetic energy stored - Total electric energy stored}|}{|\text{Total energy dissipated per cycle}|}. \tag{2.8}$$

The energy dissipated within the inductor or the capacitor is due to the associated parasitic resistance that results from wiring, connection and leakage currents. This loss in energy can be modeled as a resistance connected in series to an ideal inductor or capacitor, as shown in Figure 2.3(a) and Figure 2.3(c), respectively. It can also be modeled as a resistance connected in parallel to an ideal inductor or capacitor as shown in Figure 2.3(b) and Figure 2.3(d), respectively.

The Q can be determined from each of these simple models. Using the series model, the quality factor of the inductor Q_L and the quality factor of the capacitor Q_C are given respectively by

$$Q_L = 2\pi \cdot \frac{\frac{1}{2}(L \cdot I^2)}{\frac{1}{2}I^2 \cdot R_{SL}/f} = \frac{\omega L}{R_{SL}}, \tag{2.9}$$

$$Q_C = 2\pi \cdot \frac{\frac{1}{2}(C \cdot V^2)}{\frac{1}{2}I^2 \cdot R_{SC}/f} = \frac{C \cdot [I/(\omega C)]^2}{I^2 \cdot R_{SL} \cdot \omega} = \frac{1}{(\omega C)R_{SC}}. \tag{2.10}$$

A simpler method to derive the Q of a passive device is by utilizing the equivalent impedance (Z_{eq}), thus, the quality factor is

$$Q = \frac{Im\{Z_{eq}\}}{Re\{Z_{eq}\}}, \tag{2.11}$$

This gives the same results as equations (2.9) and (2.10). In the case for the inductor,

$$Q_L = \frac{Im\{Z_{in}\}}{Re\{Z_{in}\}} = \frac{\omega L}{R_S}. \tag{2.12}$$

While, for capacitor,

$$Q_C = \frac{Im\{Z_{in}\}}{Re\{Z_{in}\}} = \frac{1}{(\omega C)R_S}. \tag{2.13}$$

If the parallel model is used instead, the Q_L and Q_C are given by

$$Q_L = \frac{V^2/(\omega L)}{V^2/R_{PL}} = \frac{R_{PL}}{\omega L}, \tag{2.14}$$

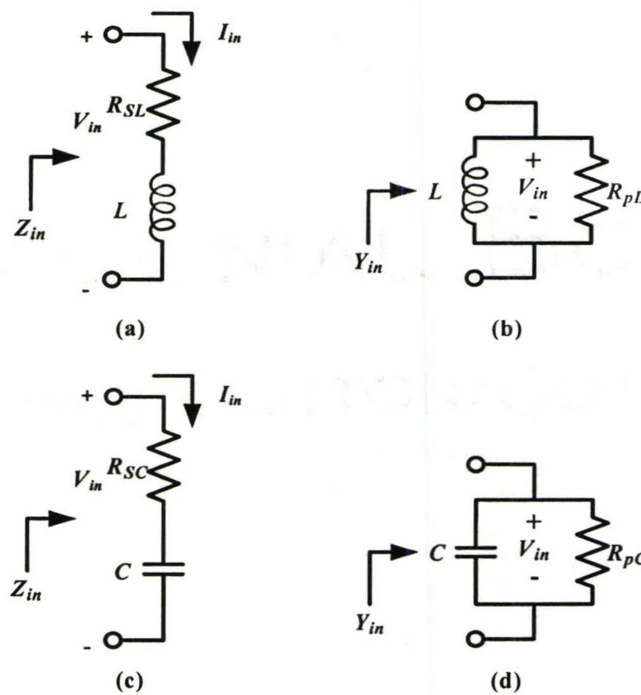


Figure 2.3 Simple (a) series and (b) parallel models for inductor. Simple (c) series and (d) parallel models for capacitor.

(2.15)

$$Q_C = \frac{V^2/[1/(\omega C)]}{V^2/R_{PC}} = R_{PC} \cdot \omega C. \tag{2.16}$$

If the inductor and the capacitor are connected together to form a parallel LC tank circuit, then the total quality factor of the parallel LC tank circuit Q_{tank} is given by

$$Q_{tank} = \frac{R_{tank}}{\omega L} = \omega C \cdot R_{tank}, \tag{2.17}$$

where

$$R_{tank} = R_{PL} \| R_{PC}. \tag{2.18}$$

It should also be noted that the Q not only determines the losses of the inductor or the capacitor, but also the bandwidth of the LC tank circuit, which is given by

$$Bandwidth = \frac{f_o}{Q}. \tag{2.19}$$

Eq. (2.19) states that for higher Q values, the bandwidth of the transfer function of the LC circuitry will be narrower. Having a narrower transfer function is very critical in the oscillator design, because higher Q value means that the output of the oscillator will have higher spectral purity. This concept will be discussed in more detail with the phase noise models later in section 2.5. The Q value also has a great impact on the power consumption of the oscillator, which will also be discussed in section 2.4.3.

2.4 Performance Characteristics of Oscillators

In this section, different performance characteristics of oscillators are discussed. Trade-offs between these performance characteristics will also be explained. The main performance characteristics are phase noise, output voltage swing, power consumption and tuning.

2.4.1 Phase Noise

In the study of noise in radio-frequency (RF) circuits such as low noise amplifiers (LNAs), mixers and amplifiers, the main focus is always on the noise that is added to the

amplitude of the signal by the circuit. Hence, the noise figure is the parameter that describes the noise performance of these circuits. However, the oscillator as a block in the receiver chain is not in the signal's path and its task is to generate a sinusoidal signal that does not make any abrupt phase changes. Therefore, phase noise is the primary noise performance parameter for oscillators.

To emphasize the importance of phase noise in the performance of oscillators, let us consider the case of an ideal local oscillator and a real oscillator that exhibit phase noise. An ideal oscillator is defined as an oscillator that generates a single tone sinusoidal signal, and its frequency spectrum is represented as an impulse at the angular frequency of oscillation ω_o as shown in Figure 2.4(a). Its corresponding time domain representation is given by

$$x(t) = A_o \cdot \cos(\omega_o t). \tag{2.20}$$

However, due to the noisy devices used in oscillators such as transistors and the tank circuit, the output signal $x(t)$ contains noise components superimposed on the impulse at ω_o. These superimposed noise components are added to the signal in two ways. First, noise that affects the amplitude of $x(t)$ and is denoted by $A(t)$. Second, the noise that affects the phase of $x(t)$ and is denoted by $\phi_n(t)$. Thus, the output signal of the real oscillator is given by

$$x(t) = [A_o + A(t)] \cdot \cos[\omega_o t + \phi_n(t)] \tag{2.21}$$

Usually, oscillators have an amplitude self-limiting mechanism, which decreases the effect of the amplitude modulation (AM) performed by $A(t)$. Hence, its effect on the output signal can be neglected. Unfortunately, the excess random phase modulation (PM) caused by $\phi_n(t)$ cannot be neglected since for small $\phi_n(t)$, the local oscillator signal is presented by

$$x(t) \approx A_o \cdot \cos(\omega_o t) - A_o \cdot \phi_n(t) \cdot \sin(\omega_o t) . \tag{2.22}$$

Eq. (2.22) reveals the effect of $\phi_n(t)$ on the output signal, where the spectrum of $x(t)$ is no longer considered as an impulse. Instead, the excess phase $\phi_n(t)$ is translated to the ideal spectrum at ω_o such that the spectrum becomes a small band of frequencies, as shown in

Figure 2.4(b), and the oscillator signal is said to have "skirts" around the carrier frequency [9].

To understand the impact of phase noise on wireless transceivers, let us consider the receiver path in Figure 2.5. Consider two signals in adjacent channels that are received at the front-end, where one is the desired signal which has a lower power level than the other, as shown in Figure 2.6(a). If both signals are mixed with a noisy local oscillator, the down converted intermediate frequency (IF) of the desired signal will be flooded by the adjacent channel, as is shown in Figure 2.6(a). The phase noise is also an important criterion in the transmitter design. For example, a transmitter that has excessive phase noise associated with the carrier can corrupt the signals in adjacent channels of nearby receivers as shown in Figure 2.6(b).

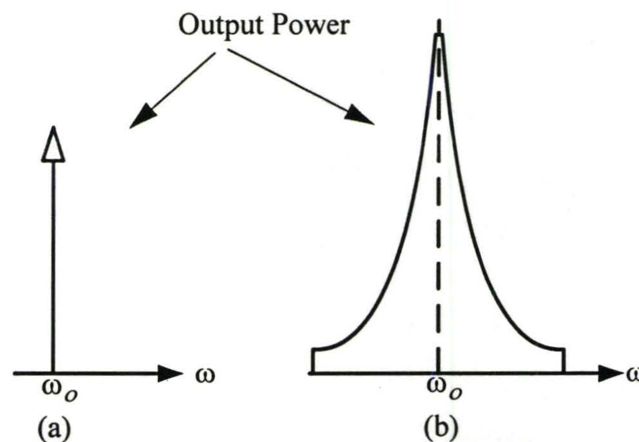


Figure 2.4 The output spectrum of (a) an ideal and (b) a real oscillator.

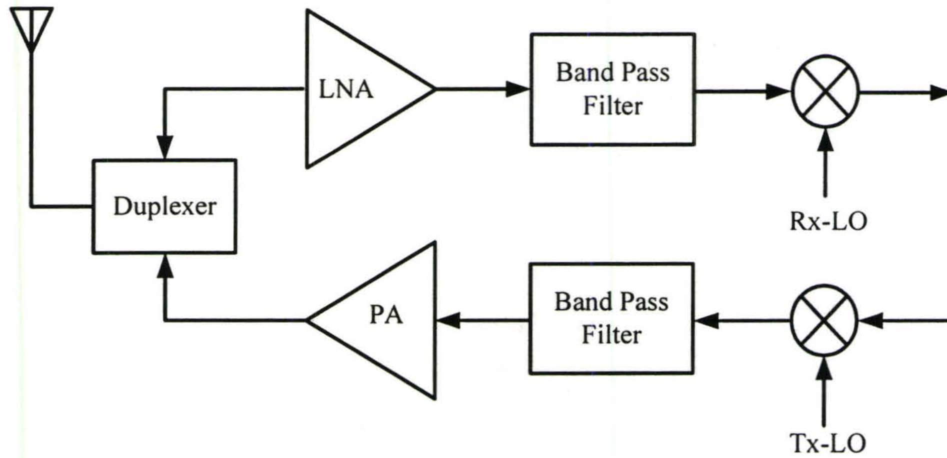


Figure 2.5 Transceiver front-end [10].

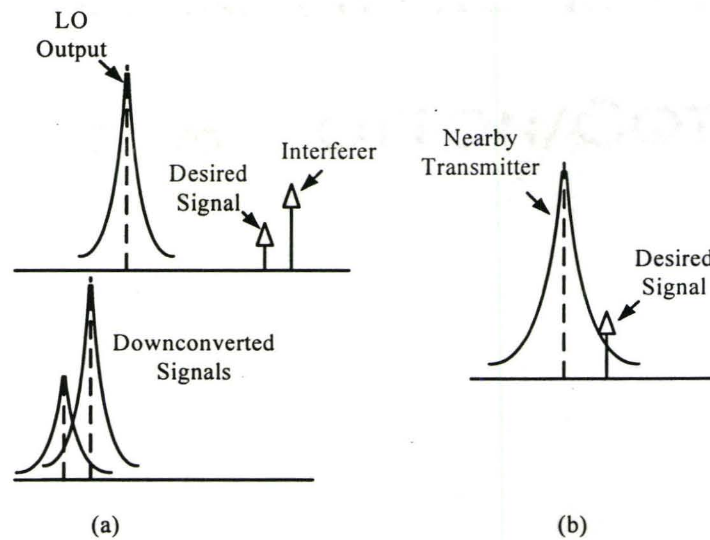


Figure 2.6 Effect of phase noise on (a) down-converted received signal and (b) transmitters [9].

The phase noise is measured from the output spectrum of the oscillator by using a spectrum analyzer. The power in a unit bandwidth is measured at the offset frequency Δf, normalized to the carrier power and the units are dBc/Hz. The oscillator must achieve a certain phase noise performance to guarantee good reception of the channel with an

acceptable bit error rate (BER). For example, in GSM-900 MHz receivers, the phase noise at a Δf of 400 kHz must not exceed -120 dBc/Hz.

2.4.2 Output Voltage Swing

In the transceiver architecture, the output of the local oscillator is connected to the switching transistors of the mixer circuit. In order to minimize the noise contribution of these switching transistors in the mixer, it is preferable to have them switched on and off with a 50% duty cycle. This requires their input which is coming from the oscillator to be a square wave rather than a sinusoidal wave. Therefore, the switching sinusoidal signal coming from the oscillator must be with large voltage swing, in order to be abrupt to imitate the effect of the square wave [10], as shown in Figure 2.7.

The output voltage swing also has great impact on the phase noise performance, where the higher the output voltage swing, the better the phase noise performance. This will be discussed later in the study of the phase noise models in section 2.5.

Finally, it should be noted that the output voltage swing of the oscillator is usually determined by its topology and operating conditions.

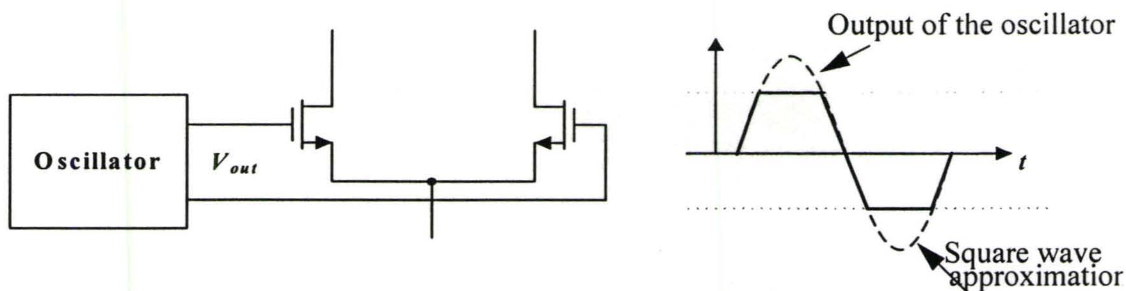


Figure 2.7 Approximation of a large amplitude sinusoid output (dashed line) by a square wave (solid line) [10].

2.4.3 Power Consumption

As discussed in chapter one, some wireless applications are powered with batteries that are required to operate for long periods of time before recharging or replacement. This

requirement influences the power budget of the integrated system and requires that the circuits operate with a minimum amount of power dissipation, while meeting all performance specifications. Unfortunately, minimizing the power consumption by minimizing the current leads to lower output voltage swings. This results in a deterioration in the phase noise and leads to a slower switching of the mixer's switching transistors.

2.4.4 Tuning

In most RF communication systems, the oscillator is required to tune to different channels. Hence, oscillators should be able to generate an output at different frequencies so that they can follow different channels. Tuning is normally defined as the maximum frequency range in which the oscillator operates in a linear fashion with respect to a control signal, divided by the center frequency of this range.

The four performance parameters discussed above - phase noise, output voltage range, power consumption and tuning - govern the performance of the oscillator. Unfortunately, most of these performance parameters have conflicting requirements and to have an oscillator that has superior performance in all four parameters at the same time is very difficult. For example, if the power consumption is assumed to be the primary concern in the VCO design, then the current provided by the supply must be decreased in order to decrease the power consumption. However, decreasing the current will decrease the output voltage amplitude ($I \times R_{tank}$), which will increase the phase noise and also affect the switching performance of the mixer. Also, to achieve lower power consumption, R_{tank} should be enlarged to reduce the amount of current that is required to achieve oscillation. Hence, larger inductance and higher Q values are needed. However, having a high Q inductance is very difficult in practice and this will be discussed later in chapter four. Therefore, large inductance values are used. As a result, lower values for the varactors are used, which degrades the tuning range of the oscillator.

Usually, a compromise between these parameters is made so that the overall performance of the oscillator still satisfies the design specifications. In order to compare the overall performance between different designs, a Figure-of-Merit (FoM) is defined for

oscillators where all these factors are considered. A suitable FoM for an oscillator that considers all the major performance parameters is

$$FoM = 20 \cdot \log\left(\frac{\omega_o}{\Delta\omega}\right) - L(\Delta\omega) - 10 \log P - 20 \cdot \log Q \qquad (2.23)$$

where ω_o is the angular frequency of oscillation of the oscillator, $\Delta\omega$ is the offset frequency at which the phase noise $L(\Delta\omega)$ is measured, Q is the quality factor of the tank circuit and P is the power consumption of the oscillator in milliWatts and normalized to 1 mW.

2.5 Phase Noise Models

Researchers in [11], [13], [15] have been studying and investigating phase noise mechanisms so that the phase noise can be modeled properly. However, deriving an accurate model for phase noise is very difficult, complicated and time consuming if an exact formulation is required due to the non-linear and time varying nature of oscillators. In this section, a brief review of two popular models is presented.

2.5.1 Leeson's Model

In 1966, Leeson [11] derived a model for phase noise that gives a simple and basic insight in the mechanisms of phase noise. Leeson described the transfer function of the oscillator as a linear time-invariant (LTI) system and assumed that the phase noise is due to the noise of the tank circuit, which is shaped by the overall transfer function of the oscillator, as shown in Figure 2.8.

Leeson's formula is given by

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{2kT}{P_{sig}}\left[\frac{\omega_o}{2Q \cdot \Delta\omega}\right]^2\right], \qquad (2.24)$$

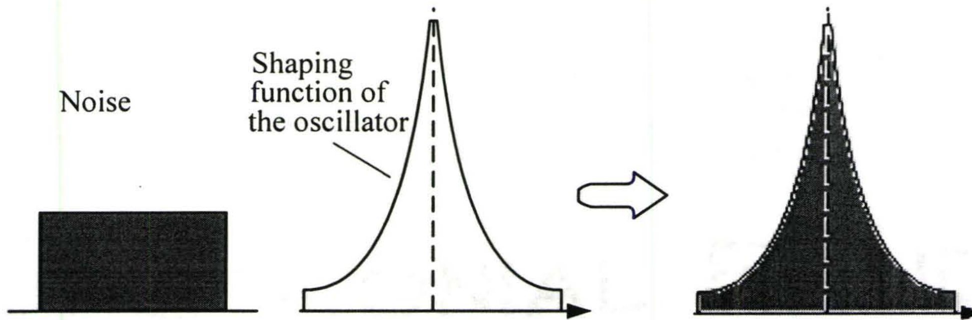


Figure 2.8 Noise shaping in oscillators [10].

where $L(\Delta\omega)$ is the noise power at an offset frequency $\Delta\omega$ from the oscillator frequency ω_o normalized to the signal power P_{sig} at ω_o and it is measured in dBc/Hz, k is Boltzmann's constant, T is the absolute temperature and the product kT is the thermal white noise energy per unit bandwidth that is produced by the lossy tank circuit.

It is important to draw attention to the effect of P_{sig} and Q on phase noise in eq. (2.24). The signal power P_{sig} is proportional to the output voltage swing and as P_{sig} at ω_o increases relative to the noise at offset $\Delta\omega$, the phase noise will decrease. As a result, the phase noise performance of the oscillator is directly proportional to the output voltage swing. Also, higher Q implies a narrower transfer function of the oscillator, and thus, less noise would be injected in the sidebands of the carrier.

Unfortunately, Leeson's formula did not provide good agreement with the measurements as schematically demonstrated in Figure 2.9. Assuming that the oscillator acts as a LTI system did not capture the $(1/\Delta\omega)^3$ behavior of the measured phase noise. Also, the assumption that the only noise source is the noise of the tank circuit made the estimation of the phase noise in eq.(2.24) become less the than what is actually measured in practice.

To overcome these deficiencies in the derived formula in eq.(2.24), fitting parameters were introduced [10], [12] and thus, $L(\Delta\omega)$ becomes

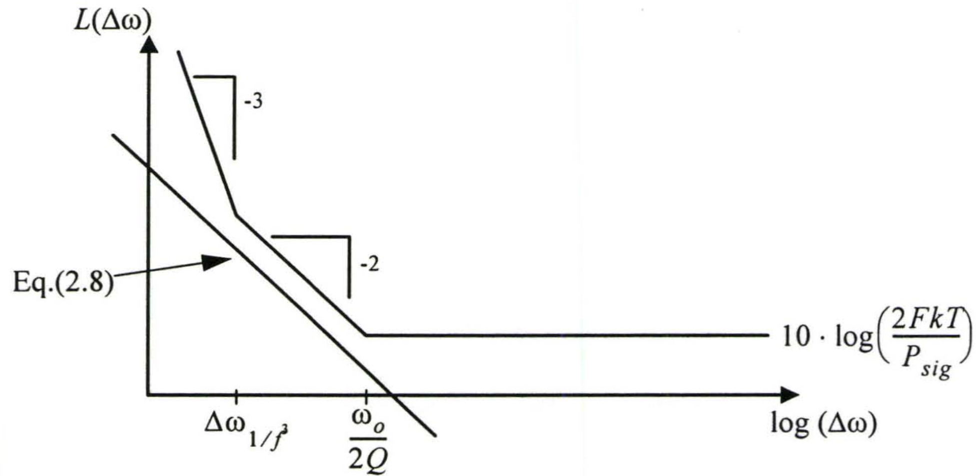


Figure 2.9 Phase noise spectrum according to Leeson's model versus measured [13]. Lines with slopes of -3 and -2 are shown.

$$L(\Delta\omega) = 10 \cdot \log\left[\left[\frac{2kT}{P_{sig}} \cdot F \cdot \left(\frac{\omega_o}{2Q \cdot \Delta\omega}\right)\right]^2 \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right], \tag{2.25}$$

where $\Delta\omega_{1/f^3}$ is equal to the *1/f* corner frequency of the flicker noise in MOSFETs and F is an empirical factor that varies depending on the oscillator's topology and biasing conditions. The factor F was only an empirical parameter, there was no formula provided to help in minimizing it. Fortunately, later in [17], the factor F was found to be

$$F = 1 + \frac{4\gamma IR}{\pi V_o} + \gamma\frac{4}{9}g_m R_{tank}, \tag{2.26}$$

where I is the bias current, γ is the channel noise coefficient of the FET, g_m is the transconductance of the current source MOSFET, and R_{tank} is the parallel equivalent resistance of the tank circuit.

2.5.2 Time Varying Model

In the attempt to derive a better expression for phase noise and overcome the deficiencies of Leeson's model, Hajimiri et al. [12], [14] considered the time varying nature of the oscillator in their analysis.

In the linear time-variant (LTV) phase noise model, a derivation of the phase noise ϕ_n due to an impulse of noise charge injected to the tank circuit was proposed [12], [14]. The first and main step in this analysis is the introduction of the impulse sensitivity function (ISF) $\Gamma(\omega_o t)$. The ISF defines the phase shift $\Delta\phi(t)$ due to an injected charge Δq through the relation

$$\Delta\phi(t) = \Gamma(\omega_o t)\frac{\Delta q}{q_{max}}, \tag{2.27}$$

where q_{max} is the maximum amount of charge injected into the capacitor to produce the maximum voltage swing V_{max}. The next step in the analysis is to derive the output excess phase $\phi(t)$. However, in order to define $\phi(t)$, the unity phase impulse response $h_\phi(t-\tau)$ for the oscillator must first be defined. By defining $h_\phi(t-\tau)$, $\phi(t)$ can then be defined for any noise sources that is expressed as a noise current source. Hence,

$$h_\phi(t-\tau) = \frac{\Gamma(\omega_o t)}{q_{max}}u(t-\tau) ; \tag{2.28}$$

and the output excess phase $\phi(t)$ is expressed as

$$\phi(t) = \int(h_\phi(t-\tau)\cdot i(\tau))d\tau . \tag{2.29}$$

Finally, the output voltage $v(t)$ is related to the output excess phase $\phi(t)$ by PM

$$v(t) = A\cdot\cos[\omega_o t + \phi(t)] . \tag{2.30}$$

Without going into the mathematical derivation in detail, there are some basic points that should be emphasized regarding the nature of the ISF. Since the switching in the oscillator has a fixed period, then the noise sources are no longer stationary. Instead, the noise sources of the core transistors are said to be cyclo-stationary with a period equal to the period of the oscillating signal.

Due to the periodicity of the noise sources, the ISF is also repeated every period, that is, the ISF is periodic. Hence, it can be expanded as a Fourier series

$$\Gamma(\omega_o t) = C_o + \sum_{n=1}^{\infty} C_n \cdot \cos(n\omega_o \tau + \theta_n), \tag{2.31}$$

where C_o is the DC component of the ISF, C_n is the Fourier coefficient of the nth harmonic and θ_n is a constant phase for the nth harmonic.

Having the Fourier expanded ISF and following the procedures described by eq. (2.27) through eq. (2.29), the $\phi(t)$ can then be calculated as

$$\phi(t) = \frac{1}{q_{max}}\left[C_o \int_{-\infty}^{t} i(\tau)d\tau + C_n \sum_{n=1}^{\infty} \int_{-\infty}^{t} i(\tau)\cos(n\omega_o \tau + \theta_n)\right]. \tag{2.32}$$

Eq.(2.32) is illustrated by Figure 2.10. *i(t)* is assumed to be white noise, that is, it is a constant noise current as a function of frequency. When it is multiplied by the nth component of the ISF, this n^{th} ISF component is multiplied by the noise of *i(t)* that is present at the frequency equal to the frequency of the nth component. Therefore, the result is equivalent to a low-frequency noise component passes through a low-pass filter (L.P.F.). The products of *i(t)* and all the DC and *n* components are then summed to produce $\phi(t)$.

The above explanation describes the so called folding down of the harmonic noise, and folding up of the DC noise to the fundamental frequency of oscillation ω_o, that is all these frequency components contribute to the phase noise. This folding mechanism is shown in Figure 2.11.

The folding mechanism provides the reason for the $(1/f^3)$ part of the curve in Figure 2.9. This $(1/f^3)$ is simply the folding up of the flicker noise that is produced by the current source transistor, which biases the oscillator. Leeson's model was not capable of describing the folding mechanism because it assumed a LTI system where the power of a certain frequency component can neither be transferred to other frequency components nor generate them.

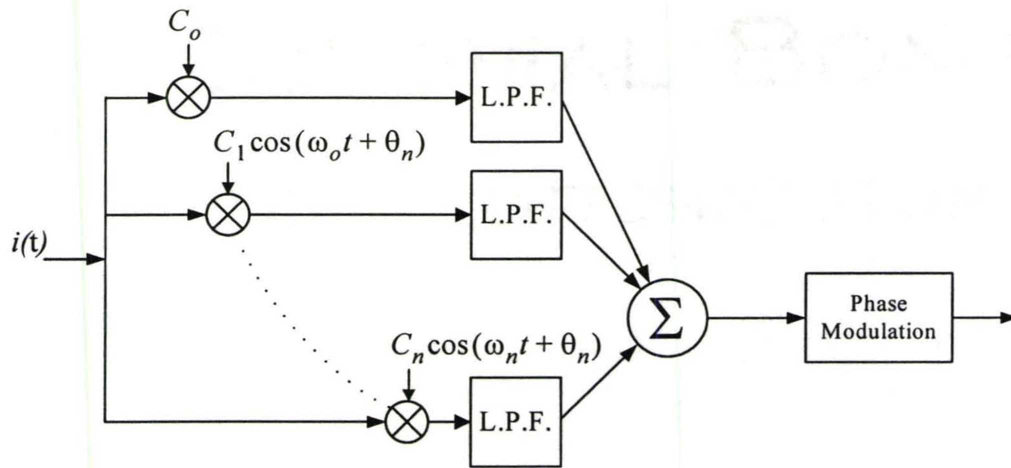


Figure 2.10 The equivalent system for ISF decomposition [14].

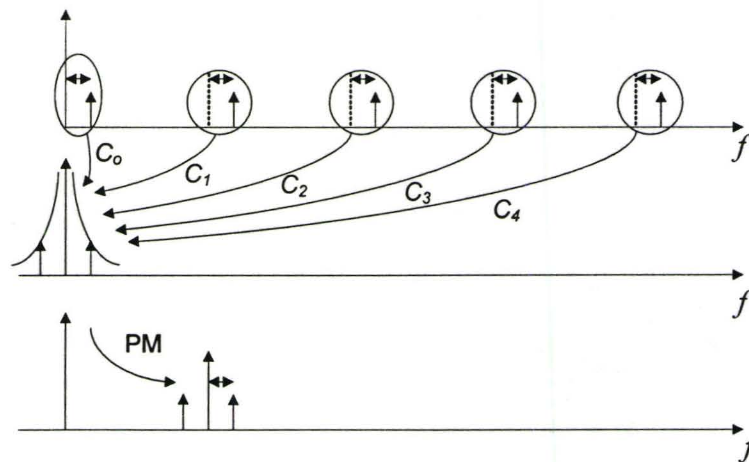


Figure 2.11 Evolution of circuit noise to phase noise [12].

Later in [15] and [16], it was shown that the separation between the perturbation in amplitude and phase was invalid. In [15], a numerical technique was developed to calculate the phase noise based on solving a set of non-linear differential equations, which indicated that the linear assumptions for any oscillator were not consistent. It also showed that

the numerical technique developed was general, could be applied to any oscillator, and all the previous LTI and LTV analyses were only special cases of it.

Although both Leeson's and Hajimiri's models are not completely accurate, the discussions in the following chapters will be based on these two models because of their simplicity and physically-based formulas that shows the impact of different circuit parameters on phase noise. It is also worth mentioning that the circuit simulator (SpectreRF) used for the oscillator design in the following chapters uses the LTV model for its phase noise calculations.

2.6 Negative Transconductance ($-g_m$) Oscillators

In most RF transceivers, it is required to have a differential oscillator with a 50% duty cycle to guarantee proper mixing of the oscillator signal with the RF signal rather than a single-ended one. The most common differential oscillators used in modern RF transceivers are called the negative transconductance or $-g_m$ oscillators. The $-g_m$ oscillator topology is used to classify any oscillator that has two differential cross-coupled transistors, connected back to back, as shown in Figure 2.12(a). This topology is called $-g_m$ because the input impedance of the connection in Figure 2.12(a) is equal to $-2/g_m$. By utilizing the one-port model, this negative resistance compensates for the losses of the resonator R_{tank}, shown in Figure 2.12(b), to ensure oscillation. From the two-port model point of view, this circuit acts as two equal forward transfer functions that provide equal gain and 180 degrees phase shift, which when connected back-to-back, closes the positive feedback loop to ensure oscillation.

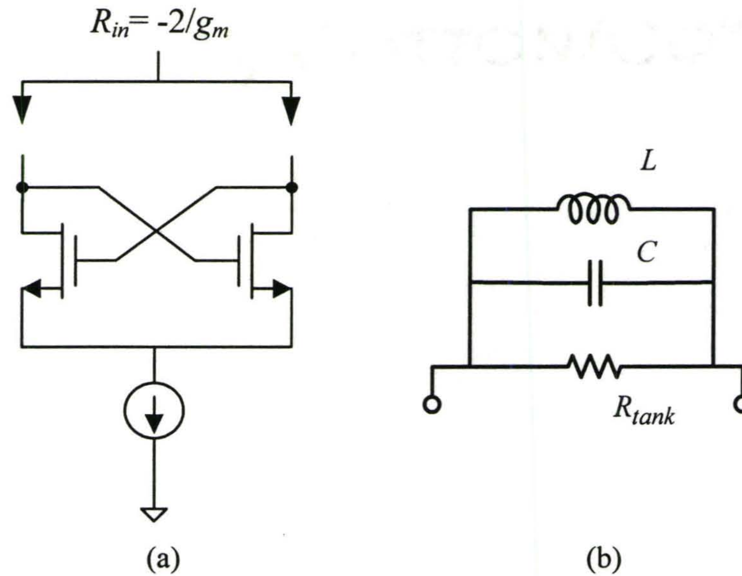


Figure 2.12 (a) Equivalent negative resistance of the cross-couple connection and (b) the equivalent resistance of the tank circuit.

There are many circuit configurations that utilize this topology. The most commonly used ones are shown in Figure 2.13. The configurations shown in Figure 2.13(a) and (b) are called the cross-coupled only N-type -g_m oscillators. The difference between (a) and (b) is the PMOS current source shown in (b), which is used to minimize the flicker noise injected into the cross-couple transistors, and thus, improves the phase noise performance of the oscillator.

The configuration shown in Figure 2.13(c) is called the complementary cross-coupled -g_m oscillator. In this configuration, the NMOS and PMOS cross-coupled transistors provide the overall gain to the tank circuit, and thus, higher gain can be achieved if this configuration is biased with the same current as the cross-coupled only N-type -g_m oscillator. The input resistance is equal to

$$R_{in} = -\frac{2}{g_{mn} + g_{mp}}, \tag{2.33}$$

where g_{mn} and g_{mp} are the transconductance of the NMOS couple and PMOS pairs of transistors, respectively.

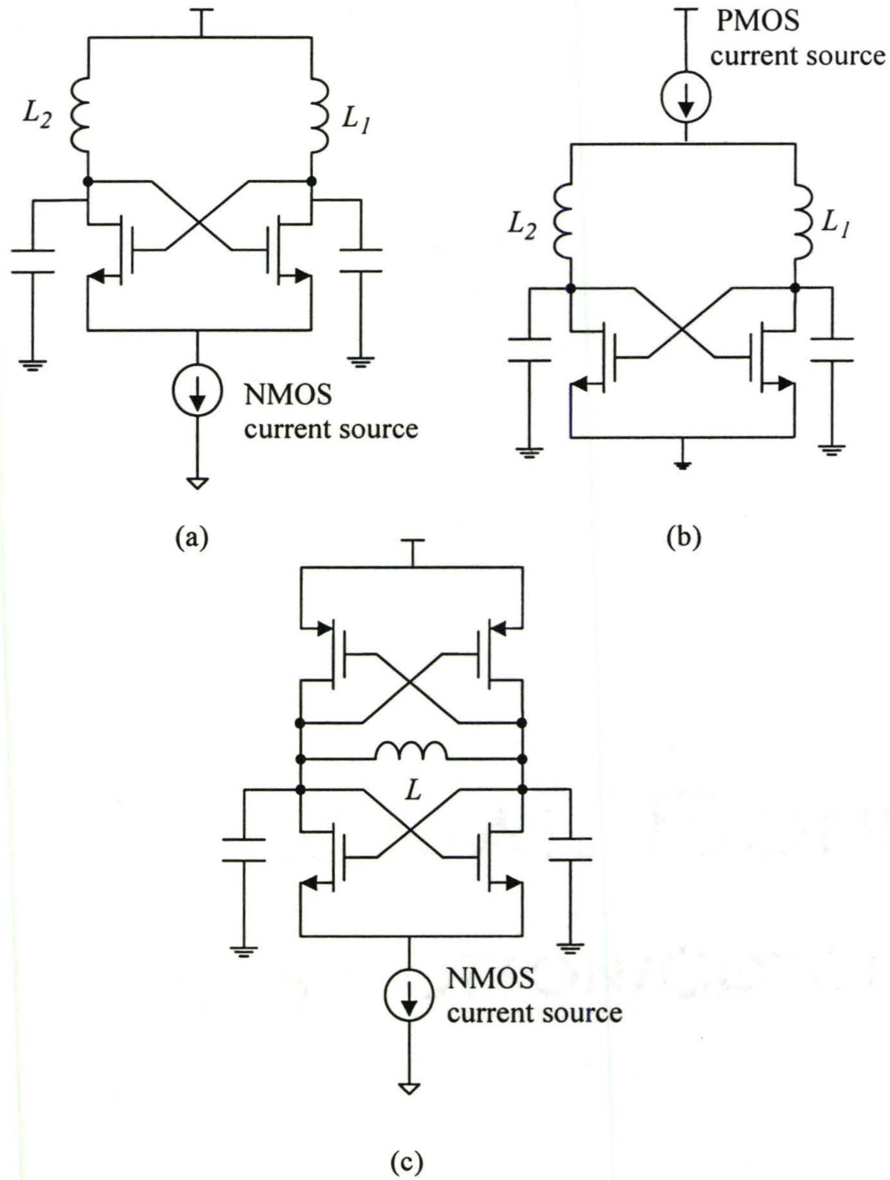


Figure 2.13 Some common architectures of -g_m oscillators.

The current waveform injected into the tank circuit of the configurations shown in Figure 2.13(a) and (b) is shown in Figure 2.14(a). These pulses are injected when the transistor is switched on, and thus, the current flowing into the tank circuit will have a DC component that will pass through the inductor and the fundamental component of the current will flow through the R_{tank}. However, in the complementary configuration, the current is forced to flow into the same tank circuit and not into different tanks as in the NMOS only configuration. The corresponding current waveform is shown in Figure 2.14(b). This current waveform minimizes the DC current that passes through the inductor and most of the current flows through the R_{tank}. Therefore, higher amplitudes can be achieved in the complementary configuration if both configurations have equal bias currents. However, if the power consumption is not a design issue, the circuit in Figure 2.13(a) and Figure 2.13(b) can have a voltage swing that reaches twice V_{DD}, and hence, the phase noise is enhanced by approximately 6 dB. In practice, the improvement in the phase noise is less than 6 dB because there is extra noise caused by the extra bias current.

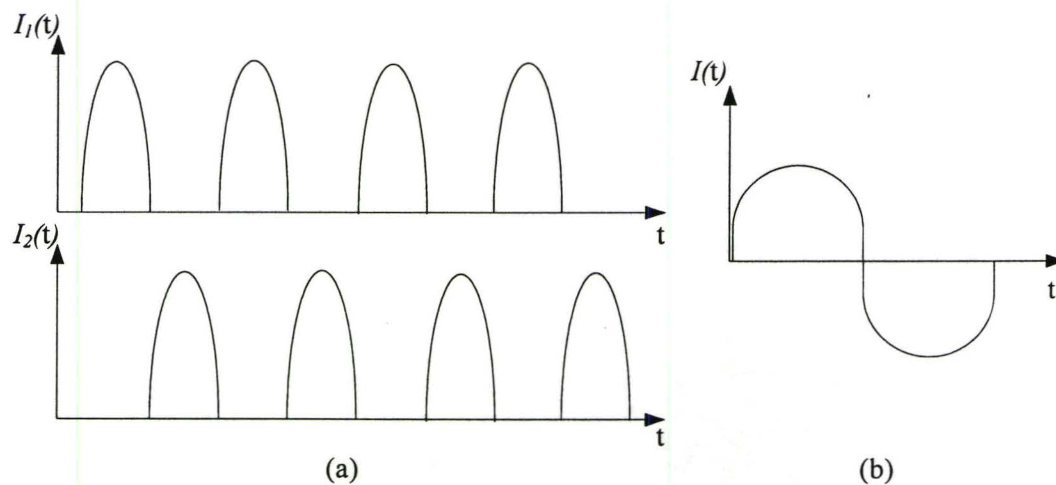


Figure 2.14 The current waveforms of (a) NMOS only and (b) complementary cross-coupled $-g_m$ oscillators as a function of time.

The complementary configuration has one inductor in the load tank circuit, which minimizes the on-chip area. In this case, it is preferred to use a symmetrical inductor, such as the inductors used in [61], [62], to achieve full symmetry between the two branches of the VCO.

In [18] and [19], an interesting argument regarding the $\Delta\omega_{1/f^3}$ in the phase noise measurements was mentioned. Generally, the corner frequency is given by [19], [20]

$$f_{corner} = \frac{K}{C_{ox}WL} \cdot \frac{1}{4kT\gamma} \cdot \frac{g_m^2}{g_{do}}, \tag{2.34}$$

where K is a constant, C_{ox} is the gate oxide capacitance per unit area, W is the gate width, L is the gate length, g_m is the transconductance, g_{do} is the zero drain voltage channel conductance of the transistor and γ is a parameter that has a value of 2~3. From the above equation, the corner frequency of the MOSFET is inversely proportional to the drain current [19]. As a result, if the configuration in Figure 2.13(a) has a tail current that is twice the tail current of Figure 2.13(c), then the configuration in Figure 2.13(a) should have a lower $\Delta\omega_{1/f^3}$. However, the measurements in [18] showed that the complementary configuration in Figure 2.13(c), in fact, had a lower $\Delta\omega_{1/f^3}$ due to its better rise- and fall-time symmetry comparing to the NMOS only configuration.

2.7 Summary

This chapter included the fundamental and most essential information and discussions needed for the oscillators that are discussed in the later chapters. The chapter began with an explanation of the main task of the oscillator and how oscillation is achieved. In this thesis, the oscillator design is based on the resonator-based type, hence, emphasis was given on the role and requirements of the LC tank circuit.

In section 2.4, the performance characteristics of the oscillator were discussed and the concept of phase noise was introduced. Based on the understanding of these performance characteristics, an example was given to show the trade-offs among them. The sec-

tion following that was devoted for the phase noise modeling methods with their corresponding cons and pros. Two models were discussed in detail as they will be used to help explain the design procedures of the oscillator in later chapters.

The final section in the chapter was dedicated for the discussion of $-g_m$ oscillator. Three different circuit configurations for this topology were illustrated and a comparison among their performance was presented.

Chapter 3 *Varactors: Design and Fundamentals*

3.1 Introduction

In chapter two, the fundamentals of LC oscillators were presented. One of the main topics that were covered was the role and requirements of the LC tank passive circuitry and the impact of their performance on the overall performance of the VCO. Therefore, it is extremely important to design the passive devices and optimize their performance to meet that of the VCO.

In order to optimize the performances of the passive devices used in the tank circuit, their tasks should be well defined and their requirements should be linked to their design parameters. Therefore, this chapter will be dedicated to the study of the operation of the varactors, their models and their optimization for low-power integrated circuit design.

3.2 Performance Characteristics of Varactors

Based on the requirements for the LC tank circuit that were discussed in chapter 2, similar requirements and performance parameters are discussed in this section. The emphasis in this discussion will be on the two main and most important performance parameters for the VCO design in chapter five, these performance parameters are the tuning and the quality factor.

3.2.1 Capacitance Tuning Ratio (C_{max}/C_{min})

Capacitance tuning ratio (C_{max}/C_{min}) is one of the most important performance parameters for varactors. C_{max} and C_{min} are the maximum and minimum capacitances, respectively, measured at the lower and the upper limit of the tuning voltage. The (C_{max}/C_{min}) ratio has a direct impact on the tuning range of the oscillator as C_{min} and C_{max} refer to $f_{o,max}$ and $f_{o,min}$ through the relation

$$\frac{f_{o,\,max}}{f_{o,\,min}} = \sqrt{\frac{C_{max}}{C_{min}}} \quad . \tag{3.1}$$

It is generally desirable to have a wide tuning range for an oscillator, and thus, a higher ratio (C_{max}/C_{min}) is usually one of the main goals in choosing the varactor. (C_{max}/C_{min}) depends on the type of the varactor and is also strongly dependent on the layout of the device as well as its process parameters.

3.2.2 Quality Factor

The overall quality factor of the tank circuit determines the phase noise and the power consumption of the VCO, as discussed in chapter two. Therefore, expressions for the quality factor of the varactor should be derived based on its physical circuit model. Physically based quality factor expressions help in understanding the main loss factors of the varactor so it becomes easier afterwards to avoid these losses and to optimize its performance. Unfortunately, the simple expressions that were derived for Q_c in section 2.3.1 are not valid if the circuit model of the capacitor becomes complicated. The expression for Q_c should take into account the changes in the circuit model. For example, in the case of integrated varactors, the expression of Q_c should have additional terms that include the losses due to the substrate, contacts, etc. The simplest way to derive the expression of Q_c is to calculate its total equivalent impedance of the varactor at the node of interest that is connected to the load of the oscillator, then the expression of Q_c would be derived by dividing the reactive imaginary component of the impedance by its real part.

In this thesis, Q_c will be the primary and main parameter for choosing the varactor as power consumption is our primary goal, and hence studying and understanding the loss mechanisms of different varactors is very important in order to find a suitable way to minimize them. It should be noted that losses in varactors depend strongly on the type of the varactor and the technology and process parameters.

3.2.3 Other performance parameters

The focus of this thesis is primarily on the parameter Q_c and then on the tuning ratio (C_{max}/C_{min}). Other performance parameters such as C-V characteristics, self-resonance frequency, absolute capacitance values and silicon area efficiency can be found in [23].

3.3 Diode Varactors

Diode varactors are based on the depletion capacitance of the reverse-biased *pn* junction. Varying the reverse biasing voltage of the diode, the width of the depletion region changes and thus results in a change in the capacitance of the junction diode through the relation,

$$C_j(V_R) = \frac{C'_{jo} \cdot A_j}{\left(1 + \frac{V_R}{\Phi_o}\right)^{m_j}} \tag{3.2}$$

where C'_{jo} is the junction capacitance per unit area at zero bias, A is the area of the junction, V_R the reverse applied biasing voltage, Φ_o is the built-in potential of the diode and m_j is a process fitting parameter that depends on the doping profile at the junctions interface. This relation, plotted in Figure 3.1(b), shows the dependence of the depletion capacitance on the reverse biasing voltage. The figure shows that the capacitance value reaches infinity when the applied reverse bias is equal to $-\Phi_o$, however, in reality the capacitance value reaches only $2(C'_{jo} \cdot A_j)$ [24].

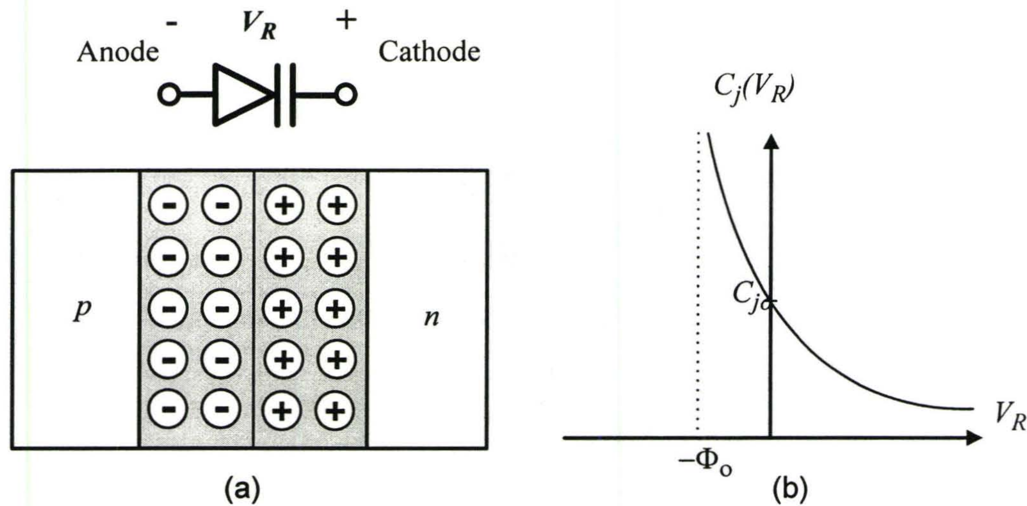


Figure 3.1 The *pn* diode varactor (a) structure and corresponding circuit symbol, (b) C-V curve.

In the CMOS 0.18 μm technology that supports the deep *n*-well (DNW) option, various combinations of *pn* junction can be formed, as shown in figure Figure 3.2. These configurations include *n+*/*p*-bulk, *n*-well/*p*-bulk, *p+*/*n*-well and *n+*/*p*-well in a DNW. For the first two configurations, the p-junction is connected to ground as it is also the substrate, and thus, to keep the junction reverse biased, the n+ should be connected to a positive control potential, beside being the terminal connected to the load of the VCO, which is not practical. As for the n-well/p-bulk and p-well /DNW options, the lightly doped *n* and *p* regions increase the resistance that is in series to the depletion capacitance, leading to a deteriorated Q_c. The combinations of *p+*/*n*-well and *n+*/*p*-well in a DNW has a lower sheet resistance for the *n+* and the *p+* regions, and hence their Q_c is much better than the other configurations.

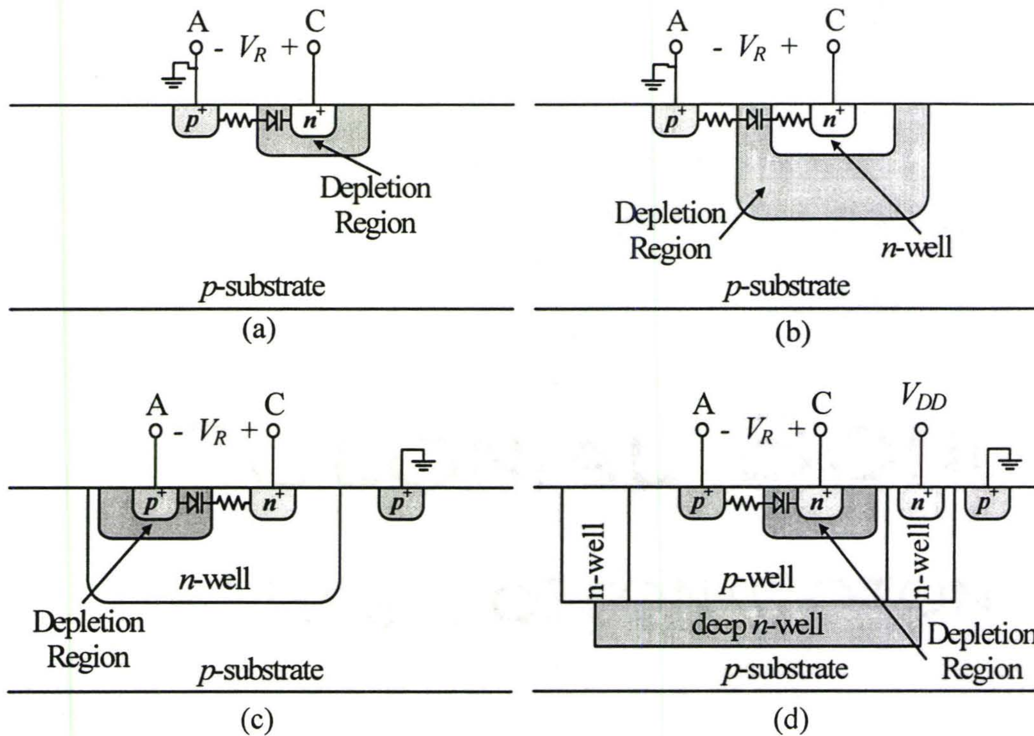


Figure 3.2 Different implementation for the *pn* diode in the CMOS 0.18μm technology. (a) *n*+/*p*-bulk, (b) *n*-well/*p*-bulk, (c) *p*+/*n*-well and (d) *n*+/*p*-well in DNW.

There is not much published on the *n*+/*p*-well in a DNW since not all technologies support the fabrication of the DNW. Inspite of this, the *n*+/*p*-well in a DNW configuration has a major advantage over other configurations which is the substrate noise isolation due to the DNW.

An important point that should be emphasized before further discussions, is that only reverse biased diodes are studied as varactors. Although forward biased *pn* junction has higher capacitance values than the reverse biased ones, which might be appealing as it saves on-chip area. However, it has the disadvantage of an extremely low Q_c due to the large DC current that flows when the diode is forward biased and the high equivalent capacitance.

3.3.1 Models

Figure 3.3b shows a simple model for the *p+*/*n*-well diode configuration in Figure 3.3a. In this figure, C_j is the reverse-biased depletion capacitance, R_p is the parasitic resistance of the depletion region and R_s models the losses of the *p+* region and the *n*-well. C_{sub} and R_{sub} are the equivalent capacitance and resistance to the substrate, respectively. The values of C_j and C_{sub} are usually close to each other. However, the value R_{sub} is much higher than R_s due to the higher resistivity of the *p*-bulk and the distance to the bulk contact. As a result, the quality factor of C_{sub} is very poor relative to C_j.

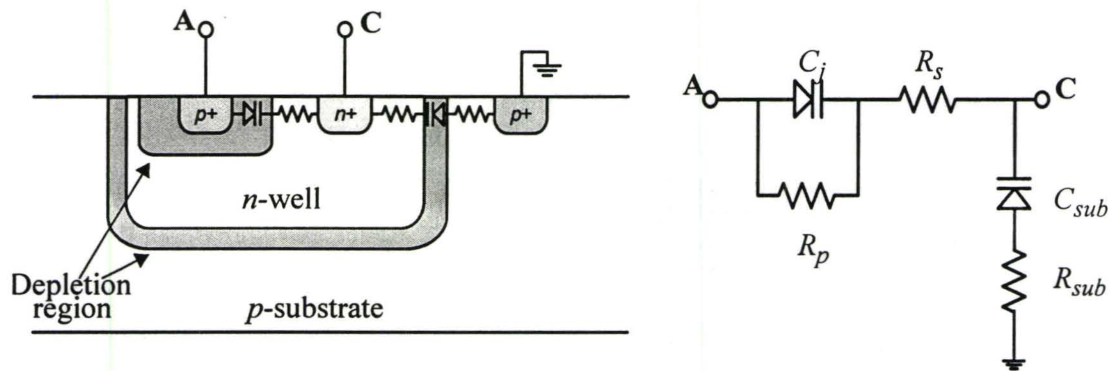


Figure 3.3 The *p+*/*n*-well diode varactor. (a) structure, (b) equivalent circuit model.

3.3.2 Circuit Design Considerations

The *pn* diode varactor should be connected to the circuit and biased in a way to achieve the best possible performance. The first circuit design rule to achieve best performance for the varactor is to prevent the *pn* junction diode from going into forward bias. The circuit designer must be aware of the maximum and minimum amplitudes of the VCO and ensure that the *pn* junction is always reversed-biased.

Another circuit design consideration is the way the *pn* diode varactor is connected to the circuit at the load node, shown in Figure 3.4(a). The way the *pn* diode is connected

to the load node of a VCO is very important and critical as it drastically affects the performance of the VCO. To further understand the significance of the diode connection to the circuit and its effect, consider the simple model of the *n+/p*-well diode of Figure 3.3b to be connected to the load node of the VCO, as shown in Figure 3.4(b) and (c). In case the cathode of the diode is the terminal connected to the load node of the VCO, as show in Figure 3.4(b), then both C_j and C_{sub} contribute to overall load capacitance. However, the quality factor is then determined by the lower quality capacitor, C_{sub}. Thus, this connection degrades the quality factor of the diode and consequently degrades the quality factor of the load node.

Another case is to consider the anode of the diode to be the one connected to the load node of the VCO and the cathode is connected to the control voltage, as shown in Figure 3.4(c). In this case, the effective capacitance is C_j which has a high quality factor and C_{sub} does not affect the overall capacitance as the cathode is considered to be AC ground.

Practically, the control voltage for the *pn* varactor has a finite impedance rather than being an AC ground. This finite impedance increases the effect of the low-quality capacitor C_{sub}. This finite impedance itself also adds to the losses of the varactor and thus, degrades the quality factor more.

In order to overcome the effect of the finite supply impedance of the control voltage, a relatively large value capacitor is connected to the cathode terminal [23]. This large value capacitor acts as a low impedance (or acts as AC short circuit) for the frequency of oscillation and hence, eliminates the losses in the C_{sub} and R_{sub}.

The above argument shows an important point that should be considered in the design of any diode varactor, that is, to connect the diode in such a way as to cancel the effect of the low-quality capacitance C_{sub} for any of its layout configurations.

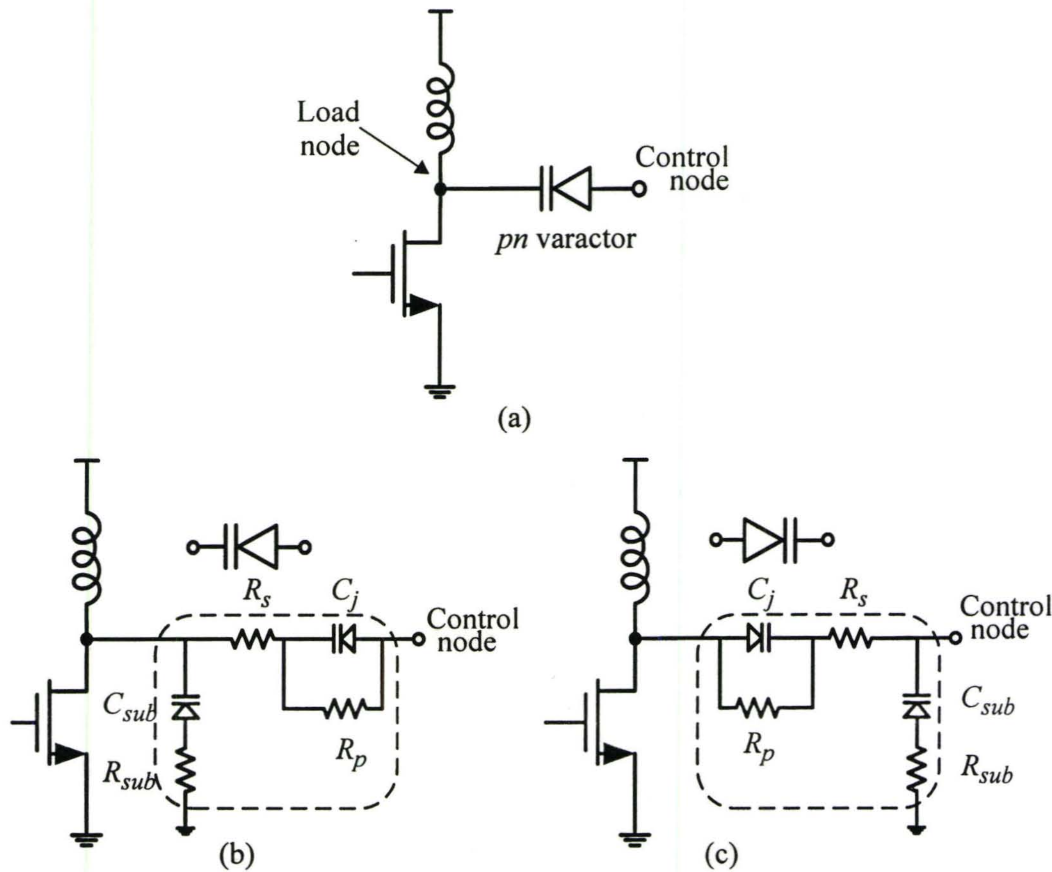


Figure 3.4 A schematic for a single branch of the VCO showing (a) a *pn* diode varactor connected to the load node and the control node, (b) the cathode is connected to the load node and (c) the anode is connected to the load node.

3.3.3 Layout Considerations

It is also very important to lay out the diode in a smart way to achieve high Q_c. In [23], [25], they explain how to lay out the diode properly to achieve the high quality factor criterion. In [25], different layouts for the p+ regions were shown and their performances were compared. However, in this section we will only explain the effect of the layout of the *p+* region on the Q_c of the diode.

To explain how the layout of the device can affect the performance of the varactor, lets assume the two diode layouts in Figure 3.5, where they both have the same equivalent area A_o. The equivalent capacitance of the diodes shown in the layout would be given by

$$C_j(V_R) = C_{j,o} + C_{j,sides} = \frac{C'_{j,o} \cdot A_o}{\left(1 + \frac{V_R}{\Phi}\right)^{m_{j,o}}} + \frac{C'_{j,sides} \cdot 2(l_{sides} + w_{sides})}{\left(1 + \frac{V_R}{\Phi}\right)^{m_{j,sides}}} \quad (3.3)$$

where $C_{j,o}$ and $C_{j,sides}$ are the junction capacitance of the area beneath the $p+$ implantation and the side walls, respectively. $C'_{j,o}$ is the capacitance beneath the $p+$ implantation per unit area at zero bias voltage. $C'_{j,sides}$ is the capacitance of the side walls per side wall length at zero bias and l_{sides} and w_{sides} are the length and the width of the $p+$ implantation, respectively. $m_{j,o}$ and $m_{j,sides}$ are the exponents of the area beneath $p+$ and the side walls respectively, where the value of $m_{j,o}$ is slightly larger than the value of $m_{j,sides}$ [23], [25].

Although, the two layouts in Figure 3.5 have the same area of the $p+$ implantation, the total capacitance of Figure 3.5(a) is greater than the capacitance of the structure in Figure 3.5(b), because the layout in Figure 3.5(a) has a larger perimeter than the layout in Figure 3.5(b). Due to this fact, it is questionable whether it is better to implement the diode to have the contribution of the capacitance by the side walls or the area beneath the $p+$ implantation.

Unfortunately, there is not an absolute answer to that question, because none of the solutions give an improved overall performance and there are trade-offs between the main two performance parameters (Q_c and C_{max}/C_{min}) depending on the layout of the device. Hence, the layout should be done to satisfy the most important requirement in the design.

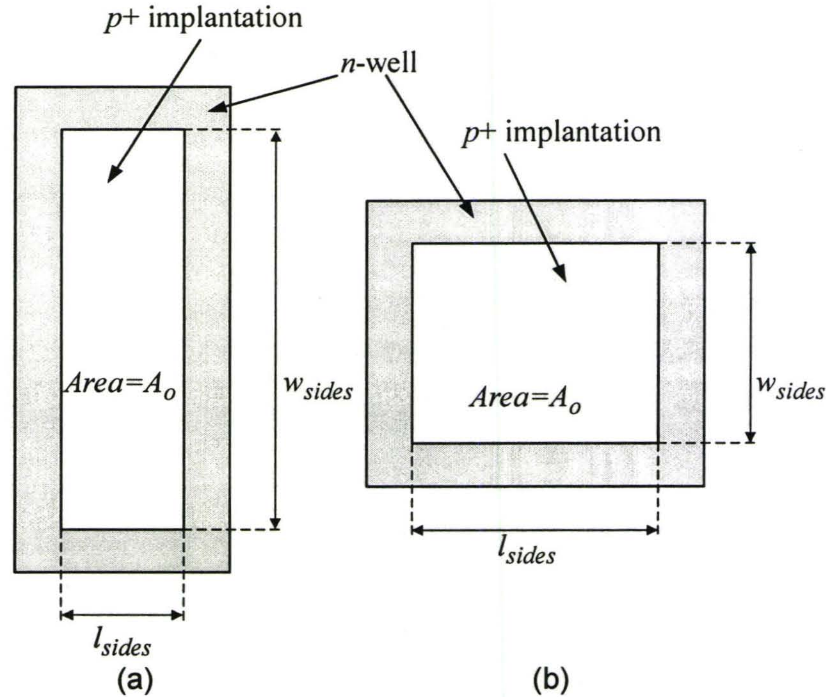


Figure 3.5 Layout of two *pn* diodes with the same on-chip area.

If C_{max}/C_{min} is the important performance parameter, then the varactor is implemented as the diode in Figure 3.5(b), because the exponent $m_{j,o}$ is slightly larger than $m_{j,sides}$,leading to a higher rate of change in the value of C_d. However, the choice is different if the Q_c is the performance parameter of interest. Implementing the *p*+ region with large l_{sides} would increase the contribution of C_o to the overall capacitance. This capacitance C_o suffers from having a high series resistance $R_{sub,o}$ as shown in Figure 3.6(a), when compared to the series resistance of C_{sides} which is $R_{sub,sides}$. As a consequence, C_o has lower Q_c values than C_{sides}. Hence, it is always preferred to minimize C_o if high Q_c is required, which is achieved by using the dimension l_{sides} to be equal to the minimum length l_{min} as shown in Figure 3.6(b).

To achieve the highest Q_c for this structure, the *n*+ of the *n*-well contacts should be implanted at the minimum distance d_{min} from the *p*+ region. Minimizing the distance

between the *n*+ and the *p*+ decreases the series resistance due to *n*-well to the lowest values possible and hence, highest values for Q_c is achieved.

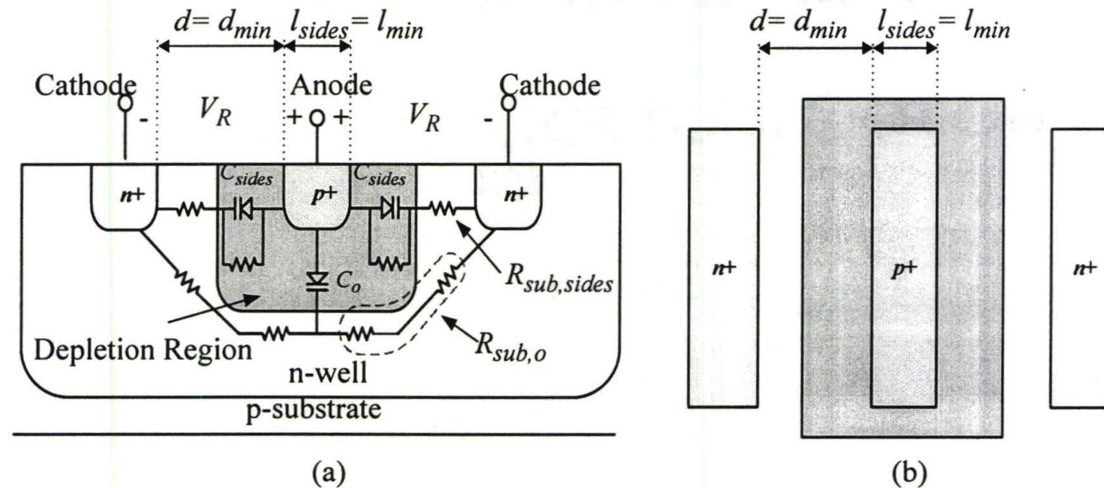


Figure 3.6 (a) The parasitice resistances of the *p*+ *n*-well diode and (b) a horizontal cross-section, showing the optimum design configuration.

3.4 MOS Varactors

Another kind of variable capacitors that is used in monolithic silicon technologies is the metal-oxide-semiconductor (MOS) varactor. The MOS varactor is simply the structure of the MOSFET, but with the bulk, source and drain terminals connected together (B=D=S). Figure 3.7 shows the basic MOS (B=D=S) varactor structure, Figure 3.7(b) shows its circuit symbol and its corresponding C-V curve is shown in Figure 3.7(c).

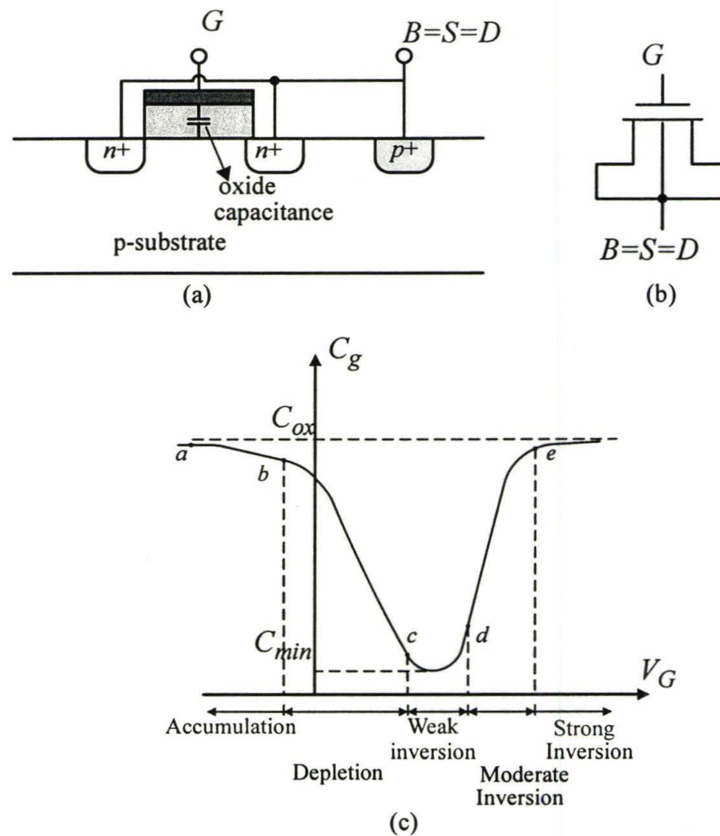


Figure 3.7 (a) Structure of the MOS varactor, (b) the circuit symbol, and (c) the C-V characteristics curve.

Unlike the *pn*-diode varactor, which has monotonic C-V characteristics, the MOS varactor does not. The capacitance curve of the MOS has a negative slope region versus the gate voltage (V_G), which is called the "depletion mode" region and a positive slope region that is called the "inversion mode" region. Both regions are shown in Figure 3.7(c).

When V_G is a high negative value, positive holes are attracted to the negative V_G and are accumulated underneath the gate oxide. The MOSFET in this case is said to be biased in accumulation. Any small change in V_G changes the charges under the gate oxide, and hence, the capacitance value in accumulation is given by [20],

$$C_G = \frac{dQ_G}{dV_G} = C_{ox} \tag{3.4}$$

and

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} \cdot W_{gate} \cdot L_{gate}}{t_{ox}} \tag{3.5}$$

where Q_G is the charge at the gate, C_{ox} is the oxide capacitance, ε_o and ε_{ox} are the electrical permittivity in free space and the relative permittivity of SiO_2, respectively, W_{gate} is the width of the gate and L_{gate} is its length.

As V_G increases, till it reaches the flatband voltage at point "b" in Figure 3.7(c), electrons become attracted to the surface rather than holes. Electrons under the gate recombine with the acceptor ions that form the *p*-bulk and produce a depletion region under the gate oxide. As a result, another capacitance is formed under the oxide, which is the capacitance of the depletion region C_{dep}. In this case, the applied potential across the MOS is then equal to [20]

$$V_G = V_{ox} + V_{bulk} \tag{3.6}$$

and for operating in depletion,

$$V_{bulk} = V_{dep}. \tag{3.7}$$

Substituting eq.(3.7) in eq.(3.6) and differentiating

$$\frac{dV_G}{dQ_G} = \frac{dV_{ox}}{dQ_G} + \frac{dV_{dep}}{dQ_G} \tag{3.8}$$

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \tag{3.9}$$

Eq. (3.9) shows that C_{dep} is added in series with C_{ox}.

The width of the depletion region increases with the increase of V_G, which consequently decrease the values of the C_{dep}, and since C_{dep} is in series with C_{ox}, therefore, the overall equivalent series capacitance of the MOS decreases. This argument is shown in *C-V* curve, by the range between point "b" and point "c".

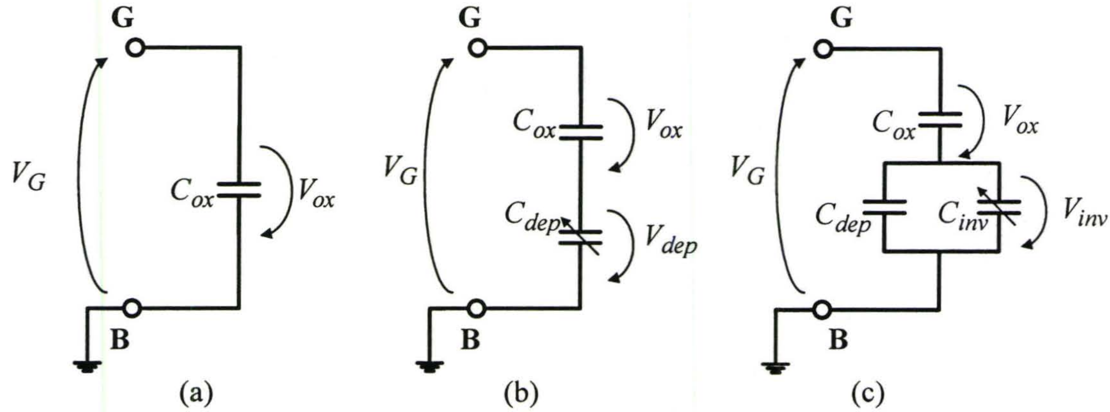


Figure 3.8 Capacitance model of the MOS (B=S=D) when based in (a) accumulation, (b) depletion and (c) inversion.

The value of C_{dep} keeps decreasing with increasing V_G. However, as V_G become close to the threshold voltage of the MOS (V_{th}), an inversion layer of electrons is formed under the oxide. Any further increase in the value of V_G results in an increase of the electrons concentration in the inversion layer. As a result, C_{dep} reaches its minimum value and the width of the depletion region remains constant and an inversion capacitance (C_{inv}) is formed. To derive the overall capacitance in this case,

$$V_G = V_{ox} + V_{bulk} \tag{3.10}$$

then, differentiating

$$\frac{dV_G}{dQ_G} = \frac{dV_{ox}}{dQ_G} + \frac{dV_{bulk}}{dQ_G} \tag{3.11}$$

and for this region of operation

$$Q_G = Q_{inv} + Q_{dep} \tag{3.12}$$

where Q_{inv} is the charge of the inversion layer. Substituting eq.(3.12) in eq.(3.11)

$$\frac{dV_G}{dQ_G} = \frac{dV_{ox}}{dQ_G} + \frac{dV_{bulk}}{dQ_{inv} + dQ_{dep}} \tag{3.13}$$

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_{inv} + C_{dep}} \tag{3.14}$$

Eq. (3.14) is modeled as shown in Figure 3.8(c). In this figure, C_{dep} is shown as a constant capacitor, however, when inversion is reached; the charge forming the inversion region varies exponentially with the DC gate voltage. Therefore, ($C_{inv}= dQ_{inv}/dV_{bulk}$), varies with the applied voltage and acts as a variable capacitance when varying V_G. Also, since the charge under the gate increases exponentially with V_G, then C_{inv} starts with a minimum value at the onset of inversion at point "*c*" in Figure 3.7, and increases with the increase of V_G. Further increase in V_G drives the MOS to strong inversion, where at this point the value of C_{inv} is much higher that C_{ox}. As a result, in strong inversion the series connection of C_{inv} and C_{ox} yields to C_{ox}, as shown at point "*e*".

3.4.1 Inversion-Mode and Accumulation-Mode MOS

A drawback of the MOS varactor is its non-monotonic C-V curve. This non-monotonic behaviour results in a different C_{max}/C_{min} ratio for large-signal operation, which is different than the small signal C-V curve of Figure 3.7. The large-signal operation of the VCO degrades the ratio C_{max}/C_{min} which becomes a function of the amplitude of oscillation. Assuming a MOS varactor biased in depletion region, then the large signal amplitude will drive the varactor beyond $V_G(C_{min})$ into inversion causing the capacitance to increase. As a result, the average capacitance for the large signal at this point will increase and will become larger than the small-signal capacitance value. Therefore, biasing the MOS varactor for large-signal operation at any point in the linear part of the C-V graph will cause the large-signal capacitance to be larger than the small-signal capacitance, which consequently increase the value of C_{min} for large signal operation. Hence, the ratio C_{max}/C_{min} is smaller for large-signal than for small-signal applications. This is considered one of the disadvantages of the MOS (B=S=D) structure [30]. However, a monotonic behaviour can be achieved by applying a different biasing to the MOS other than the B=D=S, and

depending on the biasing condition, the MOS will operate either in inversion-mode only or in accumulation-depletion-mode only.

The inversion-mode MOS (I-MOS), shown in Figure 3.9(a), has the same structure as the B=D=S MOS varactor. The difference between the B=D=S MOS and the I-MOS is that the B=D=S are separated. The bulk "B" contact is connected to ground while the source and drain contacts are connected together "S=D" to the control voltage. The gate-bulk voltage should have a value that biases the varactor in inversion. Tuning is then done by applying the control voltage to S=D connection, which changes the surface potential under the oxide, and thus, changes the level of inversion and consequently C_{inv}. When increasing the control voltage, the I-MOS goes from strong inversion to weak inversion, however, further increase in the control voltage doesn't push the I-MOS into accumulation because the surface potential under the oxide in weak inversion does not change with change in the voltage of the drain and the source [20]. A typical C-V curve for the I-MOS is shown in Figure 3.9(c)

On the other hand, the accumulation mode MOS (A-MOS) has a slight difference in its structure compared to the other MOS varactors discussed so far. Modifications are made to the structure of the MOS, where the *p+* implantations forming the drain and the source in an n-well for a PMOS are replaced by *n+* implantations. These *n+* implantations acts as the body contact "B" of the MOS. Therefore, the A-MOS in this case acts as a two terminal device, as shown in Figure 3.9(b). The structure shown in Figure 3.9(b) is referred to as a *p*-channel based A-MOS because it is implemented in an n-well and has *n+* body contacts similar to the p-channel MOSFET.

The gate-bulk potential difference initially biases the A-MOS varactor in accumulation. When the control voltage is increased, the gate-to-bulk potential decreases, which drives the A-MOS varactor into depletion as discussed earlier in section 3.4. However, when the value V_{BG} reaches weak and moderate inversion, the C-V curve keeps decreasing, as shown in Figure 3.9(d). It does not start increasing to reach C_{ox} again as in the case

of the MOS (B=D=S) varactor. C_{inv} does not take place in the model of this varactor because $\frac{dQ_{inv}}{dV}$ is equal to zero.

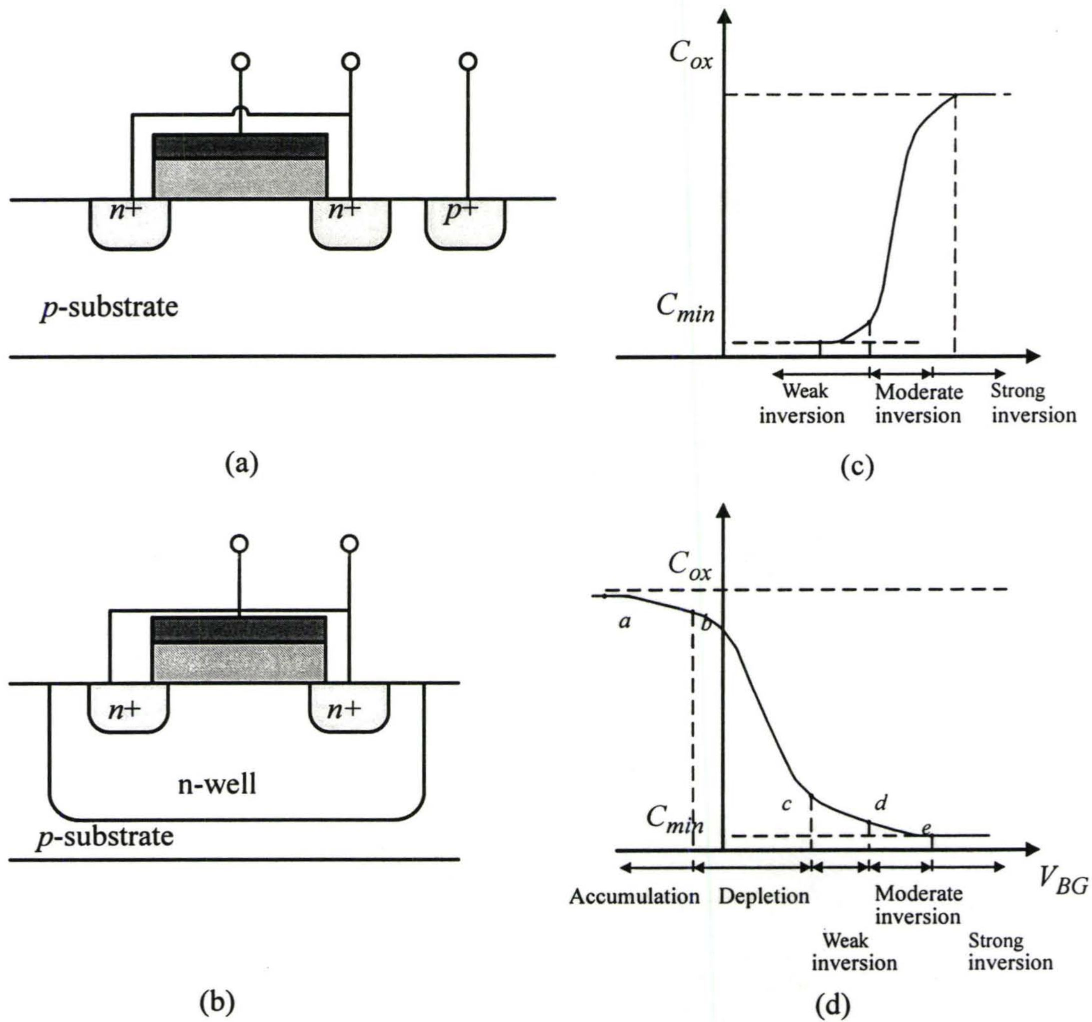


Figure 3.9 Structures of (a) I-MOS and (b) A-MOS. Their *C-V* curves in (c) and (d), respectively.

High frequency changes in the applied voltages does not cause any change in Q_{inv} because the charge in the inversion layer is isolated from the bulk that can provide holes to it by the depletion layer. As a matter of fact, there is only one source of holes for the inversion layer which is the depletion region itself. However, the thermal generation and recombination mechanisms in the depletion region are very slow processes, and hence, any fast change in the charges on the gate, can not be followed by the inversion layer charges [20].

3.4.2 Models

Figure 3.10 and Figure 3.11 show the structures and the models of the I-MOS and the A-MOS varactors, respectively. The model of the MOS (B=D=S) is a combination of both models, where it acts as the A-MOS when it is biased in the accumulation-depletion region, and as the I-MOS in the weak-to-strong inversion region.

In Figure 3.10 and Figure 3.11, the capacitance C_{par} which models the parasitic capacitances of the MOS structure is introduced. The capacitance C_{par} takes into account the parasitic capacitance due to the gate overlap with the drain and source, fringing capacitances and any other capacitance that may occur due to the interconnections.

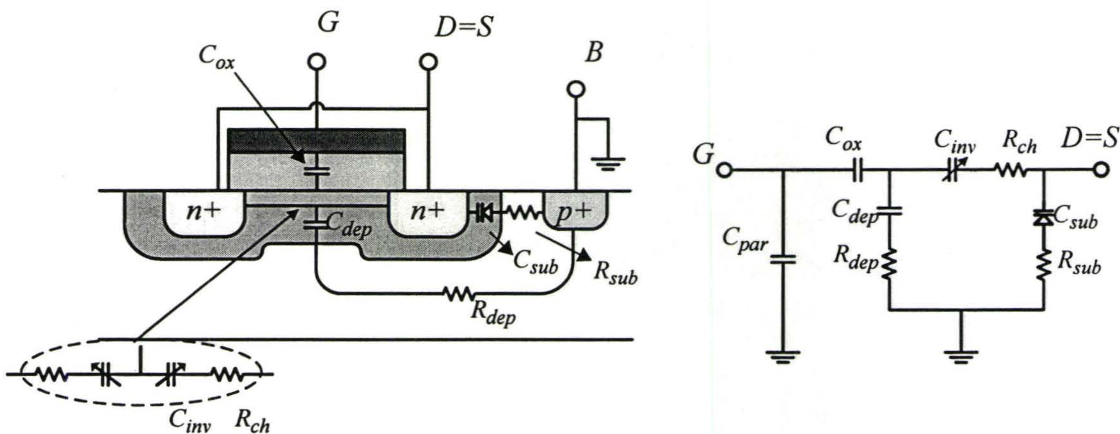


Figure 3.10 The (a) structure and (b) model of I-MOS varactor.

The parasitic capacitance C_{par} has a great impact on the C_{max}/C_{min} ratio of the varactor, as a high value of C_{par} would degrade the C_{max}/C_{min} ratio. The value of C_{min} is equal to

$$C_{min} = C_{par} + C_{ox} \| [(C_{inv} \| C_{sub}) + C_{dep}], \tag{3.15}$$

where the symbol $\|$ means that the capacitors are added in series. C_{max} is then given by

$$C_{max} = C_{par} + C_{ox} \tag{3.16}$$

Considering Eqs. (3.15) and (3.16), if the value of C_{par} is minimized in the design of the varactor, then the tuning range is enhanced.

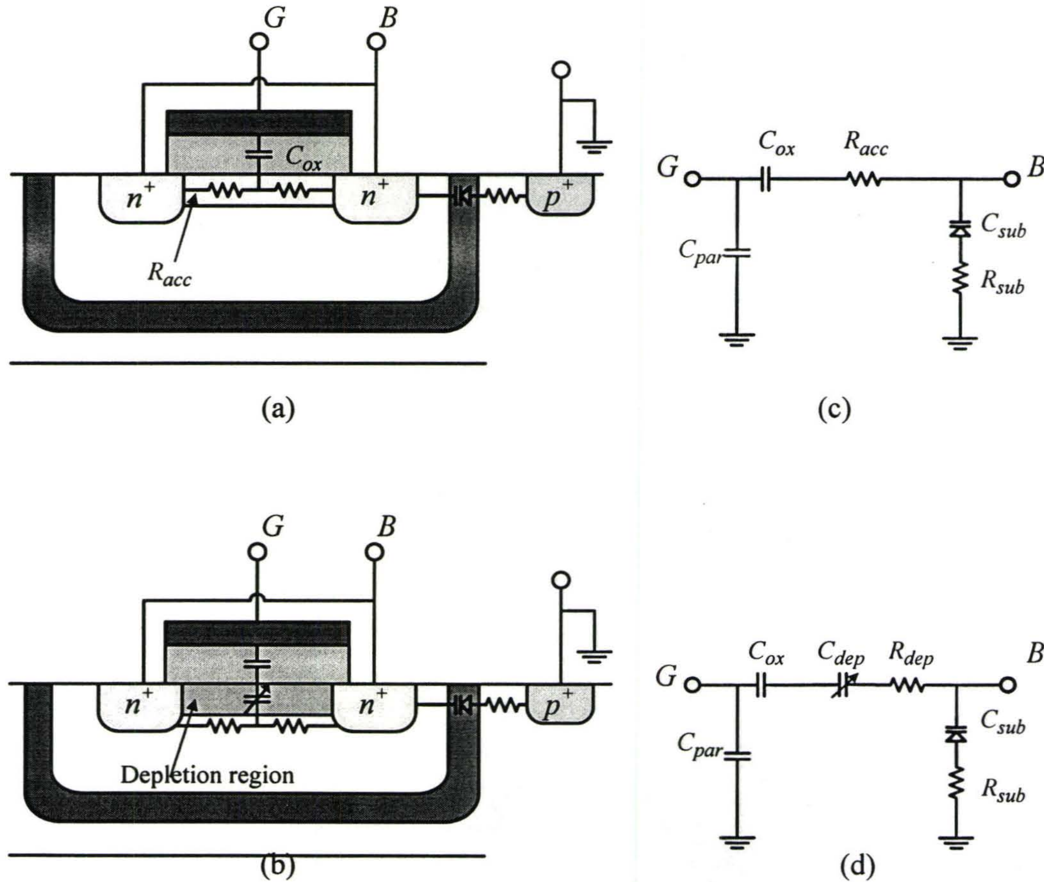


Figure 3.11 The structure of A-MOS varactor (a) in accumulation and (b) depletion. Their corresponding circuit model in (c) and (d), respectively.

The quality factor performance can also be easily understood from the circuit models of Figure 3.10 and Figure 3.11. When the A-MOS is biased in strong accumulation, the resistance R_{acc} has a small value leading to high values of Q_c as shown in Figure 3.12. As the V_{GB} increases, less electrons are accumulated under the oxide and thus, R_{acc} increases, which consequently leads to decrease in Q_c. R_{acc} reaches its largest value at point "a" in Figure 3.12. Beyond point "a", R_{acc} does not exist any more because the A-MOS turns its operation region to the depletion and the model at this point becomes the model shown in Figure 3.11(d). The quality factor starts increasing again as the varactor goes more into depletion. Further increase in the gate voltage pushes the varactor into inversion. Although no inversion capacitance is present in the A-MOS varactor model, however, the resistance R_{inv} has a loading effect on the depletion capacitance and degrades its performance more as the varactor goes deeper into inversion.

In the case of the I-MOS varactor, R_{inv} increases and the level of inversion decreases. Therefore, the Q_c values also becomes higher as the level of inversion increases.

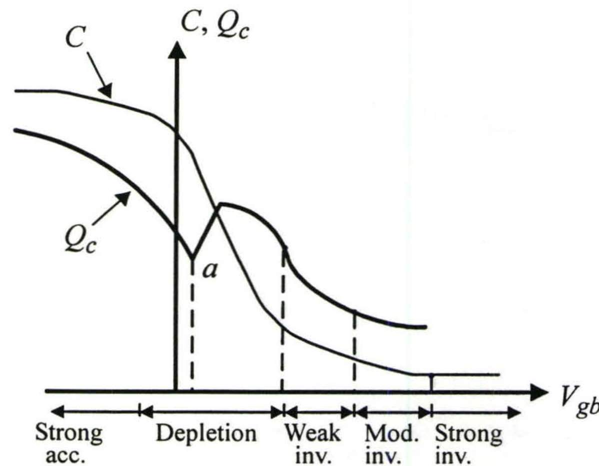


Figure 3.12 C-V curve of an AMOS varactor and the corresponding Q_c-V curve.

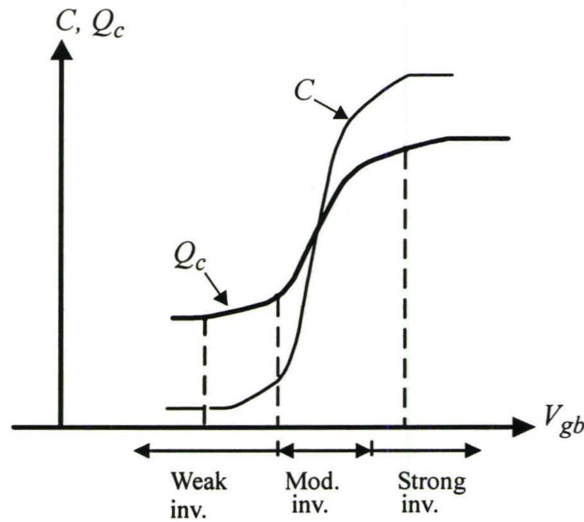


Figure 3.13 *C-V* curve of an I-MOS varactor and the corresponding Q_c-V curve.

3.4.3 Optimized Circuit Design

The most important rule that should be considered when connecting any of the MOS varactors to the circuit is that the gate terminal should be connected to the load node of the VCO. If connected otherwise, the losses of the substrate will add extra loading to the output node of the VCO which degrades the overall Q_c, and consequently degrades the overall performance of the VCO.

Similar to the discussion in section 3.3.2 for the *pn* diode varactor, the MOS varactor should also be treated in the same way. It is recommended to connect an external relatively-large capacitance to the cathode terminal to avoid the loading effect of the low Q_c substrate capacitance [23].

3.4.4 Optimized Layout

In order to achieve the desired performance of the MOS varactor, it should be properly laid-out, as its layout plays an important role on its performance. But, as men-

tioned before for the *pn* diode varactor, trade-offs are always present between optimizing the performance for high Q_c operation or high C_{max}/C_{min} operation.

For example, the ratio C_{max}/C_{min} is dependent on the area of the MOS varactor. Consider the parasitic capacitances in Figure 3.14, where C_{ov} is the overlap capacitance between the gate and the source as well as the gate and the drain and $C_{fringing}$ is the fringing capacitance between the gate and the source and the drain. Usually, the values of C_{ov} and $C_{fringing}$ are technology dependent when normalized to the width of the transistor. So in order to achieve high C_{max}/C_{min} values C_{ox}, C_{dep} and C_{inv} should be maximized with respect to C_{ov} and $C_{fringing}$. Maximizing C_{ox}, C_{dep} and C_{inv} for a fixed C_{ov} and $C_{fringing}$ can be achieved in two ways. The first approach is by maximizing C_{ox}, C_{dep} and C_{inv} by increasing the gate length of the gate (L_{gate}) of the MOSFET and decreasing its width (W_{gate}). The second approach is by minimizing C_{ov} and $C_{fringing}$ through shallow trench isolations (STI), as shown in Figure 3.15. However, introducing the STI increases the parasitic resistances shown in Figure 3.15, and consequently degrades Q_c. This approach shows the first conflict between designing the layout for maximum Q_c and maximum C_{max}/C_{min}.

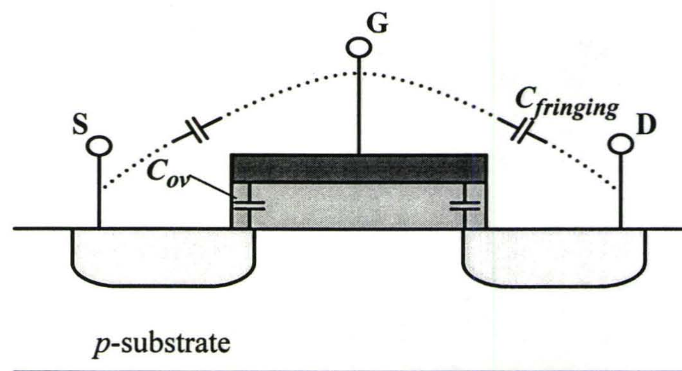


Figure 3.14 Parasitic capacitances of the MOS.

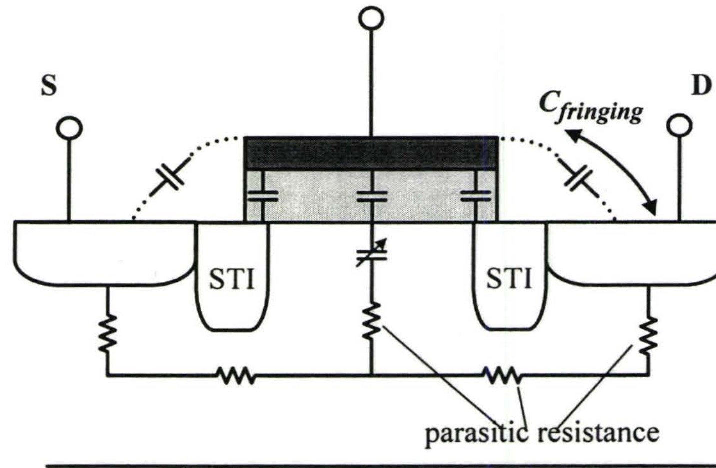


Figure 3.15 MOS with STI [27].

From the Q_c point of view, there are two main components that determine the losses of the varactor: the gate resistance R_g and the resistance of the channel under the oxide. The value of R_g is usually not dominant due to the relatively low sheet resistance of the polysilicon gate, however, using MOS varactors with wide gates will lead to higher R_g values, which will consequently decrease Q_c. Therefore, gate splitting of the MOS varactor should be done to decrease the total R_g, as shown in Figure 3.16(b). Splitting the gate into n fingers decreases the value of R_g by a factor of n^2. As a result, the factor of Q_c that is responsible for the losses of the gate is enhanced by a factor of n^2.

To further decrease R_g, double gate connections are used, as shown in Figure 3.16(c). This double gate connection reduces R_g by a factor of 4, which consequently enhances Q_c.

For higher Q_c values, the channel resistance under the oxide should be minimized. This is achieved by adjusting L_{gate} to the minimum length provided by the technology. This approach shows another conflict between designing for maximum Q_c and maximum C_{max}/C_{min}.

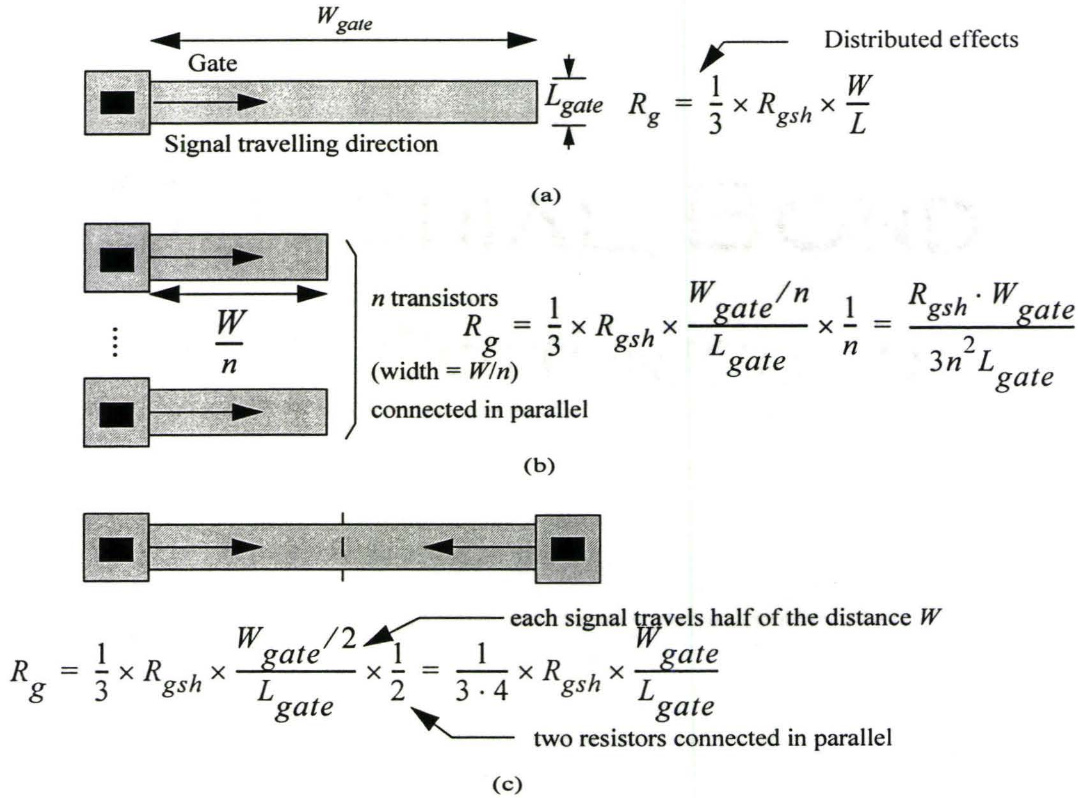


Figure 3.16 Effective gate resistance (R_g) of (a) single finger, (b) n multi-fingers and (c) single finger with double gate contacts [29].

3.5 Differential Varactors

The varactors discussed so far, whether *pn* junctions based or MOS based, are single-ended only and are used for single-ended circuits. However, in the case of differential circuits, it is better if the device is optimized for differential operation. Figure 3.17(a) and Figure 3.17(b) shows a typical differential diode and MOS varactors, respectively, that are optimized for differential operation. These varactors are composed of an even number of capacitive cells (*pn* junction or MOS), and they are laid-out in such a way such that each

capacitive cell that is connected to V_{out}^{+} of the VCO has an adjacent one connected to V_{out}^{-}. This connection makes the common node that is connected to the control voltage act as an AC ground. As a result, the effect of the lossy substrate network is eliminated and no external capacitors are needed to reduce the effect of the control voltage source resistance or the substrate network.

Single-ended varactors can also be used for differential circuits. They can be connected back-to-back in order to have an AC ground at the control voltage node. However, in the case of the differential varactors, higher Q_c values can be achieved because their compact layout eliminates the contact and the inter-connection resistances between the two varactors, as they both share the same control voltage contact. Also, differential type varactors are more compact when compared to the single-ended ones, and hence, saves on-chip space.

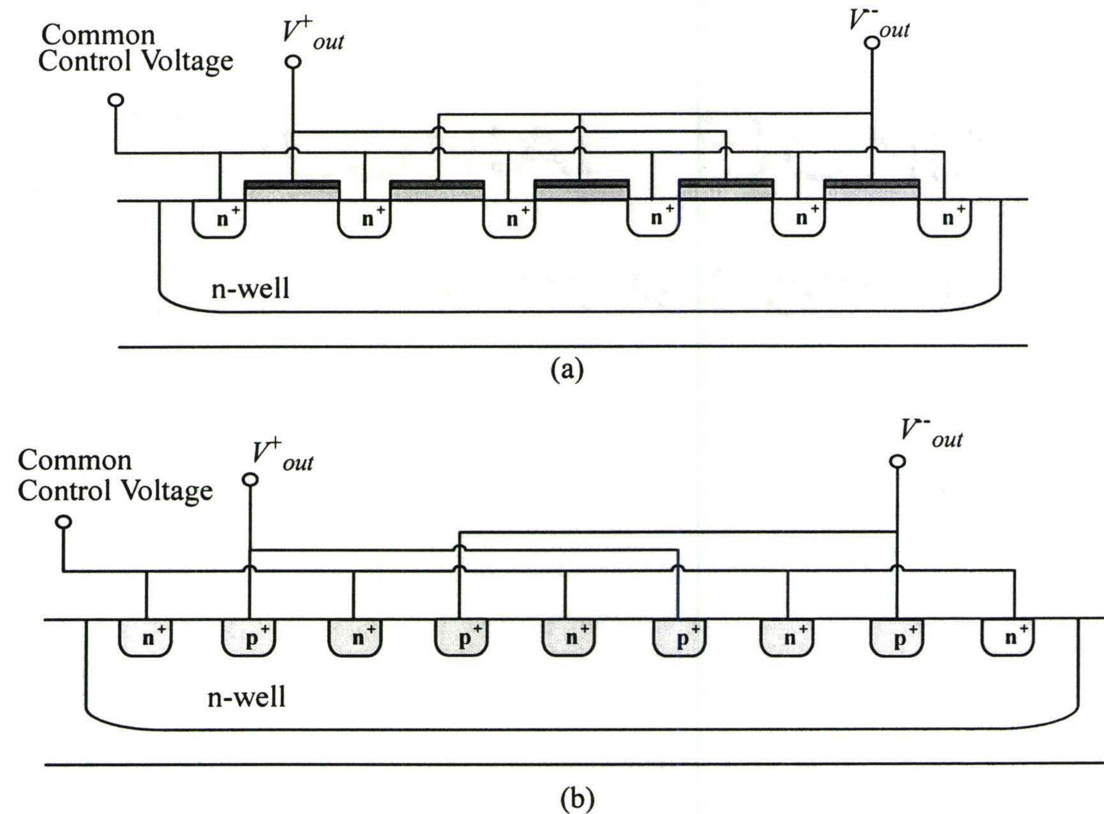


Figure 3.17 Layout of differential (a) MOS-based varactor and (b) diode varactors [32].

3.6 Comparisons

Table 3.1 shows the comparisons between the *pn* diode and the MOS varactors, with respect to the two main performance parameters Q_c and C_{max}/C_{min}. The table shows that the ratio C_{max}/C_{min} for MOS varactors is better than that of the diode varactors. However, Q_c for diode varactors show higher values when compared to MOS ones.

These comparisons were done for varactors fabricated in 0.5 μm CMOS technology. There is not much research published on more advanced technologies, specially for diode varactors. However, MOS varactors are showing an improved performance with

technology scaling, where a value of 108 for $Q_{c,min}$ was measured in [26] for A-MOS varactors, although these varactors were not optimized for high Q_c values.

Table 3.1 Comparison of capacitance tuning ratio and $Q_{C,min}$ for different types of CMOS varactors [31].

Reference	Varactor Type	CMOS Technology (μm)	Tuning Voltage (V)	C_{max}/C_{min} *Ratio*	$Q_{C,min}$
[32] 2000	p^+–to–n-well junction	0.5	V_R = [0, 1.8]	1.31	110
[32] 2000	*p*I-MOS	0.5 (l_g = 0.5 μm)	V_{GS} = [-1.6, 0.2]	1.74	19
[32] 2000		0.5 (l_g = 1 μm)	V_{GS} = [-1.6, 0.2]	2.01	3.4
[33] 2000	*n*I-MOS	0.5	V_{GS} = [0.5, 2.3]	2.15	25.8
[32] 2000	*n*A-MOS	0.5 (l_g = 0.5 μm)	V_{GS} = [-1, 0.8]	2.07	51
[32] 2000		0.5 (l_g = 1 μm)	V_{GS} = [-1, 0.8]	2.76	10.5
[33] 2000		0.5	V_{GS} = [0.5, 2.3]	1.69	33.2

3.7 Summary

In this chapter, the basic fundamentals of the varactors were discussed. The different parameters that define and evaluate the performance of the varactor were introduced. In section 3.3, the diode varactors were discussed. The discussion on the *pn* diode varactors was then focused on one type of varactor which is the *p*+ in *n*-well as it has the best quality factor performance of the *pn* diode varactors. The circuit model of this diode was described. Based on that model, the design circuit considerations of the diode varactor were discussed. The review on the diode varactors was finalized by the layout considerations when designing the varactor in order to achieve the highest quality factor possible.

Similar presentations were given for the MOS varactors and all its types. In section 3.5, the design of varactors for differential circuits was shown. Finally, a comparison was

presented between the performance of the diode varactor and the MOS varactor with all its operation regions.

Based on the discussions in this chapter, the diode varactors in chapter five are designed. The main goal was to design an A-MOS varactor for the VCO design. Unfortunately, A-MOS varactors models were not available at the time. Simulations using a GENSIS device simulator provided by *ISE* (Integrated system engineering) were done in order to characterize the A-MOS varactor. However, the simulations were not accurate because the speculated process parameters of the CMOS 0.18 μm technology were not accurate. Accurate process parameters were not available because it is considered confidential information for the manufacturer. Therefore, the varactors used in the design of the oscillators are regular B=D=S MOS.

Chapter 4 *Passive Inductors*

In chapter three, the design and operating fundamentals of varactors were discussed. This was the first passive device used in the design of the LC VCO. However, a properly designed varactor does not mean that the VCO would have the required phase noise, power consumption and tuning performances. A properly designed varactor, limits the performance of the VCO by the inductor only, which reduces the tasks of the RF designer and focuses attention to the inductor design.

In this thesis, three types of inductors are used. These inductors are off-chip surface-mount (S.M.) commercial inductors, monolithic spiral inductors and bond-wire inductors. The off-chip S.M. inductors and the monolithic spiral inductors will be used in the VCO designs in later chapters. However, a quick review should be given on the bond-wire type because they are used to connect the chip to the outside world and their effects should be added after each pad. Each type of these inductors has its own advantages and disadvantages, and there is no inductor that gives the best characteristics and performances. These advantages and disadvantages will be discussed later in this chapter while studying the inductors themselves.

4.1 Performance Parameters of Inductors

Generally, inductors are the passive components that limit the performance of the VCO the most. This is because of their low Q_L values and low self resonance frequency (f_{SR}) values. This will be discussed in detail below.

4.1.1 Quality Factor

Recall eq. (2.8) in which the quality factor of an inductor is given by

$$Q_L = 2\pi\frac{|\text{Total magnetic energy stored - total electric energy stored}|}{|\text{Total energy dissipated}|} \tag{4.1}$$

The inductors discussed in this chapter are all based primarily on the self-inductance of a long wire or a microstrip. These long wires or wound microstrips increase the total inductance by adding the effect of mutual-inductance to the overall inductance. Due to the long lengths and the finite conductance of the metals used, inductors exhibit losses due to the resistance of the metal itself, which decreases their Q_L. In the case of monolithic spiral inductors, other physical phenomena contribute to the degradation of the overall Q_L value, such as the magnetic and capacitive coupling to the conductive substrate. This will be discussed further in section 4.5.2.4.

4.1.2 Self Resonance Frequency

The self resonance frequency is defined as the frequency at which the reactive component of the passive device becomes zero. In case of an inductor, f_{SR} determines the frequency at which the inductor exhibits capacitive characteristics.

The f_{SR} of inductors is usually much less than that of varactors, and for some inductors, f_{SR} is in the range of 50 GHz.

It is always desired to operate at frequencies much less than the f_{SR}, in order to obtain high Q_L values as Q_L degrades near the f_{SR}. The reason for this can be clearly iden-

tified from eq. (4.1) where at f_{SR}, the magnetic energy stored and the electrical energy are equal and out of phase, which makes the nominator of eq. (4.1) equals to zero, and hence, a Q_L becomes zero, which is undesirable for the VCO design.

4.2 Off-chip Surface Mount Inductors

An off-chip Surface Mount (SM) inductor is a solenoid wrapped around a ceramic core. Traditionally, off-chip SM inductors were used in VCO circuit designs. These inductors have high Q_L values of about 40 at DC and low RF [34]. They are cheap and small in size. However, there is a major disadvantage from the system-integration point of view, where it is always preferable to decrease the number of off-chip components in order to reduce the P.C.B. complexity and component count [28], which results in less cost and assembly efforts.

Another disadvantage of SM inductors is the relatively high tolerance in the inductance values. The tolerance can be up to ±5 % for the inductors used in this research. This relatively high tolerance has two drawbacks on the VCO design. First, the oscillating frequency is affected by this tolerance with a value of approximately 2.4%. Second, in case of differential oscillators that use different tank circuit loads, mismatch might occur between the two tank circuits. This mismatch affects the phase noise and the power consumption performance of the oscillator and might even cause malfunction of the oscillator. This mismatch issue will be discussed later in chapter five.

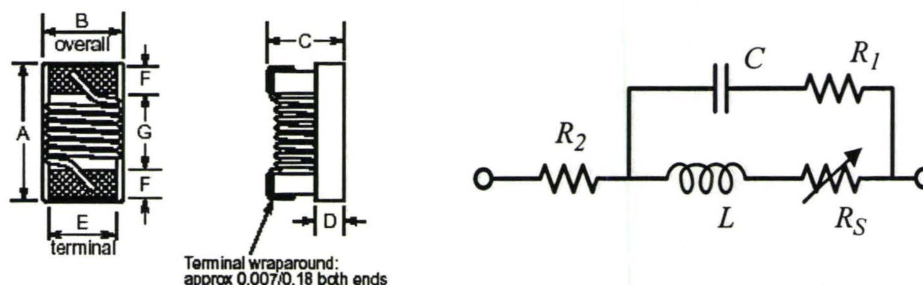


Figure 4.1 (a) A schematic of the S. M. inductors, (b) its equivalent model.

Table 4.1 Typical dimensions for S. M. inductors in mm.

Size Code	A	B	C	D	E	F	G
0402	1.19	0.64	0.66	0.25	0.51	0.23	0.56
0604	1.85	1.37	1.19	0.64	1.02	0.33	0.86

A typical S.M. inductor is shown in Figure 4.1(a), and its equivalent model in Figure 4.1(b). The dimensions for different sizes are illustrated in Table 4.1 In Figure 4.1, L resembles the inductor value, R_s models the series resistance due to the wiring of the inductor. R_s is affected by the skin effect at high frequencies. Therefore, it varies with frequency through the relation [34]

$$R_s = k \times \sqrt{f} \tag{4.2}$$

where k is a constant provided by the manufacturer.

The capacitance C is the equivalent inter-capacitance between the turns of the inductors, R_1 is the losses associated with these capacitances and R_2 is the series losses due to the contacts. The parameters k, C, R_1 and R_2 are extracted from the measured s-parameters of the inductor and are provided in the data sheets of the manufacturers.

4.3 Bond-Wires

Bond-wires are used whenever the chip is connected to the outside world. The bond-wires are gold or aluminum wires that connect the pads to the pins of the package that surrounds the chip. The inductance of the bond-wires is a function of its length through the relation [13]

$$L = \left(\frac{\mu_o l}{2\pi}\right)\left[\ln\left(\left(\frac{2l}{r}\right) - 0.75\right)\right] \approx 2 \times 10^{-7} l\left[\ln\left(\left(\frac{2l}{r}\right) - 0.75\right)\right], \tag{4.3}$$

where, μ_o is the permeability in free space, l is the length of the wire and r is its radius.

Bond-wires have Q_L values around 50, which made them very attractive for RF circuit designers. Furthermore, they save on-board space and decrease its complexity. Hence, bond-wires were used in VCO designs in [35], [36]. Figure 4.2 shows a VCO with bond wires as the tank inductances. The bond-wires shown in this figure connect the two far ends of the chip to achieve the desired inductance value, however, this would result in an on-chip routing problem. Hence, bond-wires are used in pairs (one going to the far end of the chip and the other returning back) to overcome this problem. These bond-wire pairs are shown in Figure 4.2 [35].

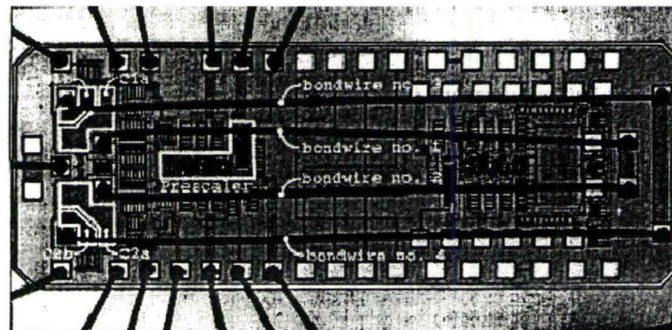


Figure 4.2 Die photo of the VCO presented in [35] which used four bond-wires to implement two inductors [37].

A disadvantage of using bond-wires occurs when multiple inductors are required, because of the mutual coupling between the bond-wires. This mutual coupling must be taken into consideration as it may result in many unwanted interactions between the bond-wires that would affect the performance of the circuit [37]. Another disadvantage of using bond-wires comes from the parasitic capacitances and resistances of the pads that are used to connect the bond-wires. Finally, due to the positioning uncertainties of the bonding process, a tolerance value of about ±6 % is expected [35], [37]. Also, the controllability of the wire size, length, spacing and curvature are not precise, which result in extra high tolerance in the inductance value. This high tolerance in the inductance value causes high toler-

ance in the frequency of oscillation and causes mismatch issues in case of differential circuits.

4.4 Spiral Inductors

Monolithic spiral inductors have attracted a lot of attention in the past decade as they present the fully-integrated, on-chip solution for RF circuit design. Extensive studies have been done on the theory, design, modeling and characterization of spiral inductors [38], [54].

The concept of the spiral inductors resembles the concept of the off-chip inductors, where the total inductance is due to the spiral self inductance and the mutual inductance between the turns of the inductor. However, monolithic spiral inductors are planar spirals unlike the three dimensional off-chip inductors. If monolithic spiral inductors were three dimensional inductors then the vias that connects different metal layers would increase the losses of the spiral. Also, using several metal layers to implement the spiral in 3-D would increase the inter-capacitances of the spiral and the capacitance to the substrate which results in a lower f_{SR} and higher substrate coupling.

Spiral inductors were first implemented in GaAs technologies [39]-[41]. The inductors showed high Q_L values that range from 10-20 [28]. Later in the 1990s, inductors were introduced into Si technology [42], however, lower Q_L values were obtained when compared to GaAs spirals due to the higher conductivity substrates that are used in Si technologies. A major part of the research done on spiral inductors has been dedicated to finding suitable techniques to increase the Q_L values of spiral inductors that are fabricated on Si substrates. Some of these approaches will be discussed later in this chapter.

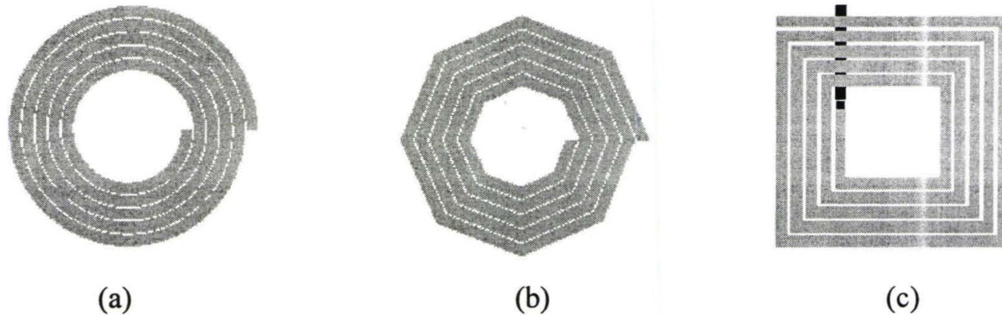


Figure 4.3 Different shapes for planar spiral inductors. (a) Circular (b) Octagonal (c) Square [58].

The implementation of spiral inductors can take the shapes shown in Figure 4.3. The circular and the octagonal spirals are reported to have 10% less series resistances than the square spirals [55]. The 90° bend in the square spiral results in current crowding at the edges which increases the losses at this point; however, the effect of the edge losses is minimized in the circular and the octagonal structures due to the smooth edges; with the circular one being superior to the octagonal. In spite of the modest performance of the square spiral inductor when compared to the circular or the octagonal, it is still the most widely used type of spirals because most technologies do not support non-Manhattan geometries. However, the TSMC 0.18 μm technology that is used in this research support the 45° angles, and hence, octagonal spirals can be implemented.

In the following subsections, the modeling methods of the spiral inductor will be briefly discussed. More comprehensive discussion will be given afterwards on the components forming the lumped circuit model and their physical origin, with emphasis on the methods used to minimize the lumped model to achieve high Q_L values. Finally, a deviation of the conventional spiral inductor will be discussed and simulation results will be presented.

4.5 Modeling of Spiral Inductors

Modeling of spiral inductors is generally preferred in one of the following three ways: using field solvers, segmented circuit models or lumped element circuit models [56]. There are always trade-offs between the accuracy of the model verses its computational time and simplicity. The field solver method is the most accurate. It solves the 3-D Maxwell's equations to derive the s-parameters of the spiral inductor. 3-D simulations are slow and have several drawbacks. One of the drawbacks of this method is that it is not compatible with circuit simulators. The 3-D simulator is used to generate a library of simulated s-parameters of the inductors that can be used later by a circuit simulator. Furthermore, this method does not give the RF circuit designer any design insight, in order to understand the trade-offs and to optimize the performance of the inductor [56].

The compatibility with circuit simulator problem was solved by using the segmented circuit models method. The inductor in this case is segmented and a lumped model is used for each segment. The self and mutual inductances of the whole spiral are calculated using the Greenhouse approach. Unfortunately, this approach is complicated and time consuming [56].

To overcome the drawback of the field solver method and the segmented circuit method, a lumped element "π" model for the inductor, shown in Figure 4.4 is used. This model offers high speed of computation and is compatible with circuit simulators. However, the lumped model is not accurate at high frequencies because it does not capture the distributed performance of the inductor.

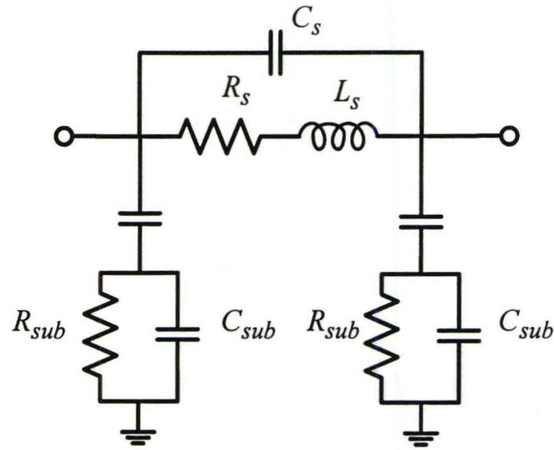


Figure 4.4 Lumped circuit model of the spiral inductor.

Researchers have tried to derive expressions for the circuit elements of this model. These expressions were derived to be functions of the geometries and dimensions of the spiral. These dimensions are [46]:

(a) The number of turns n.

(b) The turn width w.

(c) The turn spacing s.

(d) Any one of the following: the outer diameter d_{out}, the inner diameter d_{in}, the average diameter $d_{avg} = 0.5\ (d_{out} + d_{in})$, or the fill ratio, defined as $\rho = (d_{out} - d_{in})\ /\ (d_{out} + d_{in})$.

By having expressions for the spiral inductor in terms of its dimension; the RF designer can predict and have an idea about the performance of the inductor, and can change the dimensions of the spiral to achieve the suitable values and performances. These expressions are completely empirical or semi-empirical. The semi-empirical models are based on a well understood physical background, but they require fitting parameters due to approximations or neglected effects.

In the rest of this chapter, the physical phenomena behind each of the circuit elements that form the model will be discussed. Emphasis will be given to the model elements that influence the Q_L of the inductor and the methods used to reduce them.

4.5.1 Inductance Calculation

The major challenge in the modeling of spiral inductors is the expression of the inductance itself. Many expressions were proposed to estimate the values of the series inductance L_s. Some published research derived an empirical expression for L_s. A popular model was proposed in [46], where the inductance value was given as,

$$L_s = \beta d_{out}^{\alpha 1} w^{\alpha 2} d_{avg}^{\alpha 3} n^{\alpha 4} s^{\alpha 5(4)}. \qquad (4.4)$$

Here, the coefficients β and αi are tabulated values and are classified according the geometrical structure of the spiral [46].

This expression gives high accuracy because it was based on the data fitting of a library of 19,000 inductors. A major advantage of this model is that it is simple, scalable and also dependent on the geometries of the spiral. However, it does not provide any physical insight on the design of the inductor.

Physically-based models are built on the fact that the total inductance of a spiral inductor is the sum of the total self-inductance (L_{self}) of all metal strips, added to the mutual inductance between those strips. Figure 4.5 shows that segments on one side of the spiral have their currents flowing in the same direction. Meanwhile, segments on the other side of the spiral have their current flow in the opposite direction. Therefore, the interaction between adjacent metal strips produces positive mutual-inductance (*M*+) that increases the total value of the inductance. However, the interaction between the metal strips on opposite sides of the inductor produces a negative mutual-inductance (*M*-) that tends to decrease the overall inductance value of the spiral.

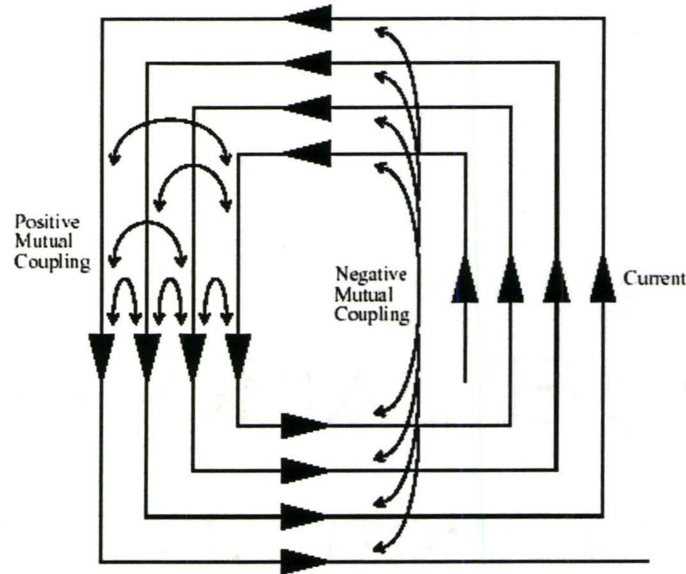


Figure 4.5 Positive and negative mutual inductance between the strips of the spiral [37].

All the inductance components are calculated, starting with L_{self}, and then $M+$ and $M-$. The total inductance L_s is then given by

$$L_s = L_{self} + |M+| - |M-| \ . \tag{4.5}$$

The starting point of the physically based models is from Grover's formula for self-inductance [47], where the self-inductance (L_{self}) of a rectangular conductor is given by

$$L_{self} = 2l\left(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right) \tag{4.6}$$

Here, l is the wire length (cm), w is the width (cm) and t is the thickness (cm).

Hence, the total self-inductance of the spiral can be given by the sum of the L_{self} of each metal strip,

$$L_{self} = \sum_j L_{self_j} , \tag{4.7}$$

where, L_{self_j} is the self-inductance of segment j.

The second step in calculating the total inductance L_s is to evaluate the overall mutual-inductance of the spiral. Starting with two segments with common equal length l, the mutual-inductance M is equal to

$$M = 2l\overline{M}, \tag{4.8}$$

where, M is in nH, l is the length of the wires in cm and

$$\overline{M} = \ln\left[\frac{l}{GMD} + \sqrt{1 + \left(\frac{l}{GMD}\right)^2}\right] - \sqrt{1 + \left(\frac{GMD}{l}\right)^2} + \frac{GMD}{l}. \tag{4.9}$$

GMD is the geometric mean distance between the wires and is given by (4.10)

$$\ln GMD = \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \frac{w^8}{360d^8} - \dots\dots\dots\dots, \tag{4.11}$$

where w and d are the wire width and the pitch between the segments in cm, respectively.

Based on eq. (4.7) for the self inductance and eq. (4.8) that shows the concept of the mutual inductance, the total inductance of a segment is equal to L_s is given by [50],

$$L_j = L_{self_j} + \sum_{n=1, n \neq j}^{N_s} (-1)^{\frac{|j-n|}{2}} M_{j,n} + \sum_{n=1}^{N_s} (-1)^{\frac{|j-n|}{2}+1} M^m_{j,n}, \tag{4.12}$$

where L_{self_j} is the self inductance value of segment j, $M_{j,n}$ is the mutual inductance value of segment j and segment n, $M^m_{j,n}$ is the mutual inductance value of actual inductor segment j and image inductor segment n, and N_s is the number of segments [50].

The total inductance of the spiral inductor is equal to the sum of inductance of all the segments [50] and is

$$L_s = \sum_{j=1}^{N_s} L_j. \tag{4.13}$$

4.5.2 Parasitics of Spiral Inductors

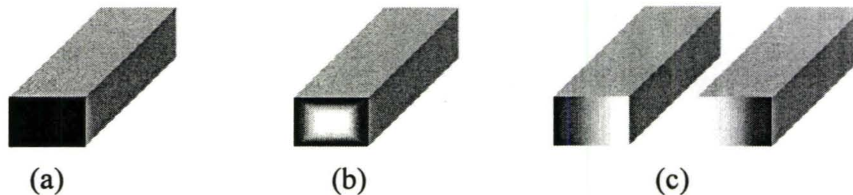
Parasitics of the spiral inductor take two main forms. The first type of parasitics is the resistive type, which affects the overall Q_L of the spiral. The resistive losses occur as metal losses and substrate losses due to electric and also magnetic coupling. The second type of parasitics is capacitive. The capacitive parasitics influence both Q_L and the f_{SR}. Parasitics can also be classified according to their origin, whether it is due to the metal strip or the substrate parasitics, where each of these has both resistive and capacitive parasitic effects.

4.5.2.1 Metal losses (Series Resistance R_S)

The metal losses of the inductor is modeled in Figure 4.4 as the series resistance R_s. At DC, the current passing in the metal strips is distributed evenly within its cross-section, as shown in Figure 4.6(a). In this case, R_s simply models the resistance of the total length of metal used to implement the inductor through the relation

$$R_{DC} = \frac{1}{\sigma} \cdot \frac{l}{w \cdot t}, \tag{4.14}$$

where, σ is the metal conductivity, w is the width of the metal, l is the total length and t is the metal thickness.



(a) (b) (c)

Figure 4.6 (a) DC current distribution, (b) skin effect, (c) proximity effect due to two adjacent strips [54].

As the frequency of operation increases to the GHz range, eq.(4.14) does not hold any more. The resistance of the metal is influenced by the skin effect, where the current tends to flow near the surface, as shown in Figure 4.6(b). Therefore, the effective cross-

section area of the current flowing decreases and thus, increasing the total resistance. The total resistance in this case is given by,

$$R_{skin} = \frac{1}{\sigma} \cdot \frac{l}{w \cdot \delta \cdot (1 - e^{-t/\delta})}, \tag{4.15}$$

where,

$$\delta = \sqrt{\frac{1}{\pi \sigma \mu_o f}} \tag{4.16}$$

where, δ is the skin depth, μ_o is the permeability in free space and f is the frequency of operation.

As shown in Figure 4.7, the current density within the metal takes an exponentially decaying profile with the metal depth. This exponential current distribution can be modeled as an equivalent current with constant distribution with a depth equal to t_{eff}, which is given by,

$$t_{eff} = \delta \cdot (1 - e^{-t/\delta}). \tag{4.17}$$

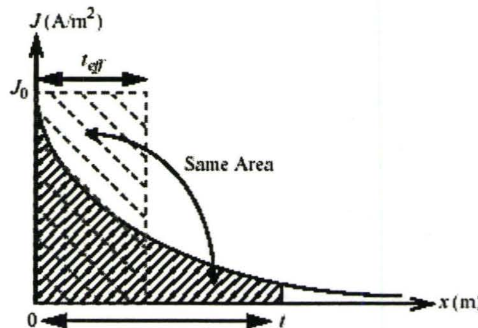


Figure 4.7 Effective thickness of a conductor with finite thickness *(t)* under the skin effect.

In order to optimize the design of the microstrip at the required frequency of operation, its width w should be set to a values equal to (4~5)δ [57]. If larger values of w are designed, the metal strip will have no current passing through its center and the resistance

will stay the same if w increases. Therefore, it is not practical to go for larger widths as it will just increase the space consumed and the capacitance.

Another high frequency parasitic effect is the current crowding mechanism due to the proximity between the metal strips of the inductor. The magnetic flux produced by the metal strips produces eddy currents within the metal of the adjacent metal strips, as shown in Figure 4.8. The eddy current produced tend to redistribute the current within the metal, where the current density increases near one end of the metal strip and deceases at the other side. As a result, the effective cross-sectional area for the current is decreased, leading to an increase in the overall resistance. The overall current distribution due to the skin effect and the proximity effect is illustrated in Figure 4.6(c).

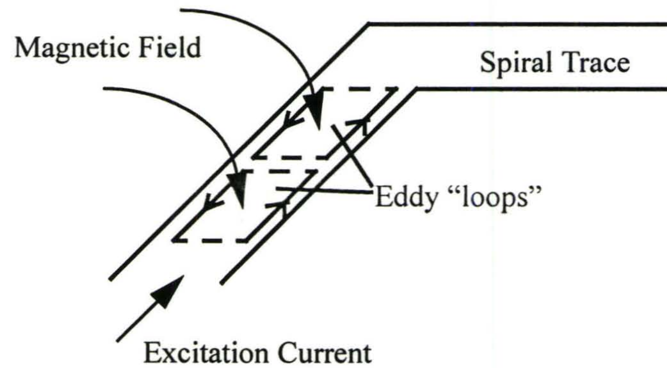


Figure 4.8 Illustration of current crowding [49], [50].

The resistance caused by current crowding is given by,

$$R_{crowd} = 0.1 \times R_{DC} \cdot \left(\frac{f}{f_{crit}}\right)^2, \tag{4.18}$$

with

$$f_{crit} = \frac{3.1}{\mu_o} \cdot \left(\frac{w+s}{w^2}\right) \cdot R_{Sheet}, \tag{4.19}$$

where l is the total length of the spiral, w and s are the width and the spacing, respectively.

The current crowding effect is related to the intensity of the magnetic flux that crosses the metal strip, which depends on the number of turns (i.e. total number of parallel strips) and the spacing between the strips. Eq.(4.18) and eq.(4.19) shows that R_{crowd} increases when the number of parallel strips increase and when the spacing between the metals decreases.

Finally, as a result of the above discussion, the overall series resistance of the inductor at high frequency is given by,

$$R_s = R_{skin} + R_{crowd} \tag{4.20}$$

4.5.2.2 The Feed-through Capacitance

Figure 4.9(a) shows the origin of the feed-through capacitance C_s of the lumped circuit model in Figure 4.9(b). The capacitance C_s is formed due to two types of capacitances, as shown in Figure 4.9(a). The first is the cross-talk capacitance (C_{ct}) between the neighbour metal strips The second is the overlap capacitance (C_{ov}) which occur between the lower level metal that is used to connect the inner port of the inductor and the other strips of the spiral. Simulations done in [37] showed that C_s is mainly due to C_{ov} and not C_{ct}, because C_{ct} is added in series and C_{ov} is added in parallel, that decreases the overall C_{ct} and increases the overall C_{ov}, respectively. The overall C_s is then given by,

$$C_s = n \cdot w^2 \cdot \left(\frac{\varepsilon_o \varepsilon_{ox}}{t_{ox,\,\mathrm{M1\text{-}M2}}}\right), \tag{4.21}$$

where n is the number of overlaps, w is the line width and t_{ox} is the oxide thickness between the spiral and the underpass [37].

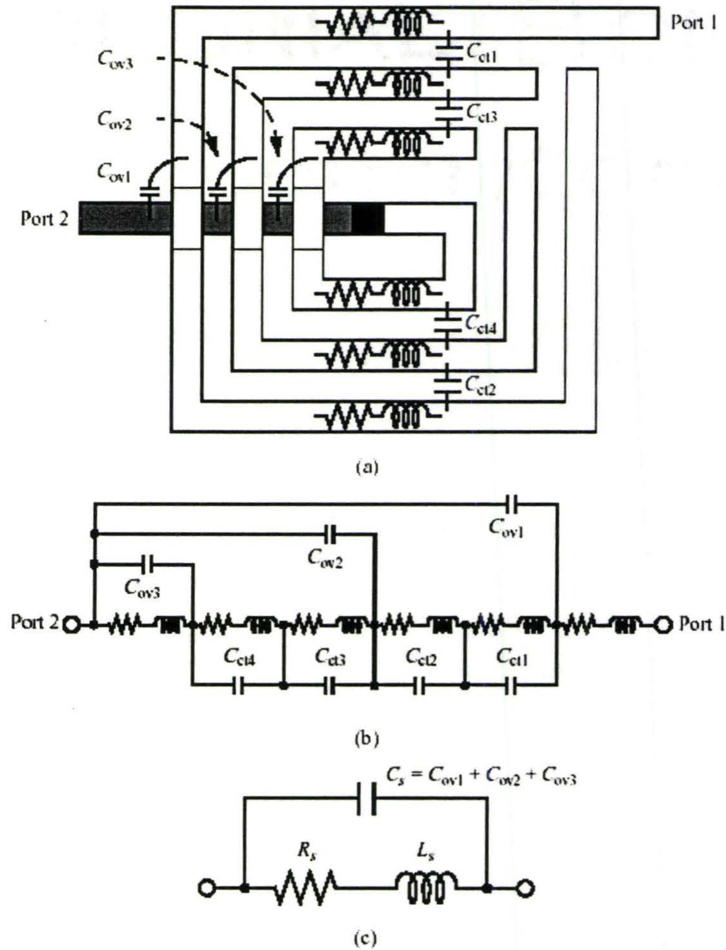


Figure 4.9 A three-turn inductor: (a) layout and relevant elements (b) distributed model and (c) lumped model [37].

4.5.2.3 The Oxide Capacitance

The oxide capacitance C_{ox} is given by [37],

$$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox}}, \tag{4.22}$$

where t_{ox} is the thickness of the oxide between the spiral and the substrate.

4.5.2.4 The Substrate Parasitics

The substrate network C_{sub} and R_{sub} models the capacitive effects occurring in the semiconductor and the high-frequency resistivity of silicon, respectively. The signal through the inductor is electrically coupled to the substrate network through the oxide capacitance C_{ox}. The substrate network elements can be calculated [37] using

$$C_{si} = \frac{1}{2} \cdot l \cdot w \cdot C_{sub} \tag{4.23}$$

$$R_{si} = \frac{2}{l \cdot w \cdot G_{sub}} \tag{4.24}$$

where, l is the spiral length, w is the spiral width and the product $w.l$ is the total area under the inductor. C_{sub} and G_{sub} are the capacitance and the conductance per unit length, respectively.

The substrate network has a great impact on the high-frequency performance and the Q_L of the inductor, where the conductive CMOS substrate degrades the f_{SR} and Q_L significantly. As high Q_L values are a major concern in this thesis, approaches that reduce or eliminate the degradation of Q_L at high frequency due to the substrate network are discussed. However, to further discuss this matter, it is better to look at the corresponding series equivalent circuit of the substrate network and C_{ox}. The one port model of the spiral in Figure 4.10(a) has its substrate network and C_{ox} converted to their series equivalent in Figure 4.10(b) [37]. The quality factor of this model is then given by,

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_P}{R_P + R_s[(\omega L_s / R_s)^2 + 1]} \cdot \left[1 - \frac{R_s^2(C_s + C_p)}{L_s} - \omega^2 L_s(C_s + C_p)\right] \tag{4.25}$$

$$= \frac{\omega L_s}{R_s} \cdot Substrate\ Loss\ Factor \cdot Self\text{-}resonance\ Factor$$

where,

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{sub}} + \frac{R_{si}(C_{ox} + C_{sub})^2}{C_{ox}^2}, \tag{4.26}$$

and $$C_p = C \cdot \frac{1 + \omega^2 (C_{ox} + C_{sub}) C_{sub} R_{sub}^2}{1 + \omega^2 (C_{ox} + C_{sub})^2 R_{sub}^2}. \tag{4.27}$$

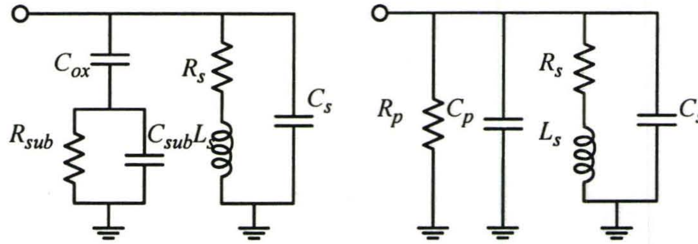


Figure 4.10 (a) One port model, and (b) the equivalent model with combined impedance of C_{ox}, C_{sub} and R_{sub} substituted by R_p and C_p [37].

The quality factor is composed of three terms. The first term includes the metal losses, the second term takes into account the substrate losses, and the last term captures the degradation of Q_L with frequency. The main goal in this section is to minimize the second term that accounts for the substrate losses. From eq.(4.25), it can be seen that the substrate loss factor will approach unity as R_p reaches infinity, which implies that R_{sub} should tend to zero or infinity.

Some approaches were proposed in order to reduce the effect of the substrate network through pushing R_{sub} to infinity. An example of these approaches is etching the substrate underneath the spiral to reduce the electrical coupling to the substrate as well as the magnetic coupling [63]. However, such an approach requires special processes and techniques that are not available in commercial digital CMOS technology. Therefore, only one approach is considered in this section which is the patterned ground shield which causes R_{sub} to approach zero.

4.5.2.5 Pattern Ground shield

Ground shields are used to terminate the electric field and prevents it from penetrating into the substrate. However, when the magnetic field crosses the ground plane it

induces image loop currents that flow in a direction opposite to the direction of the current in the spiral. As a result, a negative mutual coupling between the spiral current and the loop current within the ground plane occurs, which degrades the overall inductance of the spiral [37].

In order to avoid the induced current loops within the ground plane, the ground plane is patterned with slots. The slots should be orthogonal to the direction of current in the spiral itself to cut-off the path to any induced loop current. Also, the spacing between these slots should be narrow to avoid the leakage of the electric field to the substrate [37]. Figure 4.11 shows an example of a patterned ground shield. The outermost edges of the patterned ground shield are connected with a metal strip to ground. The ground shield itself is implemented using Metal_1 or polysilicon. In [37] measurements show that poly-silicon is the better choice for the ground plane, however, no clear explanation was given for such a reason.

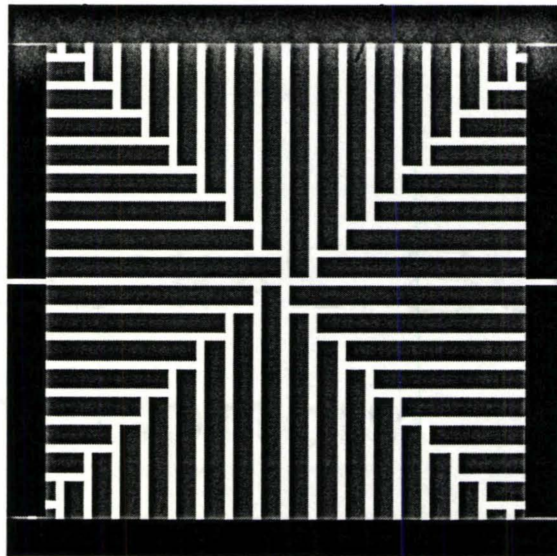


Figure 4.11 Patterned ground shield [56].

4.5.2.6 Eddy Current Losses

The modeling of the eddy currents losses induced in the substrate are not as well studied as the other losses mechanisms. Early attempts to model this phenomenon included these losses within the series resistance R_s of the inductor. This additional resistance due to the eddy current losses in the substrate were calculated and its equivalent effect was added to R_S [56]. Further improvements to model magnetic coupling to the substrate was done in [64], where the substrate magnetic induced losses were modeled by an ideal transformer that is terminated with a resistance equivalent to the impedance of the substrate, as shown in Figure 4.12.

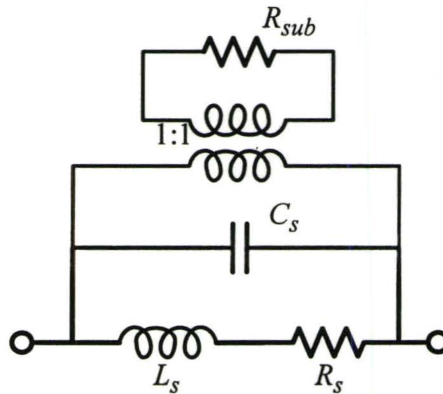


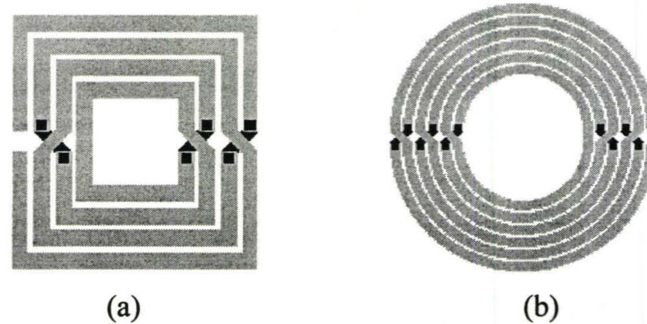
Figure 4.12 Modeling the substrate losses through using a transformer to the substrate [64].

4.5.3 Spiral Inductors in RF Circuits

Spiral inductors are connected to RF circuits in either a single ended or a differential manner. In the case of VCO design, the inductor is sometimes connected as a one-port device, such as the inductors used in the VCO configurations of Figure 2.13 (a) and (b). The spiral can also be connected as a two-port device as in the VCO configuration in Figure 2.13 (c). In previous research, it was shown that spiral inductors connected differentially can acquire higher peak Q_L values and also f_{SR} when compared to the single ended

ones [59], [62]. The reason for the different performance can be understood by considering the spiral inductor as a transmission line (TL) with a length equal to the total length of the spiral, and with an equivalent circuit that resembles the spiral's model. In the case of a single-ended spiral, the other port is short circuited, therefore, the first f_{SR} of the spiral would occur at a the quarter-wavelength frequency. However, when the spiral is used as a two-port device, the first f_{SR} will occur at the half-wavelength frequency. Therefore, the two-port spiral has a f_{SR} that is twice the f_{SR} in case of a one-port spiral. This also implies that higher Q_L values are achieved using the two-port devices and the peak Q_L values are also at higher frequencies when compared to the one-port device.

In order to utilize this observation, symmetric center-tapped inductors were designed [61], [62], as shown in Figure 4.13. The layout shown in Figure 4.13 is ideal for use in the complementary cross-coupled -g_m VCO of Figure 2.13(c). If the VCO in Figure 2.13(c) used the center-tapped inductors as its load, then this configuration can have an inductor that has a Q value twice that for the inductors used for the circuit configurations in Figure 2.13(a) and (b). Using the center-tapped inductor for Figure 2.13(c) provides the VCO with higher Q_L and a higher f_{SR}, which consequently enhances the phase noise performance and the power consumption of the oscillator. Furthermore, using a center-tapped symmetric inductor enhances the symmetry between the two differential branches of the VCO, and hence decreases any mismatch effects. Moreover, using a single two-port inductor rather than two one-port inductors saves on-chip area and decreases the substrate losses.



(a) (b)

Figure 4.13 Center-tapped (a) square spiral and (b) circular spiral [58].

4.6 Parallel Strip, Mutual-inductance Based Inductor

All the inductors discussed so far depend on the self-inductance of the wire or a strip. This wire or strip is then wound to increase the total inductance by adding the effect of the mutual-inductance that occurs between the parallel current lines. However, with increasing either the total length or the number of windings, the series losses of the inductor also increase, leading to limited Q_L values, specially in the case of spiral inductors.

In an attempt to eliminate the resistance of the inductor, that is to increase the value of Q_L, a new parallel strip mutual inductance is proposed, as shown in Figure 4.14. In this figure, *n* strips are placed in parallel to each other. The total self-inductance then is equal to the self-inductance of one strip divided by *n*. Similarly, the total resistance is also decreased by a factor of *n*, keeping the overall Q_L value equal to the Q_L of one single strip.

If these parallel strips are brought close to each other, then the mutual inductance between the strips would increase the total inductance L_s. As a result, the total value of the inductance would be equal to

$$L_{s,\,total} = L_s/n + M. \tag{4.28}$$

According to this equation, the total inductance is decreased by a factor less than the factor of the total resistance. Thus, the overall Q_L value of the inductor is increased when compared to a single strip.

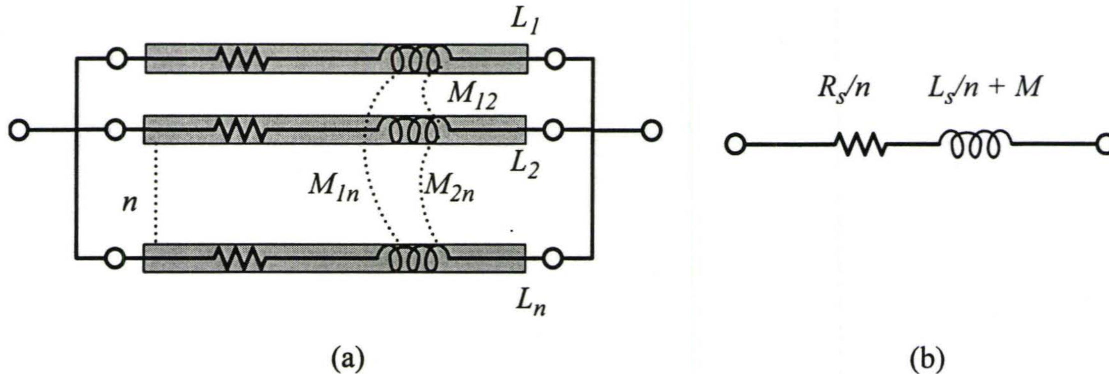


Figure 4.14 (a) Parallel Strips inductor, (b) equivalent circuit model.

A disadvantage of this approach is the low inductance values of the parallel strips, hence, it would be only practical to use this approach for high frequency circuit designs, where low inductance values are required. However, more investigations should be done to determine the f_{SR} and the increase in resistance due to the current crowding effect that is produced by proximity of the metal strips for this inductor.

Two inductors with the same inductance value were simulated to compare the performance of the single and the parallel strip inductors. Inductor 1 was 12 μm thick and was 900 μm long. Inductor 2 was composed of four strips. Each of these strips were 1mm long and 6 μm thick and they were set at 1 μm from each other. Figure 4.15 shows the equivalent inductance values of both inductors to be approximately the same. However, Figure 4.16 shows that inductor 1 has a peak Q of 11.5 while inductor 2 shows a peak Q of 14.2.

These simulation results show higher Q values for the parallel strip inductor. However, electromagnetic simulation results might be optimistic, therefore, measurements of these inductors are required to confirm the theory.

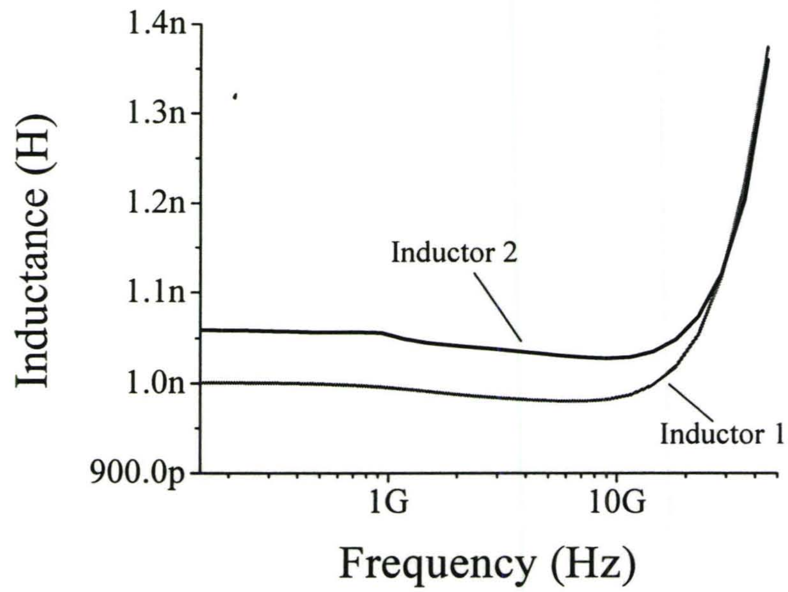


Figure 4.15 Equivalent inductance values of the two inductors.

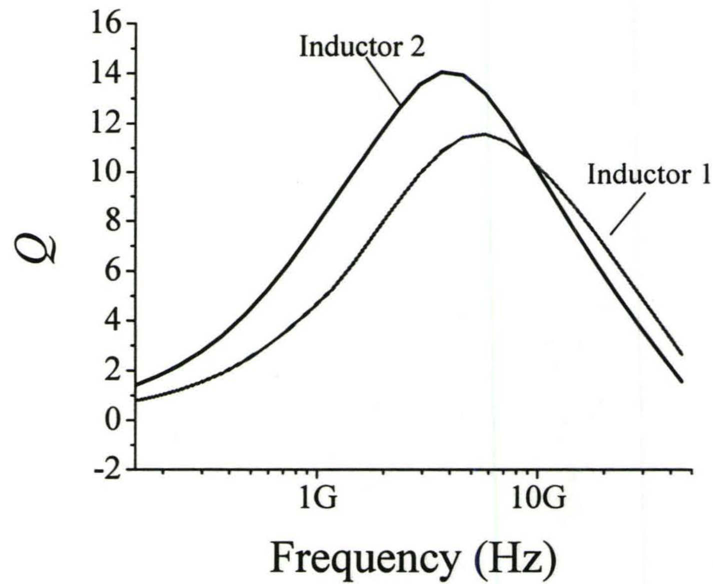


Figure 4.16 Q values for the two inductors.

4.7 Summary

In this chapter, various types of inductors used in the VCO design are presented. Main parameters that determine the performance of the inductor were also discussed. The chapter then focused on the study of the monolithic spiral inductor and its model. Means of increasing the quality factor of the spirals were discussed, and the way the spiral should be connected to a circuit in order to achieve high quality factor is illustrated.

Based on the discussion on the spiral inductor, a new technique for implementing spiral inductors was proposed in section 4.6. Simulations for this inductor were done with momentum. The simulation illustrated that with a combination of parallel strips, higher quality factor for the inductor can be reached. Simulations showed an increase of about 23% in the peak quality factor of the parallel strip when compared to an equivalent single strip. This design of the parallel strip inductor was not optimized for a specific application, however, if the combination for the length, thickness and spacing of the parallel strip were optimized, better performance can be achieved.

Chapter 5 *Low-Voltage, Low-Power VCO Design*

In this chapter, the VCO design will be discussed based on the VCO fundamentals and the basic passive components presented in the previous chapters. Although, low power consumption is the main criterion in this design, the topology will be based on its phase noise performance. Further discussion will be given afterwards on how to operate this circuit under irregular conditions, such as the ultra low-voltage supply and how to push its power consumption down as low as possible.

5.1 Noise Filtering

Recall from chapter two that the major sources of noise are the following:

- The current source transistor introduces flicker noise that is up-converted around the oscillating signal, as shown in Figure 5.1(a). The current source is also considered as the major contributor for the ($\Delta\omega_{1/f^3}$) region shown in Figure 2.9.
- The current source transistor introduces noise at the harmonics of the oscillating signalas shown in Figure 5.1(a), which is down-converted around the carrier, and thus, increasing phase noise.
- Noise at harmonics of the fundamental frequency are either produced due to the noise injection of the devices or due to harmonics produced from the nonlinearities of the VCO. The odd harmonics circulate in the differential path of the

VCO whereas the even harmonics take the common-mode path, as shown in Figure 5.1(b). Therefore, the VCO must acquire high common-mode rejection (CMR) for even harmonics [65].

- The noise produced at $2\omega_o$ (the second harmonic) from the current source affects the phase noise performance the most, because it has the highest down-conversion coefficient C_2 in eq.(2.32).

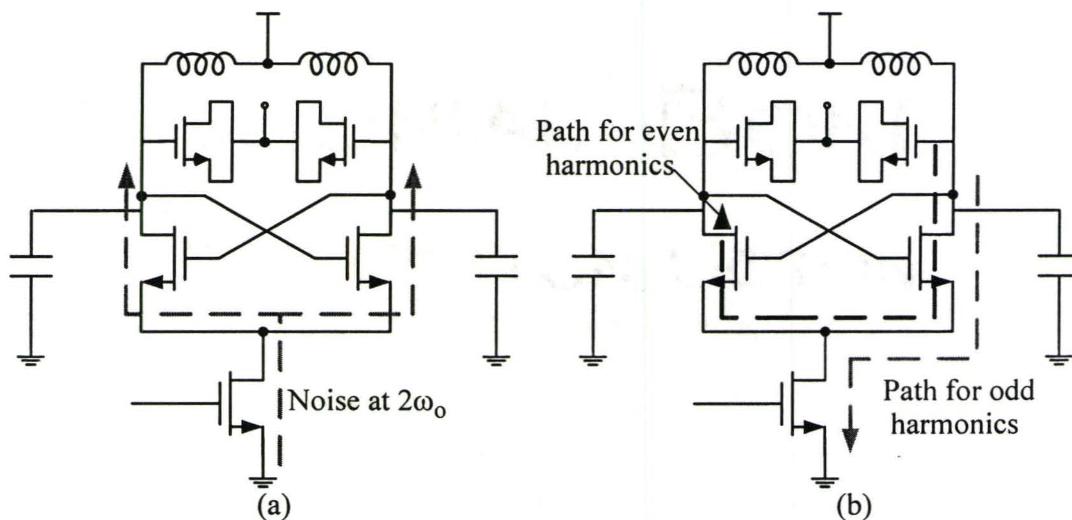


Figure 5.1 Schematic of a typical oscillator circuit showing the path of (a) noise at harmonics from the current-source, (b) odd and even harmonics.

In order to decrease the phase noise of the VCO, in [65], a filtering technique to limit the noise sources listed above from being injected into the VCO was proposed. A capacitor in parallel to the current source was introduced and its value was chosen high enough to act as a low impedance at $2\omega_o$. As a result, the $2\omega_o$ noise component injected by the current source would flow into the low impedance path to ground, and thus, it is prevented from contributing to the overall phase noise. However, this capacitor makes the common-mode node (CM node) in Figure 5.2(a) become low impedance at $2\omega_o$ instead of

being a high impedance node for the common-mode signal at $2\omega_0$. Thus, the CMR of the oscillator at high frequencies degrades, which makes the phase noise performance of the oscillator vulnerable to the common-mode signal at $2\omega_0$. Therefore, a high impedance should be introduced at the common node to increase the CMR at $2\omega_0$. This is achieved by introducing the LC tank circuit (L_sC_s) in Figure 5.2(b) which is tuned at $2\omega_0$ [65]. The measurements in [65] proved that the circuit with the noise filter has a better phase noise performance when compared to the regular circuit Figure 5.1.

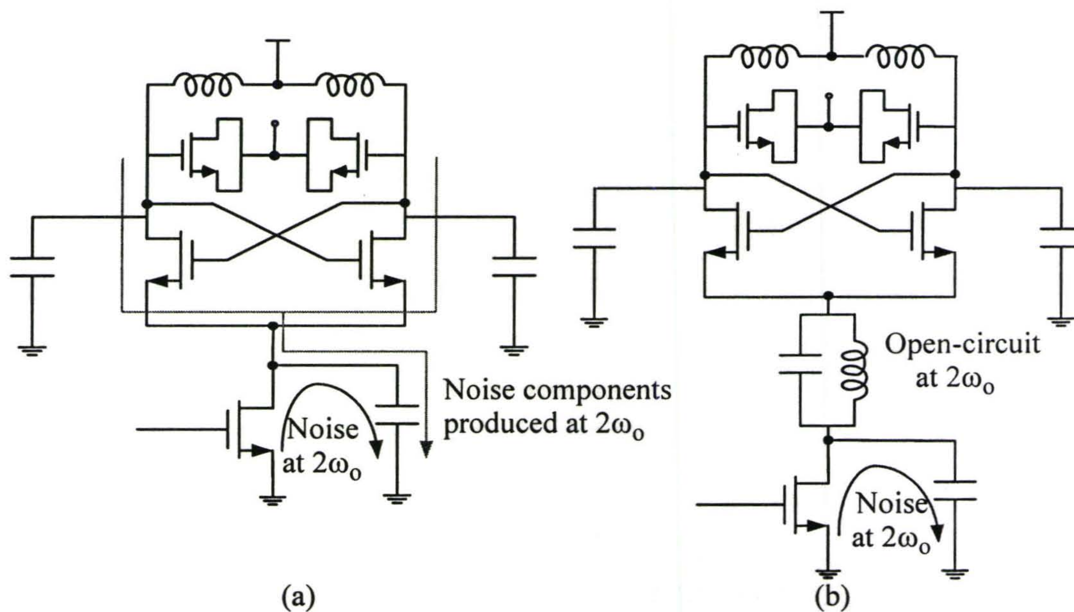


Figure 5.2 Filtering the noise (a) produced by the current-source at $2\omega_0$ and (b) introducing a tank circuit to increase the CM rejection.

However, the flicker noise induced by the current source transistor into the tank circuit remains a disturbing issue. Therefore, the current source transistor was removed and replaced by the tank circuit $L_{CS}C_{CS}$, as shown in Figure 5.3. This tank circuit is tuned at $2\omega_0$ to act as high impedance for the common-mode signal at that frequency.

The circuit in Figure 5.3 is classified as a "voltage-biased" circuit because a supply voltage used to control the biasing current of the circuit. This topology has the advantage

of achieving a high voltage swing that is as two times of V_{DD} for single-ended output. Also, due to the non-stacking nature of this circuit configuration, low voltage operation is possible. However, it suffers from large current consumption due to the absence of the current source transistor to regulate the current through the circuit. As a result, the power consumption of this topology is higher than the conventional implementations that used the current source for biasing.

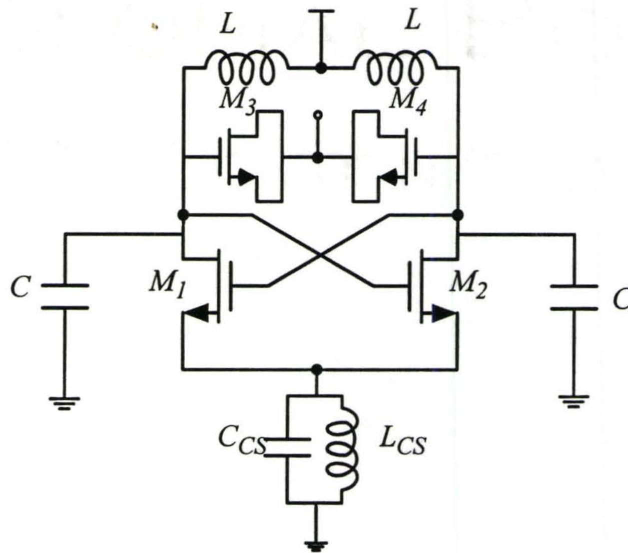


Figure 5.3 Negative g_m oscillator with a current-source tank circuit tuned at $2\omega_0$ which is used for low-voltage application.

Previous researchers [66], [67] have used this topology for low voltage applications. A supply as low as 0.7 V was used in [67] but the power consumption was 2mW, which is too high for low power applications.

5.2 Ultra Low-Voltage, Low-Power Operation

The circuit shown in Figure 5.3 has the disadvantage of having high current consumption. As a result, the power consumption

$$P = I_{DD} \cdot V_{DD} \tag{5.1}$$

becomes very high. Traditionally, in analog circuit design, to decrease the power consumption of the circuit, techniques are applied to decrease only I_{DD} in eq.(5.1). Usually, V_{DD} is preferred to be as high as possible in order to maintain high dynamic ranges. However, for the circuit shown in Figure 5.3, reducing the supply voltage is not a crucial issue because the single-ended peak-to-peak output swing can reach twice V_{DD}. In fact, decreasing the supply voltage plays a twofold role in decreasing the power consumption as it reduces both the V_{DD} and I_{DD} in eq.(5.1). However, while decreasing V_{DD}, the width of the cross-coupled transistor should be increased to achieve the condition of oscillation given by

$$g_m \cdot R_{tank} > 1 , \tag{5.2}$$

where R_{tank} is the equivalent parallel resistance of the LC tank circuit.

"Decreasing V_{DD} decreases also the current, while keeping the condition of oscillation" can sometime be a misleading statement. As it is sometime thought that the increase in the width that compensates for the decrease in V_{DD} would result in the same current value. However, this statement is not correct and the reason will be given below.

For lower power consumption, the condition of oscillation in eq.(5.2) can be achieved with lower values of g_m by using high R_{tank} values. These high values can be achieved by choosing a high Q tank circuit at the load. Choosing high Q tank circuit sets a higher value for R_{tank}, which consequently sets a lower value for g_m that ensures the condition of oscillation. However, another issue arises about whether lower currents can be achieved for the required value of g_m or not.

5.2.1 Sub-Threshold Operation of MOSFETs

Assume that we have two transistors with the same amount of current I_{DS} and that transistor M_2 operates in the sub-threshold region and transistor M_1 operates in strong inversion. In order for both transistors to operate with the same current, transistor M_2

should have a wider gate than transistor M_1 in order to compensate for the change in the bias gate voltage. The differences between the two transistors are shown in Table 5.1.

Table 5.1 Comparison between the sub-threshold and the strong inversion operation of MOS transistors.

	Transistor 1	Transistor 2
V_{GS}	$> V_{TH}$	$< V_{TH}$
Region	Strong Inversion	Sub-threshold
Gate Width	Narrow	Wide
g_m	$\sqrt{2\mu_n C_{ox}\frac{W}{L}I_{DS}}$	$\frac{I_{DS}}{n\phi_t}$

Figure 5.4 shows the difference between the DC drain current versus the DC gate-to-source voltage of the two transistors. An interesting point to be emphasized from this figure is that although the currents in both transistors are the same, the slope at point 2 on the graph is larger than the slope at point 1, which indicates that the value of g_{m2} is greater than the value of g_{m1}. Therefore, the required values of g_m that satisfy the condition of oscillation can be achieved at lower values of the drain current.

In previous analog circuit design research, circuits have been biased in sub-threshold region in order to achieve high values of g_m for low current operation [68]. However, this idea is not used in RF circuit design due to the non-linear I-V characteristics of the transistor in sub-threshold, which deteriorates the overall performance of the circuit. In addition, due to the fact that large gate widths are used when operating in sub-threshold, the overall capacitances are also large. Therefore, sub-threshold operation is not suitable for high frequency circuit design. However, in the case of the VCO design, since non-linearities are not a major issue in the design as the VCO is a non-linear circuit, then, the VCO designed in this chapter is biased in the sub-threshold.

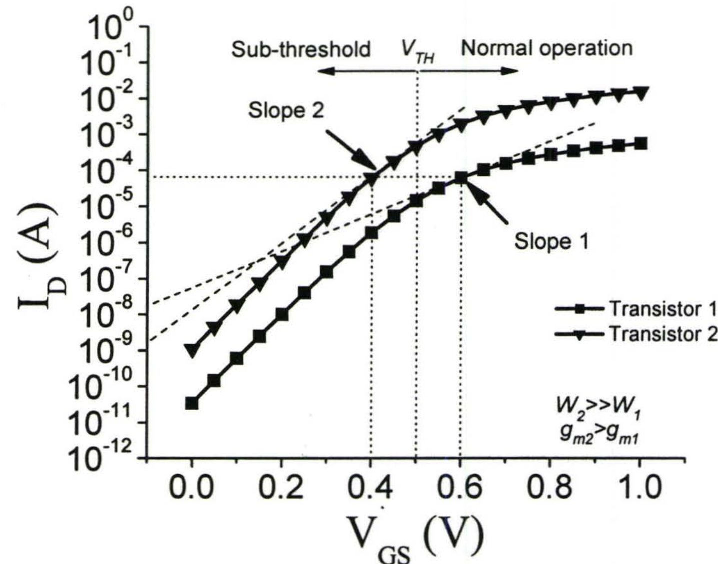


Figure 5.4 Comparison between the I-V characteristics of two transistors in different modes of operation, but at the same biasing current.

5.3 Design Procedures

The challenge in this design is to bias the transistor with a low supply voltage and to achieve the low power consumption criterion while keeping an acceptable phase noise performance. The first step to achieve this is to select the circuit configuration shown in Figure 5.3. The second step in the design is that the supply voltage is set at 0.4 V, which is about 100-150 mV below the threshold voltage of the transistor. The rest of the procedures of the design are explained in the following sub-sections.

5.3.1 Choice of the Tank circuit

The choice of the tank circuit in this design is dependent on the quality factor criterion. Based on the varactor discussion in chapter three, the varactor used in this design is a MOSFET with the bulk, drain and source connected together to form a B=D=S MOS var-

actor biased in accumulation. Although, the A-MOS varactor is preferable to the regular B=D=S MOS varactor biased in accumulation, it was not used in the design as the libraries available did not include the A-MOS type varactor. Some device simulations for the A-MOS varactor were done using the GENSIS device simulator provided by *ISE* (Integrated System Engineering), trying to predict the performance of the device. However, the simulation was not properly done due to the lack of some technology information from the manufacturer that is confidential.

Unfortunately, the model does not include the channel losses in depletion or accumulation. The current MOSFET model predicts the channel losses in inversion only. Therefore, in order to overcome that, the measurement data provided in [26] were used to estimate the channel losses of the MOSFET in accumulation and depletion.

As for the inductor part, high Q S.M. inductors that were discussed in section 4.2 were used. Although the equivalent parallel resistance R_L of a S.M. inductor is relatively high, it is still much smaller than the equivalent parallel resistance R_C of the varactors. Hence, the equivalent parallel resistance of the LC circuit will be taken to be equal to R_L only. However, at high frequency, R_L and R_C become close to each other and the total parallel equivalent resistance become equal to their parallel combination ($R_L||R_C$).

5.3.2 Transistors Size

The LC tank circuit produce an equivalent parallel impedance R_{tank}. This resistance R_{tank} resembles the losses of the resonator that should be compensated by the active circuit to achieve the condition of oscillation in eq.(5.2). Adjusting the value of g_m needed to achieve the condition of oscillation is achieved by adjusting the width W of the transistor. W is adjusted to give a value of the g_m that can achieve the condition of oscillation with a safety factor of 2. With such a small-signal gain, the circuit starts to oscillate till the amplitude saturates. Further details on the large-signal operation and amplitude saturation of this oscillator is discussed in section 5.4.2.

5.3.3 Current-Source Inductor

As stated in [65], the current-source inductor L_{CS} filters out the 2nd harmonic noise components and prevents them from circulating through the cross-coupled transistors in the signal path. An approximate value for L_{CS} is

$$L_{CS} = \frac{1}{(2\omega_o)^2(2C_{SB} + 2C_{SG} + C_{par} + C_{CS})} \tag{5.3}$$

where C_{SB} is the source-bulk junction capacitance, C_{par} is the parasitic capacitance of L_{tail}, C_{SG} is the source-gate capacitance of M_1 and M_2, and C_{CS} is current-source capacitance.

The value of the equivalent parallel resistance R_{CS} is very important. As the value of R_{CS} increases, the *CMR* for the 2nd harmonic becomes higher, and thus, it is attenuated at the output.

The value of R_{CS} can be set large by choosing an inductor of high inductance value, a high Q, or both. The problem of a low Q inductor is the finite impedance that the filter provides at ω_0, which affects the gain at that frequency.

The value of R_{CS} is also important from the power consumption point of view. Since R_{CS} rejects the 2nd harmonic, then it reduces the common mode current drawn from the supply voltage, and thus decreases the power consumption.

5.3.4 Buffer

The buffer for the oscillator is made of one source-follower transistor with a bias-Tee connected to its source. The buffer transistor and the equivalent circuit model of the bias-Tee is shown in the circuit diagram in Figure 5.5. The circuit model shows the bias-Tee to be composed of a capacitor and an inductor. The values of the capacitor and inductor of the bias-Tee are large in order for the inductor to act as an RF choke and the capacitor to act as an RF short circuit. With this configuration, the DC bias to the source of the

transistor can be connected through the RF choke while the RF output to the spectrum analyzer is taken from the capacitor terminal.

Figure 5.5 Complete circuit with the buffer.

The biased-Tee is used at the output of the buffer to avoid any non-linearities that can be introduced by the buffer. If a regular resistance at the output stage of the buffer is used, then the buffer would have needed a high V_{GS} to push the quiescent point (Q-point) away from the non-linear part of the I_{DS}-V_{GS} curve in Figure 5.6(a). Keeping the Q-point at low V_{GS} values produces a distorted and clipped signal at the output as shown in Figure 5.6(a). However, using the Bias-Tee increases the maximum swing limit that the signal can take. The bias-Tee also stabilizes the current and prevents it from taking high peak values. Therefore, the interconnections to the buffer would use metals with smaller width as there is no fear from melting the metals due to high current densities.

In order to guarantee enough power transfer to the 50Ω load of the spectrum analyzer; the width of the transistor should be set to give an equivalent impedance at the

source equal to 50Ω. The width of the transistor is set so that the real part of the output impedance is $1/g_m$, which is 50Ω. Also, the imaginary part of the output impedance is compensated by the bias-Tee.

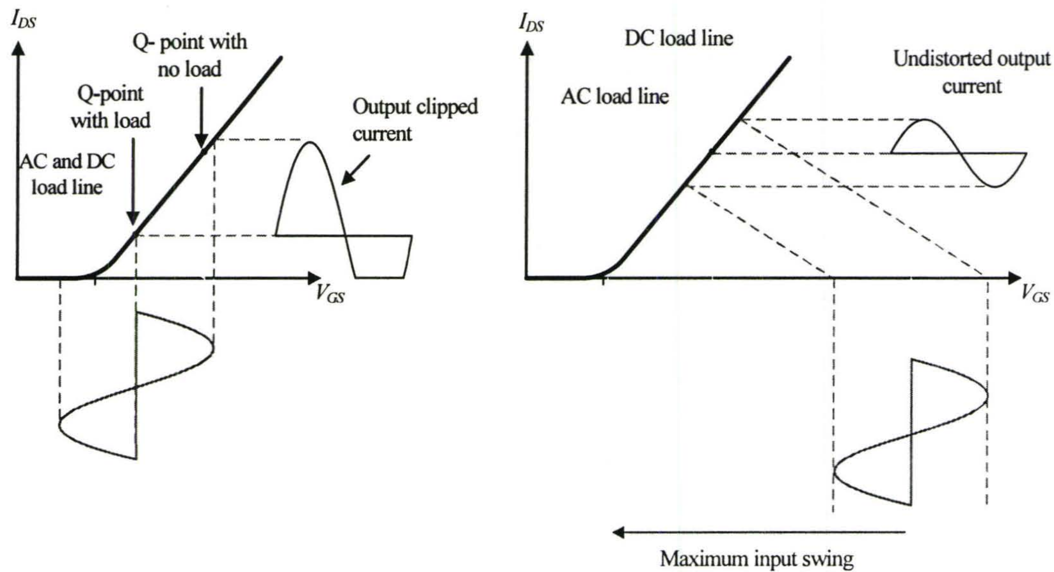


Figure 5.6 Large-signal I-V curve of the buffer transistor.

The buffer transistor is biased by a different supply voltage V_{DD_buff}, where it biases the gate through the high resistance R_{buff}. The bypass capacitor C_{bypass} isolates the basing circuit of the buffer from the VCO circuit and translates the RF signal to the gate of the buffer. In most cases, the value of C_{bypass} is set as large as possible to minimize any voltage drop across it. However, in this design the value of C_{bypass} is set small to have some voltage drop across it. C_{bypass} decreases the load capacitance due to the output stage and thus increases the Q of the capacitance of the output stage. As a result, the Q of the tank circuit will not be loaded by the buffer.

5.4 VCO Simulation

In this section, the VCO simulations and the circuit performance are discussed. Also, additional simulations are shown in order to confirm the theory of operation of the VCO.

5.4.1 Types of Simulations

There àre four main type of simulations that need to be performed for the VCO with SpectreRF. The first type is the DC simulation to determine the value of g_m that guarantees the condition of oscillation. Parametric analyses were done with the width of the transistor as the variable parameter. The biasing conditions while performing the parametric analysis were fixed. The width of the transistor was chosen from the output data of this simulation, where this chosen width is the one that gives the desired g_m value that satisfies the condition of oscillation. To guarantee the oscillation criterion, a safety factor of 2 was taken, therefore, the actual chosen g_m was the one that satisfies the condition of oscillation. Another way of doing this is to remove the feedback connection for one of the cross-coupled transistors and insert an AC source. AC analyses are then performed to check the gain of the common-source amplifier, while varying the width of the transistor by performing parametric sweeps for the AC simulation and plotting the resulting gain. The width of the transistor can be chosen from this type of analysis so that the output spectrum has the desired gain.

The second type is the transient analysis. The importance of this type of simulation is that it shows the start-up and stabilization of the amplitude of oscillation and it determines the power consumption. In order for the oscillator to start oscillating from its DC biasing, some sort of disturbance must be applied to the circuit in the simulator. The way this is done in transient simulation is to set initial current condition in the inductor model. This initial current produces the necessary perturbation to the system to start up the oscillation. One important note is not to set the value of the initial condition very high with a

low transient time analysis because the oscillation might be decaying in a long period of time.

The third type is the periodic steady-state (PSS) simulation. This type of simulation computes the steady-state response of the circuit and calculates the frequency and amplitude of the fundamental frequency component of the steady-state output and its harmonics. The resultant information leads to the fourth type of simulations, which is the Periodic noise (Pnoise) analysis. The Pnoise analysis computes the noise at the output of the oscillator due to the different noise sources in the circuits and then, utilizes the output information about the harmonic components provided by the PSS simulation, to compute the phase noise of the oscillator by applying this data to the time-varying phase noise model.

5.4.2 Simulation Results

The initial condition of the current in the inductor starts-up the oscillation of the VCO. A few periods after the oscillation starts, the amplitude starts to saturate. Usually, the value at which the amplitude saturates in VCOs is determined by the value of the current produced by the tail current source, multiplied by R_{tank}. However, in this case there is no current source to stabilize the current and the transistor's gate width are set large to achieve a high g_m at a low V_{GS}. As a result, high current pulses are produced at the drain of the transistor, as shown in Figure 5.7, which produces a fundamental component of the current that can set the amplitude of oscillation to values that can exceed $2V_{DD}$. Hence, the amplitude of oscillation produced by this circuit is not considered as current-limited but rather voltage limited by the supply, as will be discussed shortly.

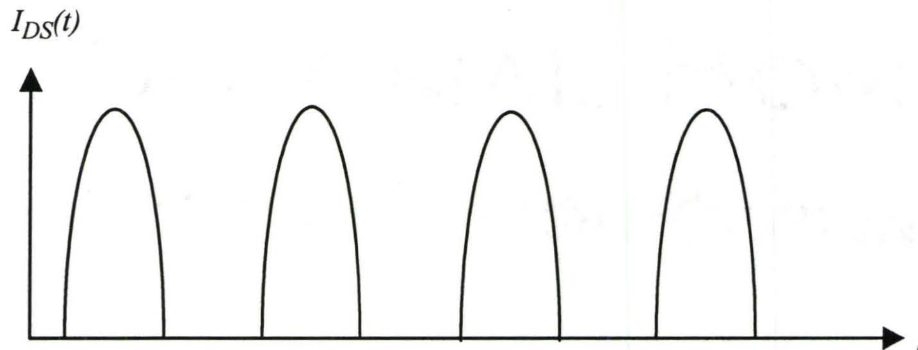


Figure 5.7 Current pulses produced by a large-signal input.

Practically, the current waveform shown in Figure 5.7 cannot be produced except by an amplifier that has a short circuit load or a tuned circuit that produces a small amplitude that keeps the transistor in saturation. However, in this circuit, the amplitude of fundamental component produced at the output is very large and the minimum output voltage can reach zero. When the output voltage reaches such low values it drives the transistor into the linear region. Hence, the current produced by the transistor becomes dependent on the output amplitude as well as the input amplitude and the resultant current waveform produced at the drain takes the form shown at the bottom graph of Figure 5.9. To further understand how this waveform is produced and how the amplitude saturation occurs, consider the transistor shown in Figure 5.8, with a large-signal input voltage at the gate and the out-of-phase large-signal output voltage produced at the drain.

At the start of each period, the gate of the transistor and the drain have the same biasing voltage, which is the DC biasing point and it is equal to V_{DD}. This condition is presented by point "a" in Figure 5.8 and Figure 5.9 which shows the equivalent output current. The current produced at this point is DC, which only flows through the inductor and does not produce any output voltage drop. When the amplitude of the input waveform at the gate starts to increase, then the amplitude at the output starts to decrease, producing a current waveform which is similar to the current pulse shown in Figure 5.7. This part of the pulse is shown in Figure 5.9 from points "a" to "b". Beyond point "b", the current

waveform starts to become different than that of Figure 5.7. At point "b", the value of V_{DS} becomes small and drives the transistor into the linear region from saturation. And as the transistor becomes biased in the linear region, the drain current becomes strongly dependent on V_{DS}, hence, I_{DS} starts to decrease, as shown in the part between point "b" and "d" in Figure 5.9.

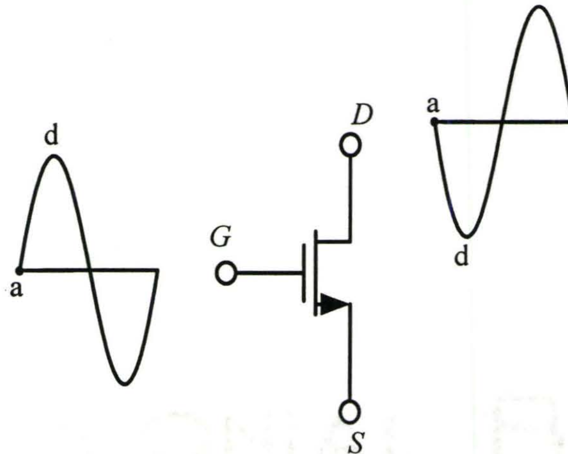


Figure 5.8 The voltage waveforms applied to a cross-coupled transistor.

During the transition from point "b" to "d", the current changes its direction and becomes negative at point "c". As the current changes its direction, the drain and source terminals of the transistors are switched, which means that V_{GS} is now the gate-to-output node voltage and V_{DS} is the ground-to-output voltage. Therefore, the amplifier transistor of the VCO becomes a source-follower with the output of the VCO as the follower node rather than a common-source amplifier. This causes the follower output of the amplifier increase to follow the input waveform at this point amplifier. Forcing the output to increase just after it reaches zero, and thus, limits the output amplitude and prevents it from having more negative values. So, if symmetric resultant fundamental components are assumed at the input and the output of the transistor, then the output amplitude will have a voltage swing that is approximately equal to twice V_{DD}. Therefore, the VCO in this

case is said to be voltage-limited rather than current-limited, because the output amplitude is always limited by V_{DD}.

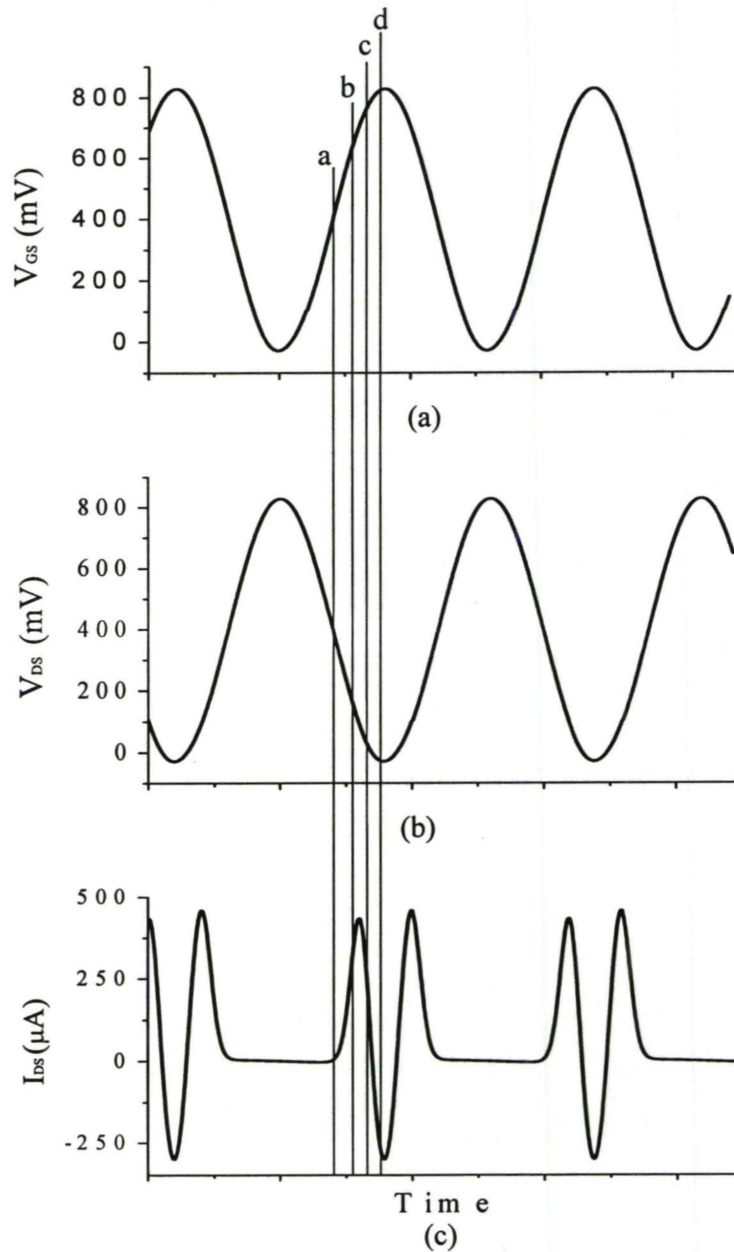


Figure 5.9 Waveforms for the core transistor, (a) V_{GS}, (b) V_{DS} and (c) I_{DS}

The designed 2.4GHz VCO at 0.4 V supply has a simulated phase noise of -123 dBc/Hz at 1MHz offset. This simulation performed assumes a perfect matching between the two tank circuits of the oscillator. This matching between the two tank circuits results in an overall transfer function that has a peak equal to the product of the peaks of the two transfer functions and is also at their center frequency, as shown in Figure 5.10(a). However, due to the tolerance of the off-chip inductors used, the two tank circuit starts to have different component values and their transfer function becomes shifted from each other instead of being at the same center frequency. This is similar to the case of stagger tuning in filters, where two transfer functions with shifted center frequencies are used to produce an overall transfer function, as shown in Figure 5.10(b), which has lower peak gain and wider bandwidth, in other words, it has less Q.

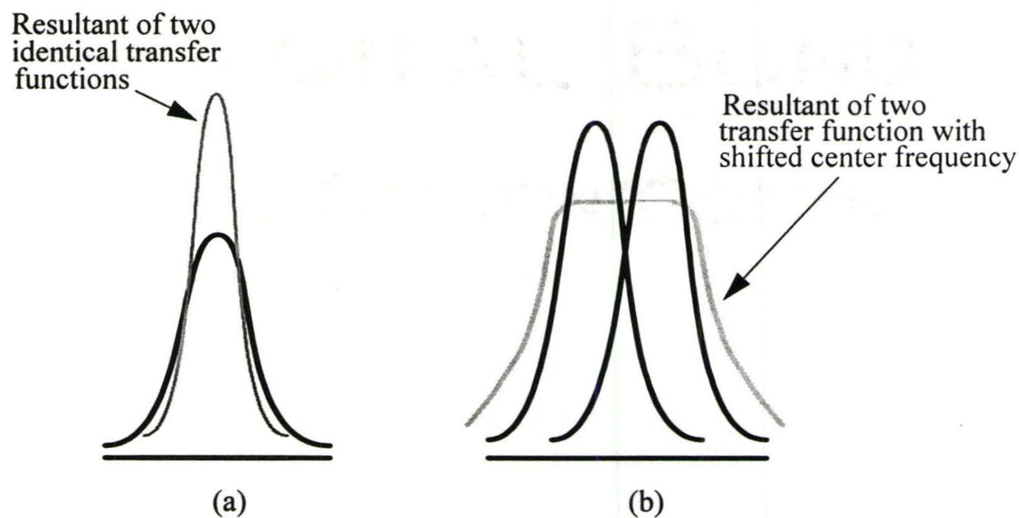


Figure 5.10 Overall transfer function of two tuned amplifiers with equal transfer functions (a) at same center frequency and (b) with shifted center frequency [22].

To study the effect of the stagger tuning due to the inductor mismatch, the value of one inductor is varied over a range of $\pm 5\%$, while the second inductor remains constant. The phase noise and the power consumption of the oscillator is then simulated as shown in Figure 5.11 and Figure 5.12, respectively. The phase noise and the power consumption

shows a minimum value (best performance) at the 0% tolerance and they increase as the degree of mismatch increases. For the phase noise curve, the minimum is at 0% tolerance because this is the point with highest Q, which when substituted in the phase noise relation in eq.(2.25), results in the best phase noise performance. As for the power consumption, the Q values becomes smaller due to the mismatch, so more power is then transferred to the harmonics. The increase in the power consumption in this case is due to the power produced at the even harmonics, which introduces a common-mode current that increases the average DC current drawn from the supply. If the tolerance of the inductor is increased more than the values shown in figures, the oscillator will not oscillate any more as the overall gain will then drop below unity.

To be able to determine the mismatch by measurements, the two varactors of the two tank circuits were isolated, where each one had its own V_{cont}. If the values of the inductors were not matched, a sweep can be done on one of the control voltages of the varactors while the other is fixed, and then monitor the power consumption. The point at which the power consumption is minimum means that the tank circuits are at their best match. Taking the value of the variable control voltage at which the power consumption is minimum, the corresponding capacitance can be calculated, and the inductance is then calculated.

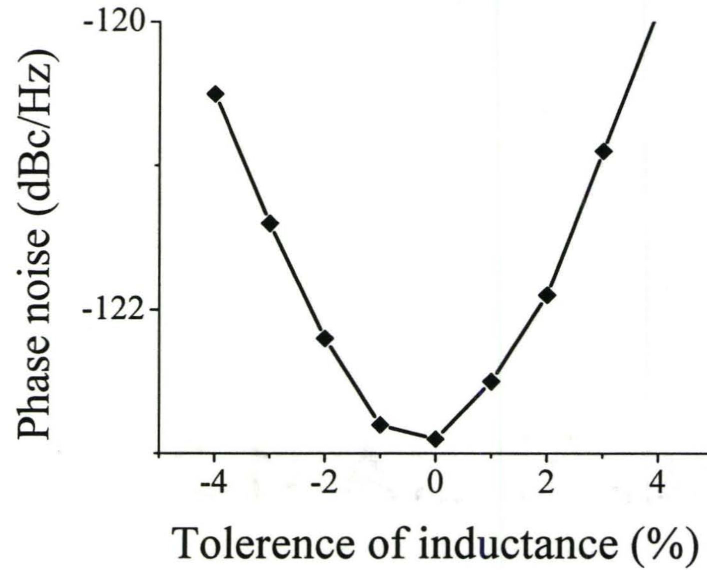


Figure 5.11 Effect of inductor mismatch on the phase noise performance of the VCO.

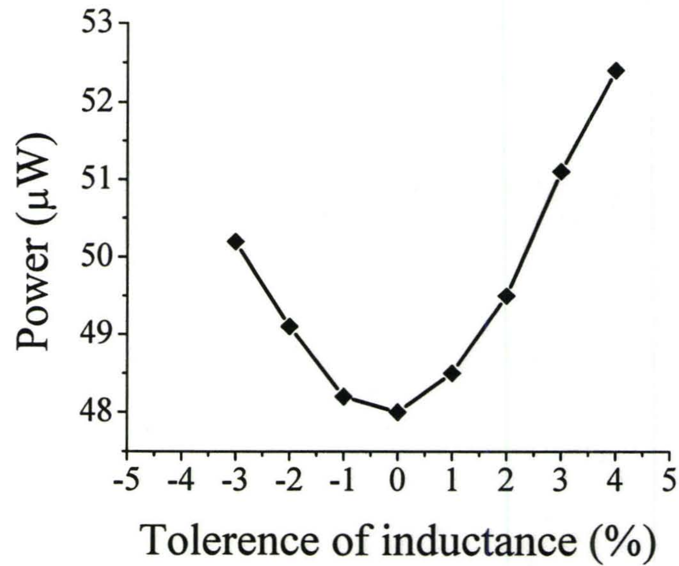


Figure 5.12 Effect of inductor mismatch on the power consumption of the VCO.

A drawback of this method is that the characteristics of the varactor are now different. The Q value of the varactors deceases significantly due to the finite impedance of the DC source V_{cont}, as discussed in chapter three. A solution was given for this problem in chapter three, where a large value capacitor can be connected to the control node. This capacitor has low impedance at the frequency of operation and this eliminates the losses due to the substrate and the DC source. However, in the case of differential circuits, it is always preferred to implement the varactors differentially, as discussed earlier in section 3.5, in order to have an AC ground between the two varactors, as shown in Figure 5.13(a), to minimize all losses and thus, maximize Q. Therefore, a capacitor was connected between the two varactors as shown in Figure 5.13(b). The advantage of this capacitor is that it isolates the biasing of the two varactors from each other, while having an AC ground between them. Also, the restrictions on the value of this capacitor are much looser than when two capacitors are used.

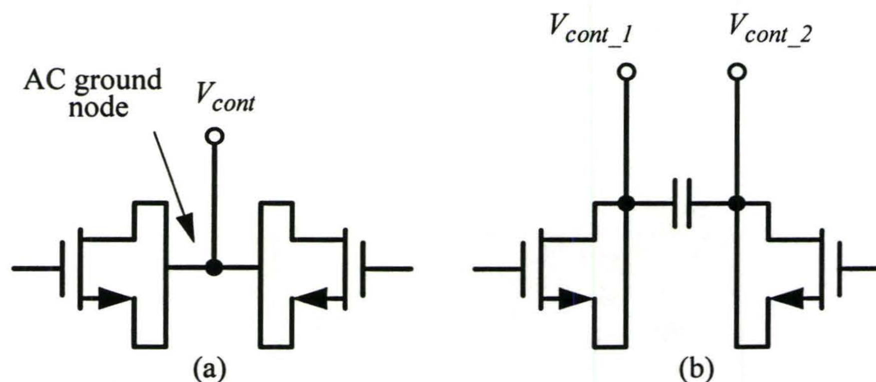


Figure 5.13 (a) Regular connection of the varactor to the control voltage. (b) Connecting the varactors to different control voltages.

It is also important to see the effect of the current-source tank circuit $L_{CS}C_{CS}$ on the performance of the oscillator. Figure 5.14 shows the effect of the Q value of the current-source inductor on the power consumption and phase noise of the oscillator. This simulation was done by varying the equivalent parallel resistance of the oscillator to achieve

the desired Q_{CS} values. Figure 5.14 shows that the phase noise is enhanced by more than 6dB if an inductor of Q_{CS} equal to 8.5 is used, which is the on-chip inductor that was really used. The decrease in the phase noise totally agrees with the theory of this circuit configuration, where the higher the Q value for the current-source inductor, the more attenuated is the second harmonic, as shown in Figure 5.15. Hence, less power is down-converted from the second harmonic around the carrier. The decrease in the second harmonic also explains why the power consumption is decreased with higher values of Q for L_{CS}, however, the decrease is only 6%.

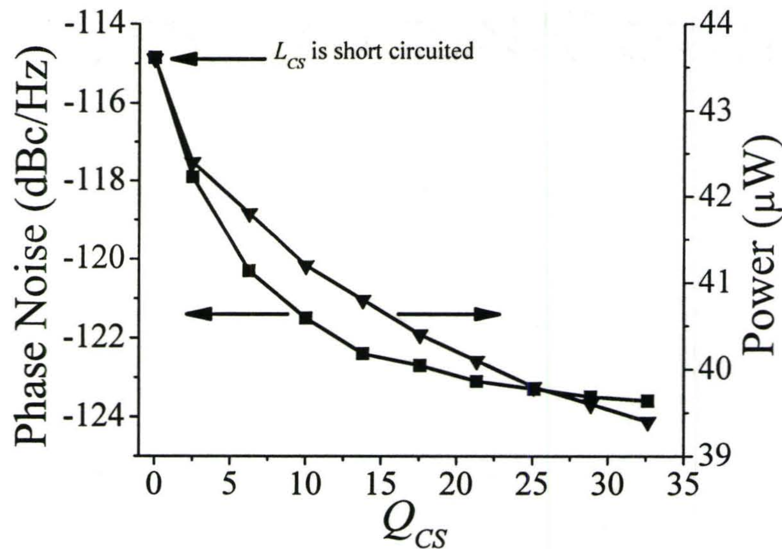


Figure 5.14 The effect of Q_{CS} on phase noise and the power consumption.

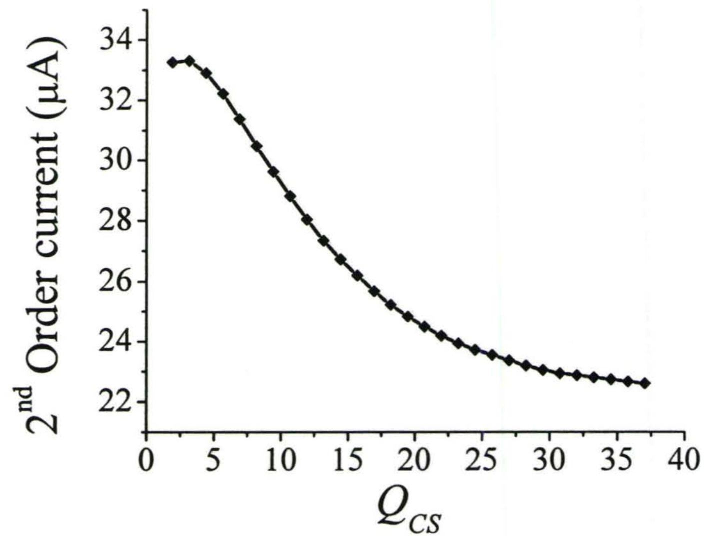


Figure 5.15 The effect of Q_{CS} on the values of the current at the 2nd harmonic.

The last simulation that was done for this circuit was to examine the effect of tuning. Figure 5.16 shows the effect of changing the control voltage on the frequency of oscillation and the corresponding phase noise at this frequency of oscillation. The frequency of oscillation decreases with increasing V_{cont}, as increasing V_{cont} drives the varactors more into accumulation where the capacitance reaches its maximum at C_{ox}. The phase noise simulation in the same figure shows a minimum at 1.3V, the value of V_{cont} where the oscillator is optimized. Any shift below or above this frequency makes the current-source tank circuit tuned at a value above or below $2\omega_0$, respectively. Therefore, the second harmonic components are less attenuated, which results in a higher 2nd harmonic power down-converted around the carrier and thus, higher phase noise.

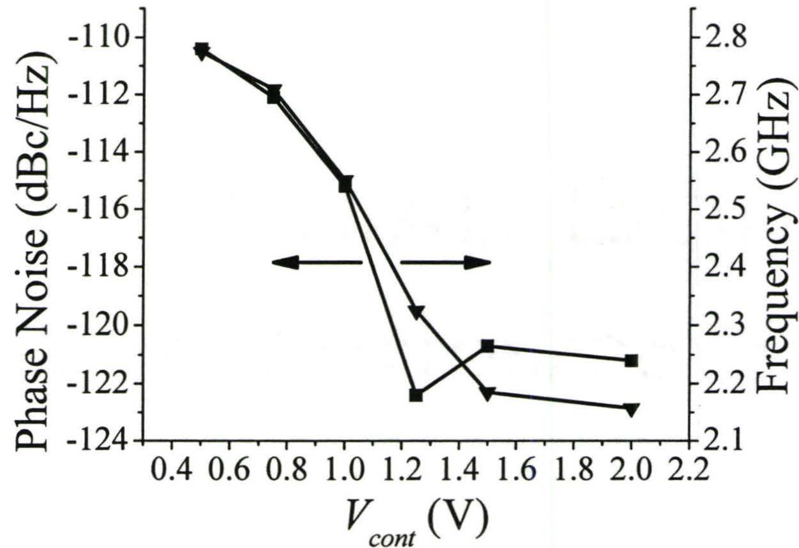


Figure 5.16 Frequency of oscillation and phase noise vs. the control voltage.

5.5 High Frequency Effects

Two circuits have been designed with a low supply voltage that reached 0.4V. These circuits operate at frequencies of 600 MHz and 2.4 GHz. However, as the frequency of oscillation is pushed to higher frequency bands, the design of the oscillator becomes more difficult. Changes in the transfer function of the oscillator are noticed when the oscillator is pushed to operate in the 5.8 GHz ISM band. When preforming an AC simulation of the oscillator to check its gain, the narrow band-pass frequency response of the amplifier of the VCO starts to have two peaks instead of one peak. Also, there are noticeable changes in the phase plot of the gain of the amplifier. To understand the cause of these effects, consider the simple small-circuit model for the amplifier that is shown in Figure 5.17.

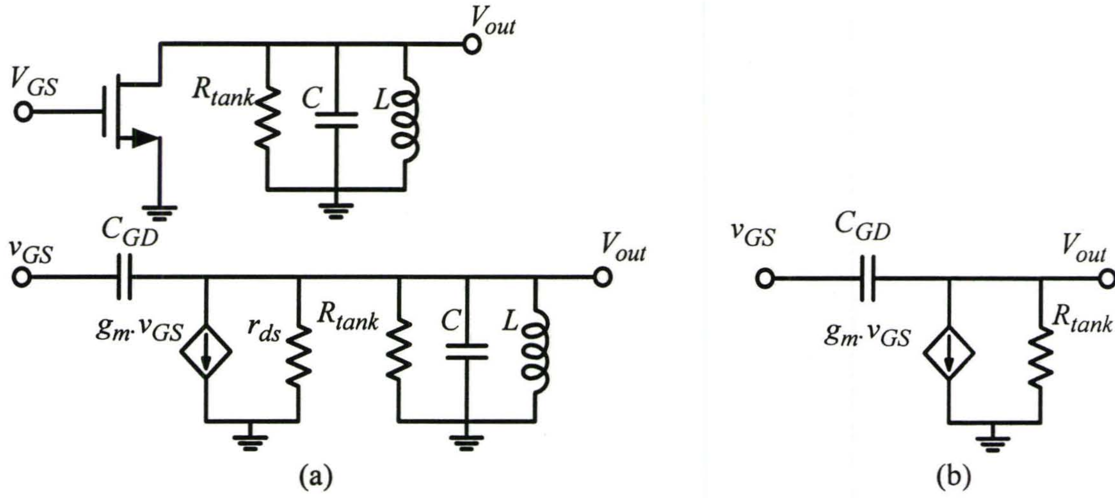


Figure 5.17 (a) The amplifier of the VCO and its equivalent small-signal model. (b) The small-signal model at resonance.

For the small-signal model of the amplifier shown in Figure 5.17(a), the voltage gain A_v is given by

$$A_v = \frac{V_{out}}{v_{GS}} = \frac{-(g_m - j\omega C_{GD})}{j\omega C_{GD} + \left(\frac{1 + j\omega L/R_{tank} - \omega^2 LC}{j\omega L}\right)}. \quad (5.4)$$

If the tank circuit is tuned to oscillate at a relatively low frequency, then the equivalent of circuit (a) at resonance will be as in (b) and the gate-to-drain capacitance (C_{GD}) can be ignored. The capacitance C_{GD} is ignored because its equivalent impedance ($1/\omega C_{GD}$) is very high compared to R_{tank}, which makes the output isolated from the input. The gain is given by

$$A_v = \frac{V_{out}}{v_{GS}} = \frac{-g_m \cdot j\omega L}{1 + j\omega L/R_{tank} - \omega^2 LC}, \quad (5.5)$$

which is the normal equation for the gain that yields to $-g_m.R_{tank}$ at resonance.

When the frequency of oscillation is increased, the equivalent impedance of the capacitance C_{GD} becomes smaller and its value is comparable to the value of R_{tank}. In the case of the sub-threshold operation of the MOSFET, the effect of the Miller capacitance C_{GD} is noticed at lower frequencies when compared to the MOSFETs that operate in strong inversion. The reason is due to the large gate widths that are used in sub-threshold that increase the overlap and the fringing capacitance between the gate and the drain. This high frequency effect is considered one of the major drawbacks of the operating in sub-threshold. In order to overcome this drawback, the capacitance C_{GD} should be decreased to avoid this effect. Hence, the gate width was decreased until the high frequency effect became negligible, however, the gain then dropped much below unity.

To increase the gain of the amplifier, the MOSFET is utilized as a four terminal device, where the body contact was is connected to the source. The body contact of each of the cross-coupled transistors are all connected together to a DC bias, as shown in Figure 5.18. By forward biasing the transistors, the threshold voltage decreases, thus, the degree of inversion increases for the fixed V_{GS} and g_m increases, as shown in Figure 5.19.

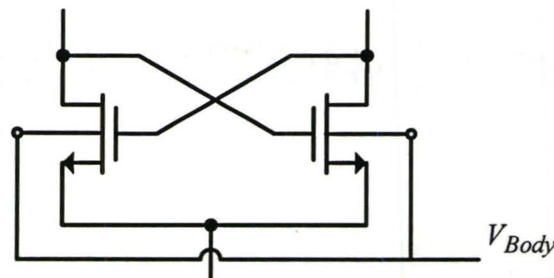


Figure 5.18 Body-biasing of the cross-coupled transistors.

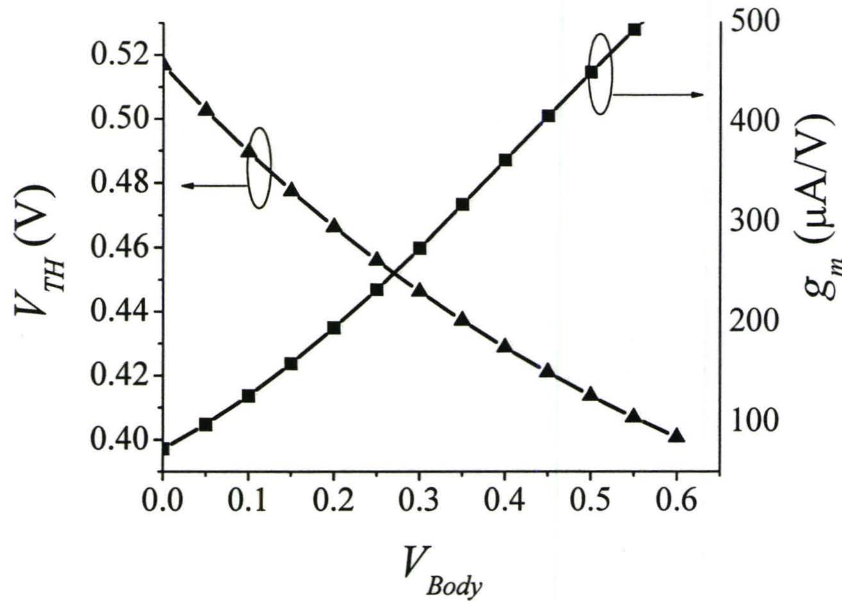


Figure 5.19 Effect of body-biasing on the threshold voltage and the transconductance.

As a result of the above discussion, a VCO at 6 GHz was designed with forward body-biasing. The simulated phase noise of the oscillator is -113 dBc/Hz at 1 MHz offset. Further details on the experimental results will be presented in the next chapter.

5.6 Experimental Results

For the VCOs discussed in this chapter, the 600 MHz VCO was tested experimentally. Figure 5.20 shows the layout of this VCO. The chip was packaged into a 80-pin CFP package and was soldered to a printed circuit board (PCB), as shown in Figure 5.21(a). The off-chip inductors were soldered on the other side of the PCB as shown in Figure 5.21(b). The equipment used to test the VCO were the Agilent E4440 26.5 GHz spectrum analyzer and the Agilent 4156C semiconductor parameter analyzer.

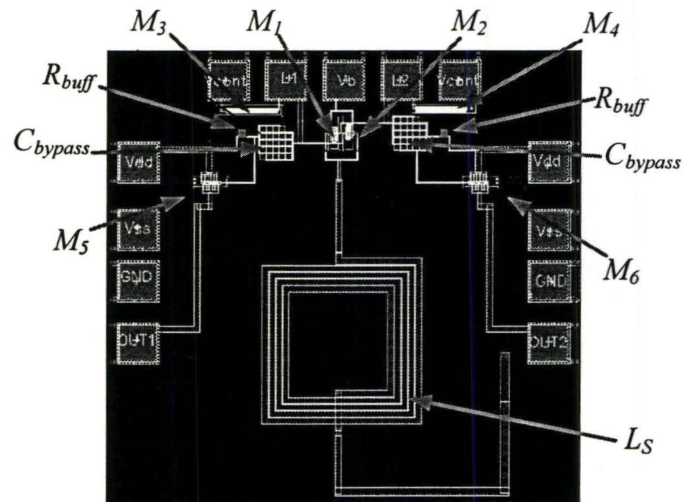


Figure 5.20 Layout of the 600 MHz VCO.

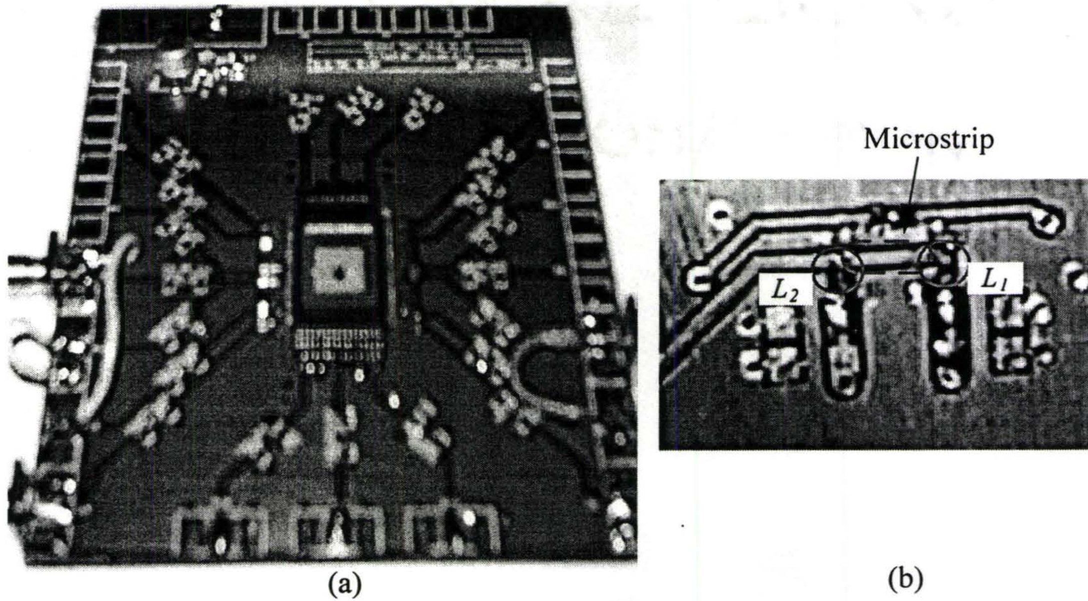


Figure 5.21 (a) Packaged chip and the PCB used for measurements with (b) the off-chip inductors soldered on the other side of the PCB.

The VCO did not oscillate at the biasing conditions that it was designed for at V_{DD} of 350 mV. Therefore, the supply voltage V_{DD} was increased in small steps to determine the voltage at which the VCO starts to oscillate. Oscillation was established at a V_{DD} of 430 mV, corresponding to a frequency of oscillation of 390 MHz, as shown in Figure 5.22, and a power consumption of 257 μW. The main reason for deviation of these results from the simulation is the parasitics of the package, which were not taken into account during the simulations because there were no circuit models available to model the parasitics of the package. In fact, no proper model for the 80-pin CFP was present in literature, Therefore, a simple model for the package was estimated, as shown in Figure 5.23, and used in to re-simulate the VCO to obtain more accurate results.

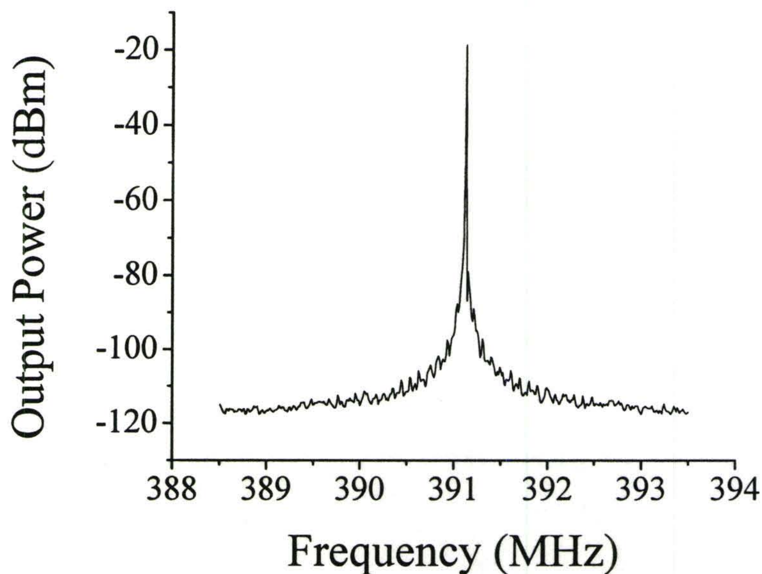


Figure 5.22 Measured output spectrum of the VCO.

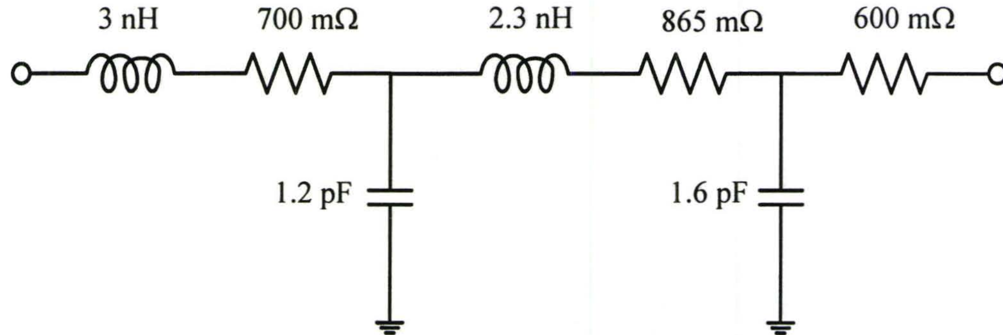


Figure 5.23 Estimated circuit model of the package parasitics.

As the frequency of oscillation is decreased, the Q_L of the inductor decreases, which decreases the equivalent resistance of the tank circuit R_{Tank}. This directly affects the condition of oscillation of the VCO, and thus, the cross-coupled transistors of the VCO are required to provide a higher gain. This effect is, actually, one of the contributors to the increased V_{DD}.

The PCB has also contributed to the increase in the V_{DD}, where the symmetry in the layout of the differential VCO was maintained only on-chip and not at the PCB level. Figure 5.21(b) shows an extra microstrip on the PCB in series with the inductor L_1, which increases the inductance of only one of the differential branches of the VCO. This microstrip was simulated using ADS-Momentum and its equivalent circuit model is shown in Figure 5.24. When the microstrip model was introduced into the circuit and then simulated, as shown in Figure 5.25, the value of V_{DD} needed to achieve oscillation was very close to measurements. Another contributor to the increase in the V_{DD} is the mismatch between the off-chip inductors used, as previously discussed in section 5.4.2. Finally, the losses in the cables that are used to connect the measurement instruments and the PCB also contributed to increasing V_{DD}.

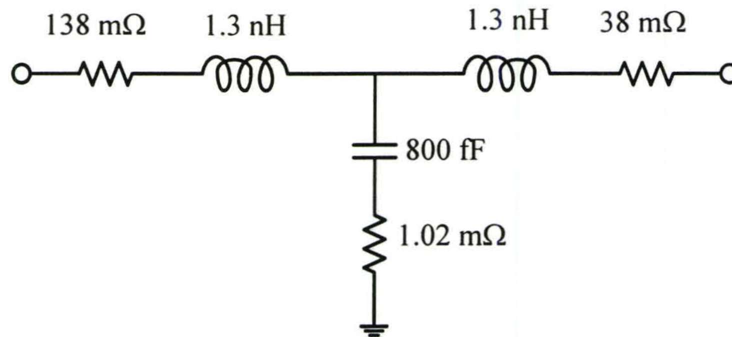


Figure 5.24 Circuit model of the microstrip.

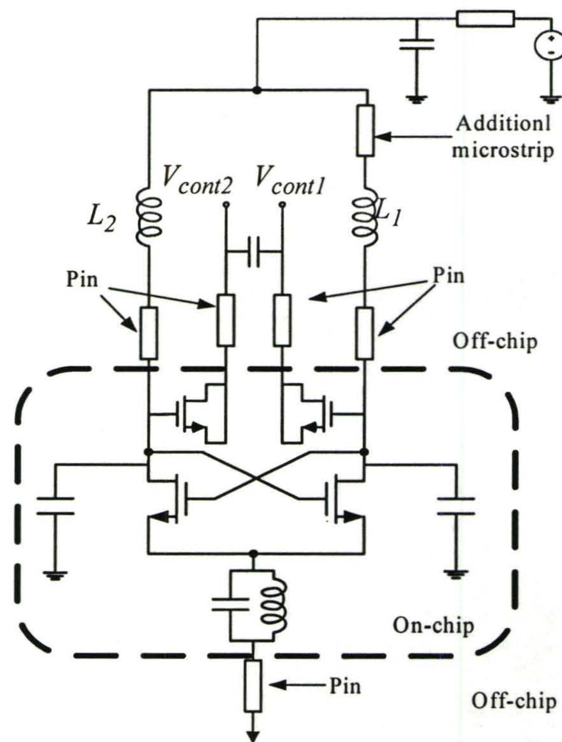


Figure 5.25 VCO circuit including all parasitics. Each pin is represented by the euivilent circuit model in Figure 5.23. The microstrip was mdelled using circuit in Figure 5.24.

The change in the frequency of oscillation with the control voltage is shown in Figure 5.26, indicating a tuning range of 7 MHz. Unfortunately, data points for V_{cont} less than 1 V were not recorded as most of the bonded chips available were burnt while performing the experiments because the simple Electro-Static Discharge (ESD) protection used was inadequet to protect the circuit. The phase noise performance of the VCO at a control voltage of 1.3 V is shown in Figure 5.27. The simulated phase noise versus the control voltage is shown in Figure 5.28, while the measured and the re-simulated results are shown in Figure 5.29. The measured phase noise curve is approximately flat within this range at a value of -132.5 dBc/Hz. This difference between the simulations in Figure 5.28 and the measurement results is due to neglecting the effect of the package at the load inductors and the common-source inductor which made the common-source tank circuit tuned at a frequency different than the 2nd harmonic. Also, any change in phase noise with the control voltage would be much smaller than expected because the implemented inductor does not attenuate the 2nd harmonic component as expected by the model from the manufacturer. In fact, the implemented inductor has losses that are about two times higher than the model because it was implemented using the regular metal 6 while the model is for inductors implemented using special metal 6 that is about two times thicker than the regular metal 6. Finally, the phase noise performance versus the control voltage can be considered constant which agrees with the simulated data shown on the same figure. However, there is about 11 dB difference between the measured data and the simulation results. This could be due to the inaccurate noise model of the MOSFETs in sub-threshold, where the channel noise is overestimated and is modeled as if the MOSFET is operating in strong-inversion. The differences between the simulated and the measured results are shown in Table 5.2.

Table 5.2 Comparison between measured data and simulation.

	Q	f_o (MHz)	PN at 0.6 MHz (dBc/Hz)	P (mW)	FoM
Measured	40	392	-132.5	0.257	162.66
Simulated	40	385	-121.5	0.21	152.8

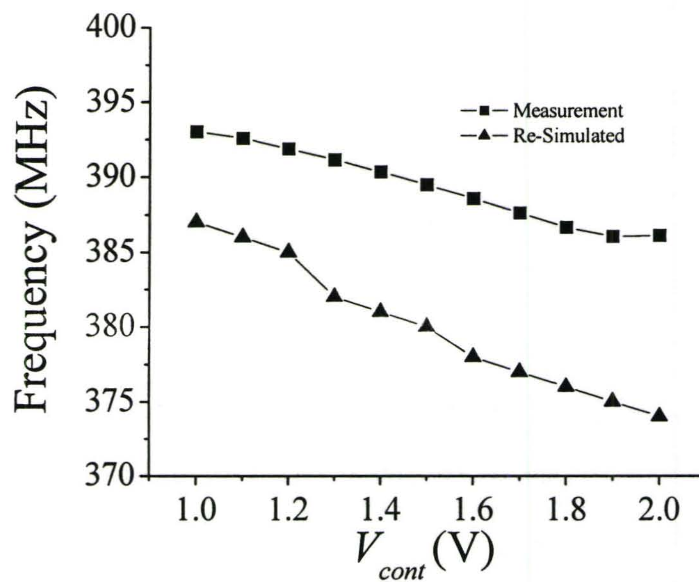


Figure 5.26 Frequency of oscillation versus the control voltage.

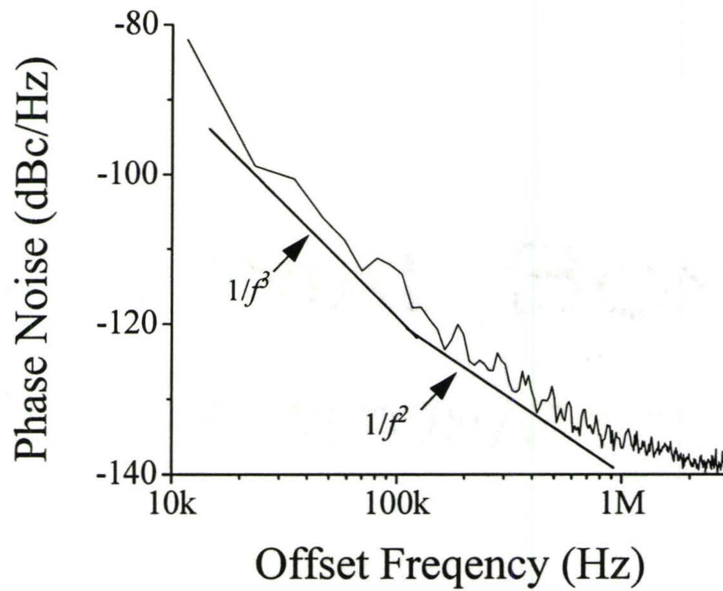


Figure 5.27 Measured phase noise of VCO.

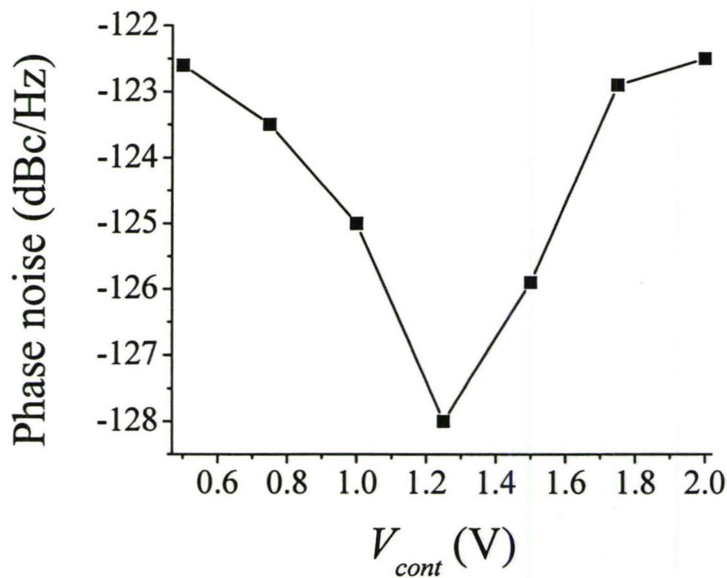


Figure 5.28 Simulated phase noise at 600 MHz versus the control voltage. Here the effect of the parasitics of the package is not included.

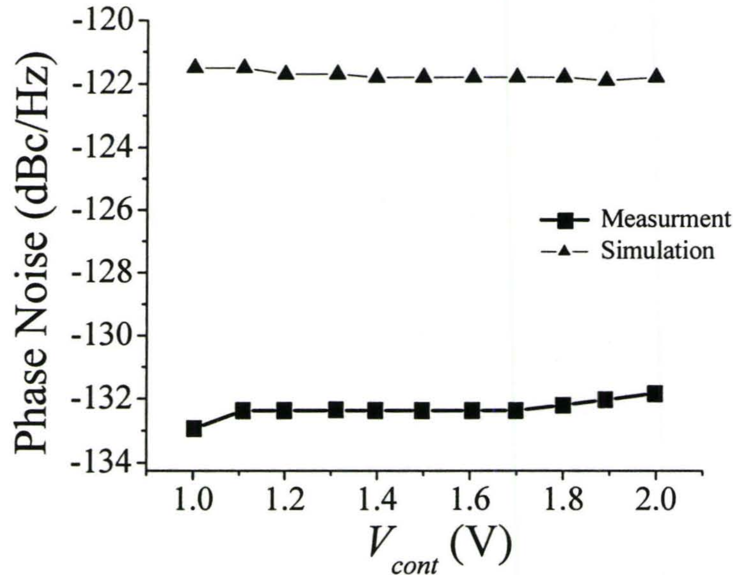


Figure 5.29 Measured phase noise versus the control voltage.

5.7 Summary

In this chapter, ultra-low voltage micro-power oscillators were discussed. In the first section, the basic theory for the oscillator topology was discussed. This was followed by a discussion of the means to minimize the power consumption and to operate this VCO under low bias. Section 5.3 was dedicated to the explanation of the design procedures. The theory was then justified with some basic simulations. Emphasis was given on the large-signal analysis and explanations were given for the current and voltage waveforms of the VCO. In the last section, the high frequency effects that occur in sub-threshold were discussed and forward body-biasing of the cross-coupled pair was given as a solution to overcome these effects.

In this Chapter, the main features of the VCOs designed is that they can operate at very low-voltage supplies. However, biasing at low-voltage does not imply low power consumption. The first step for achieving the low-power consumption was to use high quality tank circuit, which is a very intuitive approach. The second approach was biasing the transistor in sub-threshold. In section 5.2.1, a comparison between two transistors was

shown, where the first transistor was biased at regular biasing condition above threshold while the second transistor was biased in sub-threshold. Figure 5.4 shows that if the two transistors have the same current passing through them, then the transistor biased in sub-threshold will have the higher transconductance. Therefore, by biasing the transistor in sub-threshold, the drain-to-source current needed to generate the value of the transconductance that fulfills the condition of oscillation in eq. (5.2) would be less. In fact, for the two transistors shown in Figure 5.4, the first transistor that is biased at 0.7 V would have five times the drain-to-source current passing through it, when compared to the transistor that is biased with 0.4 V and have the same value of the transconductance. This approach can be used in the design of any VCO, not necessarily a VCO that already has a low-voltage supply.

Finally, The VCOs designed are at frequencies of 600 MHz, 2.4 GHz and 6 GHz. Their supply voltages were 350 mV, 400 mV and 450 mV, respectively. The power consumption of these oscillators is 36 μW, 41 μW and 90 μW, respectively. The above values for the supply voltage and the power consumption are considered the lowest recorded in literature.

The measurement results for the 600 MHz VCO were discussed in section 5.6. The measurement results show that the frequency of oscillation of the VCO is 392 MHz at a supply voltage of 430 mV. The VCO has a measured phase noise of -132.5 dBc/Hz at 0.6 MHz offset and power consumption of 257 μW. The main reason for the deviation of the measurement data from the simulation results is the package parasitics that were not taken into account during the simulations. A simple circuit model was estimated for the package. Thus, by taking into account the estimated package model in simulations, the measurement results and the simulations were close.

The control of the gain needed to provide oscillation can be done by adjusting the body-bias of the transistors, as changing V_{DD} is not practical. However, in our discussion only V_{DD} was changed in order to focus on the parasitic effects that lead to that increase.

Chapter 6

CMOS $-g_m$ Low-Power VCO

In the previous chapter, the theory and design of low-voltage, low-power VCOs were discussed. The circuit configuration of the oscillator that was used was very helpful to achieve the low-voltage, low-power and low-phase noise requirement. However, if this oscillator is to be used for higher voltage applications, the power consumption would be extremely high. Therefore, another topology should be used for designing a low-power VCO at higher supply voltages. One of the circuit configurations that can be used is a $-g_m$ topology with a current source, as shown in Figure 6.1. To achieve the low-power requirement with such a circuit, then the same steps described in chapter five must be applied. First, high quality factor tank circuits must be used. Second, the cross-coupled transistor must be biased in sub-threshold to achieve the value of g_m that satisfies the condition of oscillation at lower values of the tail current. However, to avoid the disadvantages that occur due to the mismatch between the two high quality off-chip inductors, such as the phase noise degradation and the increased power consumption, an alternative configuration must be used. The best configuration that overcomes these disadvantages is the CMOS $-g_m$ configuration shown in Figure 6.2.

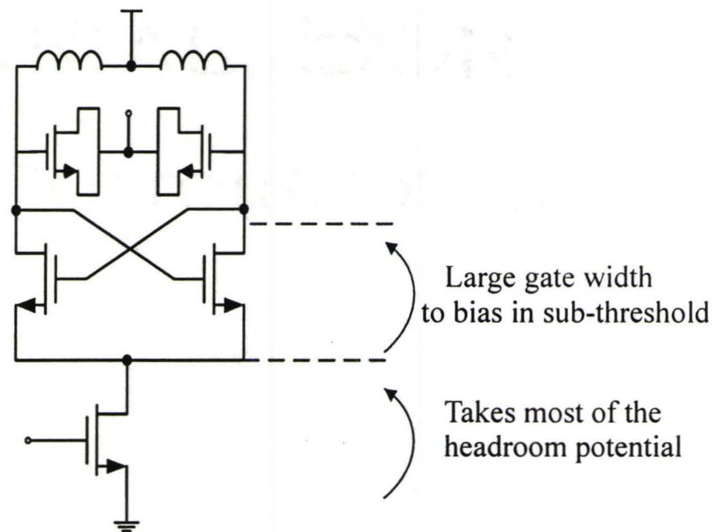


Figure 6.1 NMOS cross-coupled -g_m VCO with a current source.

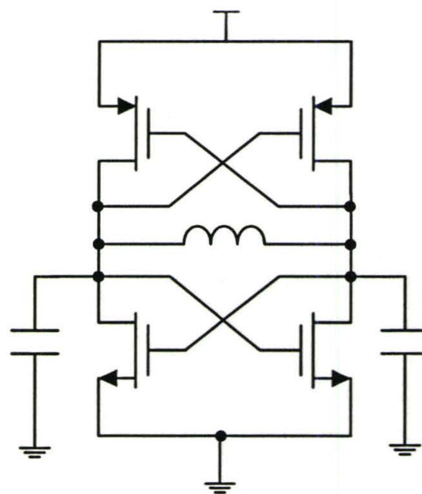


Figure 6.2 CMOS cross-coupled -g_m VCO.

6.1 The CMOS -g_m Oscillator

As discussed in chapter two, the CMOS cross-coupled -g_m oscillator has many advantages over the NMOS only oscillators. These advantages are based on the two factors, which are the presence of complementary transistors to provide the gain and also the presence of only one common load inductor between the two differential branches. The one load inductor allows only the AC component of the current to pass through it. This makes the amplitude of oscillation become twice the amplitude in the case of a NMOS only oscillator, if both oscillators are biased by the same biasing current. The use of one symmetric inductor for the CMOS -g_m oscillator makes this topology immune to the tank circuit mismatch issues that were discussed in the previous chapter. These mismatch issues lead to an increase in the power consumption and phase noise, as discussed in section 5.4.2.

6.2 Design

The design steps for this circuit are very similar to the design steps of the VCO in chapter five. This circuit is designed for a supply voltage of 1 V and the frequency of oscillation is 2.4 GHz.

6.2.1 Choice of the Tank Circuit

The choice of the tank circuit is based on the high Q value criteria. The inductor used is an off-chip inductor that has a Q greater than 40. In this design, there were no varactors used and tuning was done via the body contacts of the transistors. In this case, the tuning control voltage is connected to the body contacts of the transistor, and thus, varying the control voltage changes the substrate potential. As a result, the junction capacitances between the drain and the source from one side and the substrate from the other side will

change as a function of this control voltage. Thus, the overall load capacitance will change.

In order to avoid any problems that may occur due to the biasing of the substrate, each NMOS transistor has to be laid out in a DNW and the control voltage is connected to the p-type body contact that lies within the DNW. The disadvantage with body-biasing of the CMOS -g_m oscillator is that it requires the presence of two control voltages, where one is used for the NMOS transistors while the other is used for the PMOS transistors.

Using the body-bias for tuning makes the tuning range very small. One way to increase the tuning range is to increase the contribution of the tuning capacitance to the overall tank capacitance. This can be done by increasing the area of the source and the drain by implementing them with larger lengths L_{Source} and L_{Drain}, as shown in Figure 6.3. Increasing L_{Source} and L_{Drain} increases the width of the *pn* junction between the *n*+ implantation of the drain and the source regions and the *p*-well, and thus, increases the junction capacitance C_{DB} and C_{SB}, where C_{DB} and C_{SB} are the drain-to-bulk capacitance and the source-to-bulk capacitance, respectively. However, by making the source and the drain areas wider, this would increase the length of the path of the current in the lossy substrate, shown by R_{sub} in Figure 6.3, which degrades the overall Q of the tank circuit. However, since the value of the capacitances to the substrate are small, then $Q = 1/(\omega C R_S)$ would still have a large value.

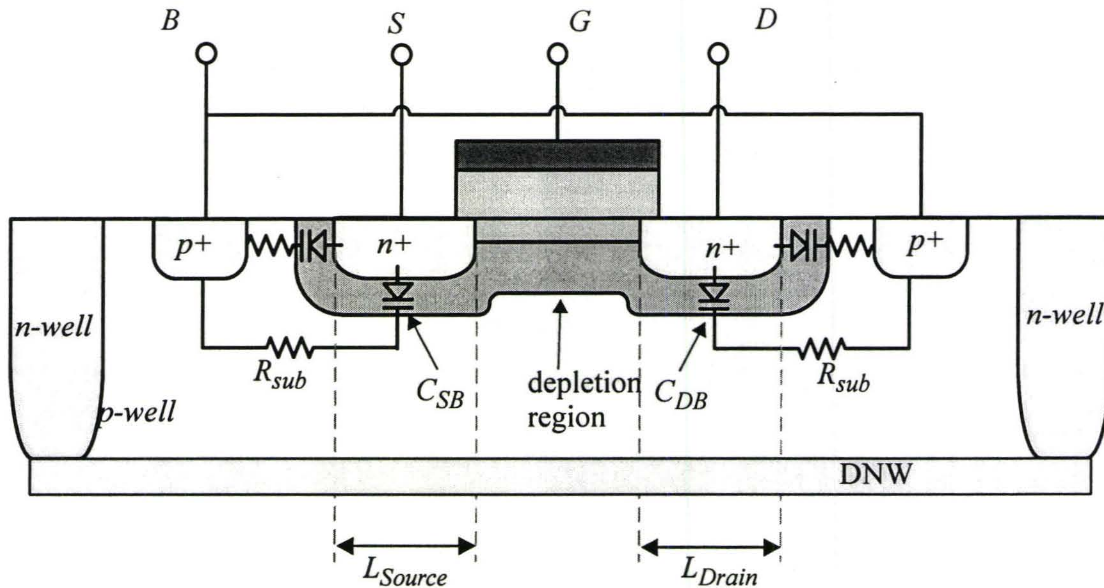


Figure 6.3 The MOS transistor with larger L_{Drain} and L_{Source} to increase C_{DB} and C_{SB}.

6.2.2 Transistors Size

For a supply voltage of 1 V, the PMOS and the NMOS transistors are estimated to have a voltage drop of 0.5 V each. The widths of their gates are then adjusted to fulfill the condition of oscillation at this biasing point. For a gain safety margin of 2, the widths of the transistors are adjusted to obtain values for the transconductance equal to

$$g_{mn} + g_{mp} = \frac{2}{R_L}, \tag{4.1}$$

where g_{mp} and g_{mn} is the transconductance values for the PMOS and the NMOS transistors, respectively. The values of g_{mp} and g_{mn} are adjusted to be approximately equal, therefore, the widths of the PMOS transistors are nearly three times the widths of the NMOS transistors, since the mobility of holes is about 2.8 times smaller than the mobility

of electrons and threshold voltage for both PMOS and NMOS transistors are approximately the same in the 0.18 μm CMOS technology.

6.2.3 Buffer

The buffer used in this circuit is similar to the buffer used for the VCO in chapter five. For further details about the design of the buffer, check section 5.3.4.

6.3 VCO Simulations

In this section, the VCO simulations are shown in order to confirm the theory of operation of the VCO and explain its performance.

A schematic of the VCO is shown in Figure 6.4. The VCO is designed to operate at 2.4 GHz with a supply voltage of 1 V. The two control voltages are shown on the figure, where V_{Bp} is the control voltage for the PMOS transistors, which is initially set to 1 V, and V_{Bn} is the control voltage for the NMOS transistors, which is initially set at 0 V.

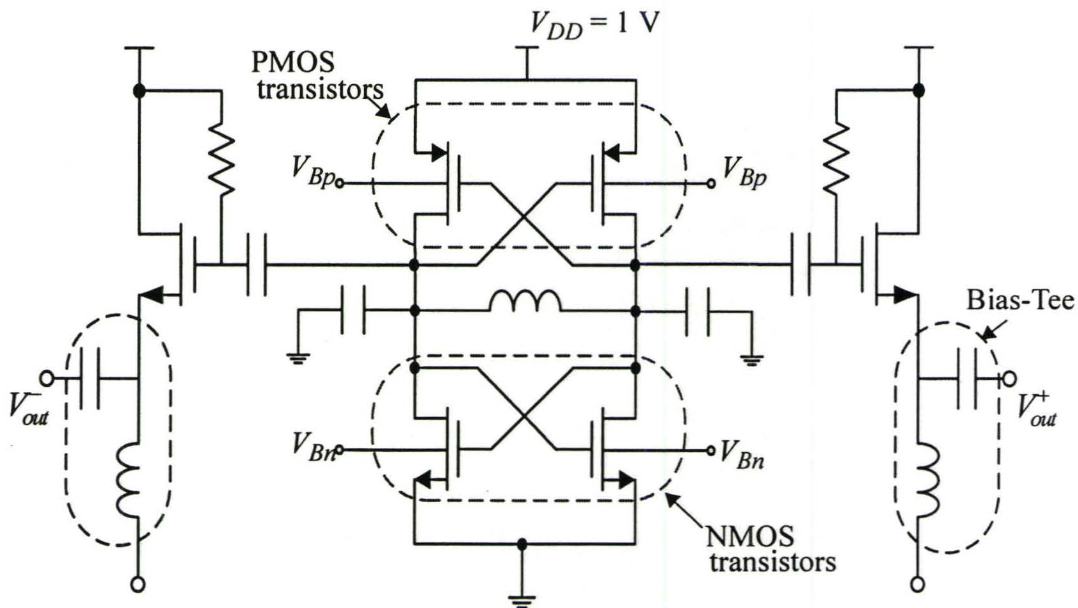


Figure 6.4 Schematic of the desgined VCO.

Figure 6.5 shows the change in the frequency of oscillation with both V_{Bn} and V_{Bp}. The two voltages V_{Bn} and V_{Bp} are adjusted in a way to make $|V_{BSp}|$ equals V_{BSn}, which $|V_{BSp}|$ and V_{BSn} are the body-to-source voltages of the PMOS and the NMOS transistors, respectivly, and change with the same steps and they are referred to by V_{cont}. The frequency of oscillation in this figure decreases as the MOSFETs are forward body-biased. Forward biasing of the body of the MOSFETs makes the *pn* junction between the the drain and source implatations of the MOSFET and its substrate becomes forward biased, which consequently increase in the *pn* junction capacitance. Unfortunately, the frequency tuning range is very small. The change in the frequency of oscillation is about 11 MHz, which makes the tuning factor about 0.5%.

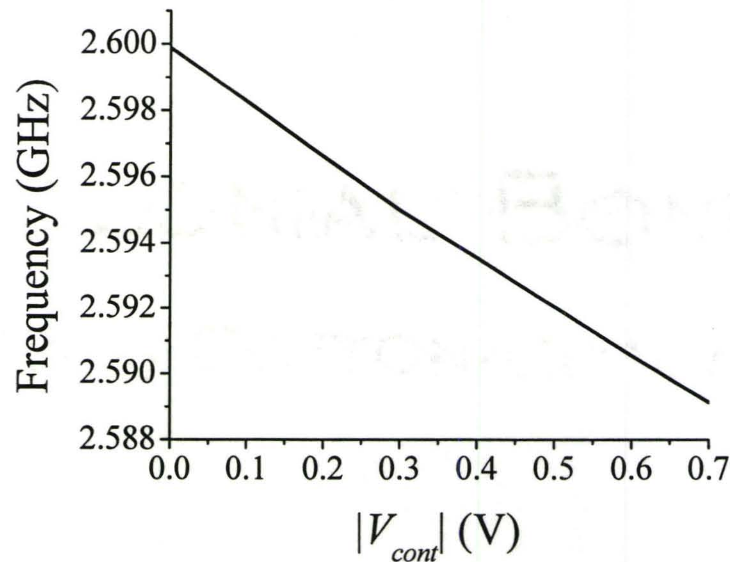


Figure 6.5 Changes in frequency versus both V_{Bn} and V_{Bp}.

One of the disadvantages of using body biasing as the tuning element is that the power consumption increases with the forward body bias. Forward biasing of the substrate decreases the threshold voltage of the transistor, as shown in Figure 6.6, and thus, pushes the MOSFET deeper into inversion. By lowering the threshold voltage of the transistor while having the same V_{GS}, the drain-to-source current I_{DS} increases. As a result, the total power consumption increases, as shown in Figure 6.7.

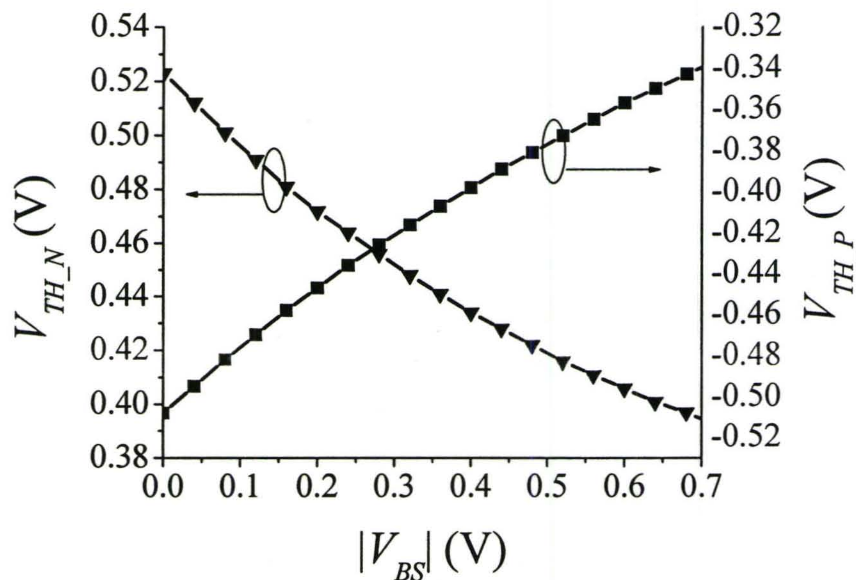


Figure 6.6 Changes in the threshold voltages of the NMOS (V_{TH_N}) and the PMOS (V_{TH_P}) with the body bias.

The VCO has a power consumption of 135 μW. Figure 6.7 shows a drastic increase in the power consumption as the forward bias of the body contact is larger 0.5 V. At this point, the *pn* junction formed by the substrate from one side and the drain and source regions on the other side of the PMOS starts conducting and most of the current flows through the substrate. Similar behaviour happens with the NMOS, however, this occurs at a body potential equal to 0.7 V. Therefore, the limiting factor for body biasing the MOSFET is set by the condition where the *pn* junction between the drain and the source and the

substrate must not be turned on. In other words, with forward body biasing the MOSFET, the potential of the substrate must be less than the built-in potential of the *pn* junction.

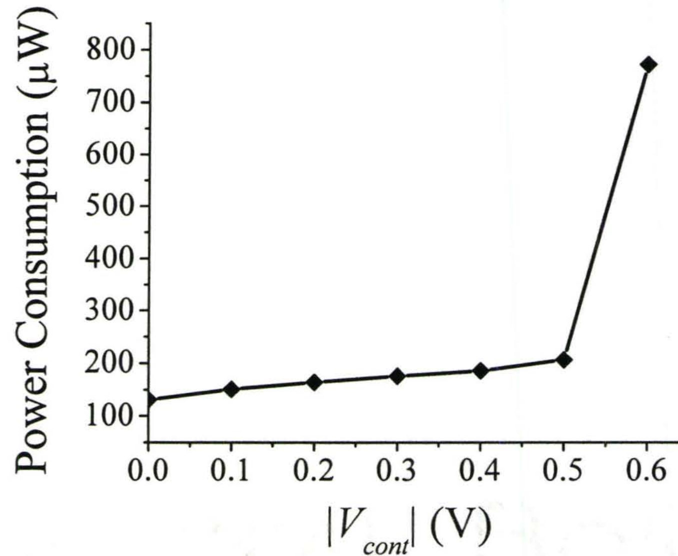


Figure 6.7 The power consumption of the VCO versus V_{cont}.

The phase noise of the VCO is -123.1 dBc/Hz @ 1 MHz offset at zero control voltage. Figure 6.8 shows the phase noise performance of the oscillator at 1 MHz offset with forward body biasing. The performance shown in this figure might be confusing as the phase noise performance is expected to degrade rather than to improve. The phase noise is expected to degrade because of two reasons. First, forward body-biasing the MOSFETs increases I_{DS}, which consequently increases the channel noise current that is injected into the tank circuit. Second, as the amplitude of oscillation is limited by the supply voltage, then any increases in I_{DS} does not increase the amplitude of oscillation and the increase in the current is an increase in the harmonic currents not the fundamental.

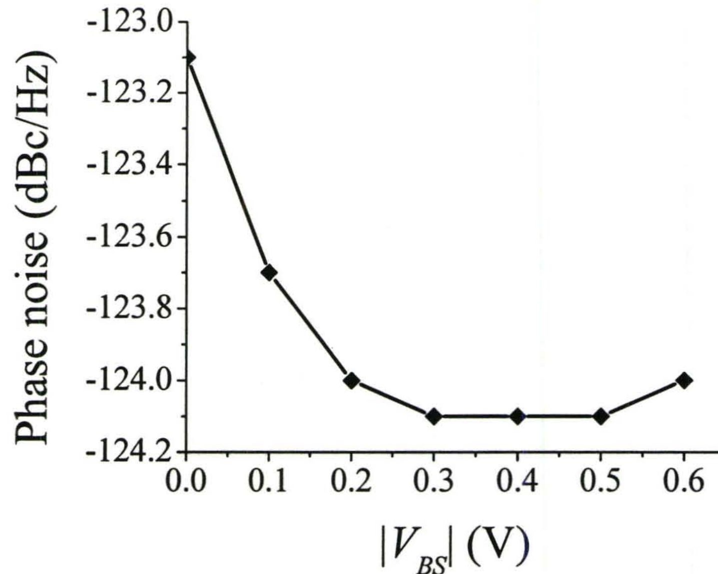


Figure 6.8 Phase noise at 1 MHz offset versus V_{cont}.

However, there is a stronger effect that leads to the improvement of the phase noise performance. Since the MOSFETs are biased to operate at the edge of strong inversion, the MOSFETs are considered highly non-linear. The non-linearties of the MOSFET at this biasing point generate high currents at harmonics, which contribute to the phase noise and degrade the performance. However, with forward biasing the MOSFET, the threshold voltage decreases and the MOSFET becomes biased more into the linear part of the I_{DS}-V_{GS} curve. Thus, by being biased in a more linear region, the currents at the harmonics start to decrease making the fundamental current increase, as shown in Figure 6.9 and Figure 6.10, and thus, contributing less to the phase noise. Therefore, the phase noise performance becomes better with forward body bias. However, driving the MOSFET further into inversion makes the other noise sources described earlier becomes dominat and thus, degrades the phase noise performance.

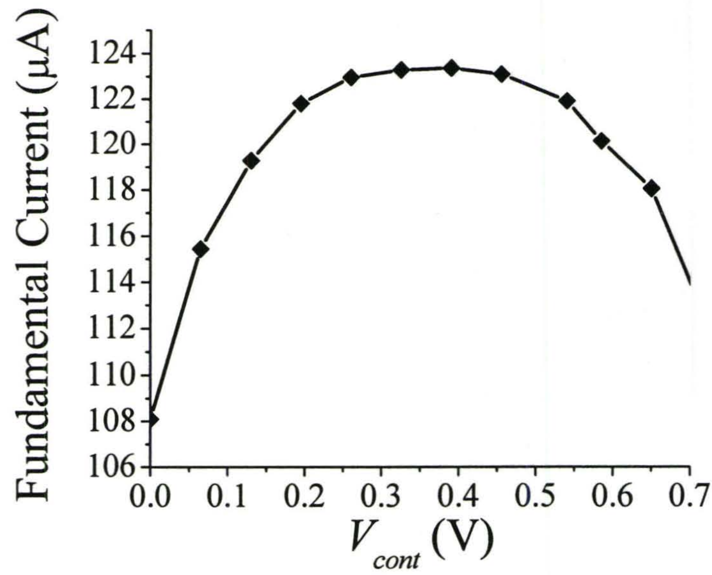


Figure 6.9 Fundamental component of the drain current versus V_{cont}.

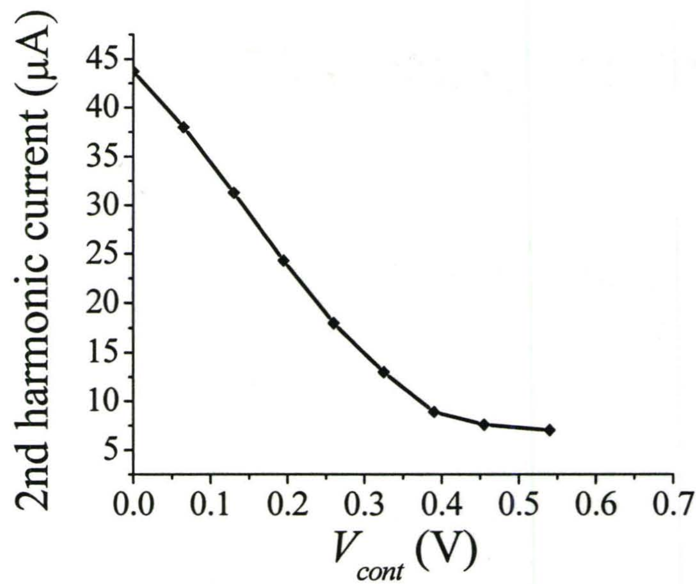


Figure 6.10 The second harmonic component of the current versus V_{cont}.

6.4 Experimental Results

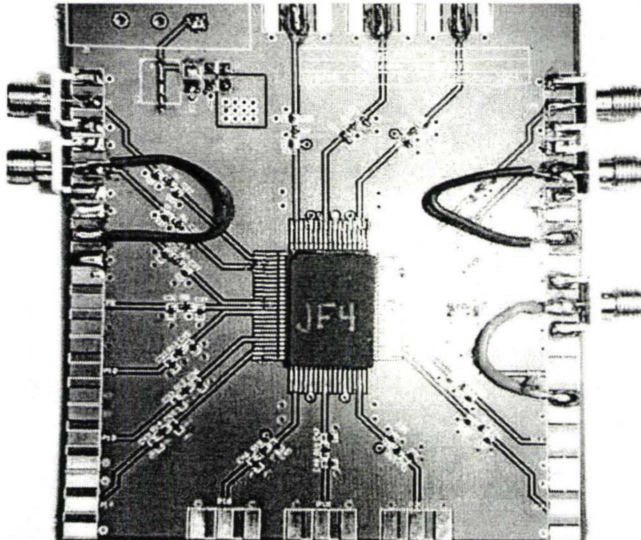
The 2.4 GHz -g_m CMOS oscillator, presented in this chapter, was tested using the Agilent E4440 26.5 GHz spectrum analyzer and a custom-made battery supply. The chip was packaged using the 80-pin CFP package and was soldered to a PCB, as shown in Figure 6.11(a), and the inductor was soldered onto the other side of the PCB, as shown in Figure 6.11(b). To examine the effect of the parasitics of the package, the off-chip inductor was short circuited so that the circuit would oscillate with its parasitic inductance of the bond wire and the package. With the short circuit load, the circuit oscillated at a V_{DD} of 2 V with a frequency of oscillation of 1.3 GHz. The short circuit load was then replaced with a 1.1 nH inductor that made the circuit oscillate at 1.105 GHz and its output spectrum is shown in Figure 6.12. With this inductive load, the oscillator started oscillating at a V_{DD} of 1.7 V. By considering the two cases of the short circuit load and the inductive load, an equivalent circuit model for the parasitics of the package can be estimated, as shown in Figure 6.12. The losses of the package were estimated from the condition of oscillation when using a short circuit load. The parasitic losses of the package led to a decrease in the value of R_{Tank}, and thus, the value of V_{DD} required to achieve oscillation was increased. The power consumption under this bias condition is 730 μW, which corresponds to a phase noise of -128 dBc/Hz at 1 MHz offset frequency and is shown in Figure 6.14. Note that at the experimental VDD of 1.7 V, the MOSFETs are operating in strong inversion. In this mode, their noise model is more accurate, so closer agreement between the measurement and simulations of the phase noise is expected, compared to the results in chapter five. This is shown in Table 6.1 where the measured phase noise is -128 dBc/Hz and the simulated one is -131 dBc/Hz. Note that the simulated power is higher than the measured one. The reason for that difference is not known at present. The differences between the simulated and the measured results are shown in Table 6.1.

The phase noise at 1 MHz offset frequency versus the control voltage is shown in Figure 6.15. The phase noise decreased with the increase in the control voltage, unlike the simulated performance shown before in Figure 6.8. The reason of this deviation is the

measured oscillator operates in a current-limited regime while the one simulated in chapter six operates in the voltage-limited regime. The reason for that is because the (R_{Tank} x I_{DS}) becomes smaller that V_{DD}. Increasing the control voltage increases the drain current, which increases the output voltage swing of the oscillator, and thus, phase noise improved with the increase of the control voltage until the oscillator is driven into the voltage-limited regime. However, in this case, the oscillator is always operating in the current-limited regime as can be observed in Figure 6.16.

Table 6.1 Comparison between measured data and simulation.

	Q	f_o (MHz)	PN (dBc/Hz)	P (mW)	FoM
Measured	40	1.105	-128	0.73	158.93
Re-simulated	40	1.105	-131	1.2	160.6



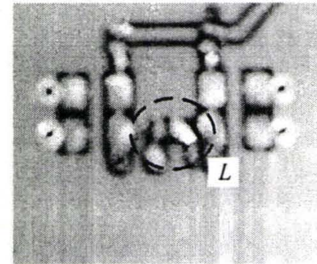


Figure 6.11 (a) Packaged chip and the PCB used for measurements with (b) the off-chip inductor soldered on the other side of the PCB.

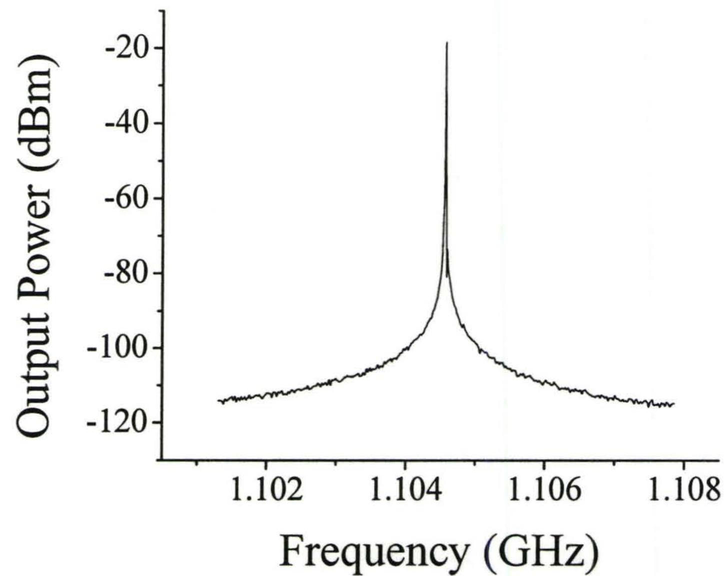


Figure 6.12 Measured output spectrum of the oscillator.

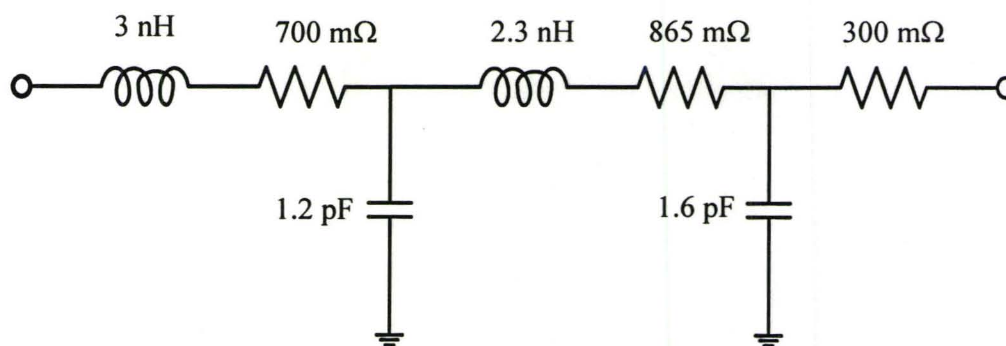


Figure 6.13 Estimated circuit model of the package parasitics.

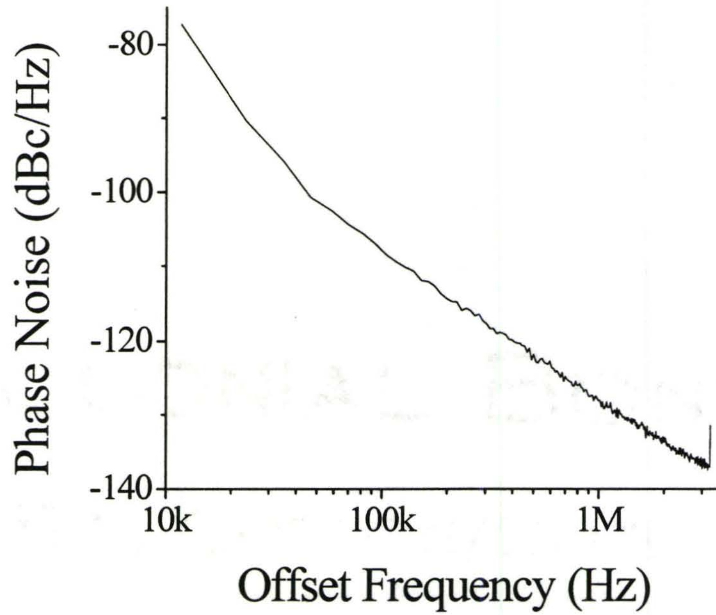


Figure 6.14 Measured phase noise of the oscillator.

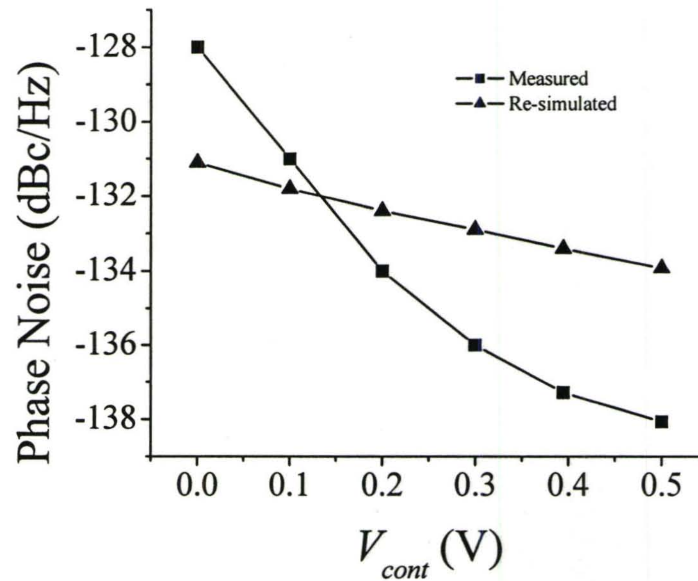


Figure 6.15 Measured phase noise at 1 MHz offset versus the control voltage.

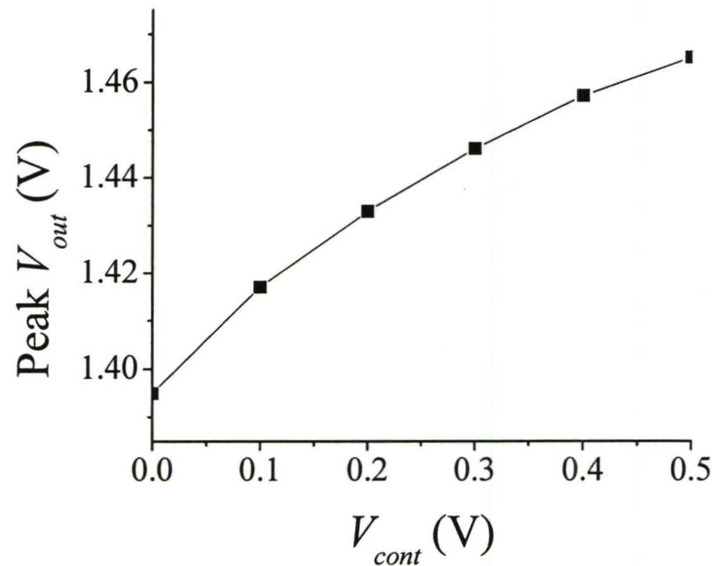


Figure 6.16 Peak output voltage versus the control voltage.

6.5 Summary

In this chapter, the design and simulation results for a 2.4 GHz CMOS -g_m VCO is presented. The VCO is designed to operate with a supply voltage of 1 V. In order to achieve low-power consumption for this design, the concepts discussed in chapter five are used. The inductor used is a high Q value inductor and the transistors are biased in sub-threshold. Tuning is realized by body-biasing the cross-coupled transistors and the effect of this body-biasing on the performance of the VCO is studied. The phase noise of the VCO is -123.1 dBc/Hz at 1 MHz offset and power consumption of 135 μW. This is considered the lowest power consumption recorded in the literature at this supply voltage. These results shows the effectiveness of the methods used to design a low power oscillator even at higher supply voltages.

The measurment results shows that the CMOS -g_m cross-coupled oscillator had frequency of oscillation of 1.105 GHz, its corresponding phase noise was -128 dBc/Hz at 1 MHz offset and the power consumption was 730 μW. The oscillator started oscillating at

a supply voltage of 1.7 V. The main reason for the differences between the measurement data and the simulation results is the package parasitics that were not taken into account during the simulations. A simple circuit model was estimated for the package by using a short circuit load for the oscillator discussed. Thus, by taking into account the estimated package model in simulations, the differences between the measurement results and the simulations were reduced.

Chapter 7 *Conclusion & Future Work*

7.1 Conclusion

The focus of this thesis was directed to the design of low-power, low-voltage VCOs. During the course of this work, much has been learnt about the design of low-voltage and low-power RF circuits. In particular, much was learnt about the design of VCOs. Also, much was learnt about passive components and the means to optimize their performance for low-power applications. This chapter concludes the research work completed.

In this thesis we have presented a new parallel strip, mutual-inductance-based monolithic inductor. Simulations for this inductor were done with momentum. The simulation illustrated that with a combination of parallel strips, higher quality factor for the inductor can be reached. Simulations showed an increase of about 23% in the peak quality factor of the parallel strip when compared to an equivalent single strip. This design of the parallel strip inductor was not optimized for a specific application, however, if the combination for the length, thickness and spacing of the parallel strip were optimized, better performance can be achieved.

A comparison between the sub-threshold operation of MOSFET and the conventional operation in inversion showed that by biasing the transistor in sub-threshold, the drain-to-source current needed to generate the value of the transconductance that fulfills the condition of oscillation would be less. In fact, for the two transistors shown in Figure 5.4, the first transistor that is biased at 0.7 V has five times the drain-to-source current

passing through it, when compared to the transistor that is biased with 0.4 V and have the same value of the transconductance.

Theory, design and simulation results of three ultra-low voltage micro-power VCOs using the -g_m topology with noise filtering were presented. The VCOs were designed at frequencies of 600 MHz, 2.4 GHz and 6 GHz. Their supply voltages were 350 mV, 400 mV and 450 mV, respectively. The power consumption of these oscillators is 36 μW, 41 μW and 90 μW, respectively. The above values for the supply voltage and the power consumption are considered the lowest recorded in literature for RF VCOs.

For this circuit configuration, the 600 MHz VCO was tested. The VCO had drastic changes in its performance. The main reason for these changes was the package used, where its parasitics were not included in the simulation. The parasitics of the package led to a decreased frequency of oscillation to 392 MHz. The VCO operates with a supply voltage of 430 mV and consumes 257 μW. The diference between the phase noise measurment and the re-simulation was around 11 dB, which is due to the inaccurate noise model in sub-threshold. In order to obtain measurement results closer to the simulated, alternative types of packages should be used. These packages should be lead-less in order to minimze the parasitic inductance and capacitance of the package. Although having different results than simulation, this oscillator agrees with the theory of operation that was discussed in chapter five.

A 2.4 GHz VCO using the CMOS -g_m topology at a supply voltage of 1 V was presented. The transistors were biased in sub-threshold to achieve low power operation. Tuning was realized using the body-biasing of the MOSFET. The phase noise of the VCO is -123.1 dBc/Hz @ 1 MHz offset and power consumption of 135 μW. This is considered the lowest power consumption recorded in the literature at this supply voltage.

This oscillator was tested using the same 80 pin CFP package. The measured frequency of oscillation was 1.105 GHz. The VCO operates with a supply voltage of 1.7 V and consumes 730 μW. This oscillator has its transistors operating in strong-inversion rather than sub-thresold, as was originally designed. Therefore, the theory of operation discussed in chapter six does not apply to this set of measured data.

A comparison between the four VCOs designed in this thesis and other oscillators in literature is shown in Table 7.1. Our oscillators show better power consumption performance when compared to others and a higher figure-of-merit.

Table 7.1 Performance of the designed oscillators.

Ref.	Q	f_o (GHz)	PN (dBc/Hz)	P (mW)	FoM
600 MHz	50	0.6	-128 @ 1 MHz	0.035	166.2
600 MHz (measured)	40	0.392	-135.5 @ 1 MHz	0.257	161.22
2.4 GHz	60	2.4	-123 @ 1 MHz	0.041	168.2
6 GHz	40	6.01	-124 @ 1 MHz	0.09	168.5
CMOS 2.4 GHz	40	2.4	-123.1 @ 1 MHz	0.135	167.3
CMOS 2.4 GHz (measured)	40	1.105	-128 @ 1 MHz	0.73	158.93
[66]	13.4	2.4	-130 @ 3 MHz	1.98	162.5
[67]	13	2.4	-124 @ 1 MHz	5.5	161.6
[70]	5	10	-101 @ 1 MHz	9	158.9

Generally, the sub-threshold operation of the MOSFETs is not suitable for RF circuit design. However, we have shown that this operation is very effective in achieving low power consumption in the VCO design without deteriorating other performance parameters.

7.2 Future Work and Recommendations

One of the areas that requires more investigations is the varactor design. With older technologies such as the 0.5 μm, the diode varactors were shown to have much higher Q values than the MOS ones. However, recent research on MOS varactors has shown that their Q values had significantly increased with the more recent technologies, as the minimum dimensions were scaled down. Therefore, more research should be done on the effect of technology scaling on the choice of the varactor for RF circuits. Also, future

research must examine whether the effect of technology scaling on the performance of different types of varactors is the same or not, as it was noticed that the performance of the MOS varactors is enhanced with a better rate with technology scaling when compared to the diode.

For the VCOs discussed in this thesis, the inductors used were high Q off-chip inductors. However, the ultimate goal is to implement the entire system on-chip. Therefore, further research should be done for monolithic inductors to improve their quality factor in order to be used in the design of low-power circuits.

One special technique to improve the Q values of the spiral inductors used in differential VCOs was discribed in [69]. In this technique the two inductors of the differential branches are used as a transformer. This transformer causes mutual coupling between the two inductors of the tank circuit and they are implemented in such a way as to produce positive mutual coupling between the inductors. The positive mutual coupling between the inductors increases the reactive component of the inductor and thus, increases the quality factor. Therefore, for the VCO designed in chapter five, the off-chip components would be replaced with this kind of transformer in order to have a fully integrated low-power VCO.

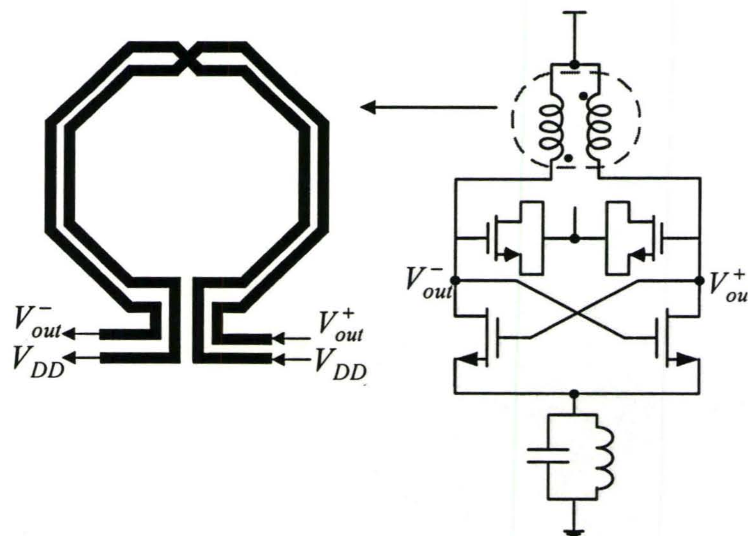


Figure 7.1 VCO using a transformer as the load inductance of the tank circuit.

In this thesis, the low-power VCO designs were only studied. However, in order to have the whole receiver chain operating with low-voltage and low-power, similar research should be done on the design of other RF circuits such as LNAs and mixers.

As for the transmitter chain, it is difficult to have a micro-power transmitter as the power budget of the power amplifier is very high. However, for application where the transmission is over short distances, the VCOs designed in this thesis can be used as the transmitter. In order to avoid loading the high Q tank circuit with the 50 Ω load, impedance transformation can be utilized to increase the effective resistance of the 50 Ω load seen by the tank circuit, as shown in Figure 7.2. This impedance transformation is done by the capacitors C_1 and C_2, and the equivalent resistance of the tank circuit at resonance becomes

$$R_{Eq} = R_{tank} \| R_{trans}, \tag{7.1}$$

where

$$R_{trans} = \frac{1}{\omega R_{Load} C_2^2} + R_{Load}\left(\frac{C_1 + C_2}{C_2}\right). \tag{7.2}$$

Unfortunately, due to the impedance transformation, most of the output voltage drop goes across the capacitor C_2. As a result, the power at the load $(V^2/2R_{Load})$ would be very small. Therefore, this technique can only be used for short distance transmission.

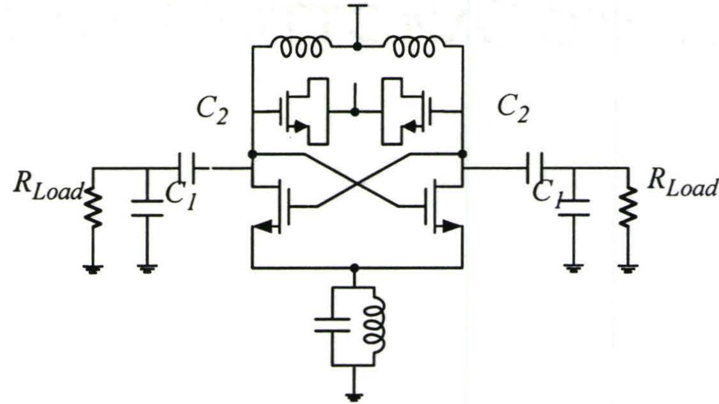


Figure 7.2 Transmitter VCO with impedance transformation of the load.

The final point that needs future investigation is whether there can be a circuit developed that can detect the mismatch of between the inductors in the differential VCO. If such a circuit can be implemented, then it would be a good idea to implement a control circuit that can compensate for the mismatch.

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