SINGLE CRYSTAL SILICON SUBSTRATE PREPARED BY VAPOUR-LIQUID INTERFACE GROWTH

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By

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Abstract

Preparing silicon wafers is a tedious multi-step process that includes etching, polishing, and cleaning. The minimum wafer thickness attainable in current high volume wafer production processes is generally 160 to 300 µm, and the kerf loss for these processes is up to 40% of the total volume. Thin silicon wafers (~30 to 100µm) are very expensive to produce and the wafering process is not cost effective due to the high amount of material loss (more than 80% at these dimensions) during the process and the risk of breakage of the wafers during wafering.

In this thesis, a new method called Vapour-Liquid Interface Growth (VLIG) is proposed. VLIG is capable of directly growing a sheet of single crystal silicon without wafering with a thickness of about 30 to 50µm. The features of the process are 1) low temperature operation; 2) the resulting silicon sheet is easily detachable and self-supporting; 3) the resulting sheet has uniform thickness and is single crystal. The system operates in a supersaturated growth solution of an indium-silicon melt. A seed line in a substrate facing down is employed. A layer of single crystal silicon grows on the seed line at the melt surface due to surface segregation during the super cooling process. The grown silicon can grow laterally due to the limited thickness of the melt depth that minimizes growth in the vertical growth direction. The grown silicon can be easily peeled off from the seed line substrate due to the presence of a gap between the grown silicon sheet and the oxide layer on the seed line substrate. The self-supporting silicon sheet now comprises a very thin silicon substrate or sheet.

VLIG silicon sheet is characterized by X-ray diffraction to determine the crystallinity. Hall Effect measurements are performed to measure the electrical properties. VLIG silicon sheet is (111) oriented single crystal and it exhibits the same orientation as

the substrate. The growth temperature is from 975 to 850^{o}C, and the VLIG silicon is p-type doped with indium. The resistivity is 4.181x10^{-3} ohm-cm, and the doping level is around 5.3.0x10^{18} /cm^{3}. The measured mobility is ranging from 280 cm^{2}/V·s. In this study, VLIG demonstrates the potential of growing thin sheet of single crystal silicon with qualities that feasible for photovoltaic application.

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1. Introduction

1.1 Background & motivation

The mainstream semiconductor material in the photovoltaic industry is silicon. The silicon based solar cell has dominated the commercial market due to the ease for mass production and reliable sourcing, and over 80% of solar-modules produced currently are composed from crystalline silicon cells [1].

Crystalline silicon based solar cells can be divided into two streams based on the crystallinities: single crystalline and poly-crystalline. The single crystalline silicon based cell has efficiency about 18% to 24%; single crystal silicon cells are made directly from sliced single crystalline silicon boules, and the near- perfect lattice and less impurities enhance the photoelectron conversion efficiency. However, the cost pressures have forced the development of multicrystalline silicon material, offering lower price accompanied with a trade off of cell efficiency. The efficiency for commercial multicrystalline silicon solar cells is from 14% to 19% [2]. In view of the advantages in terms of price currently over 50% of solar cells are produced by steadily increasing multicrystalline silicon feed [1].

In order to improve the efficiency of silicon based solar cells, monocyrstalline silicon substrate is preferred. The issues for manufacturing monocyrstalline silicon solar cells include: the growth process requires high quality materials as feed stock, sawing of silicon crystal into the thin wafers for

best cell performance consumes over 40% of the expenses [3]. This has led to the development of bulk single crystalline silicon film growth techniques.

1.2 Overview

The basic systems and theories will be discussed in the following sections pertaining to single crystal silicon or monocyrstalline and polycrystalline silicon.

1.2.1 Monocrystalline and Polycrystalline Silicon Solar Cells

Monocrystalline solar cells were first developed in 1954 in Bell Laboratories, and reached 6% efficiency with a diffused single p-n junction silicon cell, and polycrystalline entered the competition in 1981 with lower performance but competitive prices [4] [5]. Crystalline silicon solar cells can be divided into two streams based on their crystallinities, and also they have very distinct production routes. Monocrystalline silicon wafers are cut from boules that are pulled continuously from a pure melt. To minimize waste, circular wafers were trimmed on four sides retaining the original circle but maximizing the surface area in modules [5]. Polycrystalline silicon is made by melting and pouring into a mould to solidify. Blocks of silicon chunks then can be cut into square wafers. The surface of polycrystalline silicon cells has random grain orientation structure, and it causes variation of blue colours.

1.2.2 Solar Cell Principles

The theory of the solar cell can be explained by a simple model in which light is converted into electrical current when absorbed in semiconducting materials, for example silicon. Absorbed photons produce free electrons and holes in the material which can flow and produce electricity. As a result, arrays of solar cells are able to convert solar energy into a directional current with a certain amount of lost energy.

A simplified p-n junction model is shown in ***Figure 1.1***. The basic silicon solar cell is considered a *pn* junction with a narrow heavily doped n-type layer, and a depletion region (W) that extends to the p-type doped region. In the depletion region, there is a built-in field (E_0). Most of the photons are absorbed in the depletion region and p-type region, and electron-hole pairs (EHPs) are generated within this region. EHPs that are generated in the depletion region are separated by the built-in field. Electrons drift to n^+ side, and holes drift to p^+ to make the p region positive. When EHPs are generated in the p-type region, electrons are diffused into the depletion region, and similarly due to the electric field (E_0) electrons drift to n-side region make it negatively charged. As a result, the open circuit voltage can be developed across the positive p-side and negatively charged n-region. EHPs generate that are too far away from depletion region or near the n-side surface region are lost by recombination [6].

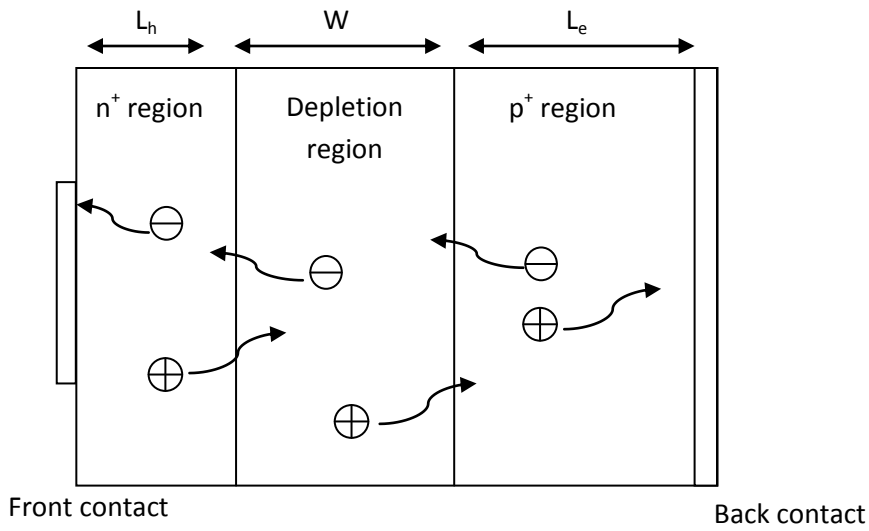


Figure 1.1 *The schematic diagram of a silicon solar cell with the front and back metal contact. The movement of the photogenerated carriers within the volume of Lh+W+Le are shown in the arrows.*

Silicon has a band gap of 1.1 eV. The wavelength corresponding to 1.1 eV band gap is about 1.1 µm (near infrared). Therefore, incident light that has energy wavelength over 1.1 µm is not able to participate in the photovoltaic effect. In addition, higher energy photons are being absorbed at or near surface region and are lost due to recombination. The loss at near surface and crystal surface can be up to 40%. In addition to surface recombination losses, the photon collection efficiency is about 80 to 90% depending on the anti-reflection design. In principle, the limit in efficiency of single crystal silicon solar cells at room temperature is about 30% [6]. Photons with higher energies, in the case of silicon based solar cell is greater than ~1.1eV, are partly wasted since they exceed the bandgap energy for silicon to absorb. It is also worth to notice that the open circuit voltage in silicon based solar cell is less than 1.1eV and has a lower value

about 0.6eV due to recombination processes in the cell and radioactive recombination.

1.2.3 Ideal Thickness

A critical parameter for silicon based solar cells is the thickness of the substrates. As shown in ***Figure 1.2*** [1], peak efficiency occurs at thickness around 50 to 120 µm. The thickness is dependent on the manufacturing and material properties, such as front and back recombination rate, carrier lifetime, and diffusion lengths. In ***Figure 1.2***, the sample with diffusion length (L_d) of 400µm has an optimum thickness of 120 µm. For a structure with 200 µm L_d, the optimum thickness is in the range of 80 µm. For a diffusion length of 100 µm sample, the highest efficiency sits at about 50 µm thickness. Theoretically, a thickness of only 50 to 120 µm of silicon wafer is the physically optimum thickness for silicon based solar cells. However, currently commercial silicon solar cells still have thickness around 200 µm because of the mechanical stability and also technology bottleneck. In the 50 to 120 µm thickness, the single crystalline silicon becomes very fragile and it is very hard to handle mechanically. In addition, manufacturing process of such thin silicon wafers is not cost effective due to kerf loss in the wafering process [1].

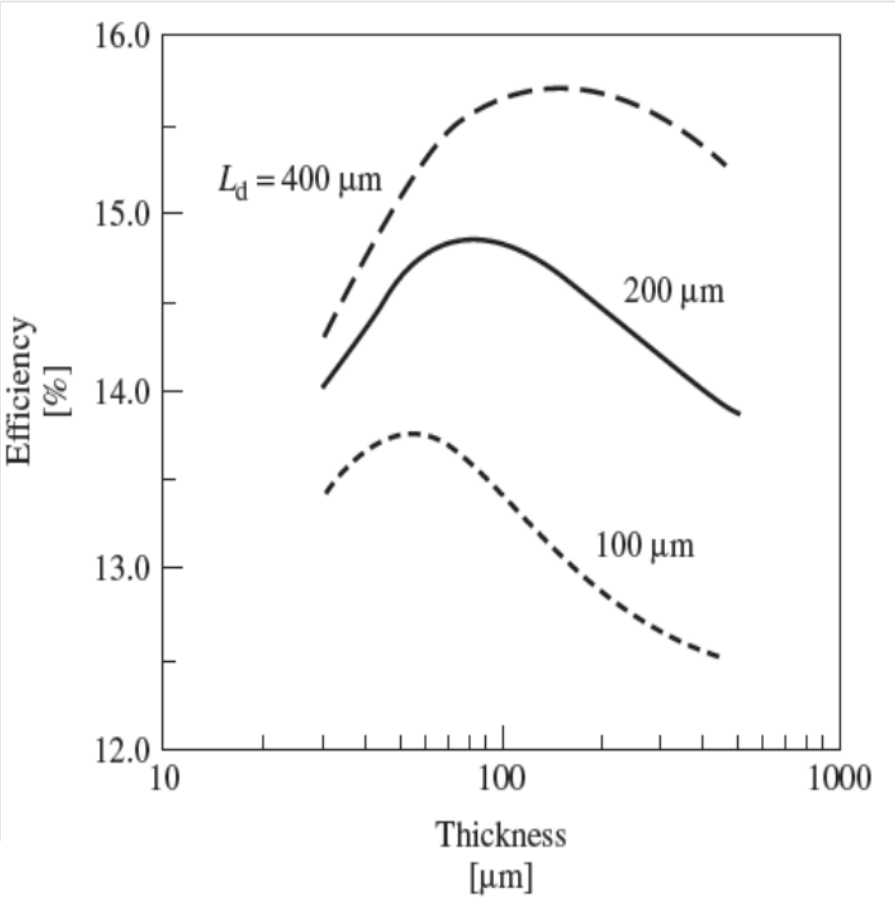


Figure 1.2 *The theoretical cell efficiency with different thickness. The single crystal silicon was grown using "String Ribbon Growth".*

1.3 Research Objectives

This thesis presents an innovated design called, vapour-liquid interface growth (VLIG) for growing thin single crystal silicon sheet as substrates for electronic or photovoltaic application. VLIG was designed based on the concepts of crystal pulling and liquid phase epitaxy techniques. To fully optimize the silicon based solar cell performance, there is a need to develop a new growth technique to produce thinner silicon wafers to reduce the energy loss in energy

conversion and light absorption. In conventional silicon growth methods, the thickness can only reach to 180μm due to the limitation of dicing technique. Silicon film grown by epitaxial methods, such as Chemical Vapour Deposition (CVD), Molecular Beam Epitaxy (MBE), and Vapour-liquid-solid (VLS) are time consuming and not cost effective. The thickness in epitaxial growth is usually in the nanometer or micron range, and thus is not applicable for substrate manufacture. With this basis, the objectives of this study include the following:

1. To develop and implement an integrated growth design (VLIG) for bulk single crystal film growth.
2. To optimize the growth results in VLIG with the considerations of surface smoothness and aspect ratio.
3. To study the growth mechanism based on vapour-liquid interface, and the electrical properties of the grown silicon.

This thesis consists of 4 chapters including background, objectives and research direction in Chapter 1. Chapter 2 provides the related growth techniques in industry and review of recent literature of growth kinetics. Experimental procedures and equipment setup of VLIG are presented in Chapter 3. Chapter 4 covers the results of grown silicon using VLIG as well as the growth mechanism. Finally, Chapter 5 contains conclusions and summary of proposed future work using VLIG.

2. Literature Review

The present trend in silicon growth technique is toward high production volume with larger diameter despite a high cost in wafering. Consequently, a simple and cost effective growth design must be applied to assist the trend of increased efficiency in photovoltaic devices. Nevertheless, silicon based solar cell is a well known area in photovoltaic devices. It is a combination of many technical areas of study. As silicon wafer growth is one of these areas the thickness of the silicon wafer is extremely crucial in the development of high efficiency solar cells.

The modern silicon manufacturing method can be divided into two streams based on the growth kinetics. The main stream is bulk silicon growth, and the examples are Czochralski (CZ), and Float zone (FZ). The other stream is epitaxial growth and the examples are liquid phase epitaxy (LPE), Molecular Beam Epitaxy (MBE), Vapour-Liquid-Solid (VLS), Chemical Vapour Deposition (CVD). The material loss is playing an increasing role in thin silicon wafering processes. Examples of the different material losses are kerf losses in wafering process, flattening losses, polish losses, and saw damage in dicing and grinding [1-6].

The current silicon growth technologies deserve a careful examination because the optimum efficiency for silicon based solar cell has a theoretical thickness around 60 to 80µm. The technology bottleneck for single crystalline silicon is at 180µm for mass production. The demand of thin silicon wafers in the past few years have increased to improve not only the solar cell efficiency but also reduce the overall weight in electronic devices. The focus of this chapter will be on conventional single

crystal silicon growth techniques and some of the proposed techniques in epitaxial growth methods.

2.1 Crystal Growth of Silicon

The starting material for growing Si crystal is silicon dioxide (SiO_2). SiO_2 feedstock reacts with coke, which is in the form of carbon in high temperature (~1800^{o}C) arc furnace to form a reduction process as the following:

$$SiO_2 + 2C \rightarrow Si + 2CO$$

Metallurgical grade Si (MGS) is referred to as silicon obtained from the high temperature reduction process with carbon. It has impurities of aluminum, iron, and high concentration of carbon. The impurity level of MGS usually is about $5x10^{16}cm^{-3}$ for 1 parts per million (ppm) of Si [7]. MSG form is not suitable for electronic application due to the high impurity content and further refinement is requiring yielding electronic grade silicon (EGS). The level of the impurities for MGS is reduced by reacting with dry HCl to form trichlorosilane ($SiHCl_3$), and pure $SiHCl_3$ is then converted to pure grade silicon by reaction with H_2. The silicon reduced by hydrogen is due to the fractional distillation process, where the mixture of $SiHCl_3$ and the chloride impurity such as $FeCl_3$ has different vapor pressures, and by condensing the vapors in different temperatures, the purified $SiHCl_3$ can be separated from the mixture [7] [8]. The reaction can be expressed in the simplified form in the following:

$$Si + 3HCl_{(g)} \rightarrow SiHCl_{3(g)} + H_{2(g)}$$

$$2SiHCl_{3(g)} + 2H_{2(g)} \rightarrow 2Si + 6HCl$$

The silicon produced by the above process route is still polycrystalline silicon with levels of impurities reduced to parts per billion (ppb) ranges. The conversion of polycrystalline silicon to single crystalline is generally done by *Czochralski* method or float zone growth and both methods will be discussed in the next section.

2.2 Czochralski & Float Zone Growth

Single crystal silicon has been widely applied in various industries such as computer chips and solar cell panels. About 75% of the single crystal silicon is produced by *Czochralski* process route; it also called *CZ* process [1]. It is named after a polish scientist called Jan Czochralski who discovered this method in 1916 while he was investigating the recrystallization of the molten metal. In 1950s, *CZ* process was applied to manufacturing single crystal silicon [7] [8].

The process begins with the melting of feedstock of poly silicon, usually metallurgical grade silicon, in the crucible. The crucible is heated up to 1500^{o}C, and the melting point of silicon is 1412 ^{o}C. When the silicon is fully melted, a small seed crystal is mounted on the end of a rotating shaft and is slowly lowered into the melt to dip just below the surface of the melt shown in ***Figure 2.1****(a)*. The seed crystal provides a template for oriented growth. The shaft and the crucible are then rotated in different directions and the rod is then withdrawn from the crucible very slowly to form a cylindrical column of silicon boule. The seed crystal and crucible are rotating slowly to provide a stirring condition in the melt and to prevent temperature variation that could cause inhomogeneous nucleation

of impurities [7] [8]. The boule length can be to up to 2m, and the diameter can reach up to 450mm.

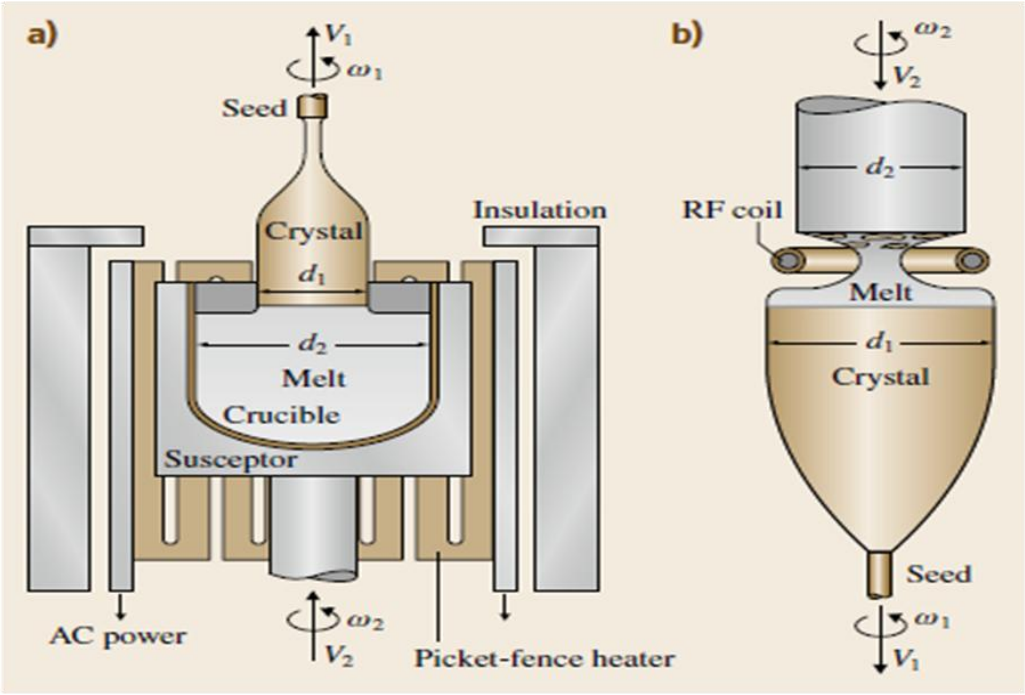


Figure 2.1 *Conventional single crystal silicon manufacturing techniques. (a) Czochralski process. (b) Float zone growth*

Single crystal silicon can be grown from the melt directly without presence of a crucible, and Float Zone (*FZ*) growth is realized. *FZ* technique was first applied in single crystal silicon growth in 1953 by Keck et al. [8] [9]. Float zone growth involves the movement of the liquid zone through the material, and zone melting takes advantage of the small segregation coefficient of impurities. The impurities contained in the feed material would then prefer to remain in the melt and thus can be easily swept to the end of the feed stock. Compare to *CZ* process, float zone can offer higher purity levels due to the lack of contamination from the crucible, but the diameter is limited to around 125 millimetres [8]. ***Figure 2.1****(b)* shows the schematic diagram of *FZ* process. The growth is initiated

by dipping single crystal seed into the melt zone, and once the seed is wetted by the molten silicon, the growth of the single crystal rod increases with lowering the seed.

2.2.1 Wafering

Wafer processing is an essential step to turn grown crystal ingots into wafers for further application in electronic devices. Wafering process is a mechanical process that involves using a diamond-tipped inner-hole blade saw or a wire saw. A suitable wafer for any application should be clean cut, and polishing the sides of the slice until all the marks are removed and the surfaces are smooth.

A typical wafering process involves: 1) crystal growth, 2) slicing, 3) Flattening, 4) Etching, 5) Polishing, and 6) Cleaning. The slicing process is done by ID saw or wire sawing, and in the flattening part usually involves grinding the silicon ingot to a more perfect cylindrical shape with precise diameter. The crystallography i.e. crystal planes are determined by using X-ray crystallography technique. The silicon cylinder is sawed into certain thickness using the diamond saw or wire saw. Then the wafers are lapped and grinded on both sides to improve the smoothness on the damaged surfaces. The wafers undergo chemical etching and polishing using slurry of fine silica (SiO_2) particles in a basic solution of NaOH to provide a mirror finish [7].

2.2.2 Challenges & Issues

Two issues arise from using CZ and *FZ* growth to meet the demand of lower wafer cost:

1. Energy intensive

Both *CZ* and *FZ* growth are high-energy intensive growth methods. For example both processes require melting the feed stock silicon and this in turn requires working temperatures about 1600^{o}C.

2. Material lost during wafering

Wafering processes cannot effectively utilize the raw material since the products have to be cropped off on both ends. The most common methods of wafering the silicon ingot is using a inner diameter diamond saw blade, and the kerf lost for the ID blade can sometimes reach up to 700um depending on the size of the blade. In ***Figure 2.2*** is the cost structure of a single crystalline solar cell. 65% of the total expense is incurred in the silicon wafer, and within the silicon wafer cost, the sawing process occupies about 1/3 of the cost per wafer [1] . The cost issue further arises when cutting thinner wafers. The optimum thickness for silicon based solar cell substrate is in the region about 60 to 100 µm thick. The challenges for wafering thin wafers are not only the process bottleneck, but also the large amount of material lost during wafering. In order to keep the overall process cost-effective, commercial wafer thickness is in the range of 180 to 350 µm.

The direct growth of silicon sheets has been undertaken using the "String Ribbon Growth" method. Here silicon multi-crystalline sheets are pulled directly from a silicon melt [10]. Disadvantages include lack of single crystal growth, very high temperatures during growth and incorporation of impurities from the liquid silicon container.

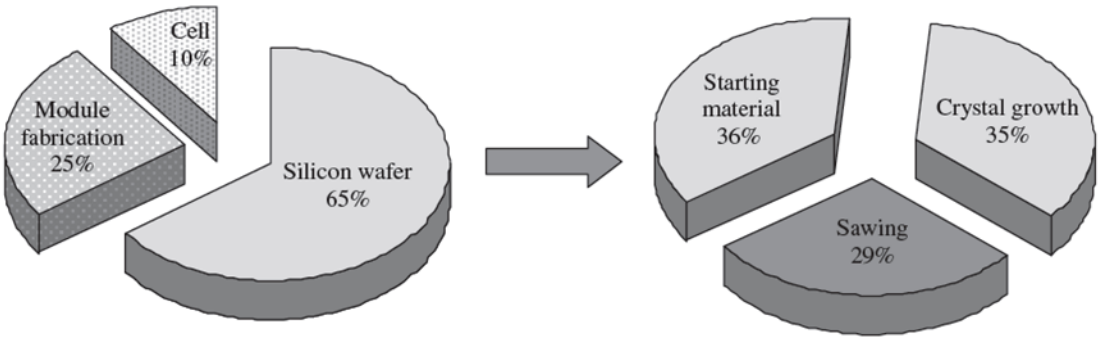


Figure 2.2 *The cost structure for typical silicon based solar cell.*

2.3 Epitaxial Growth of Silicon

Epitaxial growth is usually applied to a film growth on the crystalline substrate with certain alignment between the grown film and substrate. Epitaxial growth is widely applied in the field of optical and electronic devices. Epitaxial growth can be performed by different methods, and the methods are classified according to the growth phases, such as liquid phase epitaxy (LPE), vapor-liquid-solid (VLS) method, Molecular beam epitaxy (MBE), physical vapor deposition (PVD), chemical vapor deposition (CVD) [11] [12]. Epitaxial growth generally applies for thin film with thickness in few microns to nanometer range. Therefore, it is relatively challenging and not cost effective to use MBE, CVD, VLS and

PVD to achieve mass production of thick single crystalline silicon substrates for photovoltaic application (~100 µm thickness). LPE was successfully adapted into solar cell manufacture in 1976 by Runyan. In 1982, Ito and Kojima made 10.4% efficient silicon solar cells by using an n-type silicon wafer that was grown using LPE from a gallium melt, and in 1984, Possin propose a silicon solar cell with a thickness of 10 to 50 µm epitaxial junction that was grown by LPE system. In ***Table 1*** is the recent results for solar cells that were made with LPE method.

Researchers	Substrate	solution/ temperature	Results(Efficiency; voltage)	Reference
Samsung	p-Si	In	15.8%; 634 mV	Lee et al., 2003 [13]
MPI	SiGe buffer/Si	In, 950oC	59.1%	Gutjahr et al., 1997 [14]
MPI	p+sc-Si	In, 950oC	14.7%;659mV	Werner et al., 1993 [15]
UNSW	p+sc-Si	Sn/Ga	15.4%; 616mV	Shi et al., 1996 [16]
UNSW	p+sc-Si	In/Ga	14.7%;640mV	Shi et al., 1996
ANU	p- sc-Si	In, 950oC	18%; 666mV	Blakers et al.,1995 [17]
ANU	P+ sc-Si	In, 950oC	17%;651 mV	Blakers et al.,1995
Shinsu U.	n-Si	Al	9.9%	Ito and Kojima., 1979 [18]

Table 1 *Results for monocyrstalline silicon substrates solar cells made with LPE.*

2.3.1 Liquid Phase Epitaxy

Liquid phase epitaxy (LPE) is widely applied in compound semiconductors growth. LPE starts with high temperature growth solution and epitaxial deposition take place when the concentrated growth solution

is super cooled to precipitate the desired compound materials. The growth can be done in dilute solution under lower temperature growth or highly super saturation growth solution with higher growth temperature. The basic operating parameters for LPE are growth solution selection, substrate selection, and growth temperature.

In practice, LPE cannot reach less than 1 μm thin due to the high surface tension between liquid metallic solution and semiconductors [19]. The advantages of LPE are the following:

1. Near-equilibrium conditions are obtained during epitaxial layer growth and therefore the film structure is defect free, and the surface and interface are atomically smooth.
2. Growth rate can be controlled by solution concentration, super cooled temperature.
3. Homogeneous growth environment
4. Excellent stoichiometry of the layers due to the growth temperature is well below the melting point and below the solid solution coexistence range of the compound
5. Cost effective, and easy to scale up for mass production

LPE growth modes depend on the interface thermal dynamics, supersaturating driving force, substrate lattice mismatch, and mis-oirentations. In ***Figure 2.3*** indicates eight general epitaxial growth modes. In LPE growth, the epitaxial layer would have layer by layer growth (Frank-Vander Mere mode) if the growth solution is more diluted and the

misfit on substrate is minimized with respect to the epitaxial layer. Higher thermodynamic driving forces, for example, at higher supersaturation, result in a high concentration solid solution with larger step velocity along the surface; the growth mode becomes step bunching. Microsteps are grown due to the fluctuations of higher steps that catch up with lower steps. In LPE generally layer by layer, step flow growth, and step bunching are observed [19].

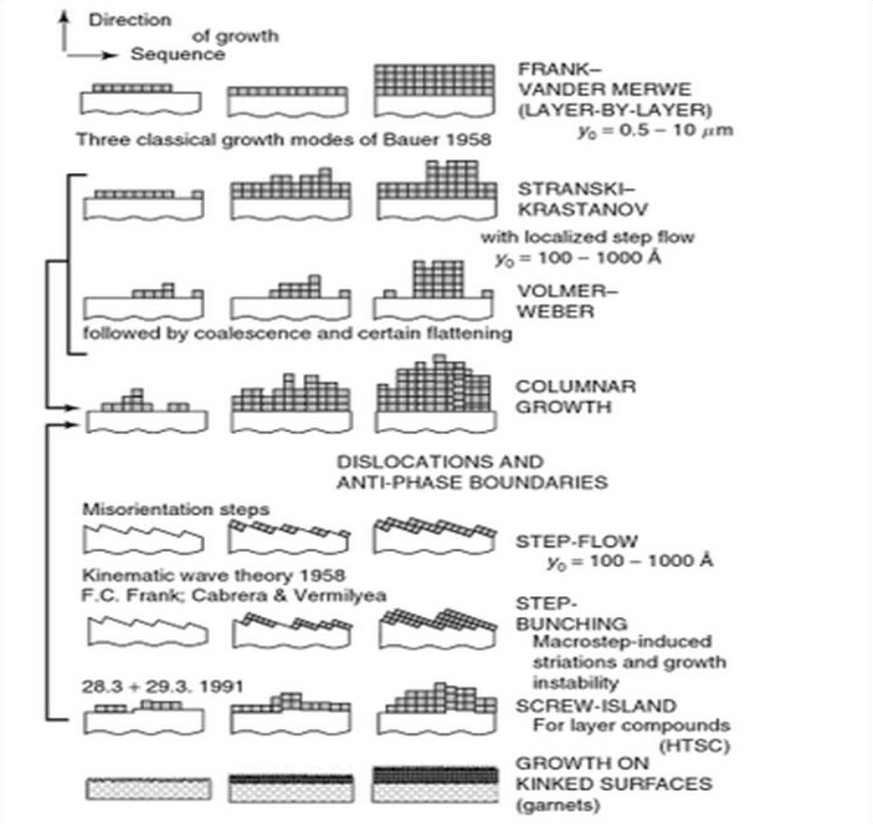


Figure 2.3 *Eight epitaxial growth modes.*

The driving force for LPE growth is based on the supersaturation of cooling the growth solution from equilibrium liquidus temperature. There are three types of cooling processes based on different cooling rates shown in ***Figure 2.4***. In ramp-cooling a constant cooling rate is

established over time and the growth starts right after the cooling starts. In the step cooling method, a rapid cooling was established and large supersaturation was obtained. The growth starts right after a large supersaturation was obtained. The advantage of the step cooled process is that the growth can be controlled by limiting the amount of supersaturation. Finally, the combination of ramp-cooling and step-cooling, results in an epitaxial layer grown by large supersaturation and growth occurs at a constant rate [20].

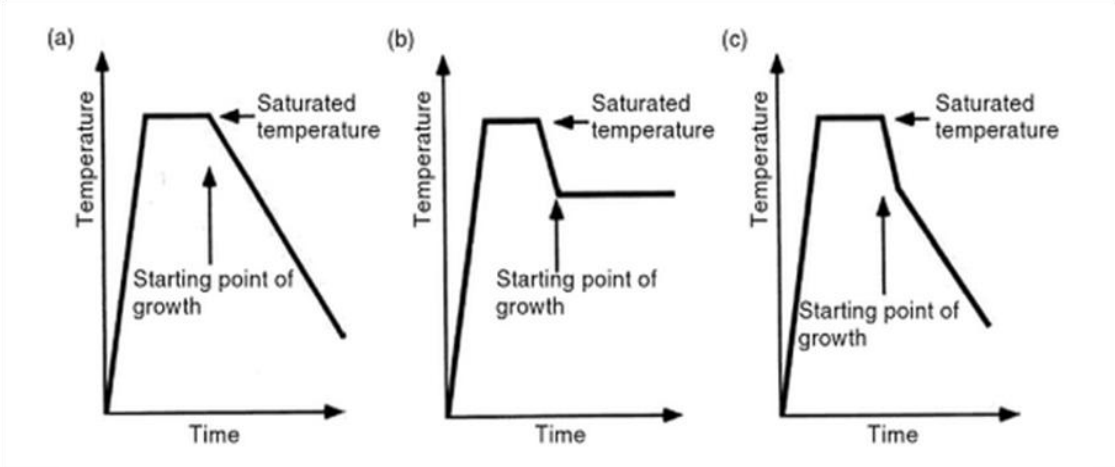


Figure 2.4 *Three different cooling process of LPE: (a) ramp-cooling; (b) step cooling; (c) super-cooling.*

The LPE process can be understood as a straightforward nucleation process lead by a supercooled supersaturated growth solution. The LPE technology can be divided into two streams: vertical dipping and horizontal slideboat. The vertical dipping system, as shown in ***Figure 2.5****(a)*, can process larger size samples and is usually used for a single thick epitaxial layer; however, the layer thickness cannot be precisely

controlled. On the other hand, the horizontal slider boat system, shown in ***Figure 2.5****(b)*, is usually for growing multilayer structures or heterojunctions. To improve the growth rate and increase the numbers of the growth junctions, there are several modifications that have been developed. ***Figure 2.5****(c)* shows the rotating-crucible method based on the vertical dipping system, where it is used to grow multiple thin-layers and silicon layers with large diameter. The rotating-crucible was capable of utilizing the centrifuge force to grow thin layers of uniformly distributed silicon 10cm in diameter on silicon substrates [21]. D. Mouleeswaran et al. demonstrated selective area growth of GaAs by current control LPE (CCLPE) based on the horizontal slider boat system [22] [23]. The application of electric field and currents is used to induce and control the growth from growth solution, where the electric current through the melt induces electromigration to solute solution and it contributes to the transportation in solution from source to substrate [24].

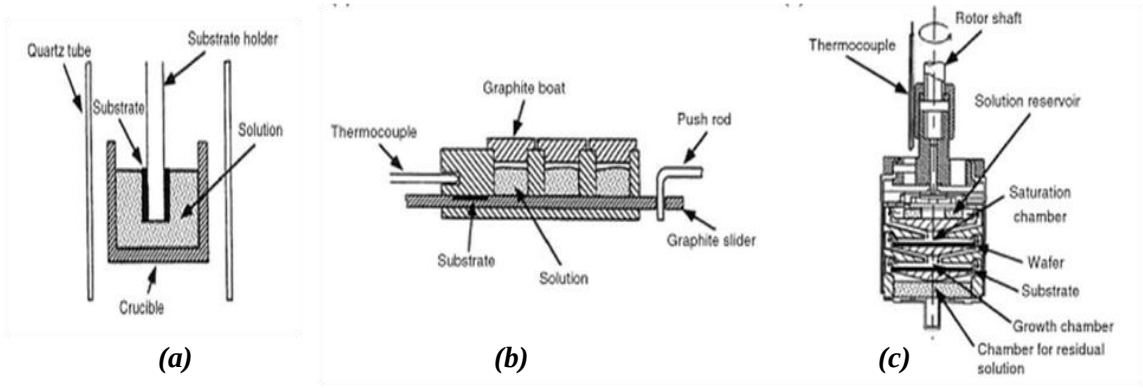


Figure 2.5 *LPE growth techniques based on the loading direction and growth solution orientation: (a) Dipping method; (b) Sliding-boat method; (c) rotational crucible*

LPE is highly sensitive to a clean, uniform, defect free substrate. The lattice match of the substrate and epitaxial layer also plays an important role. The challenge of using LPE growth arises from the substrate selection and solution selection. The orientation or mis-orientation of the substrate can determine the epi-layer quality. The largest challenge in LPE for making heterojunction epitaxial layer is the lattice match and misfit between substrate and epilayer; the thermal expansion coefficients of the two vary with temperature and thus reduce the deposition rate and crystal quality. One challenge in LPE in the case of silicon film growth; however the diffusion path for silicon is not restricted. In other words, the deposition rate of silicon atoms is similar in vertical and lateral direction.. As the result, the grown silicon usually has an aspect ratio (width: thickness) of 1 or less than 1. The definition of the width and thickness is shown in ***Figure 2.6***. One of the most important challenges of the LPE system is the poor control of the epitaxial layers resulting in poor reproducibility of the crystal quality and electrical properties [19].

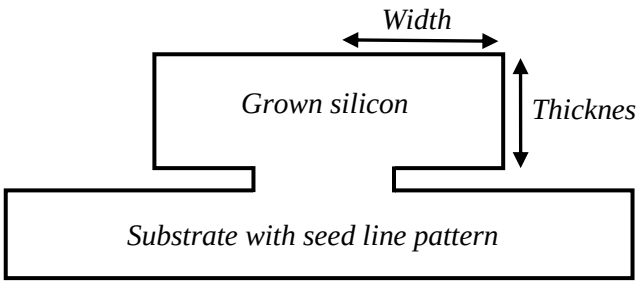


Figure 2.6 *The schematic diagram for measuring the aspect ratio in cross sectional area view. The width is from the middle of the seed line to the edge of the grown silicon.*

2.3.2 Lateral Diffusion Liquid Phase Epitaxy

Lateral Diffusion Liquid Phase Epitaxy (LDLPE) is a silicon growing method invented by Bo Le et al., 2011 [25] [26]. The objective of LDLPE system is to grow self-supported single crystal silicon platelet without wafering. The system is based on the concept of liquid phase epitaxy, the layer of silicon grow from a liquid phase by reaching super-saturation in a growth solution. The deposition of the silicon atoms on a silicon seed line (100µm) initiates the formation of a single crystal platelet. The invention is to overcome the low growth aspect ratio in conventional LPE system, and to grow thin silicon sheet around 100 µm as it received.

The epitaxial growth is achieved by the presence of an oxide silicon plate on top of the nucleation site. The function of the plate is to control the thickness by limiting vertical nucleation on the platelets, and to enhance the surface smoothness by restricting diffusion of silicon to a horizontal direction. In addition, the thickness of the film is limited by the geometry of the growth apparatus, and the lateral diffusion growth process will continue to increase the aspect ratio (width/thickness) thereby forming a silicon single crystal sheet.

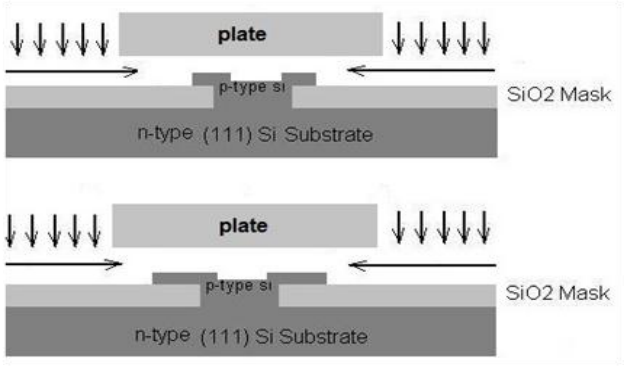


Figure 2.7 *The substrate and oxide plate setup in LDLPE.*

Figure 2.7 shows the schematic diagram of the growth silicon platelet on the substrate. The silicon growth shows that the lateral phenomenon is due to diffusion limited in vertical direction with the presence of the oxide silicon plate. The growth was done in a silicon rich solution bath. Indium was choosing as the growth solution to dissolve source silicon and form supersaturated Si-In solution at 950^{o}C. The deposition followed by a constant cooling rate of 0.25^{o}C from 950 ^{o}C to 850 ^{o}C. With the assistance of the oxide plate, silicon atoms in the growth solution will diffuse to the seed line laterally, rather from the top of the seed line. Lateral diffusion is enhanced by the diffusion limited mechanism.

Figure 2.8 is the growth cross section of the LDLPE. The aspect ratio is ranging from 0.8 to 2.75. The surface however, tend to form ledge and kinks in LDLPE system, and the ledge/kinks formation largely reduce the width and thickness aspect ratio. Atomic smoothness on the surface is therefore hard to achieve in LDLPE growth. The average aspect ratio of grown silicon strip by LDLPE is around 2 where the conventional LPE can only reach up to 1. There are opportunities to improve the surface smoothness and aspect ratio in LDLPE.

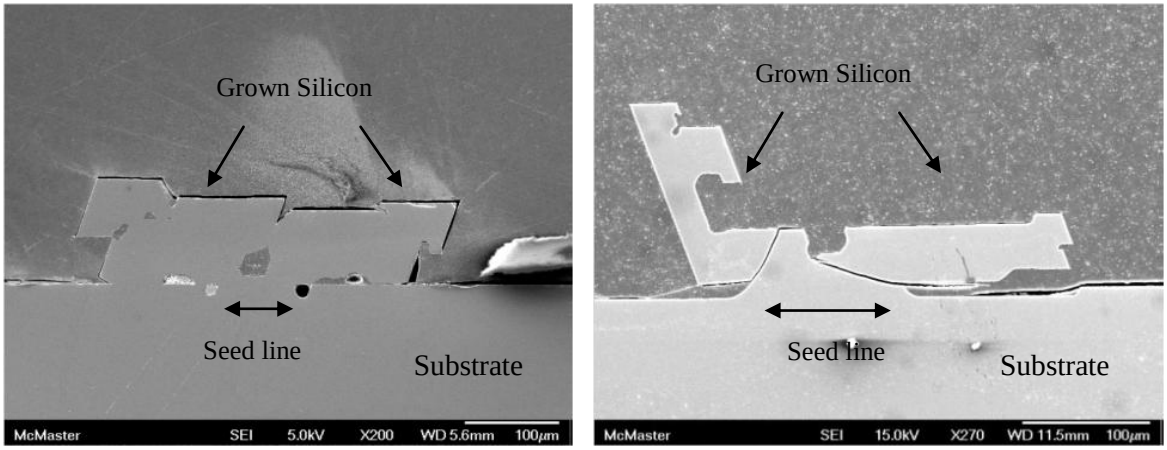


Figure 2.8 *Cross section SEM images of grown silicon strips by LDLPE method.*

LDLPE was designed based on the horizontal slider boat LPE, and as a result a narrow gap in between the seed lines and oxide plate will create a void, and later become hydrogen bubbles when immersing the seedline and oxide plate into the growth solution. The largest concern in LDLPE is the wetting issue in between the substrate seed line and the oxide plate. A pre-wetting technique is capable of overcoming the wetting issue in LDLPE however, the reproducibility is low. The hydrogen bubbles on the substrates create blocking layer to prevent silicon deposition uniformly and therefore the formation of ledges/kinks is favored to minimize the overall surface energy to encounter the pre-existing hydrogen bubbles.

2.4 Growth Kinetics

2.4.1 Surface segregation

In conventional *CZ* or *FZ* growth, silicon melts contain multiple phases with various impurities. In the molten solution growth, the impurities in the grown solid differ from that in growth solution. The crystal pulling process is a progressive freezing of the melt at a specific region. The solidifying region is also referred to as the liquid-solid interface. During the solidification in pulling the seed crystal, the impurity concentration at the growth interface is different in the grown solid silicon. The distribution of the concentration is due to the segregation effect. The impurity will progressively accumulate at the interface and the distribution is depending on the segregation coefficient or distribution coefficient, K_0. The equilibrium segregation coefficient can be calculated based on the thermodynamic parameters

$$\ln K_0 = \frac{\Delta H^f - \Delta H^s}{RT} + \frac{\sigma - \Delta S^f}{R} + \ln \gamma$$

where ΔH^f is the heat of the fusion between the melting point of the impurity and that of the host crystal, ΔH^s is the differential heat of solution of the impurity in the host solid, ΔS^f is the entropy of fusion of impurity at its melting point, σ is the change in vibrational entropy of the impurities as the result of changing its own lattice to that of the host crystal, and γ is an activity coefficient.

The impurity concentration distribution during crystal growth in CZ is highly dependent on segregation coefficient. A distance versus concentration profile can be plotted as shown in ***Figure 2.9***, whereas δ is representing the infinite closed region between the solid and liquid interface. ***Table 2*** shows the segregation coefficient at the melting point of silicon with respect to different impurities.

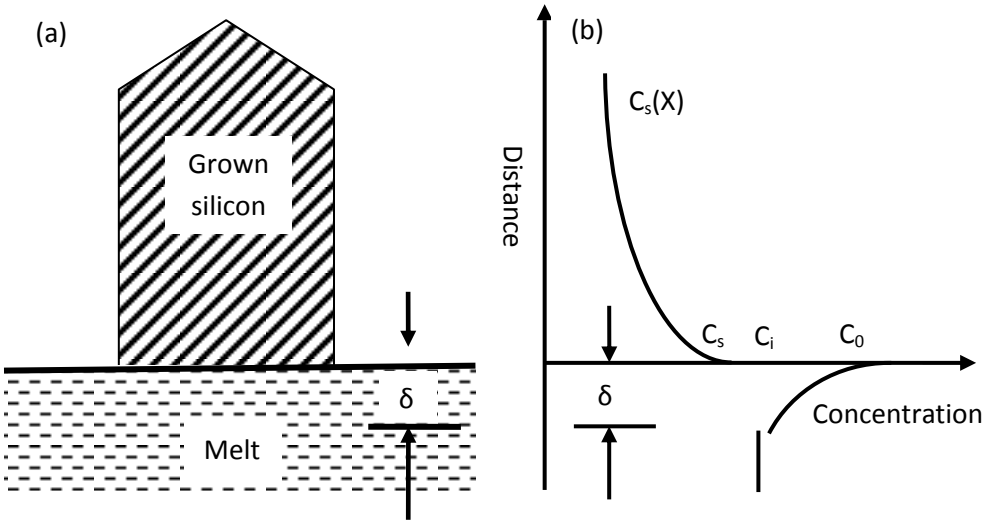


Figure 2.9 *(a)The schematic diagram of the solid-liquid interface in CZ crystal growth; (b)The concentration profile of the impurities along the crystal growth axis [8]*

	Iron	*Oxygen*	*Aluminum*	*Gallium*	*Indium/ copper*	*Germanium*	*Nitrogen*	*Phosphorus*	*Boron*
K_0	$8x10^{-6}$	0.5	0.0020	0.0080	$4x10^{-4}$	0.33	$< 10^{-7}$	0.35	0.80

Table 2 *Segregation coefficient of common impurities in silicon refining process*

The segregation effect can achieve purification of the impurities. Consider a binary phase diagram shown in ***Figure 2.10***, when the A-Si alloy is cooled from the liquid state to solid state at T_1, the composition of A is uniform in the alloy. As the temperature is lowered to T_2, solid phase starts to form and the composition of the solid formed silicon based by the intersection of a horizontal constant temperature line with the solidus line at Asi. As the temperature is lowered to T_3, more solid silicon forms. The compositions of solid and liquid change in the solid-liquid region, and the solid silicon contains less percentage amount of A. when the material is all solid at T_4, the solid equilibrium composition becomes the same as it started from in the liquid form(A_0). The last solid forming has composition A_{Lf}, and the difference between the first formed solid and last liquid to solidify is referred to as "coring" in cast metal parts.

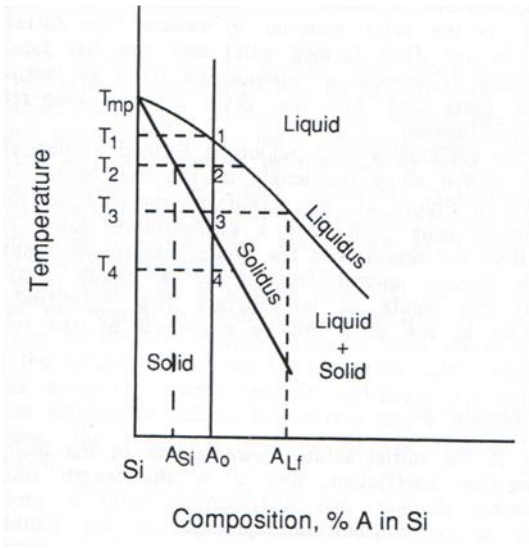


Figure 2.10 *Binary phase diagram of composition % A in Silicon during cooling process [8]*

A simplified float zone refining model can be viewed as a bar of uniform composition, C_0, which is heated to melt at one end and a molten zone travels along the length. The impurity concentration is lower at the

beginning of the rod compared to the end of the rod. The concentration of the impurity in the solid phase can be expressed as a function of segregation coefficient (k) and solidification length (g) [8] [27]:

$$C = kC_0(1-g)^{k-1}$$

The transport of impurities from melt to grown silicon involves a diffusion process through the boundary layer and solid-liquid interface and adsorption and migration on the crystal surface to incorporate lowest surface energy sites. In most case the diffusion process is a rate limiting step due to surface adsorption and migration occurs instantaneously at the melting temperature.

2.4.2 Density effect in growth solution

Epitaxial growth of silicon using liquid phase epitaxy has been studied extensively. The mass transportation in the growth solution is based on the diffusion, surface reactions, and effect of gravity. The effect of gravity or density effect plays an important role in solution growth because the growth solution usually contains multiple components. In the binary system of In-Si for example, the concentration distribution of silicon atoms varies along a vertical axis, and it is due to the atomic weight differences between silicon and indium. The density of silicon is 2.33 $g \cdot cm^{-3}$, whereas that of indium is 7.31 $g \cdot cm^{-3}$. The effect of gravity on mass transport was studied by T. Sukegawa et al [28], and ***Figure 2.11*** is a proposed sandwich model to study the effect of density. The top and

bottom substrates are silicon wafers, and in between is the indium solution. The dissolution of the lower substrate when increasing the temperature was found to be higher than the upper substrate. The saturation or supersaturation increase with the height in the solution under isothermal conditions.

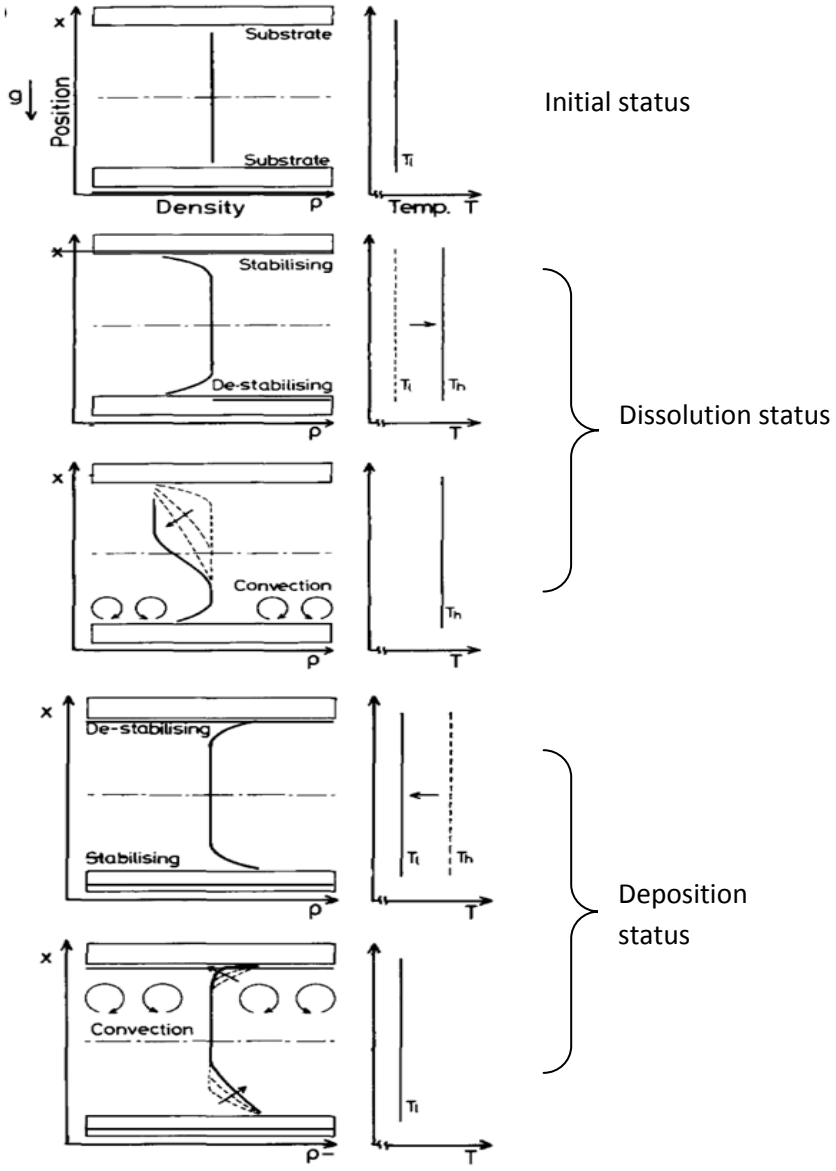


Figure 2.11 *The horizontal sandwich model. The change of solute density with respect to vertical distance during dissolution and deposition phase [29] [28]*

Growth at a constant cooling rate is also studied based on the same model shown in ***Figure 2.11***. The density changes in the vertical axis during growth. In the first figure, there is no concentration gradient along the growth solution. As the temperature is lowered at a constant rate, deposition occurs on both substrates. A free convection near the upper interface is observed. The convection is caused by the solute depletion near the interface, and lighter silicon atoms tend to stay at the upper part of the growth solution. The convection can accelerate the mass transport from the growth solution to the interface. The growth rate on the lower substrate due to a higher density of indium atoms is lower. The difference in densities results in solute depletion at different zones of the solution. It becomes critical to not only consider diffusion and surface reaction during the crystal growth but also the density effect in a binary system [28] [29] [30].

A two-dimensional numerical simulation for the dissolution and deposition of silicon in indium solute was discussed by A. Coskun et al [31]. The result shows the contribution of concentration gradient to natural convection during dissolution of silicon in indium solution with a sandwich structure of substrate-solution-substrate. The simulated result shown in ***Figure 2.12*** indicates the dissolution rate in the lower substrate is higher. The density effect phenomenon is also analyzed by M. Saitou et al [32]. based on perturbation theory, or a model for the abrupt change in

the growth rate during solution growth in LPE system of silicon. In the solute field shown in ***Figure 2.11***, an instability caused by the density effect can be determined by the nondimensional parameters GrScδc/δy., where Gr is the Grashof number, Sc is the Schmit number, and δc denotes concentration in the perturbed state [33] [31] [32] [34] [35] [36].

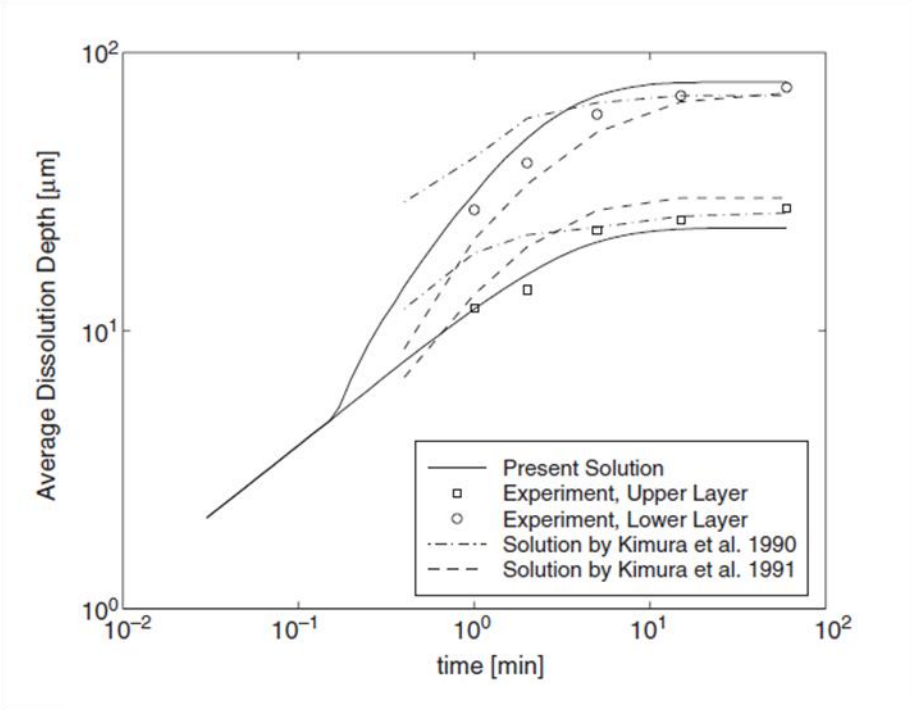


Figure 2.12 *Dissolution depth as function of time. The experimental value agrees with the model where the lower substrate is more susceptible to dissolution [31].*

The effects of density are widely applied in modern steel making processes, such as blast furnace (BF), basic oxygen furnace (BOF) and electric arc furnace (EAF). In a blast furnace iron oxide and impurities reduced by coke forming iron with slag. Liquid slag comprising such as CaS, SiO_2, Al_2O_3, MgO or CaO float on top of the liquid iron since the density is lower. In a basic oxygen furnace, pure oxygen is used as the fuel

and reactant to remove excessive carbon, silicon, magnesium, and phosphor forming CO, CO_2, SiO_2. MnO, and P_2O_5 slag. The liquid slag is again lower in density compared with liquid iron melt and floats on the top surface. In an electric arc furnace, steel scrap is heated and melted by the arc, which is created by electric current. The slag is forming in addition to lime, which is used to reduce impurities from the molten steel. The slag again has a lower density than the purer molten steel; therefore, liquid slag stays on top of the bath.

A density effect also plays an important role in deep ocean currents. A difference in ocean water density is caused by variations in salinity and temperature. Saltier water is denser than less salty water; cold water is denser than hot water. The movement of deep ocean water is driven by the density difference and gravity. At higher latitude near the north/south pole, the ocean density is higher due to lower temperature, and the water tends to sink to the bottom. As the deep ocean waters near the base at north/south pole reach salinity saturation and start to precipitate salt, the deep ocean water will get pushed away toward the equator by the newly saturated ocean water. The ocean density near the equator is lower due to the warmer climate. The lighter ocean near the equator replenishes the "fresh" water toward north/south pole to create the deep ocean current. ***Figure 2.13****(a)* is the simplified cross section model for the deep ocean current flow, and Figure ***2.13****(b)* shows the relationship between density and temperature based on latitude.

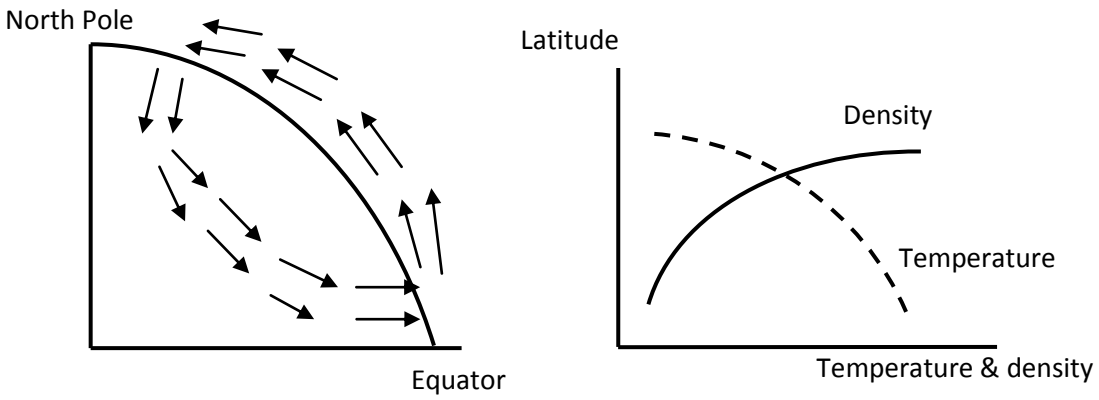


Figure 2.13 *Density effect on deep ocean current: (a) The schematic diagram of deep ocean current flow; (b) The ocean water temperature and density distribution as function of latitude*

3. Experimental Procedures and Equipments

The theory of Vapour-Liquid Interface Growth (VLIG) is based on liquid phase epitaxy and *CZ* growth methods. In this chapter the approaches, experimental setup, and procedures will be discussed in detail.

3.1 Approaches

Traditional single crystalline silicon wafer processes include: crystal growth, slicing, flattening, etching, polishing and cleaning. The objective of the Vapour-Liquid Interface Growth (VLIG) method is to grow single crystal silicon wafer or sheet as a self-supported substrate with uniform thickness under a low temperature process. ***Figure 3.1*** is the approach and the goal is to combine the crystal growth and the several finishing processes into a single process.

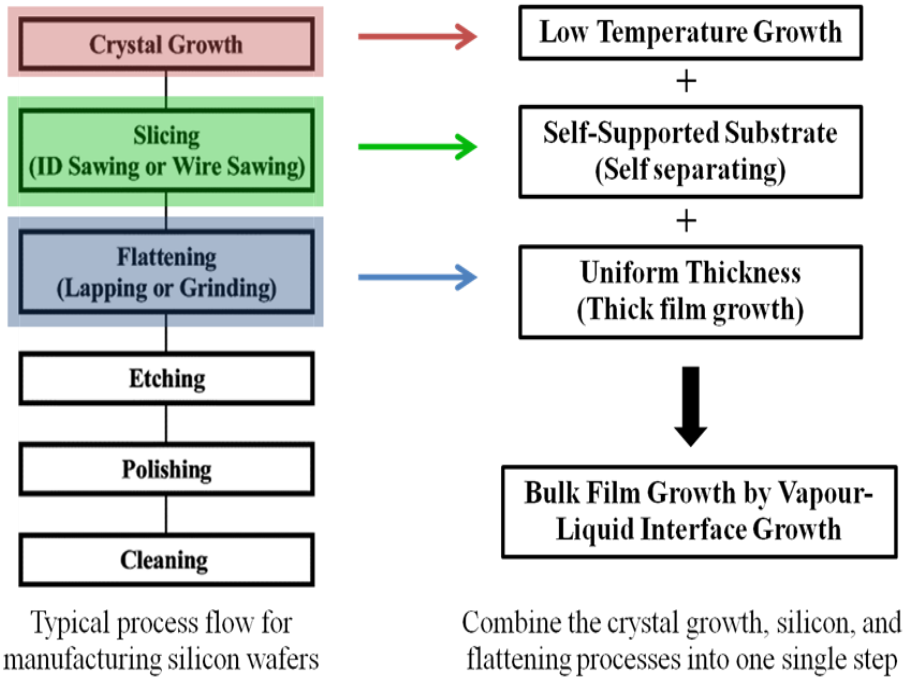


Figure 3.1 *The conceptual process to approach a more energy and cost efficient process based on VLIG*

The concept of VLIG is utilizing a solution growth method to grow a thin sheet layer of single crystal silicon with smooth surface finish. Two growth mechanisms, surface segregation and density effect were discussed in Chapter 2, section 4. VLIG system consists of three major parts: horizontal tube furnace, vacuum/purge system, graphite slider boat compounds. VLIG is utilizing high segregation tendency of silicon in the indium melt and the concentration distribution along the solution height due to density effect to achieve epitaxial lateral growth.

3.2 Experimental setup

The VLIG system is structured with a compound graphite slider boat and a 3 zone quartz horizontal tube furnace shown in ***Figure 3.2***. The 3-zone quartz

tube is able to control the temperature up to 1200^{o}C, and to keep the growth environment isothermal throughout the tube furnace; a three zone horizontal tube furnace is applied to create a homogenous temperature profile along the graphite boat, and the horizontal design allows the graphite boat to fit with a pulling rod design. The vacuum system contains mechanical pump and diffusion pump. The base pressure is in the range of 10^{-6} Torr. The purge gas system consists of a platinum membrane hydrogen purifier (Johnson Matthey HP-50) to provide eight-9s ultra high purity hydrogen purge gas. Purified hydrogen is used to react with excess air in the tube to improve the purity during the growth, and also prevent oxidation during growth.

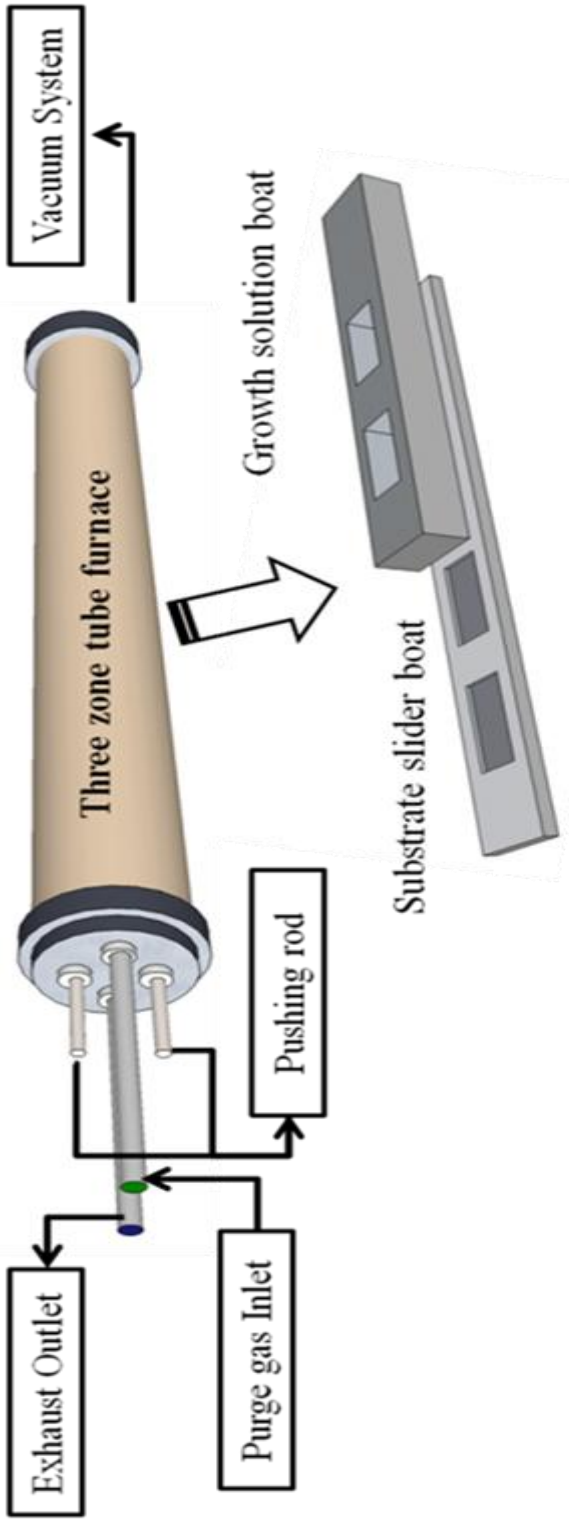


Figure 3.2 *The schematic layout of the 3-zone horizontal tube furnace and graphite boat components.*

The graphite slider boat is machined from high purity pyrolytic graphite. The graphite boat has a growth solution container part and substrate holder part.

The functions of the graphite boat are to contain the growth solution and to position the substrate with the lower slider boat and terminate growth by pulling the substrate away from the growth solution.

The growth solution we used in this particular system for growing single crystal silicon is pure indium with six-9s purity level. The solid indium dissolves silicon at temperature of 950℃ to achieve a supersaturation. A graphite crucible is used to melt and recycle the used indium solution. During the melting process, silicon flakes and indium oxides slag are floating at the melt surface and later are tabbed off from the melt surface in nitrogen rich inert atmosphere.

The main feature of the VLIG design is the preparation of the substrate containing the seed line. The substrate contains two parts: 1) silicon oxide layer; 2) seed line of single crystalline silicon. The substrate patterning is prepared by lithography. A seed line is exposed on a substrate with a width of 100 μm with a (211) orientation shown in ***Figure 3.3*** and the main function of the seed line is to create a nucleation site during the growth. The grown silicon from the seed line will possesses the same crystal orientation as the seed line crystal structure. These substrates are cut from n-type (111) oriented single crystal silicon wafer to a size of 12mm x 3mm by dicing saw; the corners of the substrate are trimmed to have rounded corners by sand paper. The plates with 12mm x20mm are cut from the same wafer. The setup of the substrate and plate is shown in ***Figure 3.4***.

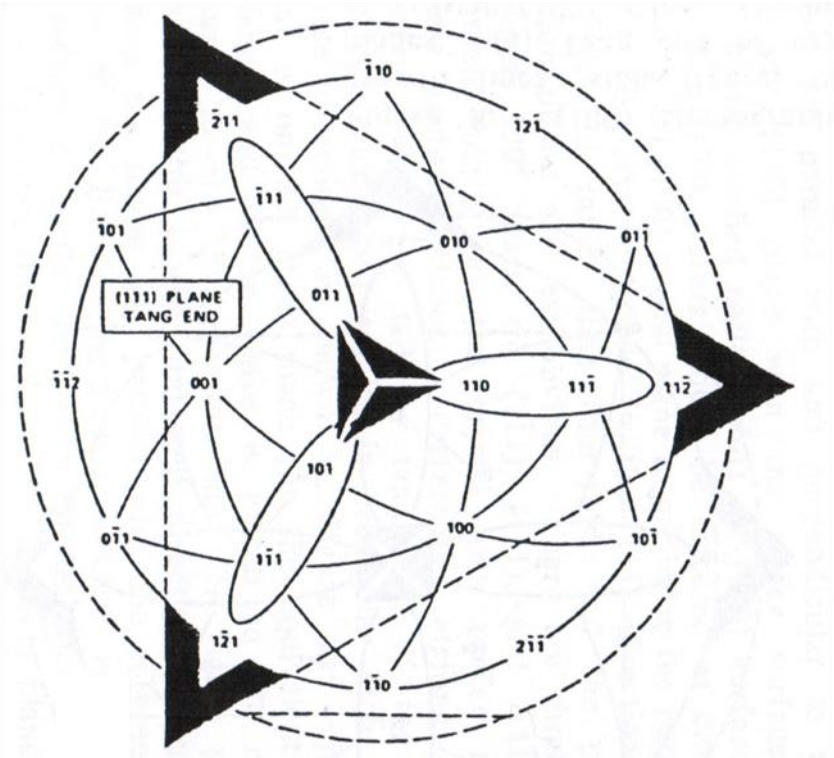


Figure 3.3 *(111) projection with superimposed growth line. Figure from D. O. Townley, "Optimum crystallographic Orientation for silicon Devices Fabrication." Solid State Technology 16:43-47, 1973*

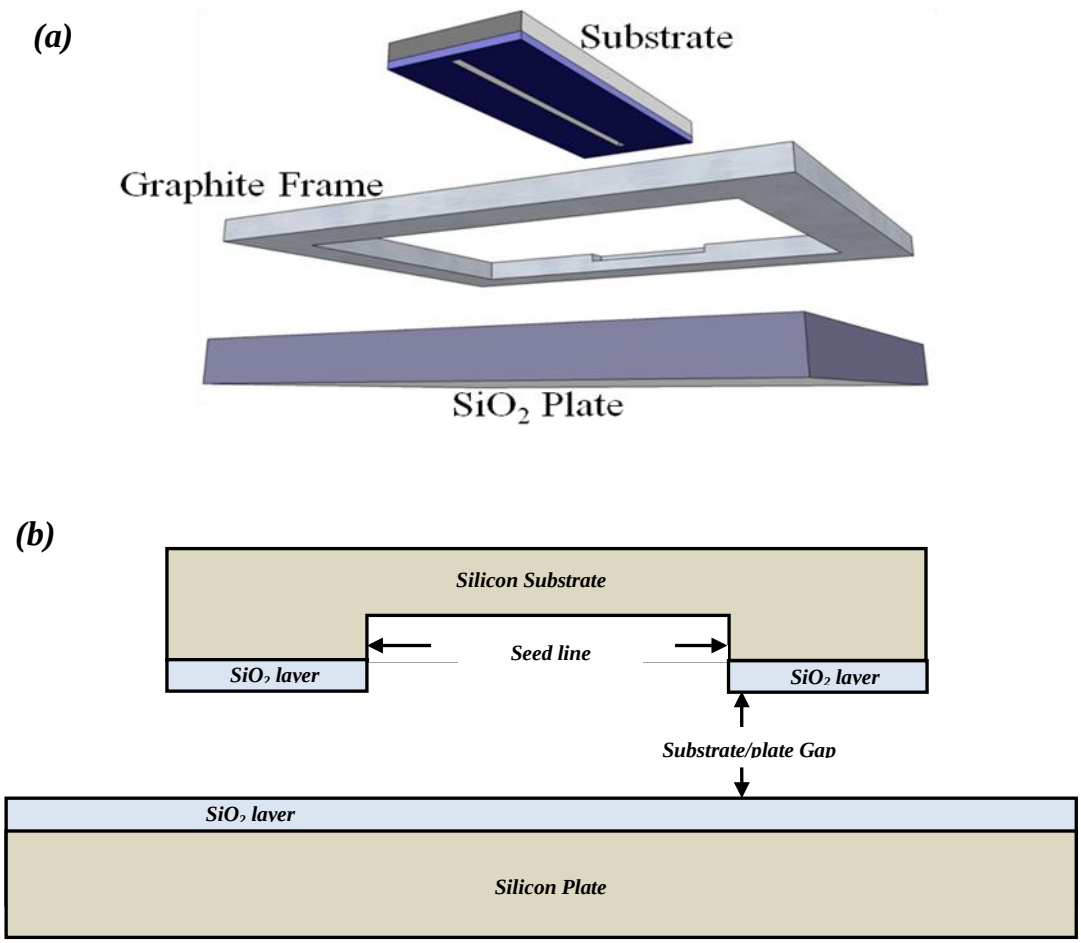


Figure 3.4 *The setup of n-type (111) silicon substrate with seed line of 100μm facing downward to the plate. (a) The substrate/plate gap is held by a graphite frame, and the gap can be 0.5mm or 0.25mm; (b) The cross-section view. The figure is not in scale, and the substrate/plate gap is one of the operating parameters.*

Another feature of this design is the presence of a silicon dioxide-coated silicon plate facing the seed line substrate. The melt thickness is determined by the separation between the substrate containing the seed line and the silicon dioxide-coated silicon plate. The seed line position in this new design is facing downward as shown in ***Figure 3.4 (a)***. The compound structure contains 3 parts: the substrate with seed line feature, graphite frame to set a certain distance

between the substrate containing the seed line and the silicon dioxide-coated silicon plate. The gap between the substrate and oxide plate is part of the operating parameter, and in VLIG growth is 0.5mm.

Experiments have been done in our systems and have shown that further reducing the gap will aggressively affect the diffusion limit during the growth. In other words, the silicon atoms in the growth solution have increasingly limited diffusion towards the growth seed line as the gap is reduced below 0.5mm, and spontaneous homo-nucleation is observed as a result on the growth solution surface. The gap may, however, be increased beyond 0.5mm. This will allow for more diffusion of silicon in the melt which will increase the thickness of the silicon plate being grown.

In addition, the melt may not fully wet both the substrate containing the seed line and the silicon dioxide-coated silicon plate. This problem can be solved by applying a small amount of growth solution in between the seed line and the silicon dioxide-coated oxide plate before the growth process starts. The pre-wetting method was found to reduce bubbles incorporated in the melt during the growth, and ensure a continuous liquid layer to provide a diffusion path for the remaining silicon atoms in the growth solution.

The characterization tools to determine the crystal quality are Scanning electron microscope (SEM: JEOL 7000F/6600), X-ray diffraction (XRD: Bruker D8 advance, with copper Kα of 0.154 nm radiation), and Hall Effect measurements (HMS-3000 system).

Table 2 is the list of the operating parameters in VLIG system and the summary of the operating selections and regions.

Operating parameters	***Operating region/selections***
Solvent	*Indium*
Substrate	*Single crystal silicon (111) orientation*
Growth temperature	*975 ~ 850^{o}C*
Cooling rate	*0.25 ^{o}C /min*
Seedline width	*100μm*
Substrate/plate gap	*0.5 mm*
Vacuum condition	*~ 10^{-6} Torr*
Purge gas	*Hydrogen*
Seed line orientation	*Facing downward oriented*

Table 3.1 *VLIG operating parameters and selections.*

3.2.1 Solvent selection

The solvent can directly affect the electrical properties of the grown silicon sheet, and also it has a large impact on growth temperature, growth mode, and cost. A good solvent should have 1) low melting point; 2) large silicon solubility; 3) good wetting on the substrate; 4) chemical stability with graphite boat; 5) high purity; 6) low cost. Indium was selected based on the low melting point (156.6^{o}C), good wetting with silicon substrate and feasible electrical properties from literature value shown in ***Table 3.2.***

Metal solvent & growth temp.(^oC)	***Doping concentration (cm^{-3})***	***Resistivity (ohm-cm)***	***Carrier mobility ($cm^{-2}V^{-1}S^{-1}$)***	***Reference***
Al (750)	*10^{19}*	*N/A*	*N/A*	*Ito. K et al. 1980*
Cu (950)	*$<10^{18}$*	*N/A*	*N/A*	*T.F. Ciszek et al. 1993*
Ga (600)	*10^{18}*	*0.42*	*70*	*Y. Satoh et al. 2005*
$Ga_{0.7}Al_{0.3}$ (500-900)	*$1.4x10^{18}$*	*0.03*	*150*	*B. Girault et al. 1977*
In (920)	*10^{16}*		*90-260*	*R. Kopecek et al. 2000*
In (946)	*$1.8x10^{16}$*	*2.17*	*285*	*W. Scott et al. 1979*
In (1056)	*$1.2x10^{17}$*	*1.3*	*275*	*--*
In (1250)	*$1.6x10^{16}$*	*0.25*	*206*	*--*
In (900-1200)	*10^{17}-10^{18}*		*N/A*	*--*

Table 3.2 *The electrical properties of grown silicon from liquid phase epitaxy (LPE)*

3.2.2 Growth temperature selection

The growth temperature also plays an important role on tuning the electrical properties as shown in previous ***Table 3.2***. From a growth mechanism perspective, higher growth temperature (>900^{o}C) yields higher crystallinity with faster growth rate and lower impurity level, however, it greatly increases the chance to thermally degrade the substrate and crucible. There are several advantages of using lower growth temperature (~600^{o}C) including less thermal degradation, steady doping level and less

energy consumption; although, the crystallinity quality is poor at low growth temperature and it usually yield polycrystalline structure.. In VLIG, in order to improve the crystal quality and lower the purity level, a higher growth temperature ranging from 975 to 850^{o}C is applied.

3.3 Experimental Procedure

VLIG procedure is divided into several steps from 1) wafer preparation; 2) slider boat preparation; 3) growth process. ***Figure 3.5*** is the growth process flow chart.

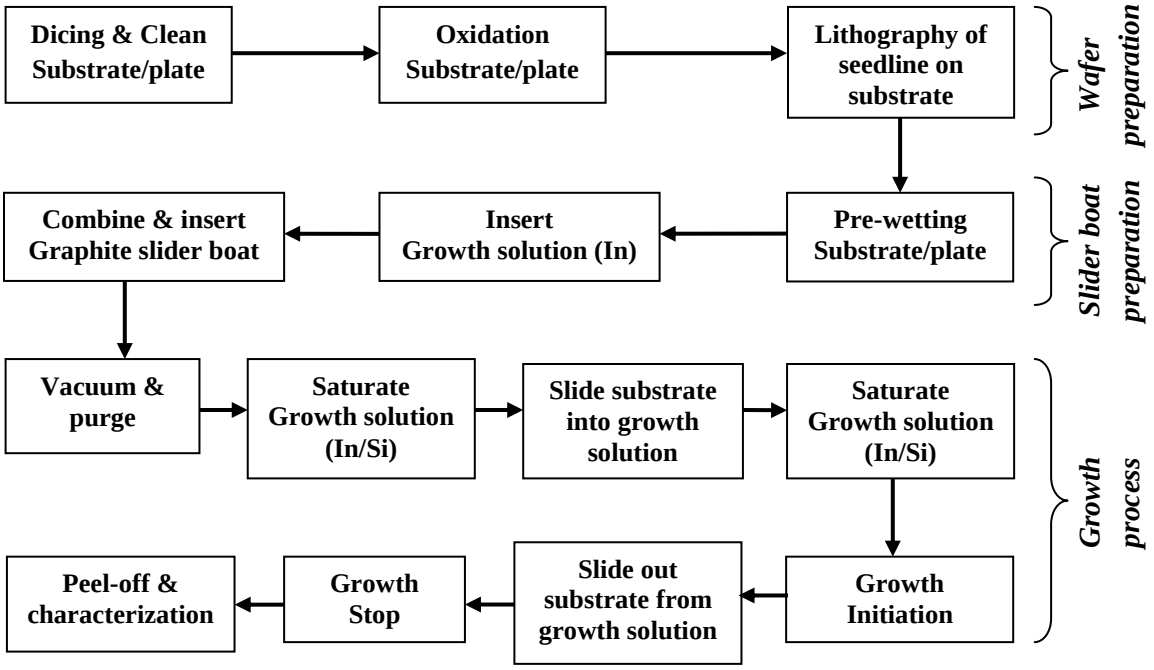


Figure 3.5 *The basic growth process for VLIG consists of three parts: wafer preparation, slider boat combination and growth process.*

In wafer preparation, the goal is to make the source wafer, pattern the substrate, and oxidize the plate. The source silicon wafer is used in making

growth solution, and it has the same dimension as the oxide plate. The only difference between the source wafer and oxide plate is the existence of the oxide layer. The following is the step-by-step experimental procedure for ***wafer preparation***:

- Rectangular substrate with dimensions of 12mm by 3mm and plate with dimension of 20mm x 12mm are cut from n-type (111) single crystal silicon wafer.
- The corners of the plate are rounded using sand paper.
- Substrate and plate are cleaned by
    1) Acetone and methanol in ultrasonic cleaner respectively for 10 minutes, and risen with deionized water;
    2) Sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) of ratio 2 to 1 for 10 minutes under gentle boiled condition (~95^oC), and risen in deionized water;
    3) Hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) with ration 2 to 1 for 10 minutes under gentle boiled (~95^oC), and clean with deionized water;
    4) Buffered Hydrofluoric acid (HF) solution dip for 20seconds to remove the oxide layers, and risen in deionized water;
    5) Dry the surface with pure nitrogen gas.
- Place the substrate and plate into horizontal quartz tube furnace. Silicon dioxide layer growth by dry oxidation in a quartz tube furnace for 3 hours with pure oxygen supply at 1200^oC to reach oxide layer around 400nm.

- Seed line pattern is fabricated by photolithography methods as following:
  1) Photoresist (Model:S1808) film coat by spin coater with 3000rpm for 30seconds. The film thickness ends up around 0.8 μm;
  2) Soft bake the substrate for 1minute and 20seconds at 90^{o}C to harden the polymeric film;
  3) Cover the substrate with patterned nickel mask, and exposed under UV light (model: ENTELA:B 100AP) for 40 seconds;
  4) Remove the pattern using developer (model: 351) for 60 seconds, and clean with deionized water;
  5) Hard bake for 5 minutes to remove the water;
  6) Etch patterned seed line using buffered hydrofluoric acid (HF) for 6 minutes; risen the substrate with deionized water and dry with pure nitrogen gas.

In the graphite slider boat preparation, the goal is to assemble the compound substrate and growth solution components into the slider boat for VLIG. The detail graphite slider boat design and peel-off technique are in Appendix I. The following lists the detailed procedures for ***slider boat preparation***:

- Place the graphite substrate holder on a heater with temperature around 150^{o}C;
- Place the oxide plate on the holder, and place the graphite frame with gap 0.5mm on top of the plate.
- Apply pure indium shot in the middle of the oxide plate; when melt, insert the seed line patterned substrate on to the plate-frame-indium structure.

- Press gentle on the substrate compound structure and lower the temperature to solidify indium melt. The structure should be as shown in ***Figure 3.3***;
- Place the compound substrate, and source wafer into the graphite substrate slider boat, and assemble the growth solution holder;
- Melt indium ingot in graphite crucible and tap into the growth solution slots in the graphite boat, and make sure the indium melt is directly contact with source wafers.

In the growth process, the goal is first to saturate the indium growth solution with silicon by dissolving the silicon source wafer at high temperature and secondly, to achieve bulk silicon film growth from supersaturated silicon-indium melts. The following procedures describe the ***growth process*** in detail:

- Open the JP-50 hydrogen purifier to pre-heat the purifier at 400^{o}C, and the temperature reach 400^{o}C, open hydrogen valve to storage purified hydrogen.
- Place the compound graphite boat in the middle of the furnace and seal the horizontal tube.
- Evacuate the horizontal tube furnace with mechanical pump to 10^{-3} Torr and followed by diffusion pump to 10^{-6} Torr to ensure minimum contamination during growth.
- Close the gate valve of diffusion pump and open up the hydrogen inlet valve to make the growth environment hydrogen-rich. The flow rate of the hydrogen is around 8 standard litres per minute (slpm).
- Setup the saturation temperature to 950^{o}C and hold for at least 6 hours to ensure the growth solution is saturated with silicon.

- Slide the substrate compound structure into the In-Si melt, and increase the temperature to 975^{o}C and hold for 1hour.
- Decrease the temperature from 975 to 850^{o}C at a constant cooling rate of 0.25^{o}C/min.
- Slide the substrate away from the growth solution when the temperature reaches 850^{o}C to terminate the growth.
- Cool the furnace to room temperature naturally. When the temperature reaches around 300^{o}C close the hydrogen inlet.
- Carefully remove the graphite slider boat and separate the substrate and holder.
- Clean the growth solution slot by tap off the oxide indium layer.
- Clean the residual indium melt on the substrate by using hydrochloric acid (HCl), and risen with deionized water.
- Separate the grown silicon sheet on the substrate by peel-off technique:
    1) Apply heat resist plastic film (~50µm Mylar^{TM} polyester film) around the silicon sheet, and leave the silicon sheet uncovered.
    2) Heat the substrate to the melting point of crystal bound (~90 ^{o}C)
    3) Apply and emerge the crystal bound on the exposed grown silicon surface, and apply a glass slider onto the molten crystal bound as a carrier.
    4) Decrease the temperature to room temperature, and ensure the crystal bound full solidifies.
    5) Mechanically peel off the glass slider to remove the grown silicon from substrate.
    6) Clean the sample with acetone, and risen with deionized water.

4. Experimental Results and Discussion

Silicon wafers are often thicker that desired. For example in high speed computing the ability to increase the density and minimize signal paths between semiconductor chips is an on-going issue. Being able to place more silicon circuitry in a smaller volume could be enabled by using thinner silicon wafers grown from our process that can be stacked above each other like a multi-storey building. A form of three dimensional circuitry is therefore enabled. In addition due to the reduction in steps in a traditional wafer preparation process the cost of the VLIG material could be favourable for a wide range of silicon substrate preparation for microelectronics, solar cells and light detectors.

The current technology for production of thin sheets of single crystal silicon is done by a cutting and slicing process. The dicing process is performed using a dicing saw which has a limitation to cut wafer thinner than 100µm. The wafering process is not cost effective as it creates over 50% material loss when wafering thin wafers.

Our invented VLIG process can directly grow high quality single crystalline silicon from a re-useable substrate and the wafer can be easily peeled off from the substrate. We are seeing silicon substrates with smooth surfaces directly as grown by VLIG.

This chapter presents the growth of single crystalline silicon sheet by VLIG and also presents a different effect in the design parameters such as substrate-plate gap distance and seed line orientation.

4.1 Single crystal silicon by VLIG

In order to quantitatively identify the single crystal strip geometry and quality, an aspect ratio (width: thickness) is determined for each growth. In a previous LDLPE method, Bo Li et al. reported a growth aspect ratio of 2, whereas in conventional Liquid Phase Epitaxy (LPE) growth, the aspect ratio can only reach to 1. ***Figure 4.1(a)*** is the setup of the LDLPE, and the seed line is oriented upward. The growth parameters were kept the same with VLIG except the seed line orientation, and the result is shown in ***Figure 4.1(b)***. The surface of the grown silicon by LDLPE does not have a smooth layer, and the growth front shows various ledges and kinks. The grown silicon platelets are limited to a width of 200µm using LDLPE.

In VLIG growth, the seed line orientation is facing downward to utilize the density effect in the mixture of silicon and indium solution. ***Figure 4.2*** is one of the VLIG growth result. In ***Figure 4.2(a)***, the average VLIG silicon width is 400µm. ***Figure 4.2(c)*** shows the cross section corresponds to ***Figure 4.2(b)***, and the thickness of the silicon is around between 100 and 80 µm. The aspect ratio (width/thickness) for this particular region is 2.3.

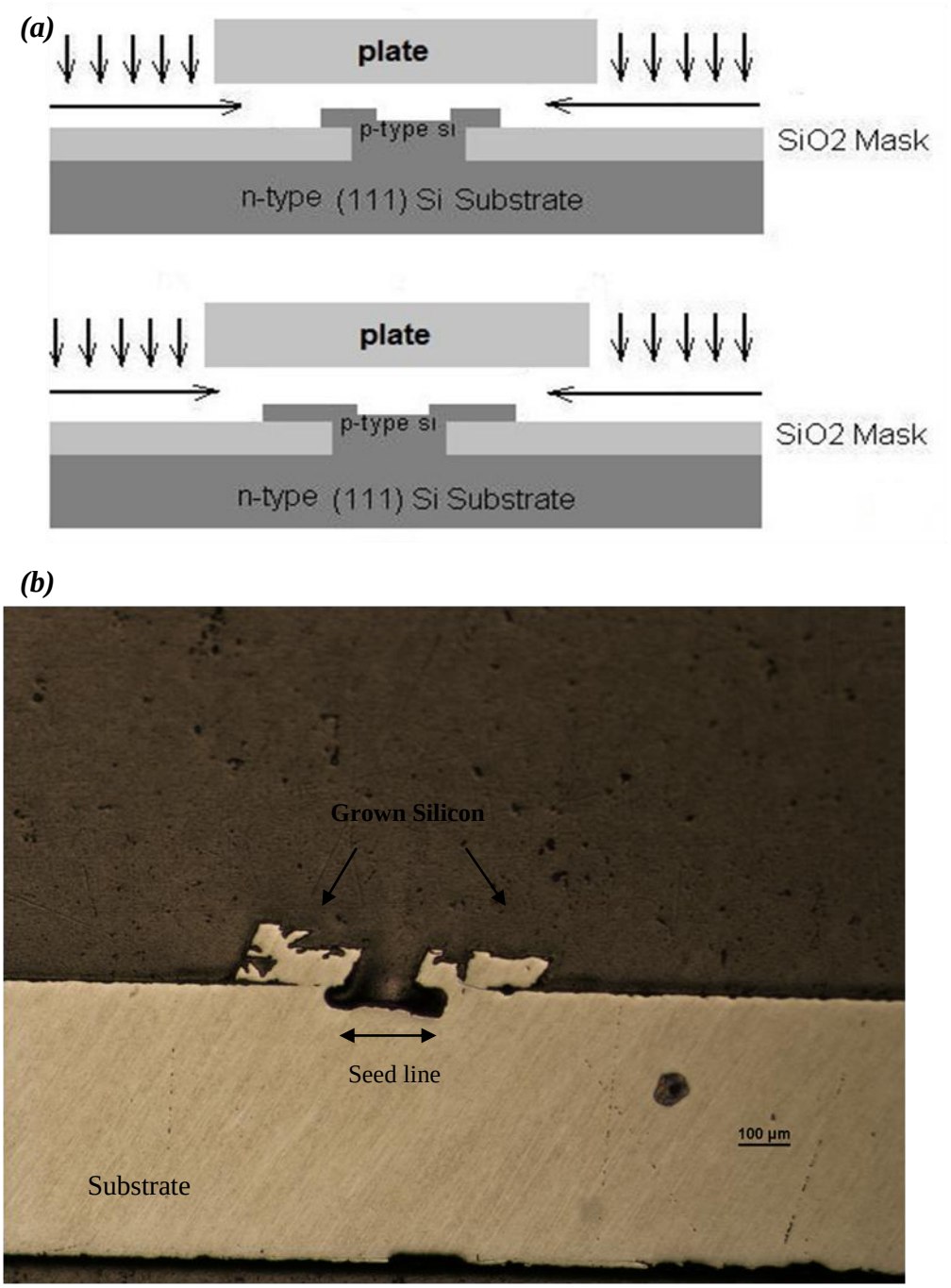


Figure 4.1 *LDLPE growth setup and result. (a) The growth setup of seed line facing upward oriented growth from Bo Li et al. 2011; (b) The cross section view under optical microscope.*

Figure 4.3 is another result from VLIG. The aspect ratio in that region is 33. Compared to LDLPE growth the improvement is about 15 times. It is also worth noting that the surface morphology in ***Figure 4.3(c)*** shows a very flat and smooth growth profile. The wide white coloured gap in ***Figure 4.3(b)*** between the grown silicon sheet and the substrate containing the seed line is about 50µm. This wide gap allows us to easily peel the silicon sheet from the substrate containing the seed line; also the grown silicon is only attached to the seed line area which is 100µm in width. The thickness of our grown single crystal silicon strip is uniform and is about 35 µm in thickness. Preparation of this thin plate of single crystalline silicon is inefficient to wafer using conventional slicing or dicing processes. The silicon surface grown by VLIG has less edges or kinks; thus it requires less polishing or grinding to achieve an atomically smooth surface. The average width for the sample in ***Figure 4.3*** is estimated to be about 650µm, and the widest part is about 1000µm.

In the plain view of ***Figure 4.3(a)***, we observed a mechanical tear off in the middle part of the silicon strip. The tear off phenomenon is related with the completion between the crystal growth void growth in between the substrate and grown silicon. The mechanical rupture and crack development will be discussed in section 4.5.

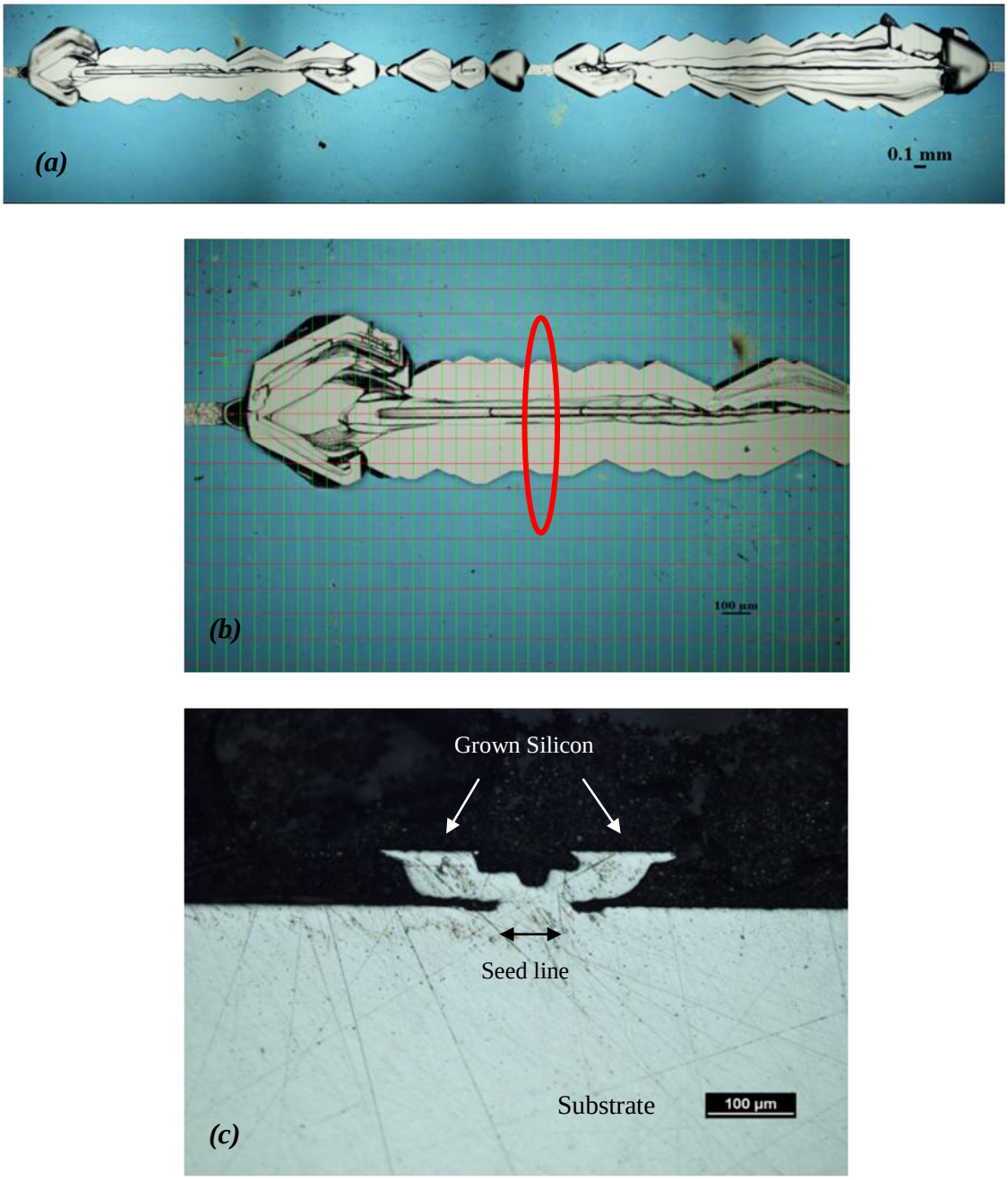


Figure 4.2 *Sample 1 plain view and cross section view under optical microscope. (a) the plain view of silicon platelet grown by VLIG system; (b) the closer view of the platelet, and the selected area corresponds to the cross section view; (c) the cross section view of the platelet.*

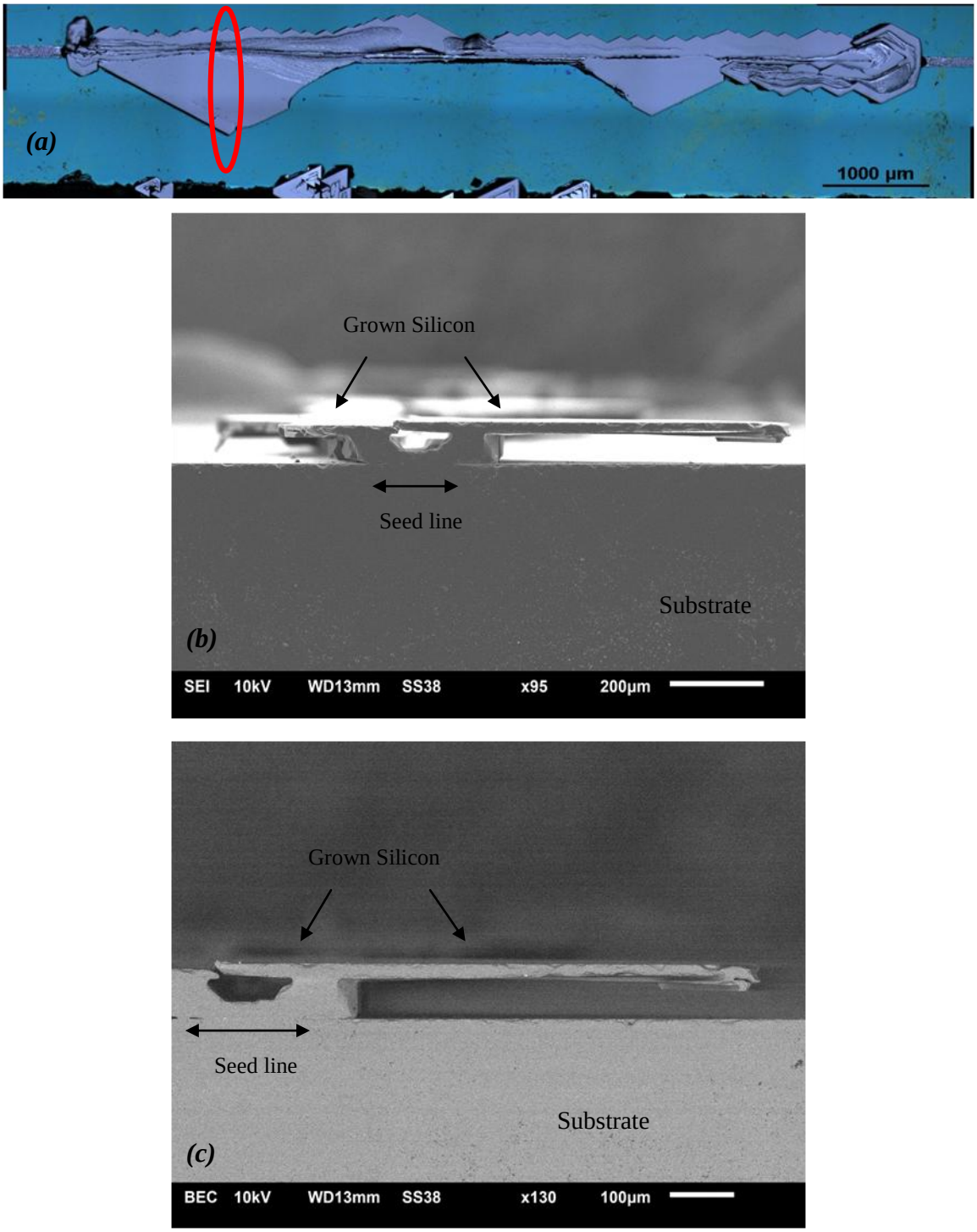


Figure 4.3 *Sample 2, plain view and cross section view under optical microscope, and SEM. (a) the plain view of silicon platelet grown by VLIG system; (b) The cross section view corresponds to the selected area in (a) under SEM of secondary electron image; (c) the cross section view of the platelet with compositional view from backscattered electron image.*

4.2 X-ray crystallography

We undertook a further investigation on the crystal structure of our grown silicon strip to determine whether it is single crystal or poly crystalline silicon. In order to obtain an accurate measurement, peeled silicon strips were used to run the X-ray diffraction patterning. Fig. 4.4 (a) shows the two theta scan of our sample form 25° to 70° to identify the different orientation in our crystal. Only one peak of 28.44° is observed, shown in Fig. 4.4(a), which is corresponding to a (111) silicon peak; this indicates that our silicon strip is a single crystalline silicon. Fig. 4.4(b) shows the rocking curve of the same sample, and the full width at half maximum (FWHM) of the sample is 0.043°, with a very evenly distributed shoulder of the curve. The sharp and symmetrical curve with a tall narrow peak indicate high crystallinity and the structures are periodic and in phase. If the crystal is more randomly arranged or having a low degree of crystallinity, the result will be peak broadening.

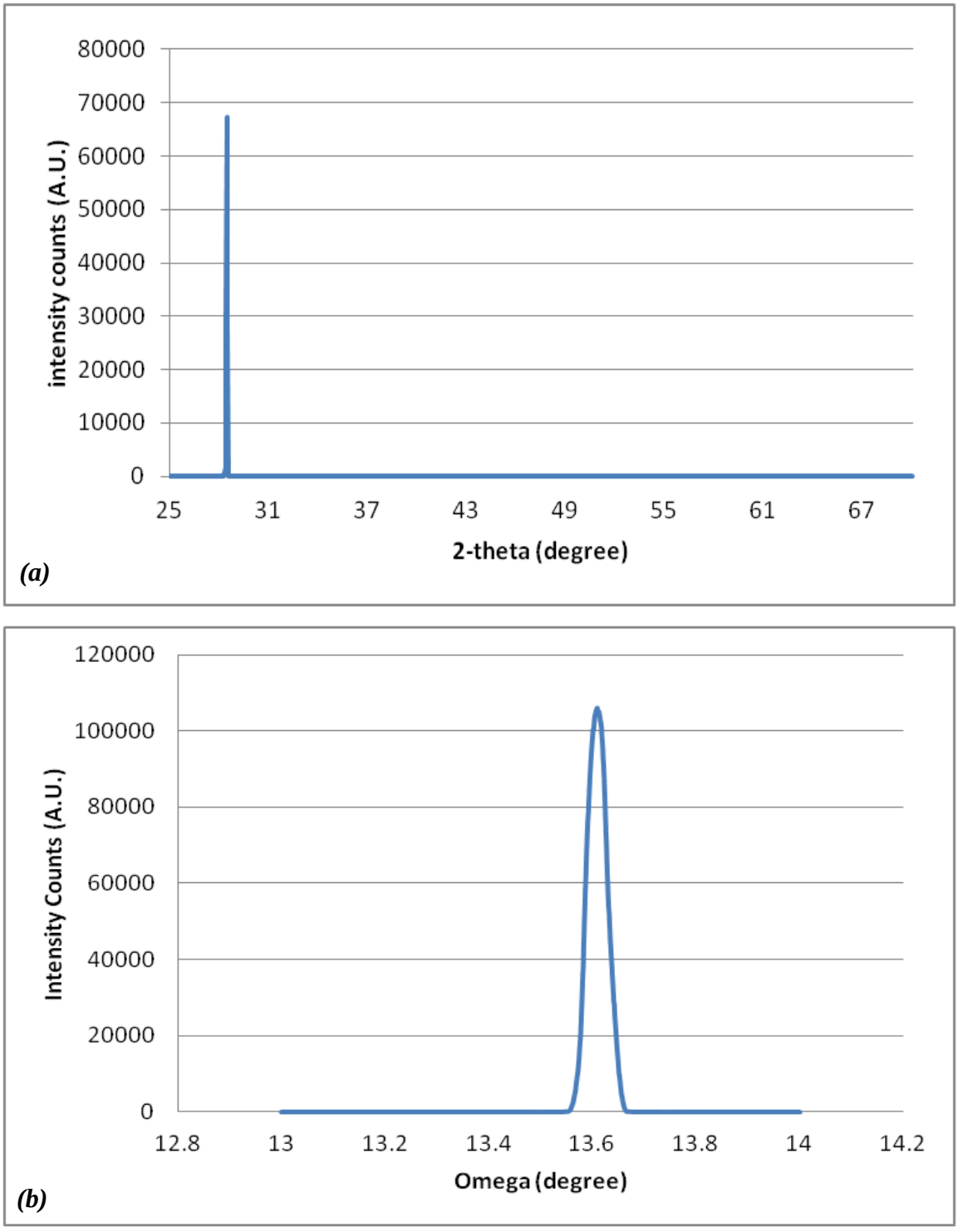


Figure 4.4 *X-ray diffraction results: (a) XRD patter of 2-theta scan for the peeled off silicon sample; (b) XRD rocking curve results of (111) orientated peeled off silicon sample.*

4.3 Electrical properties

Silicon grown by VLIG is naturally doped with indium, resulting in a p-type doping. Basic electrical properties can be determined using Hall Effect measurement. In order to perform Hall Effect measurement, silicon samples with square shapes are carefully selected from the growth melt which has identical structural and chemical composition compared with the grown silicon sheet. Aluminium contacts were deposited at the edge of the sample using electron-beam evaporation system and annealed at 700^{o}C for 5 minutes to achieve ohmic contact. The Hall Effect measurement was done using HMS-3000 system at room temperature. The measured result shows the resistivity is 4.181x10^{-3} ohm-cm, and the hole concentration is around 5.3x10^{18} /cm^{3}. The measured hole mobility is ranging from 282 cm^{2}/V·s.

4.4 Effect of substrate-plate gap distance

The substrate-plate gap distance plays an important role on limiting the vertical growth, resulting in a higher aspect ratio. However, smaller gap distance strongly limited the growth rate and resulted in narrow silicon sheet. ***Figure 4.5*** is the cross section view of the grown silicon sheet with substrate-plate gap of 0.25 mm. Other parameters were kept all the same during the growth except the gap. As shown by the narrow geometry result, the diffusion mechanism was limited not only in the vertical direction but also in the lateral direction. The structure of the seed line is broadened due to heavy etching back effect where the indium

solution from pre-wetting process could not diffuse away from the seed line, thus dissolving aggressively at the seed line. The grown silicon can only reach up to around 100µm in width despite the resulting aspect ratio being about 2.

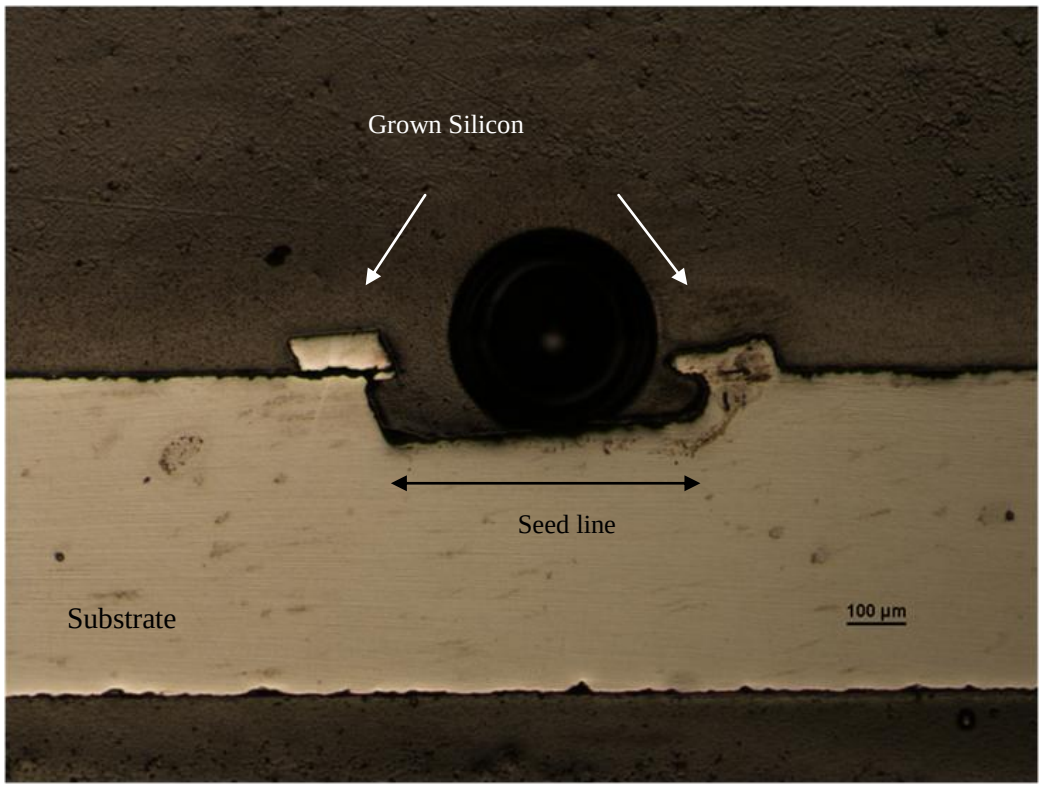


Figure 4.5 *VLIG growth with substrate-plate gap distance of 0.25mm. The seed line experienced severe etching back during the growth process. The aspect ratio in the 1/4mm setup is around 2. The width of the grown silicon is limited to about 100µm. The black circle in the middle is the void from cured epoxy.*

4.5 Growth Mode

The crystal growth mode in VLIG system is based on three effects: 1) effect of diffusion limited silicon supply due to geometry; 2) Density effect due to mixed solution of In-Si melt; 3) enhanced growth in the substrate surface. ***Figure 4.6(a)*** shows the simple model that explains the diffusion path for silicon atoms

during growth. Silicon atoms first diffuse from the side toward the middle seed line. Due to the geometry factor, the diffusion path is limited in the vertical direction. Density effect plays an important role during the growth. Consider the growth solution formed by two different atoms: indium and silicon atoms. The density effect implies the heavier atoms are more likely staying at the bottom of the solution and the lighter atoms are floating on top of the solution. The density of silicon is 2.33 $g{\cdot}cm^{-3}$, where the indium density is 7.31$g{\cdot}cm^{-3}$ at room temperature. Therefore, under isothermal condition the growth of silicon mainly occurs at the upper layer of the growth solution, and it also make the diffusion path more viable when we position the seed line at the upper surface of the solution layer. As the silicon deposits on the seed line and starts to grow laterally, small bubbles, generally hydrogen bubbles pre-exist on the oxide surface which can interrupt the diffusion path and as a result push back the silicon atoms away from the oxide layer surface. Coalescence bubbles are pure hydrogen and have been trapped due to surface tension of the oxide layer. The existence of the hydrogen bubbles creates a balance force between the growth solution and grown silicon during the super cooling process; in addition wetting of the silicon dioxide is not energetically favourable due to the tiny gap (50μm), as the growth of silicon increases laterally a negative pressure will build in the coalesced hydrogen bubble. If the forces induced by negative pressure in the void are higher than the mechanical strength of the grown silicon, it is very likely to introduce a crack along the growth front and lead to a tear-off situation. The simulated grown silicon is shown in ***Figure 4.6(b)***.

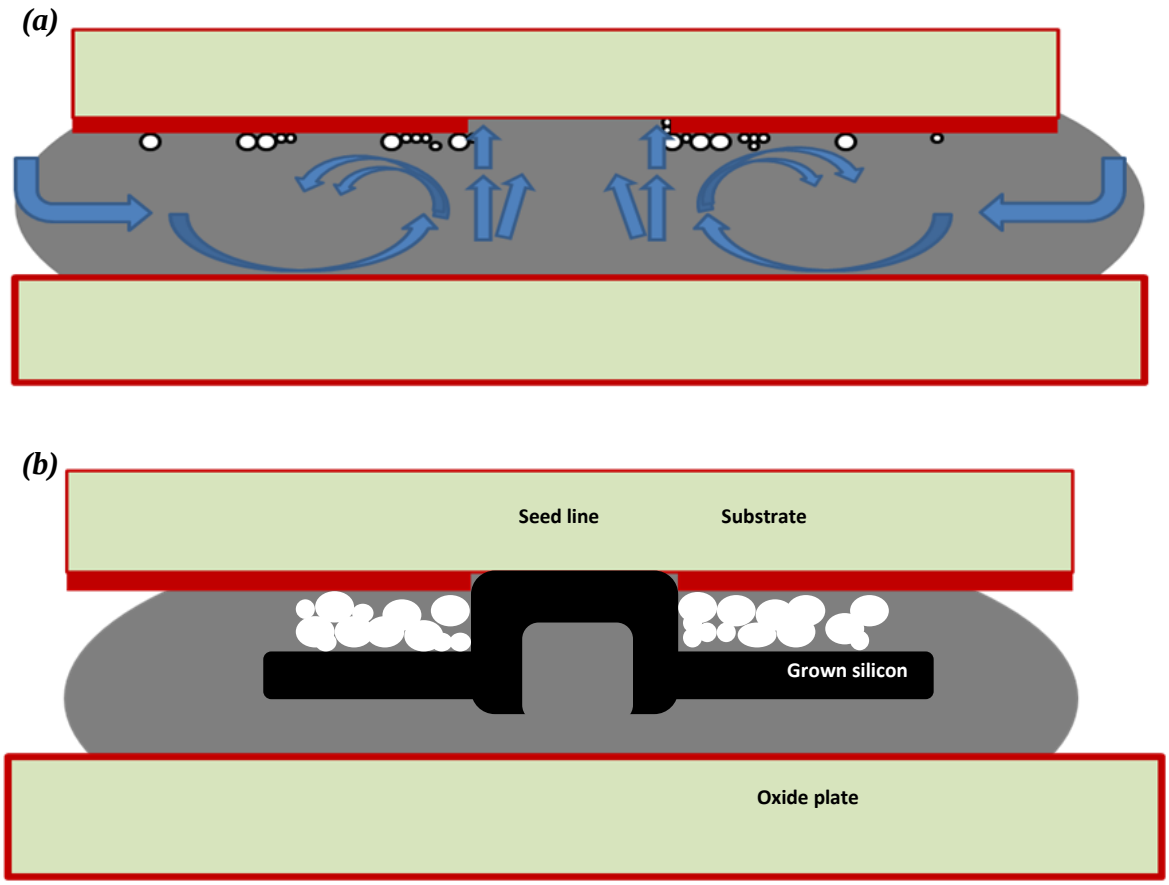


Figure 4.6 *The schematic diagram during the growth and growth result. (a)The arrows indicate the silicon atoms diffusion paths, and the deposition in the first stage occurs at the seed line site with perfect lattice match sites; (b) The silicon grows in the lateral direction due to the limited access in the vertical orientation. The trench formation at the middle part of the grown silicon is due to diffusion limited vertical growth as lateral growth proceeds. Hydrogen bubbles coalescence in create a void in between the grown silicon and substrate and create negative pressure during the overgrowth. The figure is not to scale.*

Due to the lack of an on-site monitoring system, it is very difficult to have direct evidence of the development of pre-existing hydrogen. The effect of the pre-existing bubble is shown in ***Figure 4.7***, where the vapour-liquid interface was fully eliminated during the pre-wetting and sliding process. There is no void in

between the grown silicon and oxide layer, and the topography on the surface is rough. Without the presence of the hydrogen vapour phase, silicon atoms are easily deposited near the oxide surface region; thus making the peel-off process impossible. The existence of the hydrogen bubbles enhances the lateral growth and also improves the surface finish.

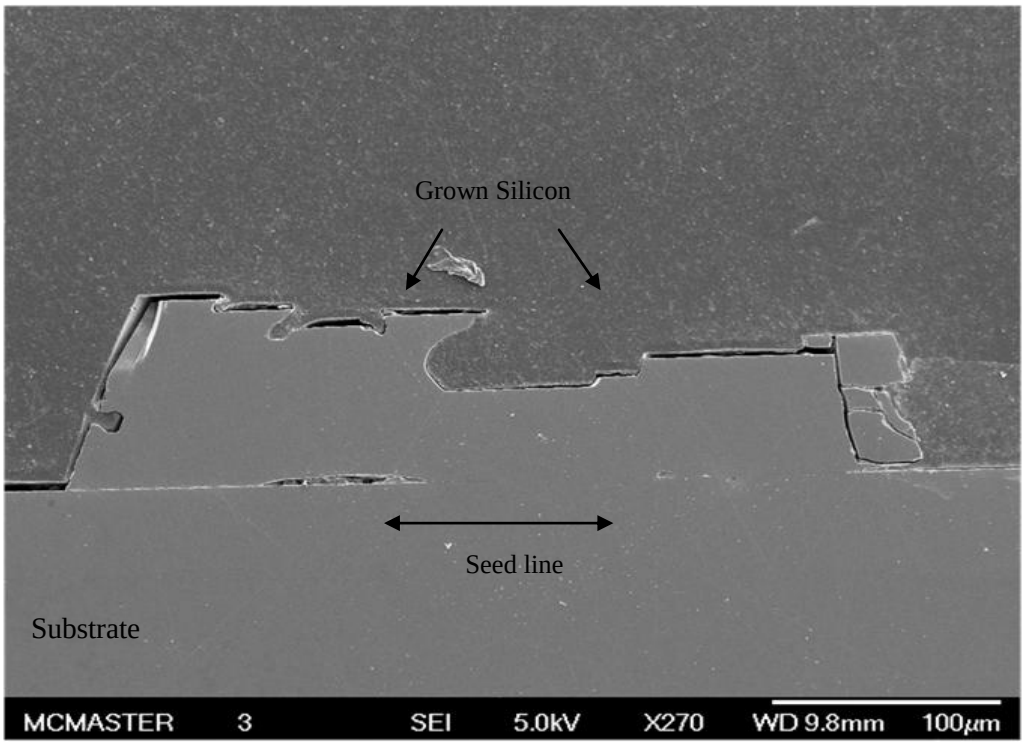


Figure 4.7 *Cross section view of VLIG growth under SEM. The substrate-plate gap distance is ½ mm, and in between the grown silicon and oxide substrate there is no sign of pre-existing hydrogen bubbles.*

VLIG samples also show step-bunching growth mechanism near the seed line region. ***Figure 4.8(a)*** is the step growth which consists of terrace and facet. The growth front is in parallel with the (111) oriented facet shown in ***Figure 4.8(b)***. The triangle facet has the minimum surface energy for the silicon atom to deposit and the structure is in (111) orientation. The step-bunching growth mode is favoured due to the substrate seed line region is 3^{o} off-cut. The small off-cut

provides micro steps which can improve the nucleation by increasing the nucleation site. At the beginning of the growth, mobile silicon atoms "transport" from the solute into nucleation site to reduce the total surface energy. Steps were built up due to concentration gradient along the lateral direction. The off-cut substrate does not affect the surface morphology.

Figure 4.9(a) shows the changing in chemical potential and silicon concentration in solute along the lateral direction. The silicon concentration in growth solution gradually decrease toward the seed line region because of the free silicon atoms are nucleate and deposit on the 3^{o} off-cut seed line. The total Gibbs free energy is reduced at the solid-liquid interface and the growth is controlled by diffusion at the growth front. The step-bunching surface is controlled by the surface process, and the surface energy is lower as it approaches to the growth front. ***Figure 4.9(b)*** is the schematic diagram of VLIG after a period of time, and the grown silicon growth front is away from the seed line region. The silicon concentration in the growth solution is high at the growth fronts and low in the grown silicon region. The change in Gibbs free energy is also higher at the growth front to reduce the total Gibbs free energy due to adsorption. Due to surface recombination and transportation, in the middle part of the grown silicon, the Gibbs free energy is slightly lower at the growth front. In addition, the silicon concentration in the growth solution at the middle part is lower since most free atoms are solidified and deposited at the nucleation sites.

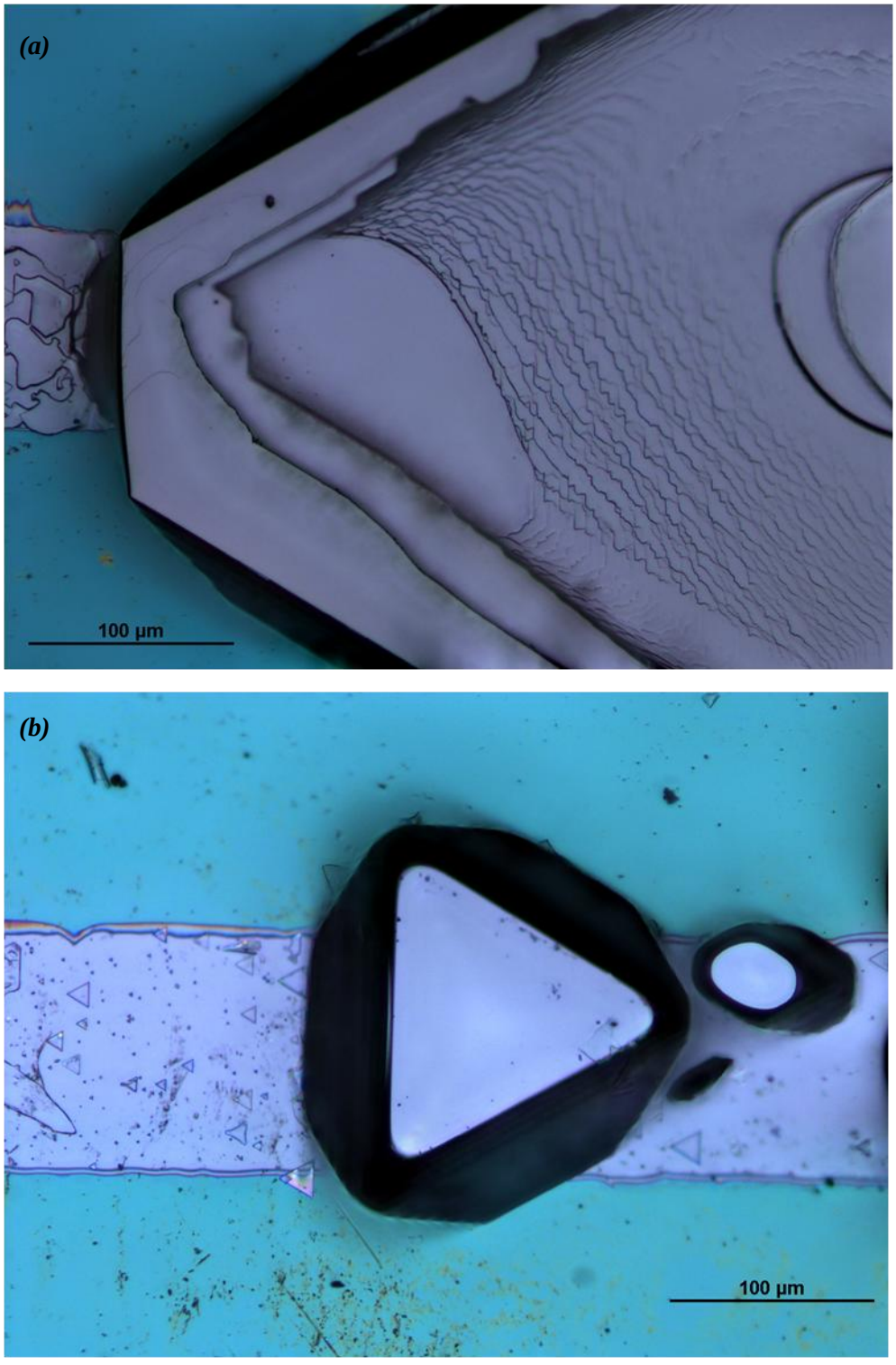


Figure 4.8 *The growth mode of the VLIG (a) Step-bunching growth; (b) Island growth at early stage for (111) facets.*

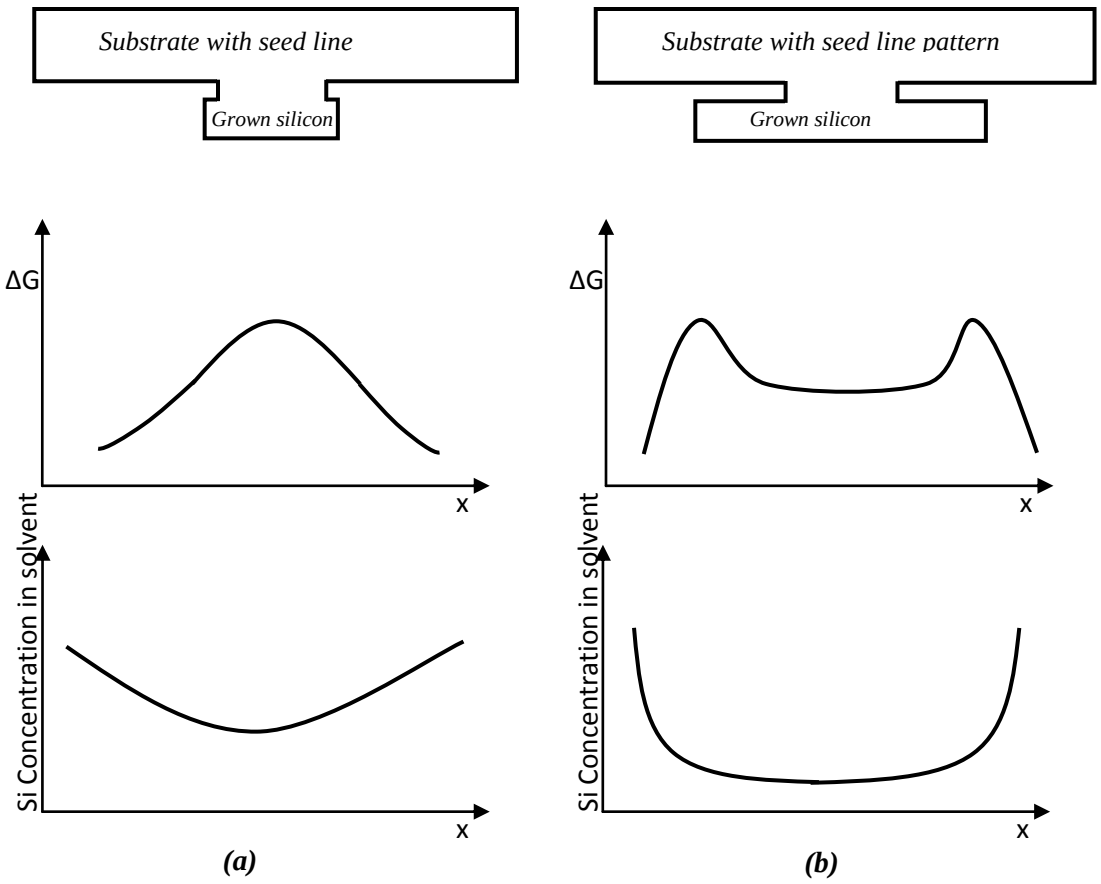


Figure 4.9 *The schematic diagram at the beginning of VLIG (a), and during growth, (b).*

Figure 4.10(a) is the top view of the cracked surface on the VLIG silicon sample. The formation of zigzag growth front is due to the growth rate competition between (111) and (211) direction. Growth rates highly dependent on the orientation. The growth rate in (211) direction in the aluminium-silicon binary phase was reported 15times higher compared to the (111) direction by P. Saidi et al. 2013. In the indium-silicon system, the zigzag growth fronts show both the interface mobility and growth velocity are functions of the orientation. The detailed relationship, however, requires more investigation based on a molecular dynamic model.

In ***Figure 4.10(b)*** is the fracture growth front corresponds to the lower part of the growth in ***Figure 4.10(a)***. The fracture surface is developed due to 1) built up negative pressure of the vapour phase in between grown silicon and substrate; 2) Vapour phase or hydrogen bubbles are not evenly distributed along the growth fronts. ***Figure 4.11*** is the schematic diagram of movement of the growth front and expansion of the vapour phase. To reduce the surface tension between hydrogen bubbles, the bubbles tend to coalescence and increase the total volume to reduce the overall surface energy. As the lateral growth increases, the vapour phase expands and is maintained as a narrow gap due to the diffusion limited effect in the narrow gap. Negative pressure builds up as the growth fronts move laterally. As a result, unbalanced forces are exerted on the grown silicon and cause the fracture. Cracks propagate along the void due to negative pressure.

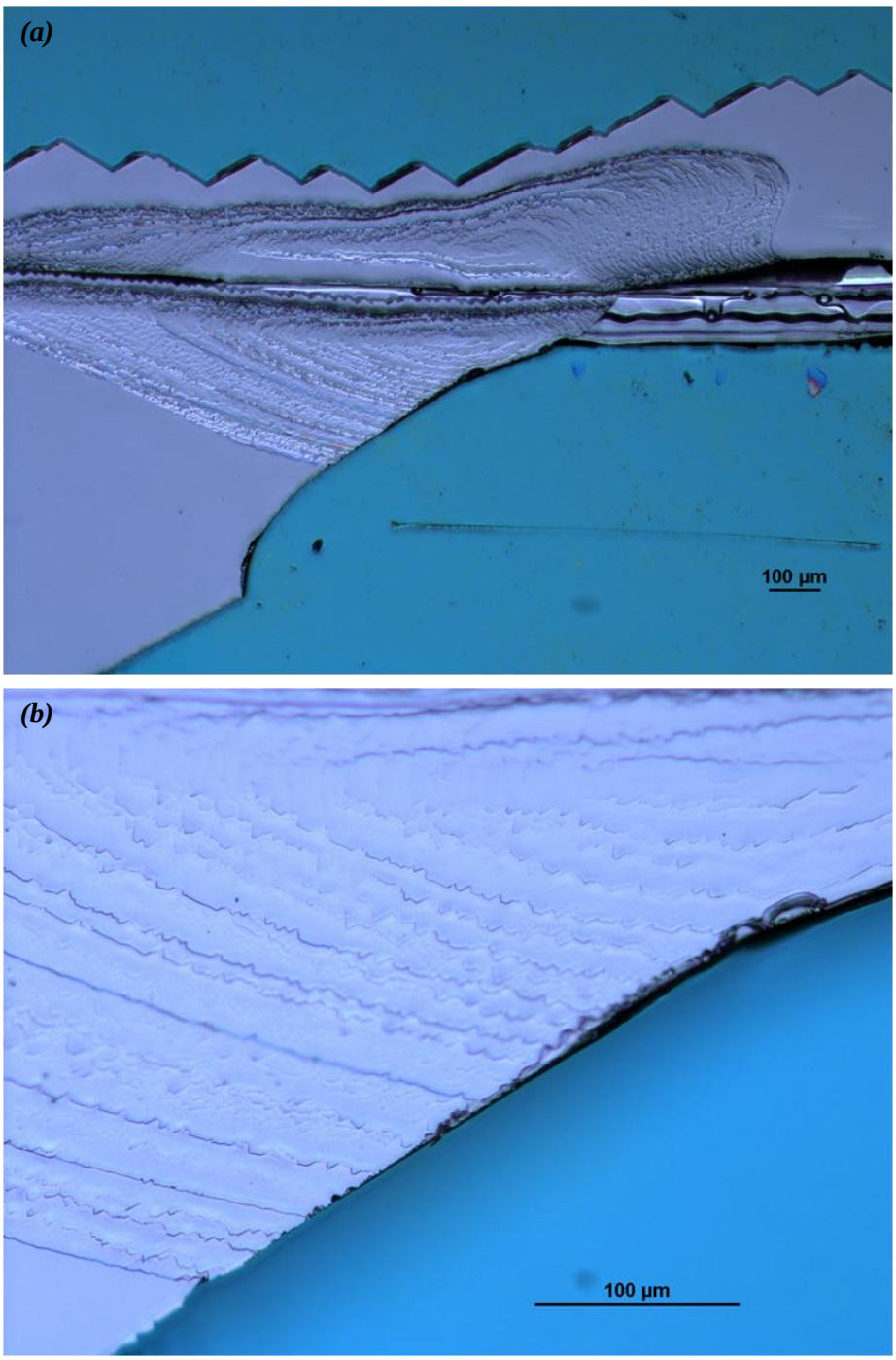


Figure 4.10 *Mechanical tear off on the interface between vapour and liquid phase. (a) The zigzag growth on the upper part of the silicon sheet is due to the competition between different growth fronts; (b) Crack developed in the interface between oxide substrate and grown silicon, and penetrates through the growth front due to built up negative pressure.*

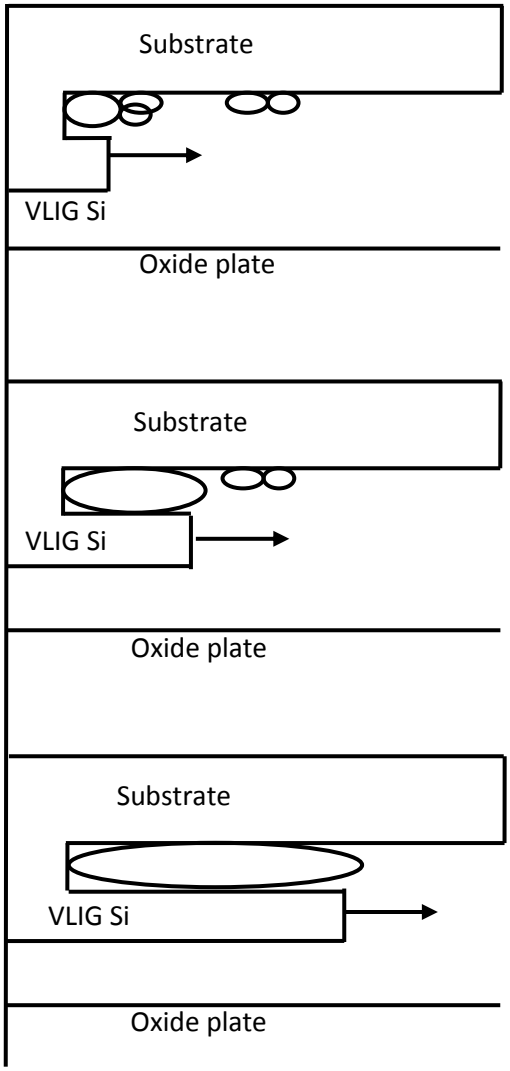


Figure 4.11 *The schematic diagram of the development of vapour phase during VLIG, and the black arrow is the growth direction. (a)The early stage of VLIG, where small bubbles are the pre-existing hydrogen bubbles due to wetting; (b)The void increase during the growth; (c) small bubbles coalescence and merge with larger bubbles to reduce surface tension. Negative pressure builds up as the void expand with insufficient supply of the vapour phase.*

5. Conclusion and Future Work

Current commercialized single crystal silicon wafers are made from Czochralski growth and float zone silicon boules. Preparing wafers is a tedious process that includes cutting and polishing. The minimum wafer thickness attainable in a high volume wafering process is generally 160 to 300 µm, and the kerf loss for wafering is up to 40% of the total volume. Thin silicon wafers (~30 to 100µm) are very expensive to produce and the wafering process is not cost effective due to the high amount of material loss during the process and the risk of breakage of the wafers during wafering.

Vapour-Liquid Interface Growth (VLIG) is capable of directly growing a sheet of single crystal silicon without wafering with thickness around 30 to 50µm. The features of the systems are 1) low temperature operation; 2) sheet is easily detachable and self-supporting; 3) sheet has uniform thickness and is single crystal. The system operates in a supersaturated growth solution of an indium- silicon melt. A seed line in a substrate facing down is employed. A layer of single crystal silicon grows on the seed line at the melt surface due to surface segregation during the super cooling process. The grown silicon can grow laterally due to the limited thickness of the melt depth that minimizes growth in the vertical growth direction. The grown silicon can be easily peeled off from the seed line substrate due to the presence of a gap between the grown silicon sheet and the oxide layer on the seed line substrate. The self-supporting silicon sheet now comprises a very thin silicon substrate or sheet.

The silicon sheet grown by VLIG is proved to be an epitaxial layer which is oriented (111) direction by XRD 2-theta scan. The quality of the single crystal has a

full width at half maximum (FWHM) of 0.043 from XRD rocking curve. The grown silicon sheet has highest aspect ratio of 33 with thickness of 35 μm and width over 1000 μm. VLIG silicon sheet is naturally doped with indium, which resulting in p-type doping. The doping level measured from Hall Effect measurements show a doping level of 5.3 $x10^{18}$ $/cm^3$, and the resistivity is around $4.181x10^{-3}$ ohm-cm.

VLIG is a new method for growing sheets of high quality single crystal semiconductor materials that we discovered and are currently pursuing. In order to have a more complete technology package this includes:

I. Mass production and contiguous growth plan

   Current VLIG chamber requires loading and refill the growth solution on each growth. A continuous growth process is needed to design for a more sustainable growth process. In addition to meet practical production volume, a scale up plan is need for the future work.

II. Preferred processing parameters

   In this thesis we reported the early stage of VLIG process. In order to optimize the growth rate and quality, the following are parameters that are highly related with the growth results i.e. aspect ratio:

Parameters	***Effects***
Melt thickness	Diffusion rate and plate thickness
Growth temperature range	Deposition/growth rate
Growth solution selection	Doping level/type
Seed line pattern/width	Geometry/aspect ratio
Void induce system to maintain positive pressure in between the grown semiconductor and seed line substrate	Surface smooth/defect free Crack-free growth
Substrate selection	p-n junctions

III. Explanation for the unique growth mechanism

Confirm the growth mechanism by doing cross sections and microscopy for a range of growth conditions including:

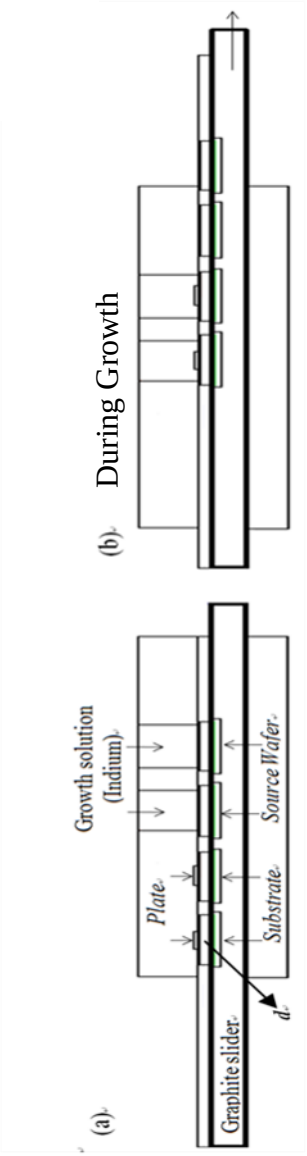
a) Partial growths to see evolution of the growth.

b) Series of saturation conditions to validate growth mechanism

c) Series of growth rates to validate growth mechanism

d) Modify seed-line to validate growth front formation

Appendix I: Graphite Boat Design Detail



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