NOISE CHARACTERIZATION AND MODELING OF MOSFETS FOR RF IC APPLICATIONS

By

CHIH-HUNG CHEN, B.A.Sc., M.A.Sc.

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ABSTRACT

This thesis develops a systematic and self-consistent framework for the RF noise characterization, modeling and simulation of deep sub-micron MOSFETs. The techniques and procedures developed in this thesis are general and can be applied to the high-frequency noise characterization of any active device. In general, there are five topics presented in this research work. First, a systematic calculation method that can directly calculate the noise parameters - minimum noise figure NF_{min}, equivalent noise resistance R_n, optimized source resistance R_{opt} and reactance X_{opt} - of an active device using matrix computation is presented. This method is general and can calculate the noise parameters of any noisy two-port network including correlated noise sources.

Second, a new de-embedding procedure based on a cascade configuration to remove the parasitic effects of the probe pads and the metal connections from the measured noise and s-parameters is developed. Two "THRU" dummy structures are proposed in the new de-embedding procedure and no equivalent circuit models for the probe pads and the interconnections are required. From theory, it has no frequency limitation (or it is valid to the frequency at which the discontinuity effect has to be taken into account) and works for any geometry of interconnection designed without introducing more dummy structures.

Third, two extraction methods to obtain the spectral densities of the channel noise, induced gate noise and their noise correlation from the intrinsic noise parameters as a function of frequency and bias condition are presented. The extracted noise spectral

densities of desired noise sources will serve as a direct target for the verification of any proposed noise model developed.

Fourth, new physics-based channel noise models to predict the channel noise, induced gate noise and their noise correlation are developed and verified with the extracted noise sources. The impact of the channel-length modulation (CLM) effect, the hot electron effect, and the velocity saturation effect on the desired noise sources in the deep sub-micron MOSFETs are discussed in detail.

Lastly, the design strategies of a low noise amplifier based on the developed noise models and extracted noise information are presented as a guide line to choose the device size and bias condition of the transistors. The impact of the model accuracy on the simulated noise performance of a two-stage low noise amplifier is also presented.

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Chapter 1

INTRODUCTION

1.1 NOISE

Noise is some unwanted fluctuation that, when added to a signal, reduces its information content. In a communication system, noise can be classified into two broad categories depending on its source -- internal noise and external noise. Noise generated by components within a communication system, such as resistors, electron tubes, and solid-state active devices is referred to as *internal noise* (or *electronic noise*). The second category, *external noise*, results from sources outside a communication system, including atmospheric, man-made and extraterrestrial sources. The "static" heard in a radio, the "snowy screen" of a television, and the fluctuation of a DC signal around its expected value are all examples of electronic noises, and this is the kind of noise of interest to us in this research.

Electronic noise in a communication system defines the lowest limit of a signal that can be detected. Fig. 1.1 shows the output power versus input power characteristics of a realistic amplifier with a gain of 10 dB. It is shown that if the power of any input signal is smaller than the noise floor of the amplifier, the signal would be "drowned out" by the background noise generated within the amplifier. Therefore, electronic noise directly

affects the accuracy of measurements and the minimum power of a signal that can be used in a circuit to transmit information.

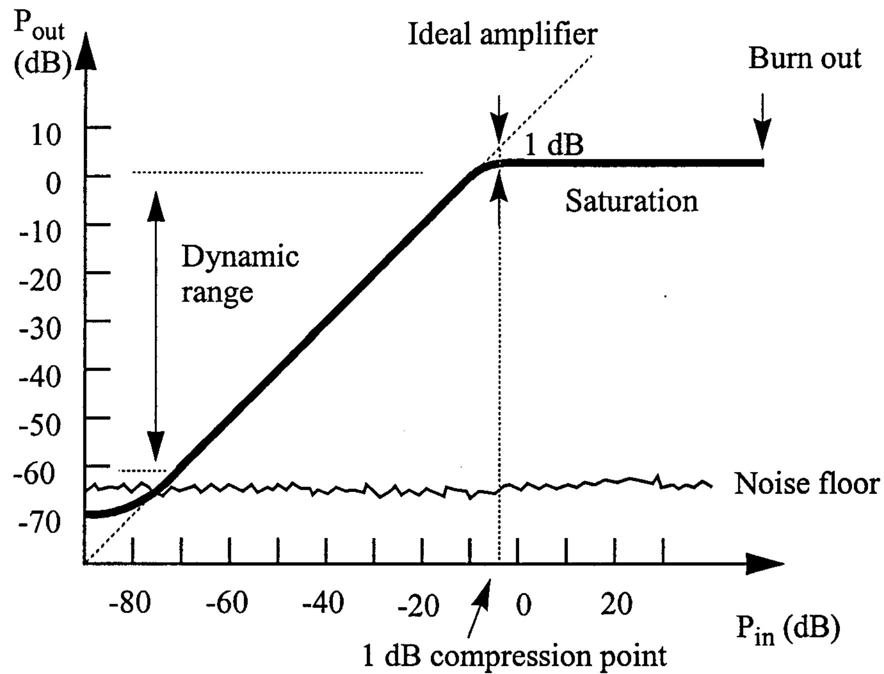

Fig. 1.1: The output power versus input power characteristics of a realistic amplifier.

Since noise is random in nature, it is represented as a time varying random variable $X(t)$ in noise theory. The mean value, $\overline{X}$, and the variance, $\overline{\Delta X^2}$, of $X(t)$ are two important parameters for characterizing the random variable $X(t)$. Another important characteristic of a random signal is its power spectral density function (PSDF) that describes how a signal distributes its power at different frequencies. By definition, PSDF represents the time averaged noise power over a one Hertz bandwidth at any given frequency f. White noise is a particular kind of noise which has a PSDF that is constant for

all frequencies. Thermal noise generated from a resistor and the shot noise generated in a bipolar junction transistor are examples of white noise.

Noise always exists in electronic signals due to the current or voltage fluctuation in a circuit. A DC current $I(t)$ or voltage $V(t)$ is actually the sum of an ideal DC component and a fluctuating AC component. The PSDFs of a DC current $I(t)$ and voltage $V(t)$ are represented by $S_I(f)$ and $S_V(f)$, and abbreviated as their "noise power spectra". These noise spectra describe how their noise powers distribute at different frequencies. The noise voltage generator $v_n(f) = \sqrt{S_V(f)}$ and noise current generator $i_n(f) = \sqrt{S_I(f)}$ are defined such that the total noise power of a circuit can be evaluated by applying AC circuit theory to these quantities.

1.2 FEATURES OF MODERN MOSFETS

Metal-Oxide-Semiconductor (MOS) technology is the dominant technology for very large-scale integrated (VLSI) circuits. The main driving force of submicrometer MOS technology is digital VLSI. However, as the speed and circuit complexity increase, it is often desirable to incorporate high-frequency analog circuits on the same chip. Radio frequency (RF) designs are increasingly taking the advantages of the advanced MOS technology that makes possible the integration of a complete communication system. As an example, global positioning system (GSP) receivers employ extensive digital signal processing to perform acquisition, tracking, and decoding functions. The use of the MOS technology for implementation of the front end electronics in a GPS system is therefore attractive because of the promise of integrating the whole system onto a single chip. In

addition to the high levels of integration of the CMOS process, many high-speed or RF integrated-circuits are likely to be implemented in CMOS technology since very high unity-gain frequencies (f_T) of deep sub-micron MOSFETs of more than 100 GHz have already been achieved [1],[2]. Therefore, high-frequency characterization and modeling of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) are becoming more important with the growth in high-frequency analog applications.

1.3 NOISE MODELING OF MOSFETS

As mentioned above, MOSFET are increasing used to implement analog functions at high frequencies. However, when working at high frequencies, the effect of the noise generated within the device itself will play an increasingly important role in the overall system sensitivity characteristics, dynamic range and signal-to-noise ratio [3],[4],[5]. Therefore it is crucial to understand the noise mechanisms in sub-micron MOSFETs. Due to the long turn-around time and the expensive cost of actual fabrication of an analog circuit, noise simulation of an analog circuit becomes a realistic alternative to determine whether the overall noise performance of a circuit would be good enough to allow the circuit to function properly [6],[7]. In order to perform accurate noise simulation, an appropriate physics-based noise model that can predict accurately the noise performance of transistors over a wide range of operating conditions is urgently needed.

1.4 OBJECTIVES

The goal of this thesis is to develop a systematic and self-consistent framework for the RF noise characterization, modeling and simulation of MOSFETs. The techniques and procedures developed in this thesis are general and can be applied to the high-frequency noise characterization of any active device. In general, there are five objectives of this research work. First, at high frequencies, the noise parameters -- minimum noise figure NF_{min}, equivalent noise resistance R_n, optimized source resistance R_{opt} and reactance X_{opt} -- of an active device are usually measured, instead of the noise spectral densities. In addition, in order to predict the high-frequency characteristics of MOSFETs, the complexity of the AC and noise equivalent circuit model has been increased tremendously. Therefore, how to calculate the four noise parameters based on any sophisticated noise equivalent circuit model is the first objective of this research work.

Second, in order to conduct the RF noise measurements, probe pads and metal interconnections are required to access the devices. These probe pads and interconnections will not affect the device characterization at DC or low frequencies. However, at high frequencies, the coupling of the probe pads and interconnections through the lossy substrate to ground will contribute some parasitics which will affect the measured scattering and noise parameters. Therefore, the second object of this research is to find out how to de-embed the parasitic effects from the probe pads and interconnections and to obtain the intrinsic noise and s-parameters of the transistors.

Third, in order to develop physics-based noise models for wireless applications, the spectral densities of the desired high-frequency noise sources in MOSFETs -- channel

noise, induced gate noise and their correlation as a function of frequency and bias -- have to be obtained from the intrinsic noise parameters. Therefore, how to obtain the noise spectral densities of desired noise sources as a direct target for the verification of any proposed noise model developed latter on is the third objective of this research.

Fourth, the physics-based noise model to be built in a compact device model for circuit simulation is the key objective of this research work. Therefore, after obtaining the spectral densities of the desired noise sources, the fourth objective is to develop physics-based noise models for RF wireless communication applications.

Lastly, when designing the low noise circuits, how to choose the device size, how to bias the devices and how to draw the layout of the transistors are the frequently asked questions by circuit designers. Therefore, the fifth object of this research work is to find out the design strategies of low noise circuits based on the developed noise models and extracted noise information.

1.5 MAJOR CONTRIBUTIONS

There are five main contributions in this thesis and they are listed as follows.

1. A systematic procedure to calculate the noise parameters of MOSFETs based on any sophisticated noise equivalent circuit model [8],[9],[13].
2. A general procedure and design of new dummy structures for the noise and s-parameter de-embedding to obtain the intrinsic noise and high-frequency performance of transistors [14],[15].

3. Two noise source extraction methods to obtain the spectral density of the channel noise, induced gate noise and their correlation directly from the intrinsic RF noise parameters [5],[16],[17],[18],[19],[20].
4. New analytical noise models to calculate the channel noise, induced gate noise and their correlation for RF wireless applications [21],[22].
5. Design strategies of a low noise amplifier (LNA) for RF wireless communication applications [23].

1.6 THESIS ORGANIZATION

The thesis consists of eight chapters. Chapter 1 describes the motivation and the objectives of the research work, followed by a description on the contribution of the work and the organization. Chapter 2 will present what the noise in MOSFETs looks like, different kinds of noise sources in semiconductor devices and the high-frequency noise and s-parameter measurement system.

In Chapter 3, a general noise theory for a noisy two-port network and the definition of the four noise parameters of a noisy two-port network -- minimum noise figure (NF_{min}), equivalent noise resistance (R_n), optimized source resistance (R_{opt}) and optimized source reactance (X_{opt}) -- are presented in detail. A technique for direct calculation of these four noise parameters based on matrix computations for any equivalent noise circuit model is also presented. In addition, circuit simulators are often used by circuit designers and they might want to verify the noise model based on the compact model in the circuit simulator.

Therefore, another calculation method using circuit simulators to obtain the noise parameters based on compact models is also presented in Chapter 3.

Parasitics of the probe pads and interconnections in the test chip become an important issue for both RF and noise characterization [24],[25],[26]. With the continuous downscaling of the device dimensions, the impact of the surrounding parasitics on a transistor's characteristics has gained importance in the RF domain. In [8] and [27], a noise de-embedding method based on a parallel-series configuration was presented. This configuration assumes that the capacitive effect of metal interconnections between the probe pads and the transistor can be lumped into the probe pads and the inductive and resistive effects are modeled in series with the transistor at the frequencies of interest. However, this might not be true for designs with long (or wide) interconnections, or at operating frequencies of several tens of GHz. Therefore, the DUT has to be modeled as probe pads, interconnections and the transistor connected in a cascade configuration. The method presented in [28] is based on a cascade configuration, but it requires specific equivalent circuit models for both probe pads and the metal interconnections. This means that the de-embedding results rely on the accuracy of the equivalent circuit models and the element values used in the calculation. In addition, this procedure is not easy to automate since the parasitic elements in the equivalent circuit model are both technology and design dependent. In Chapter 4, a new de-embedding method based on the cascade configuration is presented in detail.

Verification of the noise model has always been challenging for RF noise modeling of MOSFETs. Presently, models of the channel noise that are physics-based are

confirmed by the measured minimum noise figure (NF_{min}) of devices through the help of a device simulator or the device's small-signal model [29],[30]. However, the accuracy of the small-signal model, the values of model parameters used in simulation and the noise model itself affect the simulated noise parameters. These factors make the confirmation of noise models more difficult, even when accurate noise parameters were measured. In addition, when transistors operate in the GHz range, the random potential fluctuations in the channel resulting in the channel noise will be coupled to the gate terminal through the gate oxide capacitance and will cause the induced gate noise, which is usually correlated with the channel noise.

Because of the difficulties in the extraction of the induced gate noise and its correlation with the channel noise, several noise models [31],[32] and simulation results [33] have been presented, but they could not be verified directly with the noise parameters obtained from RF noise measurements for deep sub-micron MOSFETs. Therefore, to have the proper topology of an equivalent noise circuit suitable for RF modeling, to obtain the element values of the equivalent noise circuit directly from the measured s-parameters (or y-parameters), and to get the channel noise, induced gate noise and their correlation directly from RF noise measurements are crucial for the high-frequency noise modeling of deep sub-micron MOSFETs.

Chapter 5 presents a systematic procedure to extract the spectral densities of induced gate noise ($S_{i_g^2}$), channel noise ($S_{i_d^2}$) and their cross-correlation ($S_{i_g i_d^*}$) directly from the s-parameter and RF noise parameter measurements. With the help of the direct calculation technique described in Chapter 3, the extracted noise currents are fed back to

the equivalent noise model to calculate the noise parameters -- NF_{min}, R_n and optimized source reflection coefficient (Γ_{opt}) -- and to compare the calculations to the measured data for the verification of the extracted noise sources. After that, the extracted noise currents of the deep sub-micron MOSFETs fabricated in a 0.18 μm CMOS process as a function of frequency, bias condition and channel length are presented and discussed.

After obtaining the spectral densities of the channel noise, induced gate noise and their correlation, the next step is to verify the noise models in the literature and develop new noise models if the traditional noise models fail to predict the noise performance of deep sub-micron MOSFETs. To date, it is observed that the channel noise generated from the short-channel devices is higher than that expected from the conventional channel noise theory for long-channel MOSFETs [34],[35]. Several approaches in the literature have been proposed to explain the discrepancy by introducing extra channel noise from the velocity saturation through either the hot-electron effect [34] or the diffusion noise [36],[37]. The noise from the saturation region proposed in these models is either not physical or not proven by the measured noise data of deep sub-micron MOSFETs. In Chapter 6, a new analytical noise model using the channel length modulation (CLM) effect to calculate the channel noise of deep sub-micron MOSFETs is presented and verified by the measured data obtained using the direct extraction method described in Chapter 5. In addition, the hot electron effect and the velocity saturation effect are also discussed. The noise models published in the literature for the channel noise, induced gate noise and their correlation are also reviewed and verified either by theories or experiments.

Based on the extracted AC and noise parameters, Chapter 7 presents some considerations for the design of low-noise circuits and shows the impact of the noise models on the circuit simulation. Chapter 8 will conclude the thesis and have some discussion on the future research work for the noise modeling of MOSFETs.

Chapter 2

NOISE AND RF MEASUREMENTS

2.1 WHAT DOES NOISE LOOK LIKE

If we take an n-type MOSFET biased in a common source configuration as shown in fig. 2.1 with a positive drain bias V_D and a gate bias V_G greater than the threshold voltage V_{TH}, it is expected that there is a constant current I_o as a function of time flowing through the transistor, which is the dashed line in fig. 2.2. However, if we monitor the DC current with an oscilloscope, the actual drain current fluctuates randomly as a function of time with an average value I_o, which is the solid line in fig. 2.2. The undesired random fluctuation in the drain current will set the lowest detectable ACAC signal, and is therefore called "noise".

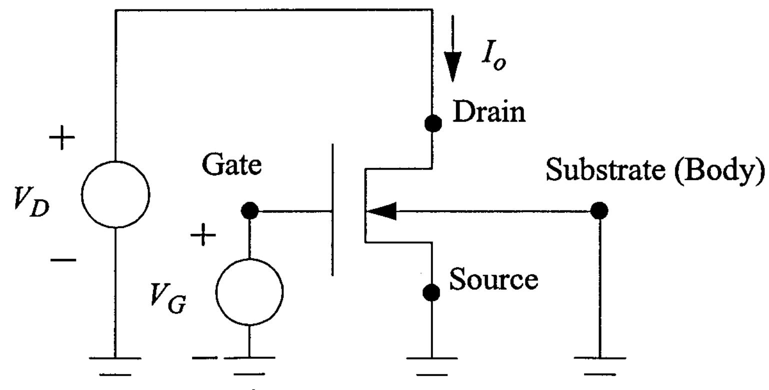

Fig. 2.1: An n-type MOSFET biased at a common source configuration.

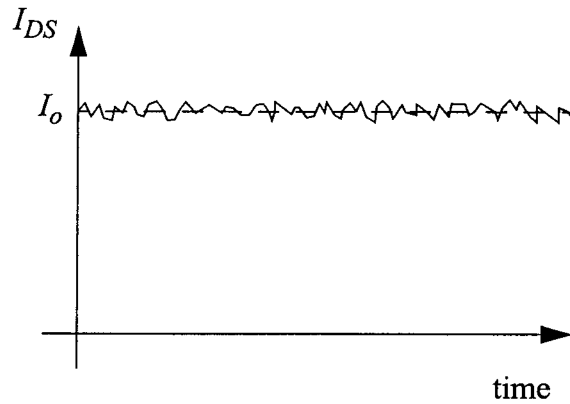

Fig. 2.2: Drain current as a function of time at a fixed bias voltages.

Since the current fluctuation is random and unpredictable in the time domain, it is often represented by its spectral density in frequency domain, as shown in fig. 2.3. In the low frequency region, the noise spectral density is inversely proportional to the frequency. However, at high frequencies, the noise spectral is almost frequency independent, and it is also called "white noise".

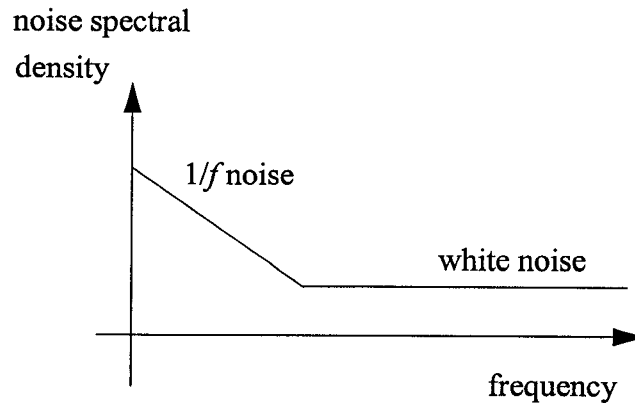

Fig. 2.3: Noise spectral density of the random fluctuation in drain current.

After knowing what the noise looks like, the next question is what is the physical mechanism that generates the noise. Fig. 2.4 shows a cross-section of an n-type MOSFET biased in a common source configuration. Consider an electron traveling along the channel, then because of the collision of the electron with the lattice due to the thermal vibration of the lattices, there is a small voltage fluctuation Δv_{xo} generated at x_o in the channel. Because of the non-zero output conductance $g_{DS}(x_o)$ at x_o, the small voltage fluctuation will be detected at the drain terminal through the current fluctuation, and this is called "channel noise". Channel noise occurs at all frequencies, and it consists of noise sources generated from different noise mechanisms which will be discussed in next section. This thesis will only focus on the channel noise at high frequencies.

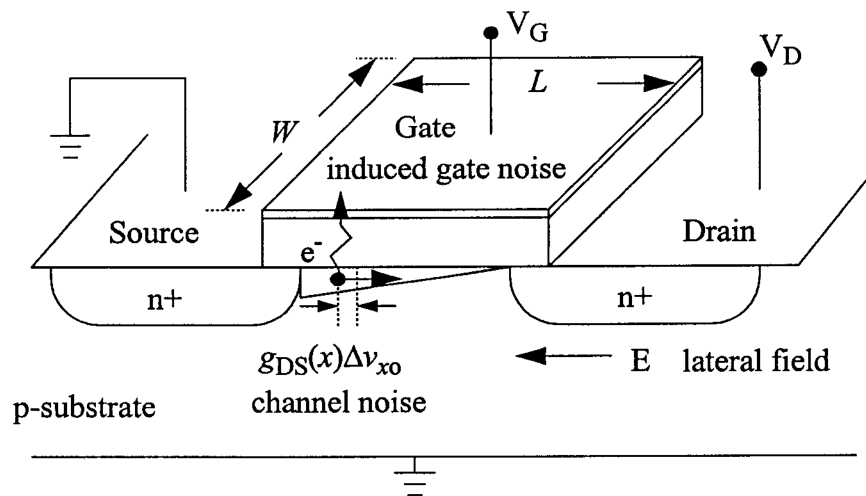

Fig. 2.4: Cross-section of an n-type MOSFET biased at a common source configuration.

At high frequencies, the gate oxide has a finite impedance and the current fluctuation caused by the voltage fluctuation Δv_{xo} will also be detected at the gate terminal -- this is termed the "induced gate noise". Because the physical origins of the channel noise

and the induced gate noise come from the same source Δv_{xo}, therefore they are usually correlated. A detailed discussion and extraction techniques for the channel noise, induced gate noise and their correlation will be discussed in Chapter 5. The physics-based noise models for these noise sources will be discussed in Chapter 6. A brief discussion of different noise sources in semiconductor devices will be presented in the next section.

2.2 NOISE IN SEMICONDUCTOR DEVICES

The noise discussed in this thesis is the electronic noise which is caused by the small voltage (or current) fluctuations generated within the device. The most important noise sources in a device are thermal noise, shot noise, generation-recombination noise and flicker noise.

2.2.1 Thermal Noise (Nyquist Noise or Johnson Noise)

Thermal noise is caused by the random changes in the motions of the carriers due to their collisions with the vibrating atoms. In general, the spectral density of the short-circuit current fluctuation $S_{I,T}$, in A^2/Hz, can be expressed by [38]

$$S_{I,T} = 4 \cdot \left[\frac{1}{2}hf + \frac{hf}{\exp(hf/kT) - 1}\right]/R \tag{2.1}$$

where h is Planck's constant, k is Boltzmann's constant, f is the frequency, T is the absolute lattice temperature, and R is the resistance of the sample. For $hf/kT << 1$, $S_{I,T}$ can be reduced to the widely used expression

$$S_{I,T} = \frac{4kT}{R}. \tag{2.2}$$

2.2.2 Shot Noise

Shot noise is generated when carriers (electrons or holes) cross potential barriers independently and at random. It is present in diodes and bipolar transistors. The external DC current I, which appears to be a steady current, is in fact composed of a large number of random independent current pulses. The physical origin of the shot noise is the fluctuation of the emission rate of carriers. For operating frequency lower than the reciprocal of the transit time, the short-circuit spectral density (A^2/Hz) of the shot noise $S_{I,S}$ is white [38] and is expressed as

$$S_{I,S} = 2qI \tag{2.3}$$

where q is the electronic charge (1.6×10^{-19}C) and I is the DC current through the sample.

2.2.3 Generation-Recombination Noise

Generation-recombination noise (g-r noise) is caused by the fluctuation of the conductance. Because of the traps and recombination centers in semiconductors, the random trapping and detrapping of carriers results in the fluctuation in the number of free carriers N per unit time, causing the conductance of the device to fluctuate. The power spectral density of g-r noise is given by [38]

$$S_N(f) = \langle \Delta N^2 \rangle \cdot \frac{4\tau}{1+(2\pi f\tau)^2} \tag{2.4}$$

where $\langle \Delta N^2 \rangle$ is the variance of N, f is the frequency, and the τ is the lifetime of the carriers.

2.2.4 Flicker Noise (1/*f* Noise)

The origin of the flicker noise is still actively researched. Because the spectrum varies as $1/f^n$, with n close to unity, flicker noise is often called $1/f$ noise. In general, two major models have been proposed to account for the origin of flicker noise -- the carrier number fluctuation model [39] and the mobility fluctuation model [40]. In the first model, the flicker noise is attributed to the random trapping and de-trapping processes of charges, for example in the oxide traps near Si-SiO_2 interface in MOSFETs. The charge fluctuations result in fluctuations of the surface potential, which in turn modulate the channel mobile carrier density. It is assumed that the channel can exchange charges with the interfacial oxide traps through tunneling. The second model considers that the flicker noise results from the bulk mobility fluctuation on the basis of an empirical hypothesis. In general, its short-circuit spectral density is given by the empirical expression [40]

$$S_I(f) = \frac{\alpha}{f^n N} \tag{2.5}$$

where α is the Hooge's constant with value between 10^{-7} and 10^{-3} depending on the device, N is the total number of charges, and n is a constant close to unity.

2.3 SCATTERING AND NOISE PARAMETER MEASUREMENTS

If the dimension of the components of circuits is comparable to the wavelength of the voltage and current waves (i.e. distributed circuits), we can not neglect the effect of the phase changes in the waves traveling along the circuit elements. In addition, a practical problem exists when trying to measure voltages and currents at microwave frequencies

because direct measurements usually involve the magnitude (inferred from power) and the phase of a wave traveling in a given direction. A representation that is in accord with direct measurements, and with the ideas of incident, reflected, and transmitted waves, is given by the scattering matrix. Therefore, s-parameters are most commonly used in characterizing the high frequency performance of devices and circuits. In addition, to characterize the AC and the noise characteristics of DUT at the same time, the s-parameter and noise parameters of transistors have to be measured successively. Therefore, the measurement system should combine the s-parameter measurement system and noise measurement system together and have the bias-T with variable input impedance for measuring the optimized source impedance. The NP5B Noise Parameter System and S-Parameter Measurement software manufactured by ATN microwave is employed for this purpose. This system is a solid-state tuner based, turn-key solution for complete small-signal device characterization. In conjunction with a network analyzer and noise receiver, it provides noise parameter and s-parameter measurements, equivalent models, and can be used for detailed characterization versus bias or frequency. All details, such as system setup, system calibration, and power level setting will be described in the following sections.

2.3.1 System Setup

The complete S-Parameter and Noise Parameter Measurement System for high-frequency noise and s-parameter measurements is shown in fig. 2.5.

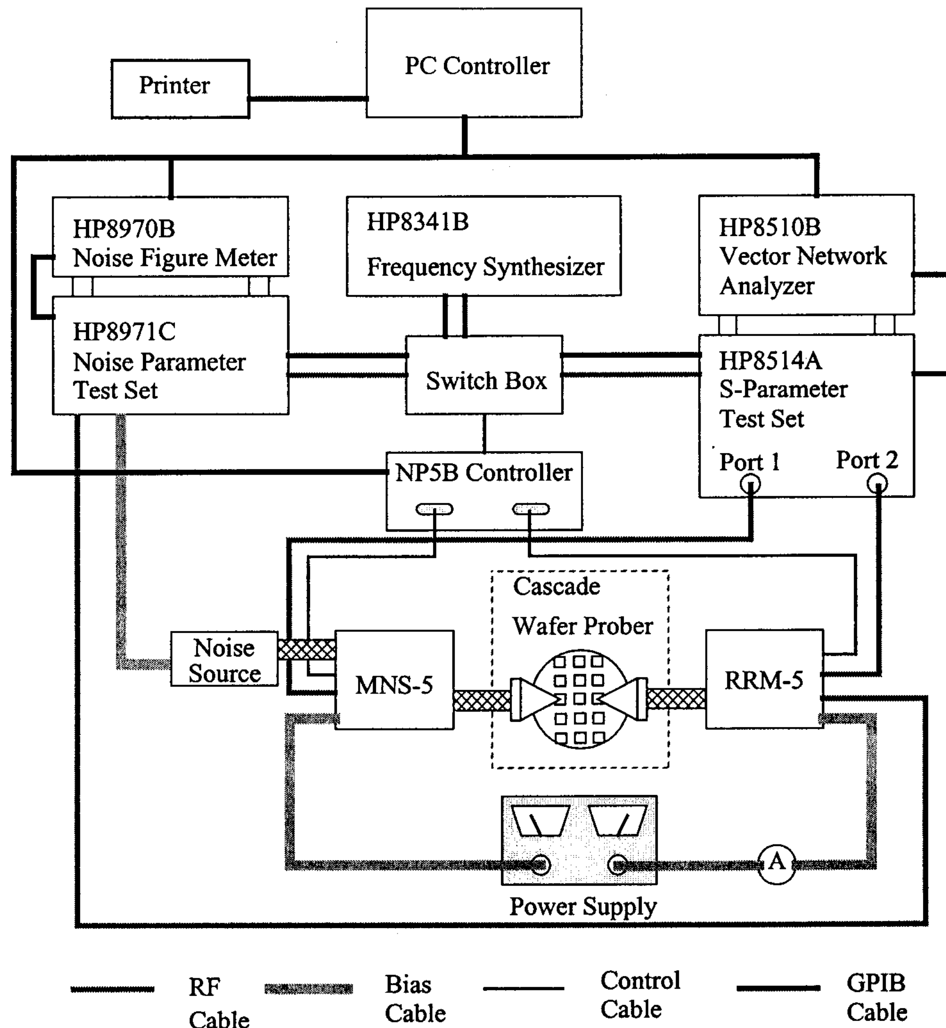

Fig. 2.5: ATN NP5B measurement system for s-parameter and noise parameter measurements.

The system basically consists of three sub-systems -- an ATN NP5B wafer prober test set, a HP8510 vector network analyzer system (VNA), a HP8970 noise measurement system, and other peripheral devices such as a printer, a computer, and a microwave probe station. The NP5B mainframe works as a switch for switching between the HP8510B for

the s-parameter measurements and the HP8970 for the noise measurements of two-port networks.

- **NP5B wafer prober test set**

The ATN NP5B Wafer Prober Test Set is comprised of a main controller unit which drives the externally connected Mismatch Noise Source (MNS5) and the Remote Receiver Module (RRM5). The MNS5 contains a solid state electronic tuner (ET) with a built-in bias-T and RF switches which alternately connect the VNA and the noise source to the DUT while the output of the DUT is connected via the RRM5 unit to either port 2 of the VNA or to the HP8970B noise figure meter via the built in low noise amplifier of the RRM5. The low noise amplifier in the RRM5 can lower system noise figure and therefore reduce the measurement uncertainty. The RRM5 also contains a bias-T and the necessary switching circuitry. The switch box in fig. 2.5 is used to pass the RF signal from the HP8341B frequency synthesizer to either the s-parameter measurement system or the noise measurement system if there is only one frequency synthesizer available for different measurement modes [41].

- **S-parameter measurement system**

The s-parameter measurement systems contains the HP8510B vector network analyzer (VNA) and HP8514A s-parameter test set to measure the scattering and gain parameters of linear two port networks. In the s-parameter measurement mode, the HP8510B controls the RF source (HP8341B) and two kinds of measurements are made - reflection and transmission. An incident signal generated by the RF source is applied to the

DUT and compared with the signal reflected from or transmitted through the DUT. Reflection measurements are made by comparing the reflected signal to the incident signal. This provides measurement data on reflection characteristics of the DUT such as return loss, standing wave ratio (SWR), reflection coefficient (S_{11} or S_{22}) and impedance. Transmission measurements are made by comparing the transmitted signal to the incident signal. This results in measurement data on transmission characteristics of the network such as insertion loss, transmission coefficient (S_{21}), electrical delay (from which electrical length can be obtained), deviation from linear phase and group delay. By applying the incident signal to the output port of DUT, the reverse characteristics, output impedance and reverse transmission coefficient (S_{12}) can be measured.

The HP8514A s-parameter test set separates the RF signal into an incident signal sent to the DUT and a reference signal to which the transmitted or reflected signals are later compared. It also routes the transmitted and reflected signals from DUT to the receiver for later processing. Internal attenuation from 0 to 90 dB, in 10 dB increments, are available to control the incident stimulus level at the DUT input without causing a change in the reference level.

- **Noise measurement system**

The noise measurement system consists of the HP8970B Noise Figure Meter and HP8971C Noise Parameter Test Set to measure the noise parameters and gain of DUT. The HP8970B can be tuned between 10 and 1,600 MHz and can also be swept over all or any part of that range. The HP8971C extends the frequency range of the noise figure meter from 1,600 MHz to 26,500 MHz.

• **Other peripheral devices**

Other peripheral devices are a dual DC voltage power supply for biasing the DUT, a current meter to monitor the drain current, a microwave probing station, a switch box used for passing the RF signal from the synthesizer to either the s-parameter measurement system or the noise measurement system depending on the measurement mode, a computer for instrument control and data collection, and a printer for printing the measurement results.

2.3.2 System Setting

After all the instruments are properly set up, we turn on the power switch of each instrument in the following order: s-parameter measurement system or noise measurement system, and then NP5B main control unit. When turning on the power of the s-parameter measurement system, one should follow the following power-on sequence: frequency synthesizer, s-parameter test set, system peripheral devices if there is any, and network analyzer.

To achieve the maximum measurement accuracy, the power level of the RF signal generated by the HP8341B synthesizer should be as high as possible without overloading the test set. According to the HP8510 *Network Analyzer Operating and Programming Manual* (p. 55-6), the source power between 0 to 10 dBm is optimal. However, when measuring a highly non-linear device such as MOSFETs, we must ensure the power applied to the device is sufficiently low to avoid non-linear distortion and gain compression. Attenuators included in the ports 1 and 2 signal paths of the s-parameter measurement test

set provide a way of reducing the actual power supplied to the device. The attenuators can be set from 0 to 90 dB in 10 dB increments.

At low frequencies, the drain current I_D varies approximately as $(V_{GS} - V_{TH})^2$, where the threshold voltage, V_{TH}, is ~ 0.5V for the 0.18 μm CMOS technology. The small-signal model of the transistor is only valid when the ACAC voltage is small compared to the DC voltages i.e. $\Delta V/V << 1$. However, if the power level is too small, the measured s-parameters will appear noisy. On the other hand, if the power level is too large, the measured s-parameters will again be reduced because of gain compression, as shown in fig. 1.1. In addition, the measured s-parameters should remain constant over a range of intermediate power levels. For greatest measurement accuracy, we set the power level to a value in the middle of dynamic range of DUT. The procedure must be repeated for both ports 1 and 2.

Since the output of the MOSFETs is not as non-linear as the input, less attenuation is required at port 2. In our measurements, the power level is set to 5 dBm (at the starting frequency of 0.5 GHz) with 30 dB attenuation at port 1 and 10 dB attenuation at port 2. Taking into account about 2 dB loss in the cables, there will be about -27 dBm at port 1 and -7 dBm at port 2.

The optimal power levels vary with frequency. At higher frequencies, more power is lost in the test set, cabling and bias-T. In addition, the input and output impedance of the DUT vary with frequency. In order to compensate for the change in the optimal source power, the HP8510B provides a Power Slope setting which allows the source power to

either increase or decrease with frequency. In our measurement, the power slope is set to 0.2 dB/GHz.

All s-parameters were measured over the maximum frequency range of the s-parameters test set, from 500 MHz to 18 GHz, and noise parameters were measured from 2 GHz to 6 GHz, in steps of 0.5 GHz. Because the time for the noise parameter measurements is quite long (depending on the number of measurement averages) and we do not want the devices to be stressed, the number of measurement points (for different frequencies and bias conditions) and the bias voltages applied (especially V_{DS}) are set to compromised values.

The VNA provides a fast-sweep-mode and a continuous-wave-mode for sweeping the frequency. In the fast-sweep-mode, the synthesizer frequency is gradually swept over the entire frequency range while the VNA measures the s-parameters at the specified frequency points. In continuous-wave-mode, the synthesizer frequency is stepped from one frequency value to another and the VNA measures the s-parameters after a specified settling time. We used the continuous-wave-mode, which is slower but more accurate. According to the HP8510B manual, a settling time of 2 ms per point is more than sufficient. The settling time is specified indirectly by the Sweep Time parameter. The settling time is approximately equal to the Sweep Time divided by the total number of points.

The HP8510B provides simple data processing features such as data smoothing and data averaging. We disabled the data smoothing feature but enabled data averaging to lower the noise floor. With data averaging on, the s-parameters are repetitively measured a specified number of times and averaged at each frequency point. Although, averaging

improves the signal-to-noise ratio (SNR), it also dramatically increases measurement time. The averaging factor can be set up to 4096; however, we opted for an averaging factor of 1024 to reduce the measurement time, but still having good SNR.

All configuration parameters are entered from the NP5B controlling software under the SET CONFIG and SET FREQ manuals of SYSTEM CONFIG. The next section discusses calibration of the overall system to correct for the parasitics of the measurement setup.

2.3.3 System Calibration

The NP5B noise parameter measurement system is based on the Adamian and Uhlir concept which states that the knowledge of the total hot output noise power of a standard noise source plus the total output noise power of several passive one port terminations is sufficient for complete noise parameter characterization of a linear receiver [42],[43]. This fundamental receiver concept can be extended to the characterization of a linear two-port by simply using the correlation matrix to de-embed the linear two-port from the overall system and receiver noise parameter [12],[44]. According to the circuit theory of linear noisy networks, the necessary and sufficient requirements to calibrate a linear receiver and make noise parameter measurements of linear two-port networks [45] are as follows.

1. A calibrated vector network analyzer at the DUT reference planes to make s-parameter measurements over the frequency range of interest.

2. A linear noise power receiver at the DUT reference plane with known noise parameters and input reflection coefficient over the frequency range of interest. This requires a known noise source at the receiver reference plane.
3. A large number of known terminations at the DUT input reference plane over the frequency range of interest.

According to the ATN NP5B Operation Manual, there are several calibration steps which have to be completed in sequence before the s-parameter and noise measurements are made. These steps are explained according to the sequence in the calibration procedure.

1. Calibration of the Short, Open, and Load (C SOL): With a thru' of known delay as the DUT, the NP5B system makes raw S_{22} measurements with a short, open, and load in the place of the noise source. This raw data will be combined with the data taken during the full 2 port calibration (at the device plane) to determine the s-parameters of the MNS5.
2. Calibration of the Noise System- Part 1 (C NS1): With the same thru' as in the SOL calibration and having established a reference plane at the noise source from the SOL calibration, the NP5B system makes raw S_{22} measurements with the noise source on and off and calculates the corresponding reflection coefficients for the noise source. It displays these results for information purpose to the system CRT. The NP5B system then proceeds to make hot and cold power measurements with the noise figure meter. These power measurements are used later to establish the gain and noise figure for the receiver.

Fine tuning calibration (Peaking the YIG) is used to align the passbands of the noise figure meter and noise figure test set at the measured frequencies defined by START FREQ, STOP FREQ and STEP SIZE. Because the noise measurements were done under the single sideband operation and usually most of the measurement frequencies are higher than 2400 MHz, Fine Tuning Calibration is always recommended. The noise measurement system will perform better the more frequently a Fine Tuning Calibration is done. However, once the Fine Tuning Calibration is done, a new fine Tuning Calibration should not be required unless the Noise Figure Test Set is turned off, the ambient air temperature around the Noise Figure Test Set changes more than ±5°C since the last Fine Tuning Calibration or the START FREQ, STOP FREQ or STEP SIZE have been changed.

3. Calibration of the S-Parameters (C SP): This is a standard s-parameter calibration by any of the standard acceptable methods - Short-Open-Load-Thru' (SOLT), Line-Reflect-Match (LRM), Thru'-Reflect-Line (TRL), or Line-Reflect-Line (LRL). Note that the s-parameter reference planes are the noise parameter reference planes in the NP5B software. It is useful to end on a thru' so that once the s-parameter calibration is finished, the thru' can be checked. If the thru' is bad, stop and re-do the s-parameter calibration.

4. Calibration of the Thru' Delay (C TD): With the same thru' as in the SOL and NS1 calibrations as the DUT, the corrected s-parameters are measured and the thru' delay is calculated and displayed for confirmation.

5. Calibration Calculation of the SOL (C CSOL): From the information obtained in the SOL, NS1, SP, and TD calibrations, the s-parameters of the MNS from the noise source to the s-parameter port 1 reference plane are calculated. Also the noise and gain references as measured in C NS1 are transferred to the s-parameter port 2 reference plane.
6. Calibration of the Source Reflection Coefficients - Gammas (C SG): With the same thru' as before, S_{22} measurements are made for the 88 impedance states of the solid state tuner. These impedances are then referred to the s-parameter port 1 reference plane and stored.
7. Calibration of the Post Receiver (C PR): With the same thru' as before, S_{11} measurements are made to determinate the input reflection coefficient of the post receiver. This information is referred to the s-parameter port 2 reference plane and stored.
8. Calibration of the Noise System - Part 2 (C NS2): With the same thru' as before, noise power versus source impedance is measured and the receiver noise parameters are calculated and stored at the s-parameter port 2 reference plane.

After going through the eight calibration procedures listed above, the whole system is ready for the s-parameter and noise parameter measurements.

Chapter 3

NOISE PARAMETER CALCULATION

3.1 INTRODUCTION

The noise models of BJTs and MOSFETs, in general, are made up of active two-ports, passive components, and some noise current (voltage) sources. The accuracy of noise modeling relies on the topology of the small-signal model with appropriate values for model elements which can accurately predict the electrical performance of the devices, and the knowledge of the physical noise sources.

In this chapter, the general noise theory of a two-port network will be introduced first. This is followed by the methods of calculating the noise parameters - minimum noise figure (NF_{min}), equivalent noise resistance (R_n) and optimized source reflection coefficient (Γ_{opt}). Assuming that an appropriate small-signal model of the device is available, and all the element values of the capacitors, resistors, etc. and the noise sources in the small-signal model are obtained, then two calculation methods to obtain the noise parameters of a noisy two-port can be used. These are the direct matrix analysis [8],[9] or the circuit simulation (e.g. Spectre) based on compact models.

3.2 THEORY OF NOISY TWO-PORT NETWORKS

The noise figure, defined as the signal-to-noise ratio at the input port divided by signal-to-noise ratio at the output port, is widely used as a measure of noise performance of a two-port network. The noise figure (*NF*) is generally affected by two factors - the source (input) impedance at the input port of a network and the noise sources within the two-port network itself. In general, the noise figure of a two-port network with any arbitrary source impedance can be calculated by [10]

$$NF = NF_{min} + \frac{R_n}{G_s} \cdot [(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \tag{3.1}$$

or

$$NF = NF_{min} + \frac{4R_n|\Gamma_s - \Gamma_{opt}|^2}{(1-|\Gamma_s|^2) \cdot |1 + \Gamma_{opt}|^2}; \quad \Gamma_s = \frac{R_s + jX_s - Z_o}{R_s + jX_s + Z_o} \tag{3.2}$$

where G_s is the source conductance, B_s is the source susceptance, Γ_s is the source reflection coefficient, G_{opt} is the optimized source conductance, B_{opt} is the optimized source susceptance, Γ_{opt} is the optimized source reflection coefficient and Z_o is the system impedance which is 50 Ω in our system. From (3.1) and (3.2), it is shown that the four noise parameters -- the minimum noise figure (NF_{min}), the optimum source (input) admittance $Y_{opt} = G_{opt} + jB_{opt}$ at which the NF_{min} occurs, and the equivalent noise resistance R_n, which characterizes how much the noise figure will change if the source impedance deviates from the optimum value -- will reflect how noisy a two-port network itself will be.

A noisy two-port may be represented by a noise-free two-port and two current noise sources as shown in fig. 3.1(a), and these two noise sources are usually correlated with each other.

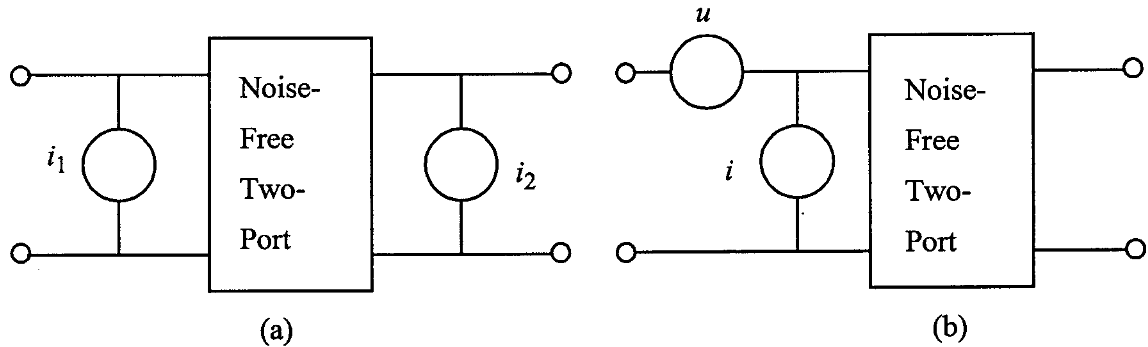

Fig. 3.1: Different representations of a noisy two-port network

From the y-parameters of the two-port and the noise source information (i_1, i_2 and the correlation term $\overline{i_1 i_2{}^*}$), we may evaluate the noise parameters of the two-port by transforming the noisy two-port to a noise-free two-port with a noise current source and a noise voltage source at the input side of the two-port (fig. 3.1(b)). Here, i and u and the correlation factor (Y_{cor}) are calculated using [11]

$$i = i_{un} + uY_{cor} \tag{3.3}$$

and

$$\overline{iu^*} = Y_{cor}\overline{|u|^2}, \tag{3.4}$$

where

$$u = -\frac{1}{Y_{21}}i_2, \tag{3.5}$$

$$i = i_1 - \frac{Y_{11}}{Y_{21}} i_2, \tag{3.6}$$

$$Y_{cor} = Y_{11} - Y_{21} \frac{\overline{i_1 i_2^*}}{\overline{|i_2|^2}} = G_{cor} + jB_{cor}, \tag{3.7}$$

and the noise power of i and u can be calculated from

$$\overline{|u|^2} = \frac{\overline{|i_2|^2}}{|Y_{21}|^2} = 4kT\Delta f R_u, \tag{3.8}$$

and

$$\overline{|i|^2} = \overline{|i_1|^2} + \overline{|i_2|^2} \left| \frac{Y_{11}}{Y_{21}} \right|^2 - 2Re\left\{ \overline{i_1 i_2^*} \cdot \frac{Y_{11}^*}{Y_{21}^*} \right\} = 4kT\Delta f G_i. \tag{3.9}$$

From (3.7) to (3.9), we can calculate the four noise parameters from [11]

$$R_n = R_u, \tag{3.10}$$

$$G_{opt} = \sqrt{\frac{G_i}{R_n} - B^2_{cor}}, \tag{3.11}$$

$$B_{opt} = -B_{cor}, \tag{3.12}$$

and

$$NF_{min} = 1 + 2R_n(G_{cor} + G_{opt}). \tag{3.13}$$

Another approach to calculate the noise parameters which is suitable for computer-aided analysis is to use the generalized admittance matrix of a noisy two-port

network [9],[13],[11]. According to the noise circuit shown in fig. 3.1, we can write the admittance node equations at port 1 and port 2 as

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} B \\ D \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.14}$$

where B = [1 0] and D = [0 1], and define the noise correlation matrix C [12] as

$$C = \begin{bmatrix} \overline{i_1 i_1{}^*} & \overline{i_1 i_2{}^*} \\ \overline{i_2 i_1{}^*} & \overline{i_2 i_2{}^*} \end{bmatrix}. \tag{3.15}$$

Using the y-parameters, B, C, and D matrixes defined in (3.14) and (3.15), R_u, G_i and Y_{cor} can be calculated from the following expressions [9]

$$R_u = \frac{1}{4kT\Delta f} Re\left\{ \frac{1}{|Y_{21}|^2} \times [D]^* \times [C] \times [D]^T \right\}, \tag{3.16}$$

$$G_i = \frac{1}{4kT\Delta f} Re\left\{ \left([B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^* \times [C] \times \left([B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^T \right\}, \tag{3.17}$$

$$\begin{aligned} Y_{cor} &= G_{cor} + jB_{cor} \\ &= \frac{-1}{4kT\Delta f R_n Y_{21}{}^*} \left\{ [D]^* \times [C] \times \left([B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^T \right\} \end{aligned} \tag{3.18}$$

where the asterisk (*) denotes the complex conjugate and T denotes the transpose of the matrix. Once R_u, G_i and Y_{cor} calculated from (3.16) to (3.18), then the noise parameters can be calculated using (3.10) to (3.13).

3.3 NOISE PARAMETER CALCULATION

The capability of calculating the four noise parameters - minimum noise figure (NF_{min}), equivalent noise resistance (R_n), optimized source resistance (R_{opt}) and reactance (X_{opt}) of MOSFETs based on any sophisticated equivalent circuit model that can accurately predict the RF performance of devices is the foundation of RF noise modeling. This section will describe two calculation methods based on matrix analysis and circuit simulator techniques.

3.3.1 Direct Matrix Analysis

The advantage of the direct matrix analysis is that it easily allows us to characterize the noise sources in the model if there is any correlation existing between the noise sources. This analysis can serve as a tool to develop proper noise models and to verify their implementation in compact models of a circuit simulator. In this section, the theoretical background for the noise parameter calculation of MOSFETs will be introduced.

Direct calculation of noise parameters uses a matrix operation based on the noisy two-port network theory mentioned above. Fig. 3.2 shows a RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications. In order to perform the matrix calculation of the noisy two-port shown in fig. 3.2, we transform our noisy circuit model into its graph shown in fig. 3.3.

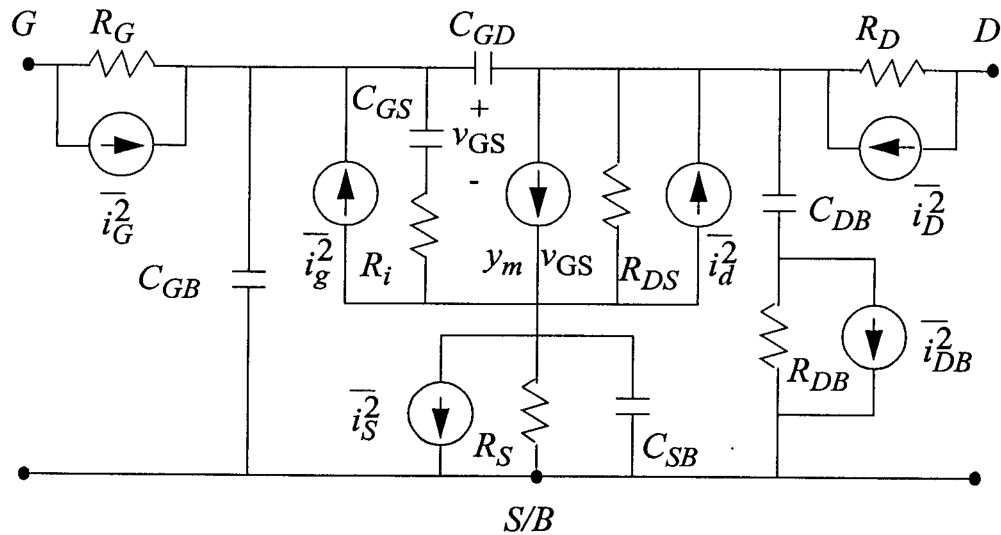

Fig. 3.2: RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications.

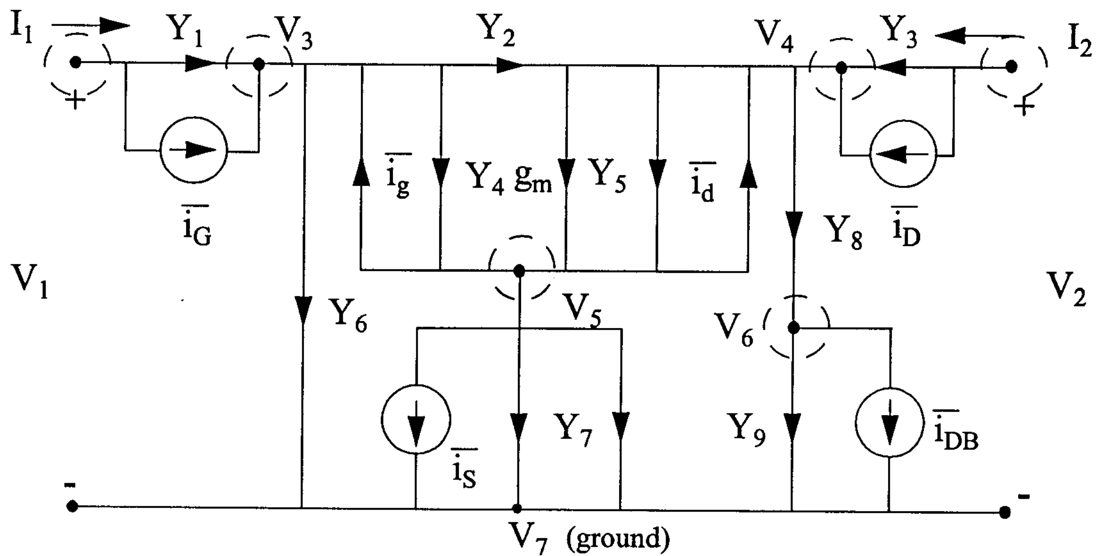

Fig. 3.3: The graph of the equivalent noise circuit model of DUT.

Based on the graph of DUT shown in fig. 3.3, we write the node equations corresponding to each node (sub-set) in a matrix form as

$$\underbrace{\begin{bmatrix} Y_1 & 0 & -Y_1 & 0 & 0 & 0 \\ 0 & Y_3 & 0 & -Y_3 & 0 & 0 \\ -Y_1 & 0 & Y_1+Y_2+Y_4+Y_6 & -Y_2 & -Y_4 & 0 \\ 0 & -Y_3 & g_m-Y_2 & Y_2+Y_3+Y_5+Y_8 & -g_m-Y_5 & -Y_8 \\ 0 & 0 & -g_m-Y_4 & -Y_5 & g_m+Y_4+Y_5+Y_7 & 0 \\ 0 & 0 & 0 & -Y_8 & 0 & Y_8+Y_9 \end{bmatrix}}_{[Y]6x6} \underbrace{\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix}}_{[V]} \tag{3.19}$$

$$+\underbrace{\begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ -1 & 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{[A]6x6} \underbrace{\begin{bmatrix} i_g \\ i_d \\ i_G \\ i_S \\ i_D \\ i_{DB} \end{bmatrix}}_{[i_n]} = \begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

where $Y_1 = 1/R_G$, $Y_2 = sC_{GD}$, $Y_3 = 1/R_D$, $Y_4 = 1/(1/sC_{GS} + R_i)$, $Y_5 = 1/R_{DS}$, $Y_6 = sC_{GB}$, $Y_7 = sC_{BS} + 1/R_S$, $Y_8 = sC_{DB}$, $Y_9 = 1/R_{DB}$, $s = j\omega$ and ω is the angular frequency. Once the matrix equations are formulated, the network is reduced by eliminating four nodes - node 6, 5, 4, and 3, one by one, leaving only the input and output nodes (node 1 and node 2). For example, we eliminate the node 6 first, then each element of Y and A not in row 6 will be transformed according to the following formulas

$$Y'_{ij} = Y_{ij} - \frac{Y_{6j} \times Y_{i6}}{Y_{66}} \qquad (1 \le i < 6) \qquad (1 \le j < 6) \tag{3.20}$$

$$A'_{ij} = A_{ij} - \frac{A_{6j} \times Y_{i6}}{Y_{66}} \qquad (1 \le i < 6) \qquad (1 \le j \le 6). \tag{3.21}$$

Row 6 and column 6 are deleted from the Y matrix at the first step, however only the 6th row of A is deleted and 6 columns remain. This procedure is followed until only the input and output nodes remain, and then the Y matrix at this time is 2×2, and the A matrix is 2×6 with complex elements. Now we define the B and D matrix by

$$\begin{bmatrix} B \\ D \end{bmatrix} = [A]. \tag{3.22}$$

The correlation matrix C of our noise circuit model is

$$C = \begin{bmatrix} \overline{i_g i_g^*} & \overline{i_g i_d^*} & 0 & 0 & 0 & 0 \\ \overline{i_d i_g^*} & \overline{i_d i_d^*} & 0 & 0 & 0 & 0 \\ 0 & 0 & \overline{i_G i_G^*} & 0 & 0 & 0 \\ 0 & 0 & 0 & \overline{i_S i_S^*} & 0 & 0 \\ 0 & 0 & 0 & 0 & \overline{i_D i_D^*} & 0 \\ 0 & 0 & 0 & 0 & 0 & \overline{i_{DB} i_{DB}^*} \end{bmatrix}. \tag{3.23}$$

By using (3.16) to (3.18), and (3.10) to (3.13), we can directly calculate the noise parameters of MOSFETs.

3.3.2 Circuit Simulator Analysis

As mentioned above, the noise figure (NF) of a noisy two-port can be represented by its minimum noise figure (NF_{min}), equivalent noise resistance (R_n), and optimized source admittance (Y_{opt}) as shown in (3.1). Equation (3.1) can be rearranged to give

$$NF = A + \left(G_s + \frac{B_s^2}{G_s}\right) \cdot B + \frac{1}{G_s} \cdot C + \frac{B_s}{G_s} \cdot D \tag{3.24}$$

where G_S is the source conductance and B_S is the source susceptance. Then the four noise parameters can represented by

$$R_n = B, \tag{3.25}$$

$$G_{opt} = \frac{\sqrt{4BC - D^2}}{2B}, \tag{3.26}$$

$$B_{opt} = -\frac{D}{2B}, \tag{3.27}$$

and

$$NF_{min} = A + \sqrt{4BC - D^2}. \tag{3.28}$$

If we provide values for four sets of linearly independent source admittance (Y_S) and calculate the corresponding noise figure (*NF*), we obtain four linear equations and can solve for the four variables A, B, C, and D in (3.24). The four noise parameters can then be calculated from (3.25) to (3.28).

The next question is how to calculate the noise figure of a noisy two-port by using a circuit simulator? By definition, the noise figure is the signal-to-noise ratio at the input port divided by signal-to-noise ratio at the output port, i.e.

$$NF = \frac{\dfrac{S_{in}}{4kTR_s}}{\dfrac{G_a \cdot S_{in}}{G_a \cdot 4kTR_s + N_{DUT}}} = \frac{\overbrace{(G_a \cdot 4kTR_s + N_{DUT})/G_a}^{\text{noise power referred to the input port}}}{4kTR_s} \tag{3.29}$$

where G_a is the power gain of the device and N_{DUT} is the noise power at the output port generated by the device itself. In (3.29), the numerator of the second expression at the right hand side can be obtained from the square of INOISE which is the total output noise power referred to the input port and is usually calculated by a circuit simulator. Therefore, NF can be obtained by the square of INOISE divided by $4kTR_S$ where R_S is the real part of the source impedance $Z_s = 1/(G_s + jB_s)$.

Chapter 4

PARAMETER DE-EMBEDDING

4.1 NOISE PARAMETER DE-EMBEDDING

With the continuous downscaling of the device dimensions, the impact of the surrounding parasitics on a transistor characteristics has gained importance in the RF noise measurements [25],[26]. In [27], a noise de-embedding method based on a parallel-series configuration was presented. This method assumes that the distributed capacitive effect of metal interconnections between the probe pads and the transistor can be taken care of as a lumped element at the bonding pads (or signal pads) and the inductive and resistive effects are modelled in series with the transistor. This assumption is fine for lower frequency applications or for a test structure designed with special care. The question is up to what frequencies will this assumption be still valid and if the layout of any interconnection will satisfy this assumption? It might not be valid for long (or wide) interconnections or at operating frequencies of a few tens of GHz. In addition, the traditional methods treat the substrate coupling between the input and output pads (Y_{SUB} shown in fig. 4.1) which is modelled in parallel with the transistor as an extrinsic parasitic and de-embeds it from the measured parameters. However this is not correct because for all transistors fabricated on wafer, there is always a Y_{SUB} connected in parallel with each transistor and therefore we

should treat Y_{SUB} as a part of transistor performance and include it in the substrate model of a transistor.

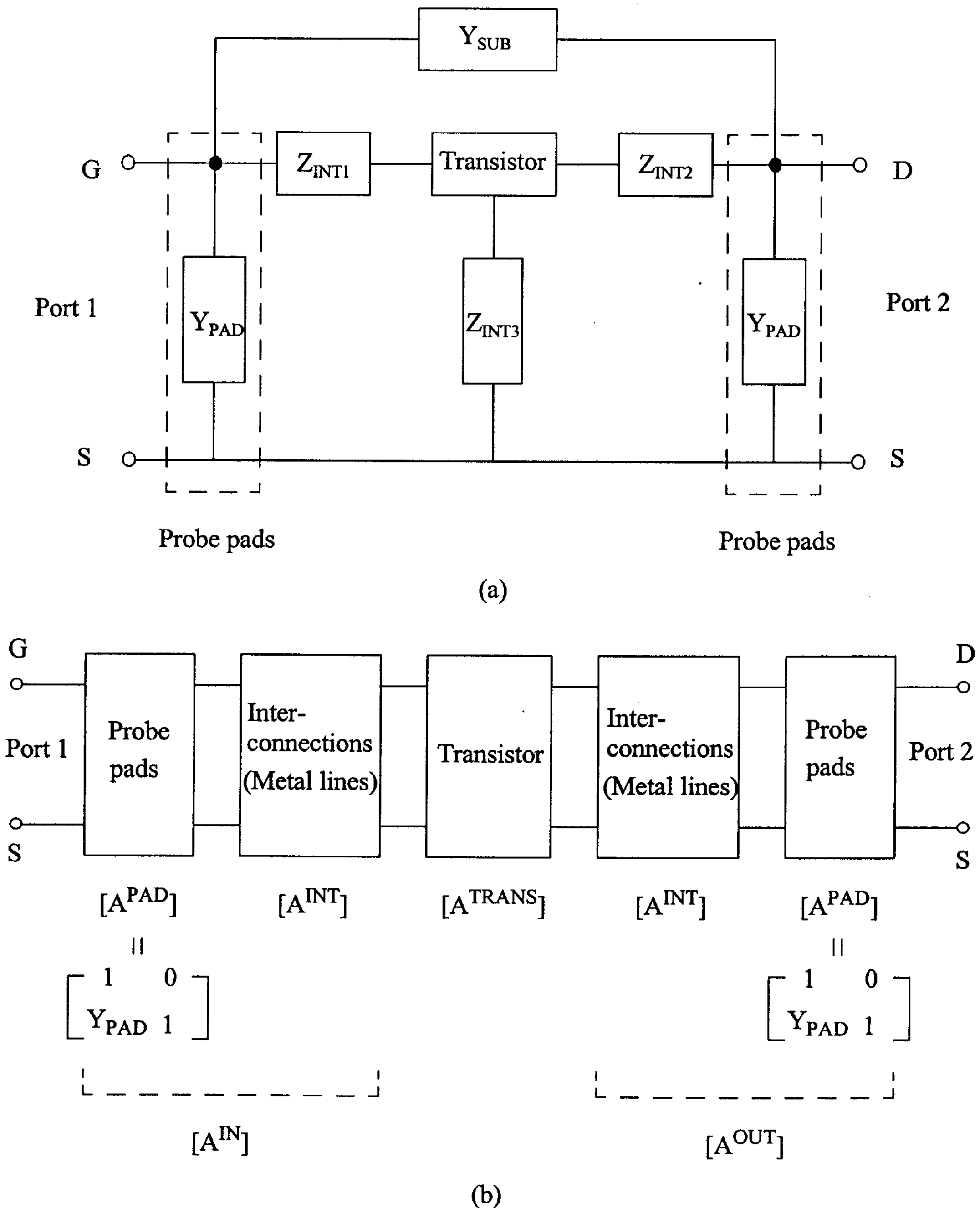

Fig. 4.1: Equivalent circuit diagram representing the structure of a DUT which includes probe pads, metal interconnections and a transistor modeled in (a) parallel-series and (b) cascade configurations.

Therefore, it is natural to model the DUT as probe pads, interconnections and the transistor connected in a cascade configuration. It is also preferable to develop a de-embedding method, which, from theory, has no frequency limitation (or to the frequency at which the discontinuity effect has to be taken into account), requires no equivalent circuit models of the pads or interconnections, and works for any geometry of interconnection designed without introducing more dummy structures. The method presented in [28] is based on a cascade configuration, but it requires specific equivalent circuit models for both probe pads and the metal interconnections. This means that the de-embedding results rely on the accuracy of the equivalent circuit models and the element values used in the calculation. In addition, this procedure is not easy to automate since the parasitic elements in the equivalent circuit model are both technology and design dependent.

In this chapter, a general noise and scattering parameter de-embedding procedure based on a cascade configuration without the requirement of any equivalent circuit model of probe pads and interconnections is presented [14],[15]. The de-embedded results are compared with those obtained from the de-embedding procedure based on the traditional parallel-series configuration.

4.2 DE-EMBEDDING ALGORITHM

De-embedding techniques are based on the noise power matrix first introduced by Haus and Adler [45] and later renamed the noise correlation matrix by Hillbrand and Russer [12]. In general, the DUT can be modeled by a physical equivalent circuit which is either in a parallel-series configuration (shown in fig. 4.1(a)) or in a cascade configuration (shown

in fig. 4.1(b)). In fig. 4.1(a), Y_{PAD} is the admittance between signal pads and ground, Y_{SUB} is the admittance between the input port and the output port and Z_{INT}'s are the impedances of the interconnections between the pads and the transistor.

The traditional procedure for noise parameter de-embedding [8],[27] is based on a parallel-series configuration carried out with the help of the "OPEN" and SHORT" dummy structures as shown in fig. 4.2.

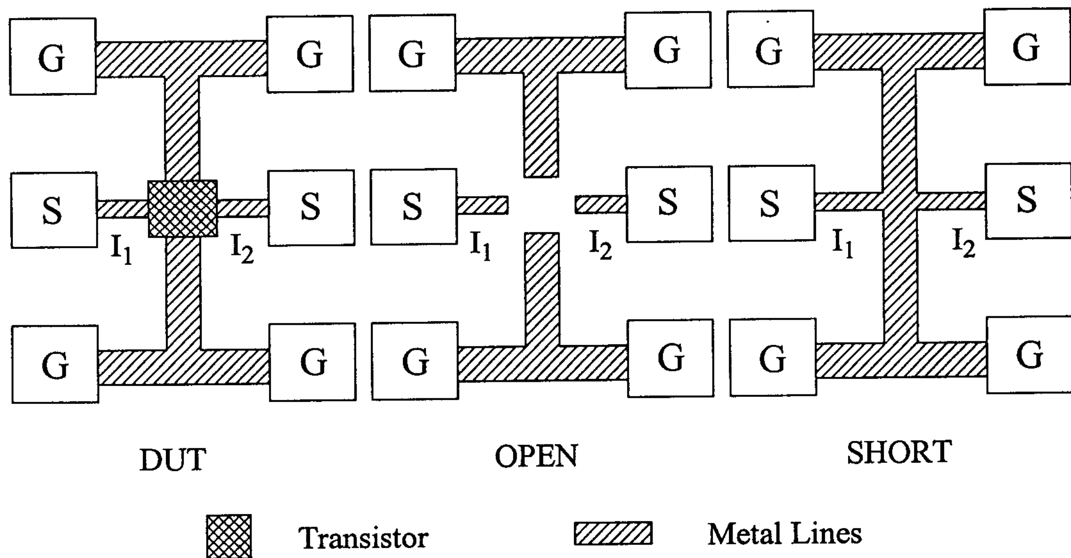

Fig. 4.2: A device-under-test (DUT) and its corresponding "OPEN" and "SHORT" dummy structures for the DUT modeled in the parallel-series configuration.

However, in this proposed de-embedding procedure, the DUT is modeled by the network of probe pads, interconnections and a transistor connected in a cascade configuration, and two new dummy "THRU" structures are introduced. This is presented in fig. 4.3. For the proposed dummy structures, the "OPEN" dummy structure consists of RF probe pads without the metal interconnections and the transistor, the "THRU1" dummy structure consists of the RF probe pads with the section of the interconnection at the input

port of the transistor in the DUT, and the "THRU2" dummy structure consists of the RF probe pads with the section of the interconnection at the output port of the transistor. The electrical chain matrices of the interconnections at the input and output ports of the DUT can be directly obtained from the s-parameter measurements of the two additional "THRU" dummy structures.

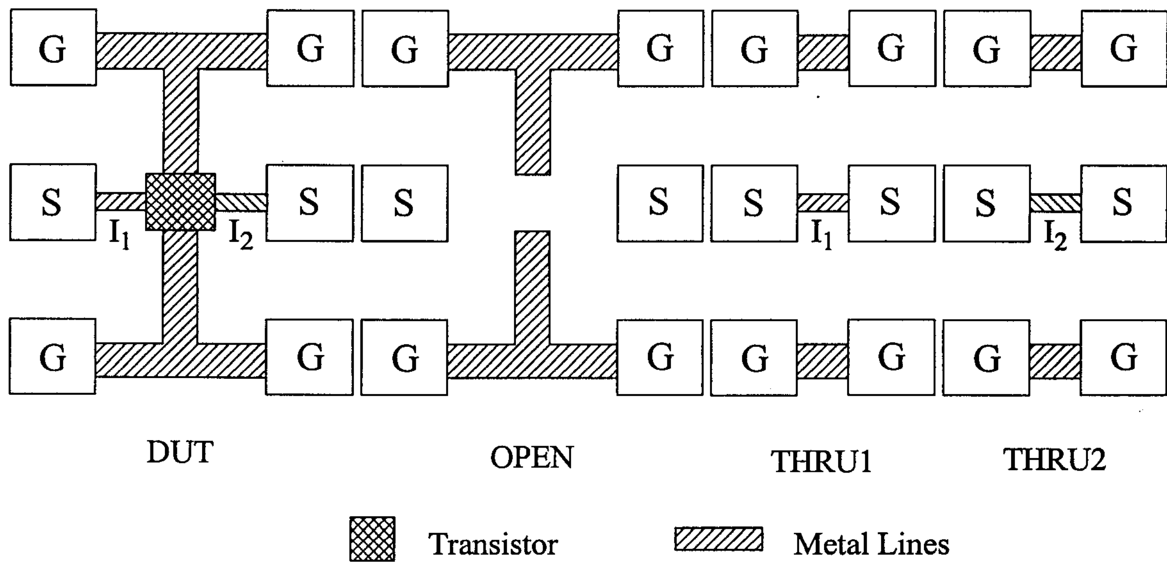

Fig. 4.3: A device-under-test (DUT) and its corresponding "OPEN", "THRU1" and "THRU2" dummy structures for the DUT modeled in the cascade configuration.

Based on the DUT and dummy structures shown in fig. 4.3, the procedure for noise parameter de-embedding, in detail, is as follows. The intrinsic chain (ABCD) parameters (or Z-parameters) of the devices can be obtained at the step 6 (or 7) in the procedure of the noise parameter de-embedding.

1. Measure the scattering parameters $[S^{DUT}]$, $[S^{OPEN}]$, $[S^{THRU1}]$ and $[S^{THRU2}]$ of the DUT, "OPEN", "THRU1" and "THRU2" dummy pads.

2. Measure the noise parameters - NF_{min}^{DUT}, Y_{opt}^{DUT} and R_n^{DUT} of the DUT and calculate the correlation matrix $[C_A^{DUT}]$ using

$$[C_A^{DUT}] = 2kT\begin{bmatrix} R_n^{DUT} & \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}(Y_{opt}^{DUT})^* \\ \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}Y_{opt}^{DUT} & R_n^{DUT}\left|Y_{opt}^{DUT}\right|^2 \end{bmatrix}. \quad (4.1)$$

3. Convert $[S^{OPEN}]$ to its Y parameters $[Y^{OPEN}]$ using

$$[Y] = \frac{\begin{bmatrix} (1-S_{11})(1+S_{22})+S_{12}S_{21} & -2S_{12} \\ -2S_{21} & (1+S_{11})(1-S_{22})+S_{12}S_{21} \end{bmatrix}}{Z_o \cdot [(1+S_{11})(1+S_{22})-S_{12}S_{21}]}, \quad (4.2)$$

calculate Y_{PAD} using

$$Y_{PAD} = Y_{11}^{OPEN} + Y_{12}^{OPEN} \text{ or } Y_{22}^{OPEN} + Y_{21}^{OPEN} \quad (4.3)$$

and the ABCD parameters of the input/output pads $[A^{PAD}]$ from

$$[A^{PAD}] = \begin{bmatrix} 1 & 0 \\ Y_{PAD} & 1 \end{bmatrix}. \quad (4.4)$$

4. Calculate the ABCD parameters $[A^{THRU1}]$ and $[A^{THRU2}]$ from $[S^{THRU1}]$ and $[S^{THRU2}]$ using the conversion formula

$$[A] = \frac{1}{2S_{21}}\begin{bmatrix} (1+S_{11})(1-S_{22})+S_{12}S_{21} & [(1+S_{11})(1+S_{22})-S_{12}S_{21}]\cdot Z_o \\ [(1-S_{11})(1-S_{22})-S_{12}S_{21}]/Z_o & (1-S_{11})(1+S_{22})+S_{12}S_{21} \end{bmatrix} \quad (4.5)$$

where Z_o is the system characteristic impedance.

5. Calculate the ABCD parameters [A^{IN}] and [A^{OUT}] which include the parasitic effects of probe pads and interconnections in cascade at the input and output ports from

$$[A^{IN}] = [A^{THRU1}][A^{PAD}]^{-1} \tag{4.6}$$

and

$$[A^{OUT}] = [A^{PAD}]^{-1}[A^{THRU2}]. \tag{4.7}$$

where the superscript "-1" denotes the inverse of the matrix.

6. Convert [S^{DUT}] to its ABCD parameters [A^{DUT}] using (4.5) and calculate the ABCD parameters [A^{TRANS}] of the intrinsic device from

$$[A^{TRANS}] = [A^{IN}]^{-1}[A^{DUT}][A^{OUT}]^{-1}. \tag{4.8}$$

7. Convert the ABCD parameters [A^{IN}] and [A^{OUT}] to their Z parameters [Z^{IN}] and [Z^{OUT}] with the conversion formula

$$[Z] = \frac{1}{C}\begin{bmatrix} A & AD-BC \\ 1 & D \end{bmatrix}. \tag{4.9}$$

8. Calculate the correlation matrix [C_Z^{IN}] and [C_Z^{OUT}] which include parasitic effects from the probe pads and interconnections in cascade at the input and output ports from

$$[C_Z^{IN}] = 2kT\Re([Z^{IN}]) \tag{4.10}$$

and

$$[C_Z^{OUT}] = 2kT\Re([Z^{OUT}]) \tag{4.11}$$

where $\Re(\,)$ stands for the real part of the elements in the matrix.

9. Convert the $[C_Z^{IN}]$ and $[C_Z^{OUT}]$ matrixes to their $[C_A^{IN}]$ and $[C_A^{OUT}]$ correlation matrixes with the conversion formula

$$[C_A^{IN}] = [T^{IN}][C_Z^{IN}][T^{IN}]^{\dagger} \quad (4.12)$$

and

$$[C_A^{OUT}] = [T^{OUT}][C_Z^{OUT}][T^{OUT}]^{\dagger} \quad (4.13)$$

where the transformation matrix $[T^{IN}]$ and $[T^{OUT}]$ are

$$[T^{IN}] = \begin{bmatrix} 1 & -A_{11}^{IN} \\ 0 & -A_{21}^{IN} \end{bmatrix} \quad (4.14)$$

and

$$[T^{OUT}] = \begin{bmatrix} 1 & -A_{11}^{OUT} \\ 0 & -A_{21}^{OUT} \end{bmatrix}. \quad (4.15)$$

10. Calculate the correlation matrix $[C_A]$ of the intrinsic transistor using

$$[C_A] = [A^{IN}]^{-1}([C_A^{DUT}] - [C_A^{IN}])([A^{IN}]^{\dagger})^{-1} - [A^{TRANS}][C_A^{OUT}][A^{TRANS}]^{\dagger}. \quad (4.16)$$

11. Calculate the noise parameters - NF_{min}, Z_{opt} and R_n of the intrinsic transistor from the noise correlation matrix $[C_A]$ by

$$NF_{min} = 1 + \frac{1}{kT}\left(\Re(C_{12A}) + \sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2}\right), \quad (4.17)$$

$$Y_{opt} = \frac{\sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2} + i\Im(C_{12A})}{C_{11A}} \quad (4.18)$$

and

$$R_n = \frac{C_{11A}}{2kT}. \tag{4.19}$$

In step 7, the reason for transforming the ABCD parameters [A^{IN}] and [A^{OUT}] to their Z parameters for calculating the correlation Z matrixes instead of to their Y parameters to calculate the correlation Y matrix is to avoid the singularity error for the designs without the interconnections during the transformation.

4.3 MEASUREMENTS AND DISCUSSIONS

In order to test the de-embedding procedure based on the cascade configuration and to compare it with the traditional de-embedding procedure, three different DUTs - PAD50×40M, INT160L and INT160R (as shown in fig. 4.4) and their corresponding dummy structures - "OPEN", "SHORT", "THRU1" and "THRU2", are designed for the verification of the algorithm. All test structures are designed as ground-signal-ground (GSG) configurations and fabricated in a standard 0.35 μm CMOS technology through the Canadian Microelectronics Corporation (CMC). The scattering and noise parameters are measured by using the ATN NP5B S-Parameter and Noise Parameter Measurement System (0.3 - 6 GHz) and both de-embedding procedures are applied.

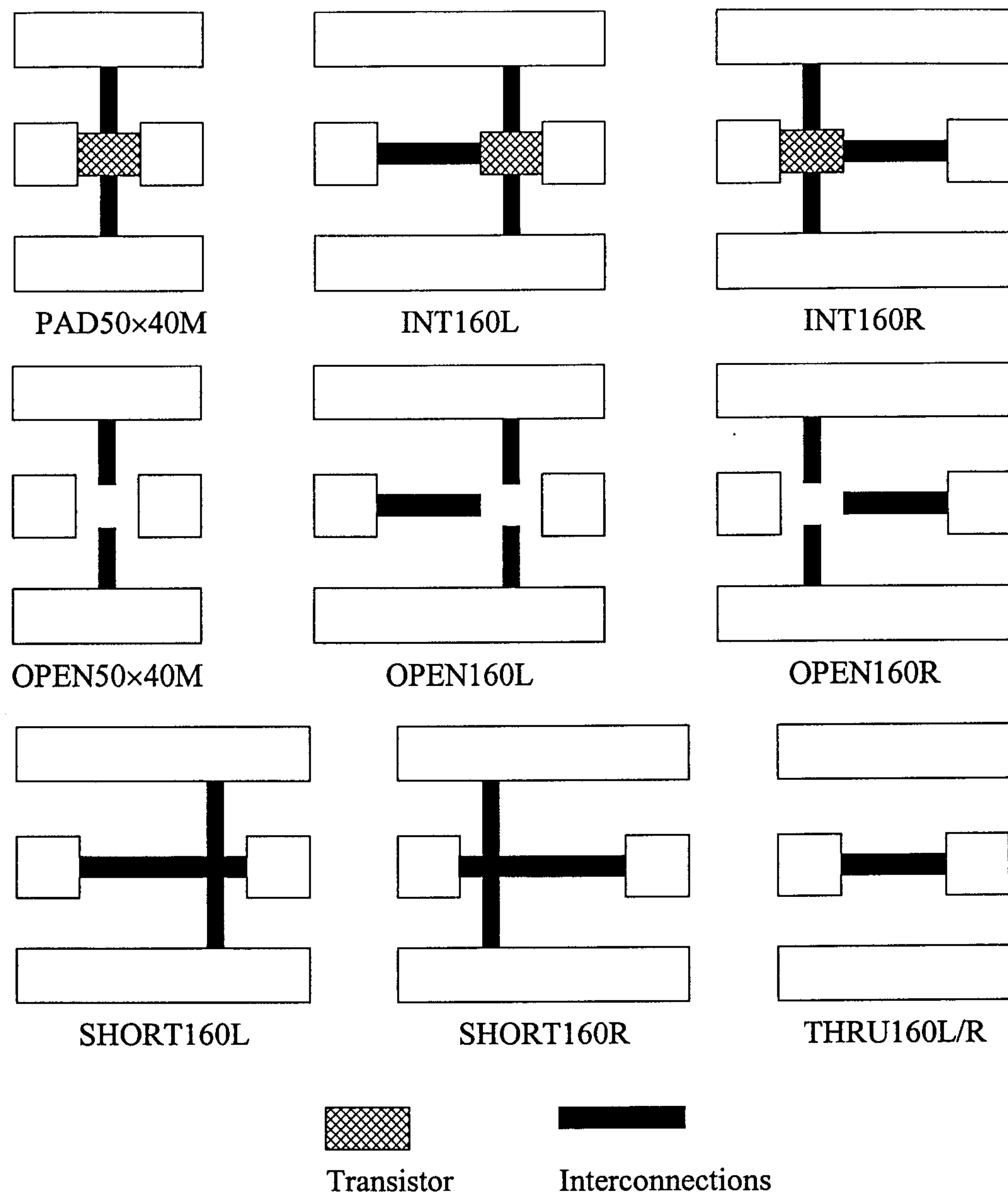

Fig. 4.4: Layouts of the test DUTs (PAD50×40M, INT160L and INT160R) and their corresponding dummy structures used in the de-embedding method based on the parallel-series configuration (OPEN50×40M, OPEN160L, OPEN160R, SHORT160L and SHORT 160R) and the proposed method based on the cascade configuration (OPEN50×40M and THRU160L/R) for the verification of the proposed de-embedding method.

In these structures, the dimensions of signal pads are 50μm×40μm (PAD50×40M) and the channel length and width of the transistor are 0.35 μm and 12 × 10μm (twelve 10 μm wide fingers in parallel), respectively. The dimensions of the metal interconnections at the input port (I_1) and output port (I_2) are approximately zero for PAD50×40M. For INT160L, I_1 is 160 μm × 1 μm and I_2 is ~ 0 μm^2 (the drain of the transistor is connected right next to the output pads). On the other hand, for INT160R, I_1 is ~ 0 μm^2 and I_2 is 160 μm × 1 μm (the gate of the transistor is connected right next to the input port).

Based on the layouts of three different "OPEN" structures - OPEN50×40M (I_1 = I_2 ≅ 0 μm^2 for PAD50×40M), OPEN160L (I_1 = 160μm × 1μm and I_2 ≅ 0 μm^2 for INT160L) and OPEN160R (I_1 ≅ 0 μm^2 and I_2 = 160μm × 1μm for INT160R) shown in fig. 4.4, in figs. 4.5 and 4.6, the measured Y_{11} and Y_{22} versus frequency characteristics are shown.

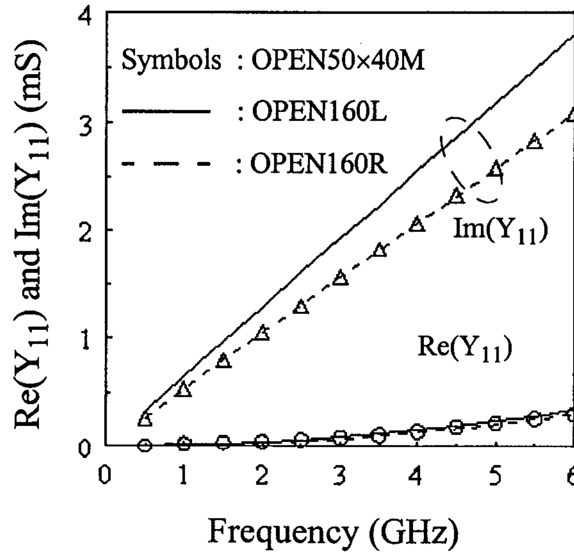

Fig. 4.5: Measured Y_{11} versus frequency characteristics of three "OPEN" dummy structures - OPEN50×40M (symbols), OPEN160L (solid lines) and OPEN160R (dashed lines).

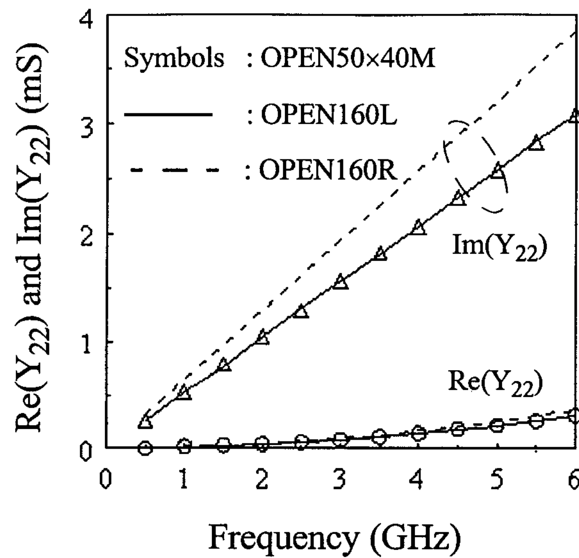

Fig. 4.6: Measured Y_{22} versus frequency characteristics of three "OPEN" dummy structures - OPEN50×40M (symbols), OPEN160L (solid lines) and OPEN160R (dashed lines).

It is shown that the metal interconnection introduces about 24% susceptance at 6 GHz, and this will increase at higher frequencies. In addition, the distributed capacitance of the interconnections should be connected in cascade with the signal pad and the transistor instead of being lumped into the signal pads.

For the de-embedded noise parameters, figs. 4.7 and 4.8 show the measured (squares) and de-embedded minimum noise figure (NF_{min}) and equivalent noise resistance (R_n) versus frequency characteristics of an INT160L biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V (I_{DS} = 7.8 mA) based on the cascade (solid circles) and the parallel-series (lines) configurations. The dummy structures used in the de-embedding method based on the parallel-series configuration are designed according to those shown in fig. 4.2 ("OPEN" and "SHORT" structures) and those shown in fig. 4.3 ("OPEN", "THRU1" and "THRU2" structures) are used in the method based on the cascade configuration.

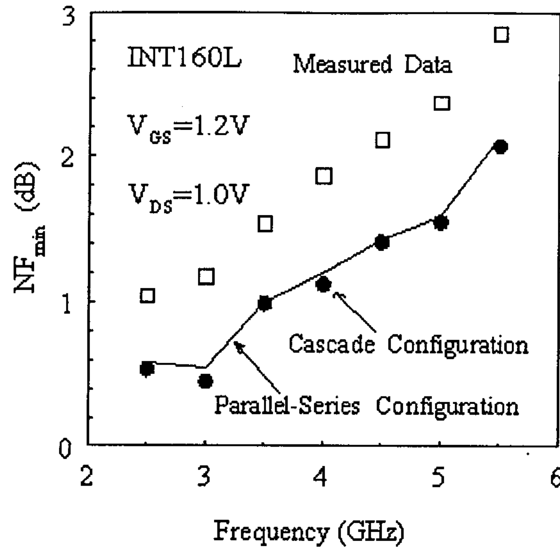

Fig. 4.7: Measured (squares) and de-embedded minimum noise figure (NF_{min}) versus frequency characteristics of an INT160L with an n-type MOSFET (L = 0.35μm and W = 12 × 10μm) biased at V_{DS} = 1.0V and V_{GS} = 1.2V (I_{DS} = 7.8mA) based on the cascade (solid circles) and parallel-series configurations (lines).

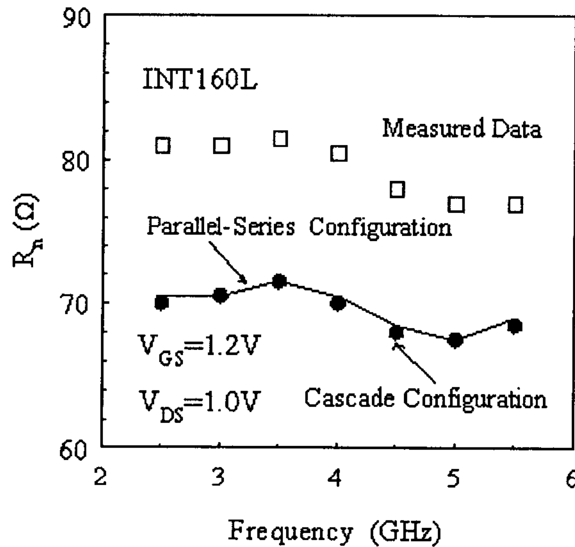

Fig. 4.8: Measured (squares) and de-embedded equivalent noise resistance (R_n) versus frequency characteristics of an INT160L with an n-type MOSFET (L = 0.35μm and W = 12 × 10μm) biased at V_{DS} = 1.0V and V_{GS} = 1.2V (I_{DS} = 7.8mA) based on the cascade (solid circles) and parallel-series configurations (lines).

In addition, figs. 4.9 and 4.10 show the measured (squares) and de-embedded optimized source resistance (R_{OPT}) and optimized source inductance (L_{OPT}) versus frequency characteristics of an INT160L biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V (I_{DS} = 7.8 mA) based on the cascade (solid circles) and the parallel-series (lines) configurations. It is shown that the de-embedding procedure based on the parallel-series configuration will give higher R_{OPT} and L_{OPT}, although the deference between the de-embedded NF_{min} and R_n based on cascade and parallel-series configurations are less than 1%. The reason for the higher R_{OPT} and L_{OPT} obtained based on the parallel-series configuration is because it gives smaller phase $\angle\Gamma_{OPT}$ than that obtained based on the cascade configuration. On the other hand, for the test structure PAD50×40M, only the OPEN dummy structure - OPEN50×40M which has no interconnection sections is used in parameter de-embedding and both methods give the same R_{OPT} and L_{OPT}. Therefore it is suspected that the smaller $\angle\Gamma_{OPT}$ obtained from the parallel-series configuration is caused by lumping the capacitive effects into the signal pads, and this configuration overestimates the admittance of the probe pads.

For INT160R, both methods give the same R_{OPT} and L_{OPT}, and this is not surprising because the overestimation of the admittance of the signal pads at the source side (input port) has more impact on the de-embedded noise parameters than that at the load side (output port). Therefore the traditional de-embedding methods are valid only when the admittance of the interconnects is much smaller than that of the signal pads at the frequencies of interest.

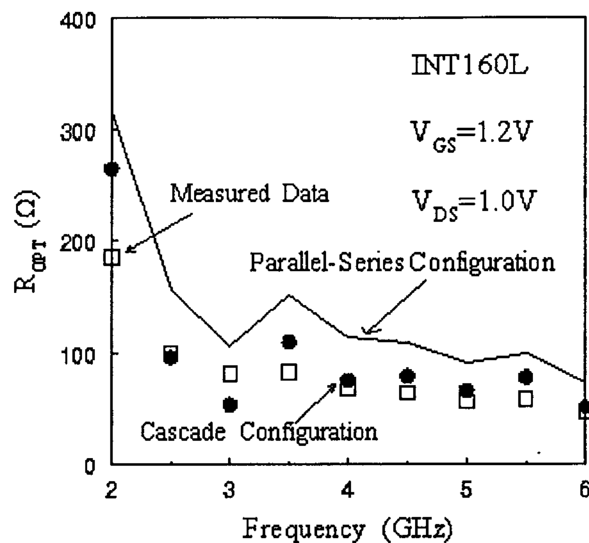

Fig. 4.9: Measured (squares) and de-embedded optimized source impedance (R_{OPT}) versus frequency characteristics of an INT160L with an n-type MOSFET (L = 0.35μm and W = 12 × 10μm) biased at V_{DS} = 1.0V and V_{GS} = 1.2V (I_{DS} = 7.8mA) based on the cascade (solid circles) and parallel-series configurations (lines).

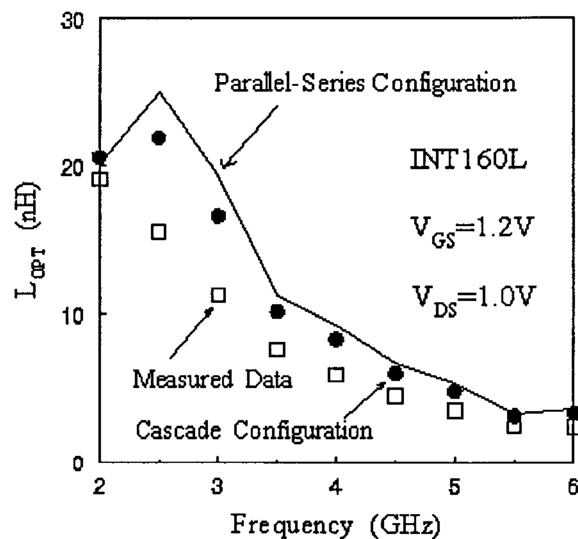

Fig. 4.10: Measured (squares) and de-embedded optimized source inductance (L_{OPT}) versus frequency characteristics of an INT160L with an n-type MOSFET (L = 0.35μm and W = 12 × 10μm) biased at V_{DS} = 1.0V and V_{GS} = 1.2V (I_{DS} = 7.8mA) based on the cascade (solid circles) and parallel-series configurations (lines).

For the effect of the metal interconnections at different locations of a DUT, figs. 4.11 and 4.14 show the measured (dashed lines with symbols) and de-embedded (symbols) noise parameters versus frequency characteristics of PAD50×40M (circles), INT160L (triangles) and INT160R (squares) biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V (I_{DS} = 7.8 mA) based on the cascade configuration. In fig. 4.11, it is shown that the metal interconnection (I_1) at the input port of a transistor has more impact on NF_{min} and R_n than that (I_2) at the output port because the resistive effect of the interconnection is amplified by the transistor to the output port. In addition, from measured and de-embedded R_n of PAD50×40M, the effect of probe pads will not affect the measured R_n of the transistor. Finally, figs. 4.11 to 4.14 show the de-embedded results for the three different test structures based on the cascade configuration.

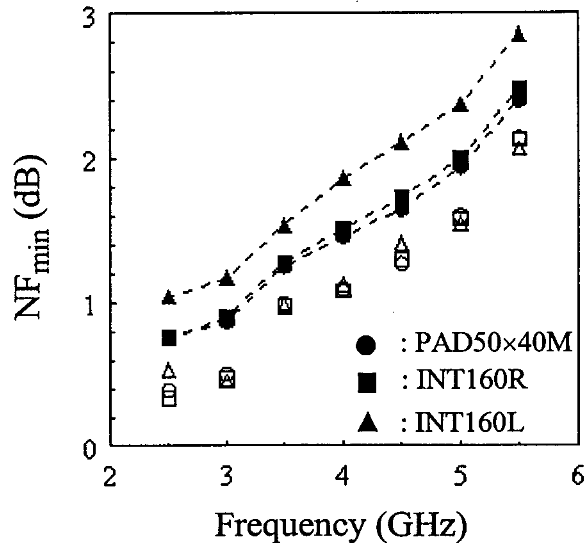

Fig. 4.11: Measured (dashed lines with symbols) and de-embedded (symbols) minimum noise figure (NF_{min}) versus frequency characteristics of PAD50×40M (circles), INT160L (triangles) and INT160R (squares) with an n-type MOSFET (L = 0.35μm and W = 12 × 10μm) biased at V_{DS} = 1.0V and V_{GS} = 1.2V (I_{DS} = 7.8mA) based on the cascade configuration.

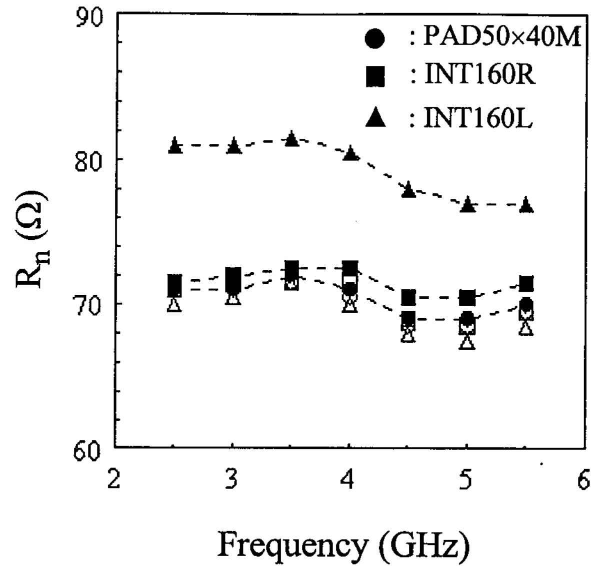

Fig. 4.12: Measured (dashed lines with symbols) and de-embedded (symbols) equivalent noise resistance (R_n) vs. frequency characteristics of PAD50×40M (circles), INT160L (triangles) and INT160R (squares) with an n-type MOSFET (L = 0.35μm and W = 12×10μm) biased at V_{DS} = 1.0V and V_{GS} = 1.2V (I_{DS}=7.8mA) based on the cascade configuration.

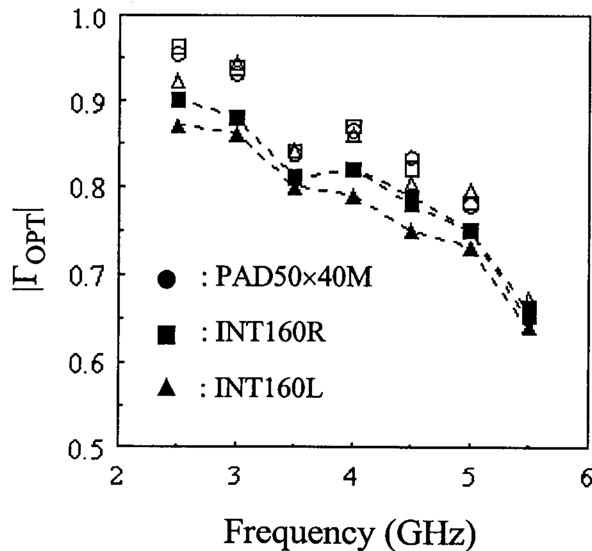

Fig. 4.13: Measured (dashed lines with symbols) and de-embedded (symbols) magnitude of optimized source reflection coefficient ($|\Gamma_{OPT}|$) vs. frequency characteristics of PAD50×40M (circles), INT160L (triangles) and INT160R (squares) based on the cascade configuration.

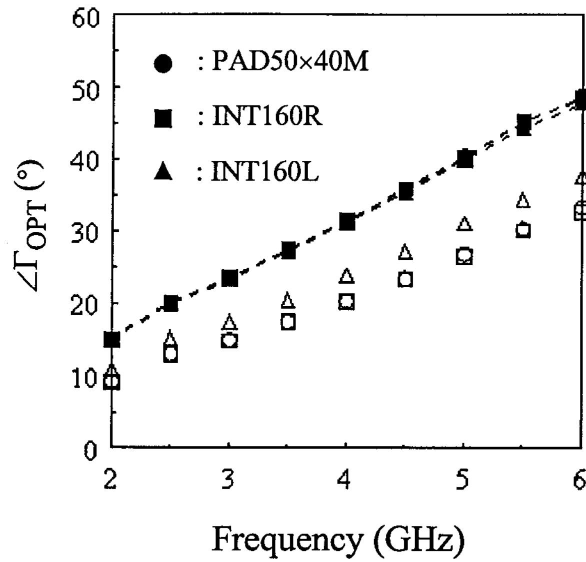

Fig. 4.14: Measured (dashed lines with symbols) and de-embedded (symbols) angles of optimized source reflection coefficient ($\angle\Gamma_{OPT}$) versus frequency characteristics of PAD50×40M (circles), INT160L (triangles) and INT160R (squares) with an n-type MOS-FET ($L = 0.35\mu m$ and $W = 12 \times 10\mu m$) biased at $V_{DS} = 1.0V$ and $V_{GS} = 1.2V$ ($I_{DS} = 7.8mA$) based on the cascade configuration.

Chapter 5

NOISE SOURCE EXTRACTION

5.1 EXTRACTION OF CHANNEL NOISE

With the very high unity-gain frequencies (f_T) of deep sub-micron MOSFETs of more than 100 GHz, many high-speed or radio-frequency (RF) integrated circuits (ICs) which were fabricated exclusively in III-V or bipolar technologies are likely to be implemented in CMOS technology because of its low cost and high levels of integration [1],[2]. However, when working at high frequencies with sub-micron devices, the noise generated within the device itself will play an increasingly important role in the overall noise performance of analog circuits, especially for the front-end transceiver. Therefore, an accurate noise model for the channel noise in MOSFETs is crucial for the design and simulation of RF CMOS circuits.

Presently, models of the channel noise that are physics-based are confirmed by the measured minimum noise figure (NF_{min}) of devices through the help of a device simulator or the device's small-signal model [29],[30],[46]. However, the accuracy of the small-signal model, the values of model parameters used in simulation and the noise model itself will all affect the simulated noise parameters. These factors make the confirmation of the noise model more difficult, even when accurate noise parameters were measured.

Therefore, obtaining the channel noise of MOSFETs directly from RF noise measurements is crucial for noise modeling. This chapter presents a method to obtain the channel noise directly from measurements of their DC characteristics, scattering parameters and RF noise parameters. Physics-based noise models can then be verified from the extracted channel noise results in a direct way.

5.1.1 Extraction Algorithm

As mentioned in Chapter 3, the noisy two-port may be represented by a noise-free two-port and two noise current sources, one at the input port (i_1) and the other at the output port (i_2). From (3.8) and (3.10), the power spectral density of i_2 can be obtained from

$$\frac{\overline{|i_2|^2}}{\Delta f} = 4kTR_n \cdot |Y_{21}|^2 \tag{5.1}$$

where k is the Boltzmann's constant, T is the absolute temperature, Y_{21} is the transadmittance from port 1 to port 2 of the noise-free two-port and R_n is the equivalent noise resistance which is a resistance cascaded at the input port that will produce the same amount of noise power spectral density as i_2 does at the output port.

At low frequencies, if we convert the noise current sources associated with the parasitic resistance to noise voltage sources and assume that all the capacitors in the equivalent noise circuits of BSIM3 [47],[48] (shown in fig. 5.1), MOS 9 [49],[50] (shown in fig. 5.2), EKV [51],[52] (shown in fig. 5.3) or other equivalent circuit models as shown in fig. 5.4 are open-circuited (i.e. all the admittances of the capacitors are approximately zero), the equivalent noise circuit can be simplified to that shown in fig. 5.5.

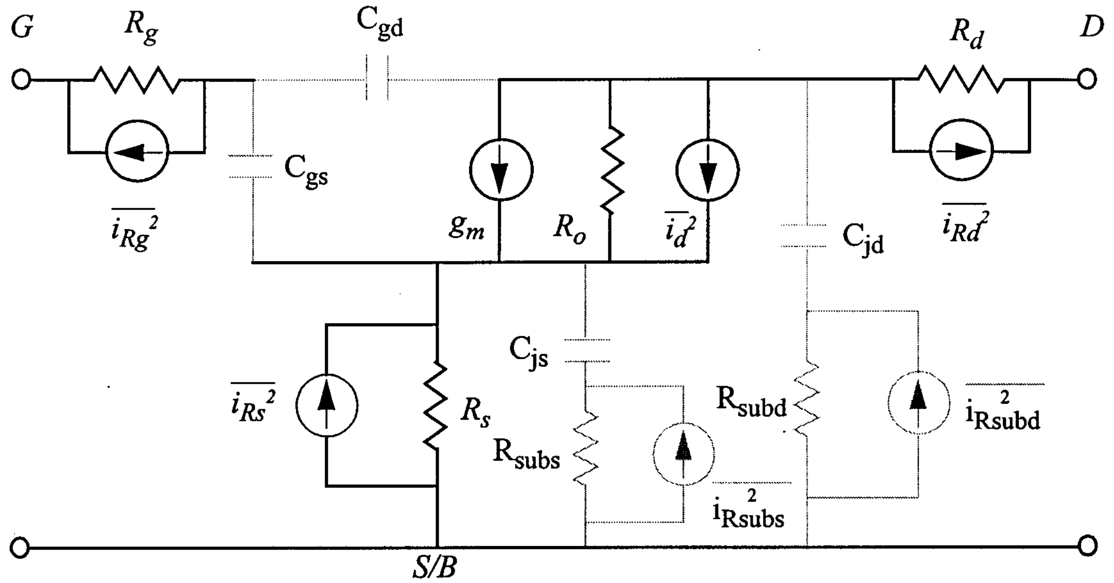

Fig. 5.1: BSIM3v3 RF noise model and its simplified noise equivalent circuit (parts with thicker lines) at DC or low frequencies [47],[48].

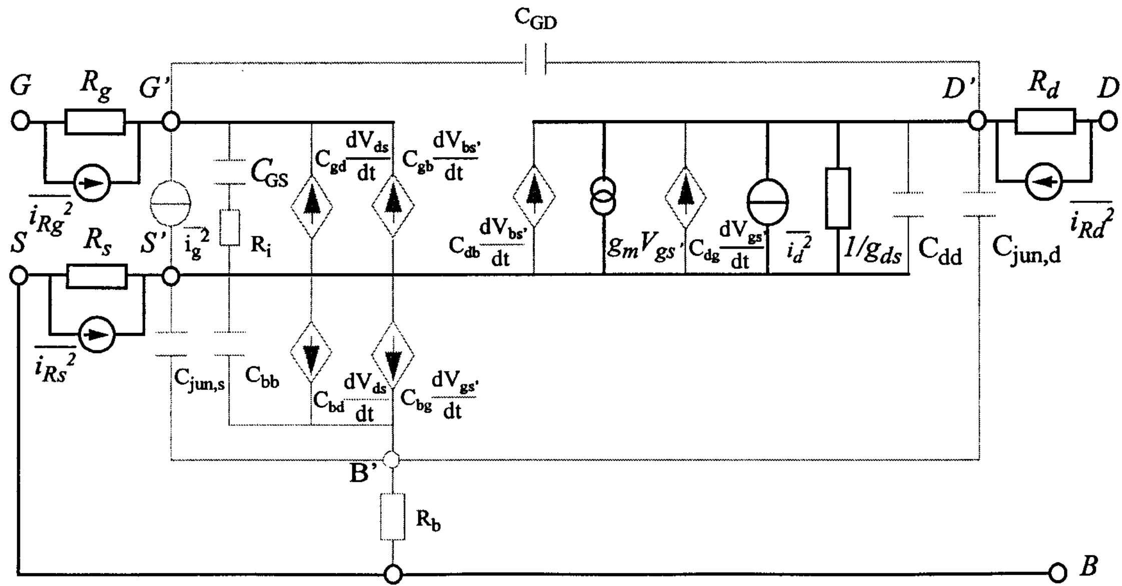

Fig. 5.2: Philips MOS 9 noise model and its simplified noise equivalent circuit (parts with thicker lines) at DC or low frequencies [49],[50].

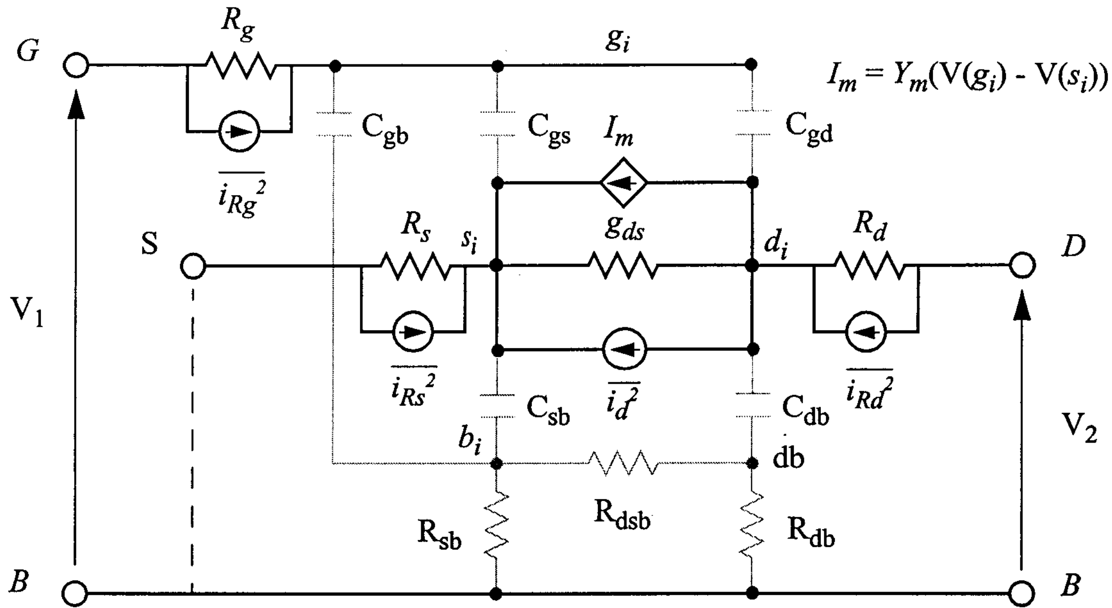

Fig. 5.3: EKV noise model and its simplified noise equivalent circuit (parts with thicker lines) at DC or low frequencies [51],[52].

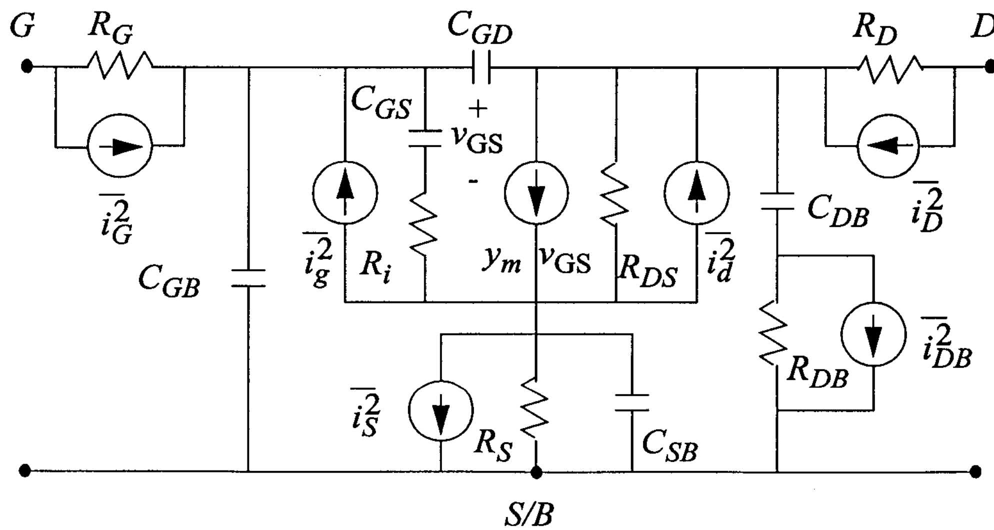

Fig. 5.4: A complete equivalent noise circuit model suitable for RF noise simulation with $y_m = g_m \times (1 - j\omega\tau)$.

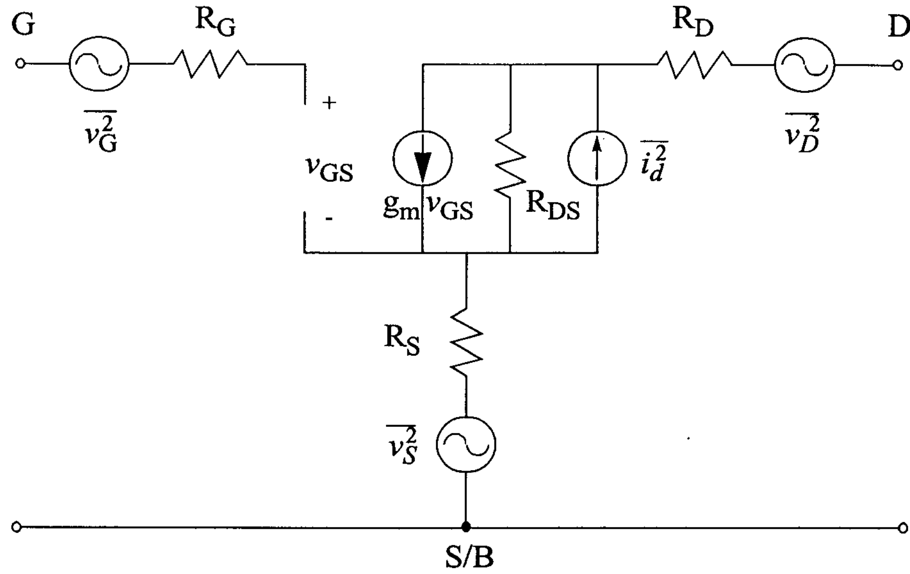

Fig. 5.5: Simplified equivalent noise circuit model at DC or lower frequency assuming all the capacitors are open-circuited and inductors are open-circuited [16],[17],[18],[53].

Here, the thermal noise sources associated with the resistance as well as the channel noise current have been included in the figure. Also, note that at low frequencies, the induced gate noise and its correlation with the channel noise tend to zero and have therefore been omitted from the figure [16],[17],[18],[53]. In fig. 5.5, $\overline{v_S^2}$ and $\overline{v_D^2}$ are the noise voltage sources of the source (R_S) and drain (R_D) resistances, and $\overline{v_G^2}$ is the noise voltage source of the polysilicon gate resistance (R_G) [16],[17],[18],[53].

From definition, the current noise power spectral density (Amp^2/Hz) of the total noise currents (i_2) at the output port can be obtained from

$$\frac{\overline{|i_2|^2}}{\Delta f} = \frac{\overline{|i_{Gout}|^2}}{\Delta f} + \frac{\overline{|i_{Sout}|^2}}{\Delta f} + \frac{\overline{|i_{Dout}|^2}}{\Delta f} + \frac{\overline{|i_{dout}|^2}}{\Delta f} \tag{5.2}$$

$$= 4kTR_n \cdot |Y_{21}|^2$$

where

$$Y_{21} = \frac{g_m R_{DS}}{g_m R_S R_{DS} + R_D + R_S + R_{DS}}. \tag{5.3}$$

Here, $\overline{i^2_{Gout}}$, $\overline{i^2_{Sout}}$, $\overline{i^2_{Dout}}$ and $\overline{i^2_{dout}}$ are the noise currents contributed at the output port by $\overline{v^2_G}$, $\overline{v^2_S}$, $\overline{v^2_D}$ and the channel noise ($\overline{i^2_d}$) respectively, and they are given by

$$\frac{\overline{|i_{Gout}|^2}}{\Delta f} = 4kTR_G \cdot \left(\frac{g_m R_{DS}}{g_m R_S R_{DS} + R_D + R_S + R_{DS}}\right)^2, \tag{5.4}$$

$$\frac{\overline{|i_{Sout}|^2}}{\Delta f} = 4kTR_S \cdot \left(\frac{1 + g_m R_{DS}}{g_m R_S R_{DS} + R_D + R_S + R_{DS}}\right)^2, \tag{5.5}$$

$$\frac{\overline{|i_{Dout}|^2}}{\Delta f} = 4kTR_D \cdot \left(\frac{1}{g_m R_S R_{DS} + R_D + R_S + R_{DS}}\right)^2, \tag{5.6}$$

and

$$\frac{\overline{|i_{dout}|^2}}{\Delta f} = \overline{|i_d|^2} \cdot \left(\frac{R_{DS}}{g_m R_S R_{DS} + R_D + R_S + R_{DS}}\right)^2. \tag{5.7}$$

The induced gate noise ($\overline{i^2_g}$) and its correlation with the channel noise are negligible at low frequencies and are therefore neglected in (5.2). In addition, because C_{DB} causes an open circuit at low frequencies, then there is no noise current contributed by $\overline{i^2_{DB}}$ at the output port. Substituting (5.3) - (5.7) into (5.2), the power spectral density of the channel noise in MOSFETs can be calculated from [16],[17],[18],[53]

$$\overline{|i_d|^2} = 4kT \cdot \left[(R_{no} - R_G - R_S)g_m^2 - \frac{2g_m R_S}{R_{DS}} - \frac{R_D + R_S}{R_{DS}^2}\right] \tag{5.8}$$

where R_{no} is the equivalent noise resistance extrapolated at low frequencies from the measured R_n versus frequency characteristics.

5.1.2 Measurements and Discussions

The device-under-test (DUT) is a 0.36 μm n-channel MOSFET which consists of ten 12 μm wide transistors connected in parallel. It was fabricated in a 0.25 μm CMOS technology by Conexant Systems Inc. The device is biased at V_{DS} = 1.0 V and V_{GS} = 0.9 V (I_{DS} = 3.09 mA, and the unity-gain frequency f_T = 16.3 GHz). Based on the measured s-parameters and the parameter extraction method described in [55] to obtain the element values in the small-signal model, the extracted values of the model elements in fig. 5.4 are g_m = 16.5 mS, R_G = 9.2 Ω, R_S = R_D = 1.1 Ω, R_i = 9.9 Ω, R_{DS} = 2.6 kΩ, R_{DB} = 11.5 Ω, C_{GB} = 0 F, C_{GS} = 133 fF, C_{GD} = 36.8 fF, and C_{DB} = 125 fF.

The last extracted parameter used in (5.8) is R_{no}. By extrapolating the R_n versus frequency characteristics (shown in fig. 5.6) at low frequencies, R_{no} is 80 Ω for this bias condition. Based on these element values and (5.8), the power spectral density of the channel noise ($\overline{i_d^2}$) in this device is 3.18×10^{-22} Amp^2/Hz at this bias condition.

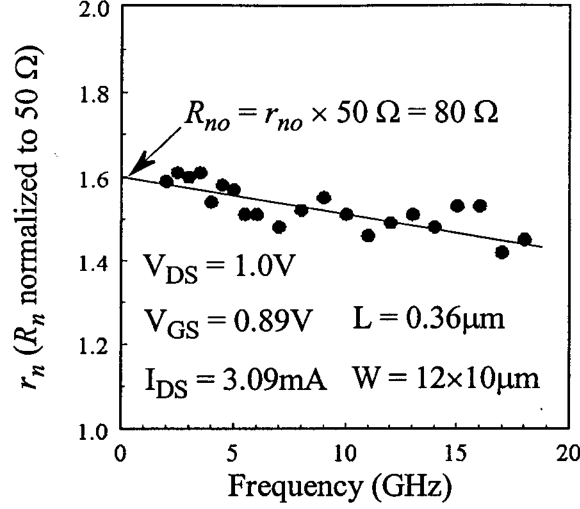

Fig. 5.6: Extraction of R_{no} from the measured equivalent noise resistance vs. frequency characteristics.

In order to confirm the extracted $\overline{i_d^2}$, the minimum noise figure NF_{min} and equivalent noise resistance R_n are calculated based on the noise model shown in fig. 5.4 by using the calculation method described in Chapter 3. Figs. 5.7 and 5.8 show the measured and simulated NF_{min} and r_n (R_n normalized to 50 Ω) versus frequency characteristics of a 0.97 μm n-type MOSFET biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V by using the measured y-parameters without including the induced gate noise ($\overline{i_g^2}$ in fig. 5.4) and its correlation with the channel noise $\overline{i_g i_d^*}$. It is shown that using the extracted channel noise and the measured y-parameters, the extracted channel noise has a good prediction for the equivalent noise resistance r_n. The discrepancy between the measured and calculated NF_{min} is caused by not including the induced gate noise and its correlation with the channel noise. The extraction of $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ from intrinsic RF noise parameters of MOSFETS will be presented in next section.

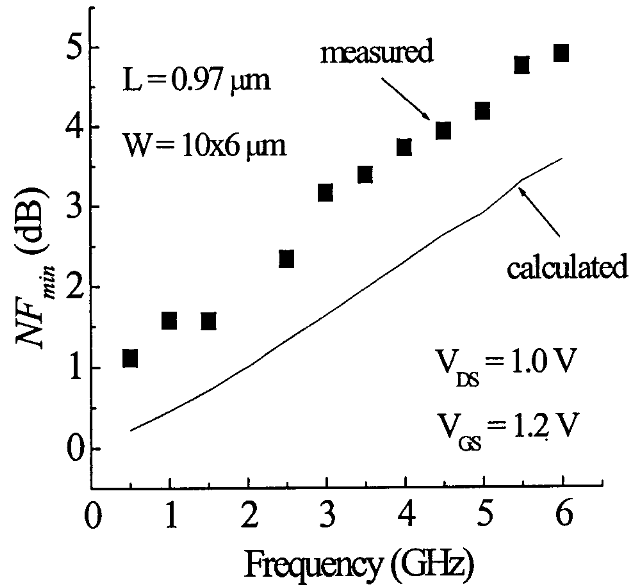

Fig. 5.7: Measured and simulated minimum noise figure NF_{min} versus frequency characteristics of a 0.97 μm n-type MOSFET.

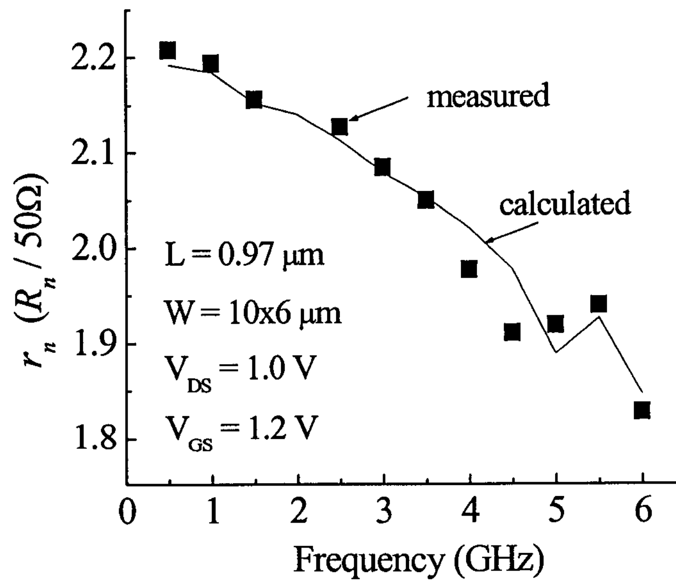

Fig. 5.8: Measured and simulated normalized equivalent noise resistance r_n versus frequency characteristics of a 0.97 μm n-type MOSFET.

Fig. 5.9 shows the extracted and calculated channel noise vs. bias current characteristics of a 0.36 μm n-type MOSFET biased at V_{DS} = 1.0 V. It shows that the calculated $\overline{i_d^2}$ based on the equations discussed in [54] -- $\overline{i_d^2} = 8kTg_m/3$, $\overline{i_d^2} = 8kTg_{do}/3$, or $\overline{i_d^2} = 8kT(g_m + g_{ds})/3$ -- cannot model the channel noise of MOSFETs biased in the saturation region. Also, the extracted channel noise is lower than the equivalent shot noise of the drain current due to the source-channel n^+-p junction.

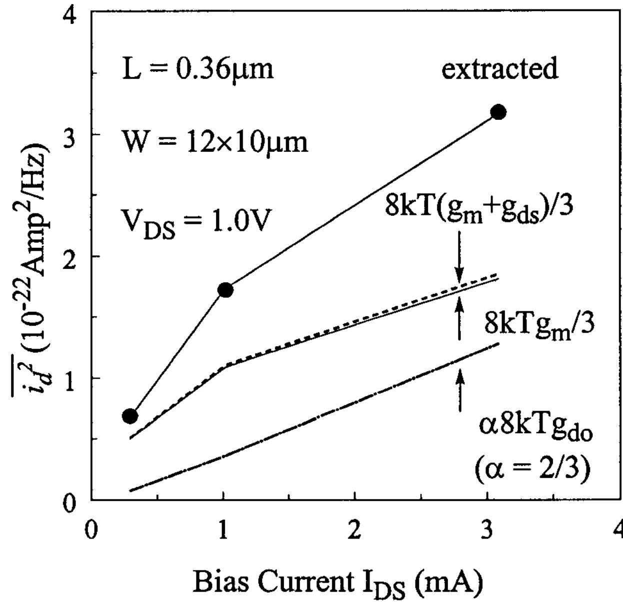

Fig. 5.9: Measured and calculated power spectral density of channel noise vs. bias current of a 0.36 μm n-type MOSFET.

Another set of the devices-under-test (DUTs) were fabricated in a 0.18 μm CMOS technology by Conexant Systems Inc. Five DUTs with channel width W = 10×6 μm and channel length L = 0.18 μm, 0.27 μm, 0.42 μm, 0.64 μm and 0.97 μm respectively were designed. The DC measurements were conducted at V_{DS} = 1.0 V with V_{GS} from 0.5 V to 2.0 V. In addition, the noise and s-parameter measurements of the five DUTs were

performed by using the ATN noise and s-parameter vector network analyzer measurement system. The measured results were de-embedded using the methods presented in [53],[56]. Figure 2 shows the extracted and calculated channel noise as a function of V_{GS} based on the equations $\overline{i_d^2}/\Delta f = 8kTg_m/3$, $\overline{i_d^2}/\Delta f = 8kT(g_m+g_{ds})/3$ and $\overline{i_d^2}/\Delta f = \gamma 4kTg_{do}$ with $\gamma = 2/3$ where g_{ds} is the output conductance and g_{do} is g_{ds} at $V_{DS} = 0$ V.

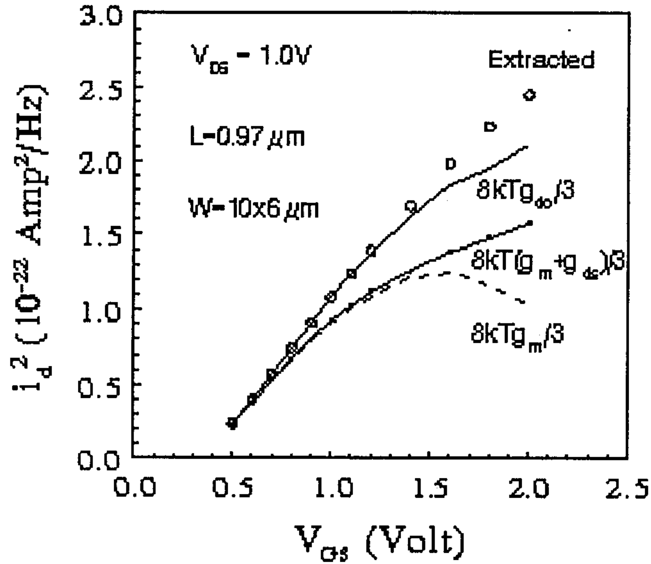

Fig. 5.10: Extracted and calculated $\overline{i_d^2}$ for the DUT with L = 0.97 μm and W = 10 × 6 μm biased at V_{DS} = 1.0 V.

In fig. 5.10, the parameters g_m and g_{ds} are extracted from the s-parameter measurements [8] and g_{do} is extracted from the I_{DS} vs. V_{DS} measurements. It is shown that $\overline{i_d^2}$ given by $8kTg_{do}/3$ predicts reasonably well the channel noise current density in long channel devices operated in the saturation region. However, the equations $\overline{i_d^2}/\Delta f = 8kTg_m/3$ and $\overline{i_d^2}/\Delta f = 8kT(g_m+g_{ds})/3$ give a wrong trend, especially in the high V_{GS} region. Fig. 5.11 shows the

extracted and calculated channel noise for short channel devices. It is shown that all three expressions underestimate the channel noise current. Therefore, they cannot be used for the noise current prediction of short channel devices.

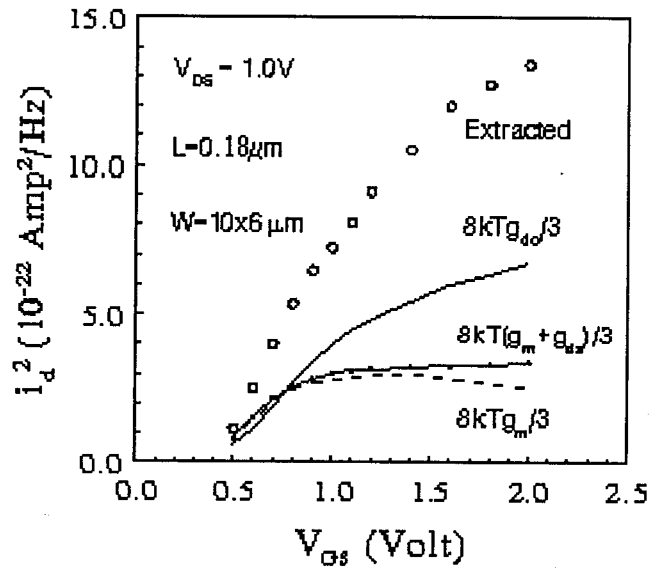

Fig. 5.11: Extracted and calculated $\overline{i_d^2}$ for the DUT with L = 0.18 μm and W = 10×6 μm biased at V_{DS} = 1.0 V.

Sometimes, circuit designers are interested in the value of γ used in the equation $\overline{i_d^2}/\Delta f = \gamma 4kTg_{do}$. Fig. 5.12 shows extracted γ as a function of V_{GS}. For long channel devices, γ is about 2/3 for the devices operated in the saturation region. However, as the channel length reduces, γ increases and is about 1.3 for 0.18μm devices. Fig. 5.13 shows the extracted γ as a function of different channel lengths at constant V_{GS} and V_{DS} biases.

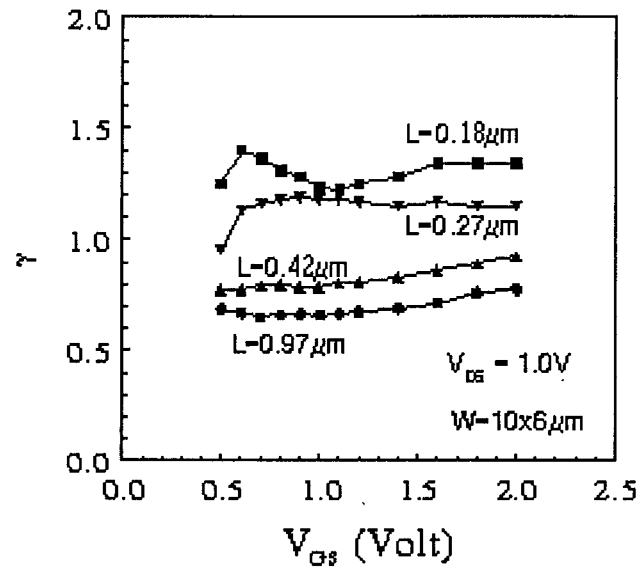

Fig. 5.12: Extracted γ ($\overline{i_d^2}/\Delta f = \gamma 4kTg_{do}$) as a function of V_{GS}.

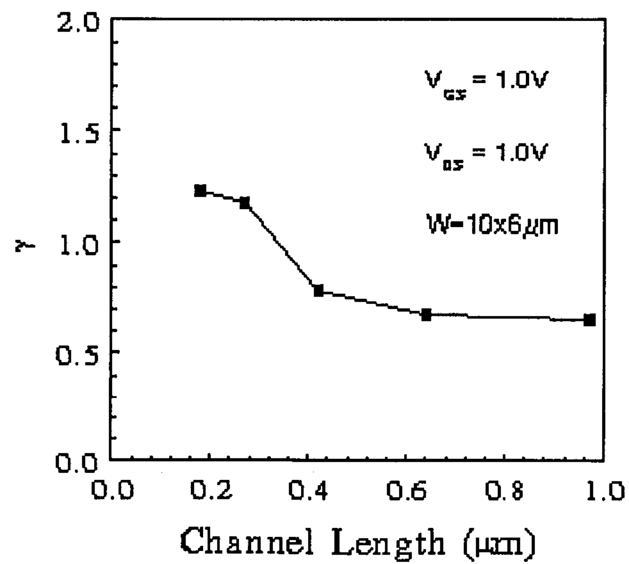

Fig. 5.13: Extracted γ ($\overline{i_d^2}/\Delta f = \gamma 4kTg_{do}$) as a function of different channel lengths.

Finally, fig. 5.14 shows the extracted channel noise as a function of V_{GS} for five different channel lengths. As expected [38],[57], the channel noise increases when the channel length decreases.

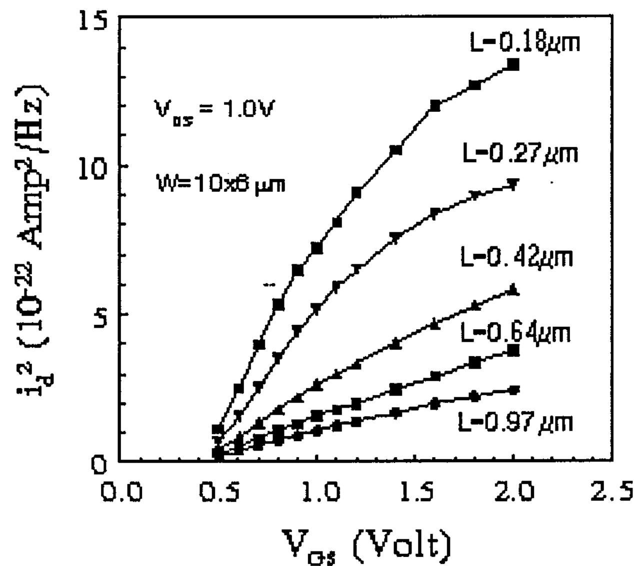

Fig. 5.14: Extracted channel noise as a function of V_{GS} for different channel length.

5.2 EXTRACTION OF INDUCED GATE NOISE

When transistors operate in the GHz range, the random potential fluctuations in the channel producing in the channel noise will be coupled to the gate terminal through the gate oxide capacitance and will cause the induced gate noise, which is usually correlated with the channel noise. Because of the difficulties in the extraction of the induced gate noise and its correlation term with the channel noise, several noise models [31],[32] and simulation results [33] have been presented, but they could not be verified directly with the noise sources obtained from RF noise measurements for deep submicron MOSFETs.

Therefore, obtaining the noise currents directly from RF noise measurements is crucial for the high-frequency noise modeling of deep submicron MOSFETs.

In this section, a systematic procedure to extract the induced gate noise ($\overline{i_g^2}$), channel noise ($\overline{i_d^2}$) and their cross-correlation ($\overline{i_g i_d^*}$) directly from the s-parameter and RF noise parameter measurements is presented. With the help of the direct calculation technique presented in Chapter 3 for the noise parameters of transistors, the extracted noise currents are fed back to the equivalent noise model to calculate the four noise parameters - NF_{min}, R_n, R_{opt} and X_{opt} - and to compare them to the measured data for the verification of the extracted noise sources. After that, the extracted noise currents of the MOSFETs fabricated in a 0.18 μm CMOS process versus frequency, bias condition and channel length are presented and discussed.

5.2.1 Extraction Algorithm

Because the induced gate noise ($\overline{i_g^2}$) and its correlation with the channel noise ($\overline{i_g i_d^*}$) shown in fig. 5.15 are frequency dependent, they have to be extracted at each measured frequency. This section describes a general and systematic procedure for any equivalent noise circuit to extract the power spectral densities of $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ [19],[20]. Note that a similar procedure can be applied to bipolar junction transistors.

For any given noise equivalent circuit (e.g. the one shown in fig. 5.15), we define the internal part which consists of C_{GS}, C_{GD}, R_i, g_m, R_{DS}, $\overline{i_g^2}$ and $\overline{i_d^2}$, as a two-port network with port 3-3' as port 1 and port 4-4' as port 2. On the other hand, the external part which includes all the components outside of the dashed box in fig. 5.15, such as R_G, C_{GB}, R_S,

R_{SB}, R_{DB}, C_{DB} and R_D, is characterized as a four port network with port 1-1' as port 1, port 2-2' as port 2, port 3-3' as port 3, and port 4-4' as port 4. Note that ports 1-1' and 2-2' do not share a common reference terminal with the ports 3-3' and 4-4'.

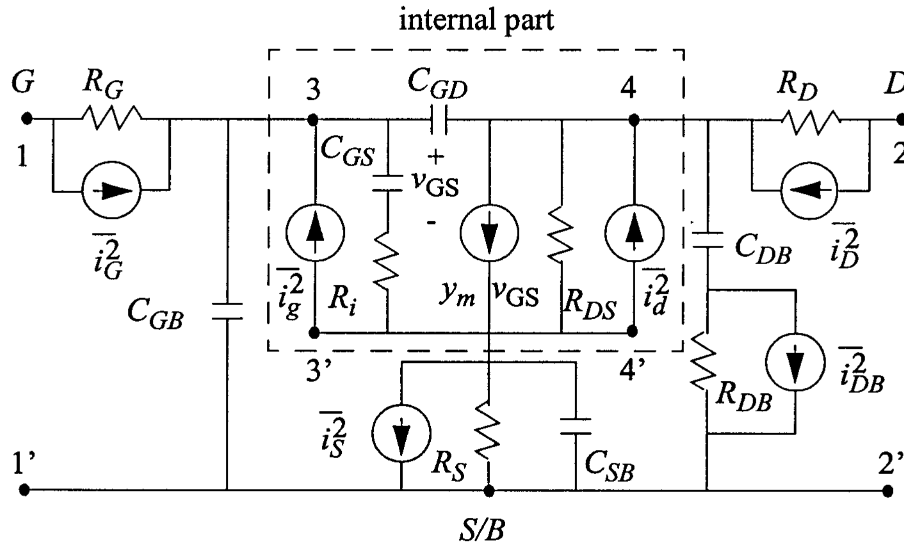

Fig. 5.15: A complete equivalent noise circuit model suitable for RF noise simulation with $y_m = g_m \times (1\text{-}j\omega\tau)$.

Using the DUT and the dummy structures described in section 4.2, the induced gate noise, channel noise and their correlation in MOSFETs can be extracted by using the following 15-step procedure [19],[20].

1. Measure the scattering parameters $\boldsymbol{S_{DUT}}$, $\boldsymbol{S_{OPEN}}$, $\boldsymbol{S_{THRU1}}$ and $\boldsymbol{S_{THRU2}}$ of the DUT, OPEN, THRU1 and THRU2 dummy structures, respectively.
2. Measure the noise parameters, $NF_{min,DUT}$, $Y_{opt,DUT}$ and $R_{n,DUT}$ of the DUT.
3. Perform a parameter de-embedding to get the intrinsic scattering ($\boldsymbol{Y_{dev}}$) and noise parameters ($NF_{min,dev}$, $Y_{opt,dev}$ and $R_{n,dev}$) [14],[15].

4. Perform a parameter extraction based on $\boldsymbol{Y_{dev}}$ and other measured data to get all the element values (e.g. g_m, C_{GS}, C_{GD},... etc.) in the RF noise model [58].

5. Calculate the chain correlation matrix $\boldsymbol{C_{Adev}}$ of the transistor based on the intrinsic noise parameters by

$$C_{Adev} = 2kT_o \begin{bmatrix} R_{n,dev} & \frac{NF_{min,dev}-1}{2} - R_{n,dev}(Y_{opt,dev})^* \\ \frac{NF_{min,dev}-1}{2} - R_{n,dev}Y_{opt,dev} & R_{n,dev}|Y_{opt,dev}|^2 \end{bmatrix} \quad (5.9)$$

where k is Boltzmann's constant, T_o is the standard reference temperature (290°K) and the asterisk denotes the complex conjugate.

6. Calculate the four-port admittance matrix $\boldsymbol{Y_{extr}}$ of the extrinsic part in the RF transistor model by excluding C_{gs}, C_{gd}, g_m, R_{DS} and R_i which define the intrinsic part, and partition $\boldsymbol{Y_{extr}}$ as [59]

$$Y_{extr} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \quad (5.10)$$

where the submatrixes - $\boldsymbol{Y_{ee}}$, $\boldsymbol{Y_{ei}}$, $\boldsymbol{Y_{ie}}$ and $\boldsymbol{Y_{ii}}$ are 2×2 matrixes.

7. Calculate the two-port admittance matrix $\boldsymbol{Y_{intr}}$ of the intrinsic part in the RF transistor model.

8. Calculate the matrix $\boldsymbol{D}$ as follows

$$D = -Y_{ei}(Y_{ii} + Y_{intr})^{-1}. \quad (5.11)$$

9. Convert the noise correlation matrix $\boldsymbol{C_{Adev}}$ to its admittance form $\boldsymbol{C_{Ydev}}$ by using

$$C_{Ydev} = T_Y C_{Adev} T_Y^{\dagger} \quad (5.12)$$

where the † in $T_Y^{\dagger}$ denotes Hermitian conjugation (transpose and complex conjugate) and the transformation matrix T_Y is given by

$$T_Y = \begin{bmatrix} -Y_{11,dev} & 1 \\ -Y_{21,dev} & 0 \end{bmatrix}. \tag{5.13}$$

10. Calculate the admittance noise correlation matrix C_{Yextr} of the extrinsic part by [60]

$$C_{Yextr} = kT(Y_{extr} + Y_{extr}^{\dagger}) \tag{5.14}$$

or

$$C_{Yextr} = 2kT\Re(Y_{extr}) \tag{5.15}$$

where T is the device temperature, $\Re()$ denotes for the real part of the matrix elements. Partition C_{Yextr} as

$$C_{Yextr} = \begin{bmatrix} C_{ee} & C_{ei} \\ C_{ie} & C_{ii} \end{bmatrix} \tag{5.16}$$

where the submatrixes - C_{ee}, C_{ei}, C_{ie} and C_{ii} are 2×2 matrixes.

11. Calculate the admittance correlation matrix C_{Yintr} of the intrinsic part in the RF transistor model from

$$C_{Yintr} = D_i(C_{Ydev} - C_{ee})D_i^{\dagger} - C_{ie}D_i^{\dagger} - D_iC_{ei} - C_{ii} \tag{5.17}$$

where $D_i = D^{-1}$.

12. Convert Y_{intr} to its chain representation A_{intr} using the conversion formula

$$A_{intr} = \frac{-1}{Y_{21,\,intr}} \begin{bmatrix} Y_{22,\,intr} & 1 \\ Y_{11,\,intr}Y_{22,\,intr} - Y_{12,\,intr}Y_{21,\,intr} & Y_{11,\,intr} \end{bmatrix}. \tag{5.18}$$

13. Convert C_{Yintr} to its chain matrix form C_{Aintr} by using

$$C_{Aintr} = T_A C_{Yintr} T_A^{\dagger} \tag{5.19}$$

where T_A is given by

$$T_A = \begin{bmatrix} 0 & A_{12,\,intr} \\ 1 & A_{22,\,intr} \end{bmatrix}. \tag{5.20}$$

14. Calculate the noise parameters, NF_{min}, Y_{opt} and R_n of the intrinsic part in the RF transistor model from the noise correlation matrix C_{Aintr} by using the following expressions.

$$NF_{min} = 1 + \frac{1}{kT_o}\left(\Re(C_{12A,intr}) + \sqrt{C_{11A,intr}C_{22A,intr} - (\Im(C_{12A,intr}))^2}\right) \tag{5.21}$$

$$Y_{opt} = \frac{\sqrt{C_{11A,intr}C_{22A,intr} - (\Im(C_{12A,intr}))^2} + j\Im(C_{12A,intr})}{C_{11A,intr}}, \tag{5.22}$$

and

$$R_n = \frac{C_{11A,intr}}{2kT_o} \tag{5.23}$$

where $\Im()$ stands for the imaginary part of elements and j is the imaginary unit.

15. Calculate the power spectral density of the channel noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$ and their correlation $\overline{i_g i_d^*}$ from

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kT_o R_n |Y_{21,intr}|^2, \tag{5.24}$$

$$\frac{\overline{|i_g|^2}}{\Delta f} = 4kT_oR_n\{|Y_{opt}|^2 - |Y_{11,intr}|^2 + 2\Re[(Y_{11,intr} - Y_{cor})Y_{11,intr}^*]\}, \quad (5.25)$$

and

$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT_o(Y_{11,intr} - Y_{cor})R_nY_{21,intr}^* \quad (5.26)$$

where Y_{cor} is given by

$$Y_{cor} = \frac{NF_{min} - 1}{2R_n} - Y_{opt}. \quad (5.27)$$

5.2.2 Measurements and Discussions

The devices-under-test (DUTs) are n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, fabricated by Conexant Systems Inc., Newport Beach, CA. Measured data were obtained by using an ATN NP5B Noise and S-Parameter Measurement Systems (0.3 ~ 6 GHz). All the parasitic effects from probe pads and interconnections were de-embedded from the measured s-parameters using the procedure described in [14],[15]. Figs. 5.16 and 5.17 show the measured I_{DS} versus V_{GS} and V_{DS} characteristics to demonstrate the DC performance of the devices.

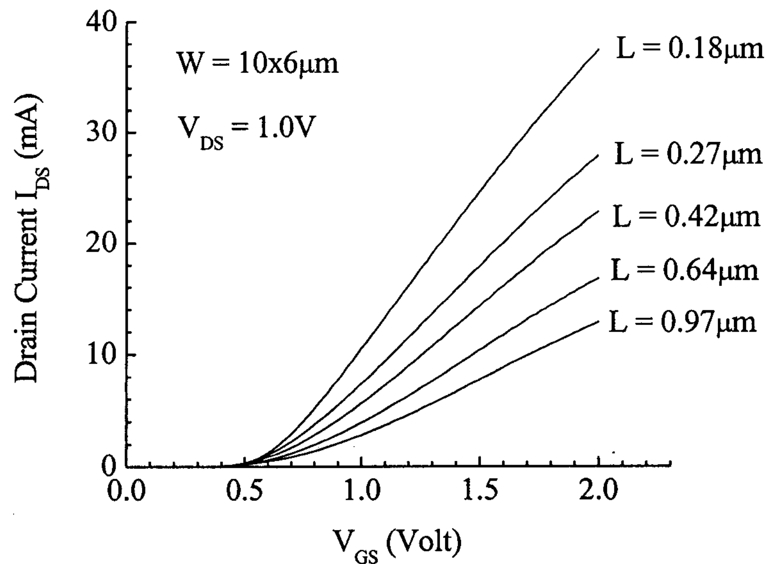

Fig. 5.16: Drain current (I_{DS}) versus gate voltage V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

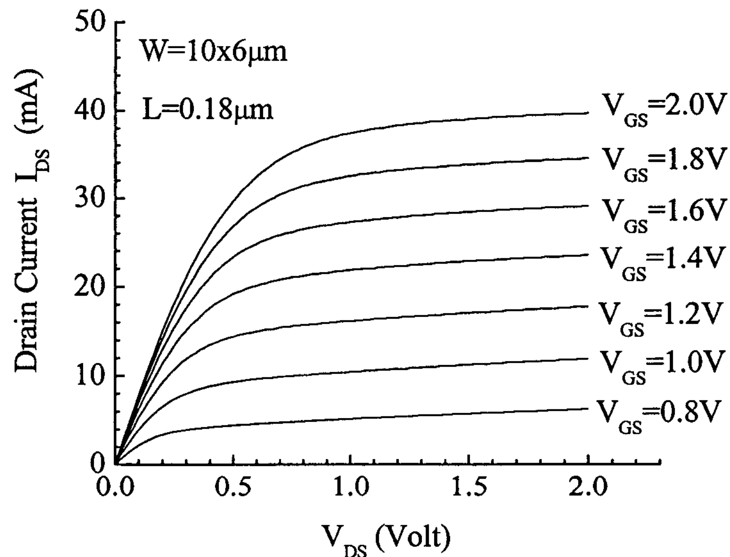

Fig. 5.17: Drain current (I_{DS}) versus drain voltage V_{DS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.18 μm biased at gate voltage V_{GS} = 0.8 V, 1.0 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V and 2.0 V, respectively.

In the extraction procedure, accurate element values used in the RF noise model are crucial to obtain the power spectral density of the noise sources. They are directly obtained from the intrinsic y-parameters [58]. Figs. 5.18 to 5.21 show the measured (symbols) and simulated (lines) y-parameters of an n-type MOSFET with channel width W = 10 × 6 μm (10 fingers) and length L = 0.18 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V based on g_m = 28.4 mS, R_G = 5.8 Ω, $R_D = R_S$ = 1.6 Ω, R_{DS} = 486 Ω, R_i = 90.6 Ω, R_{DB} = 134 Ω, C_{GS} = 68.5 fF, C_{GD} = 30.6 fF, $C_{GB} \cong$ 0.0 fF, C_{DB} = 76.9 fF, C_{SB} = 496 fF, and τ = 4.5×10^{-12}s. As shown, excellent agreement is obtained between measured and simulated data for all four y-parameters.

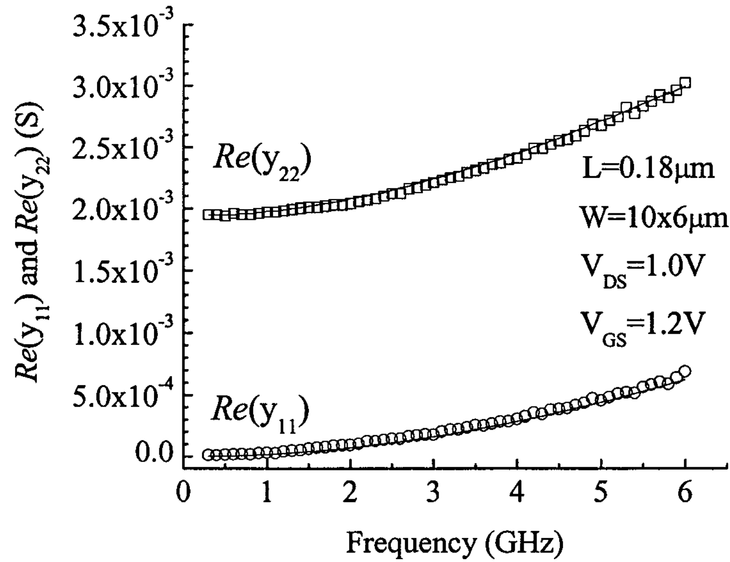

Fig. 5.18: Measured (symbols) and simulated (lines) real parts of y_{11} and y_{22} versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.18 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

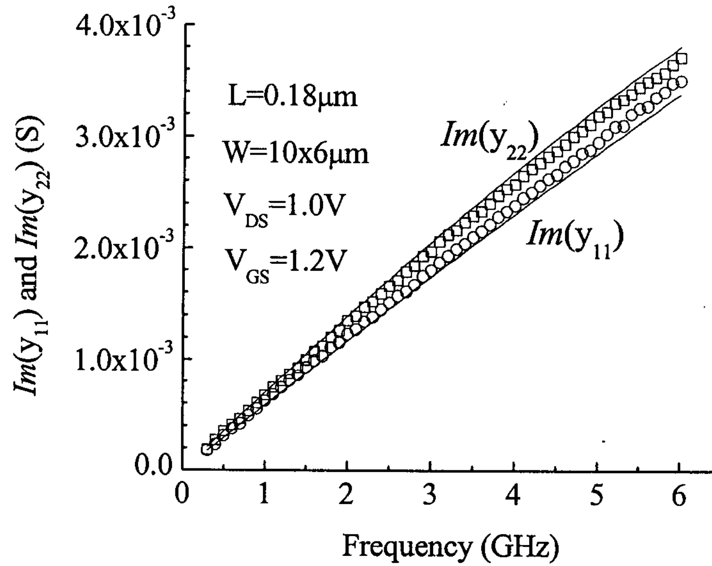

Fig. 5.19: Measured (symbols) and simulated (lines) imaginary parts of y_{11} and y_{22} versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.18 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

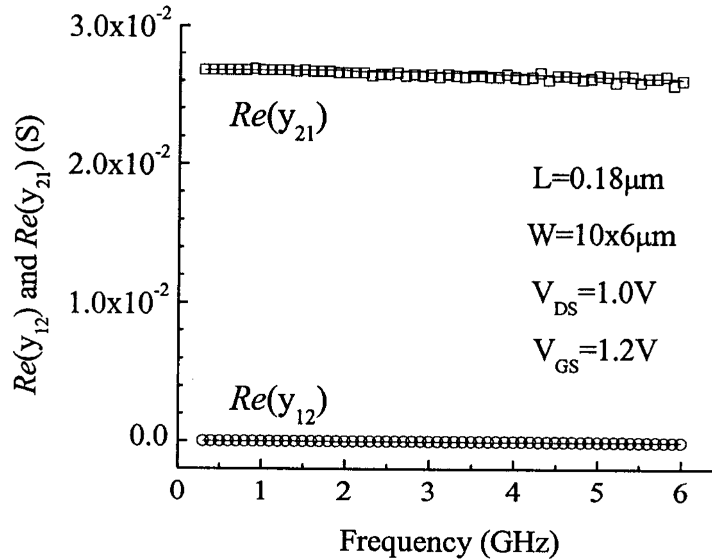

Fig. 5.20: Measured (symbols) and simulated (lines) real parts of y_{12} and y_{21} versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.18 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

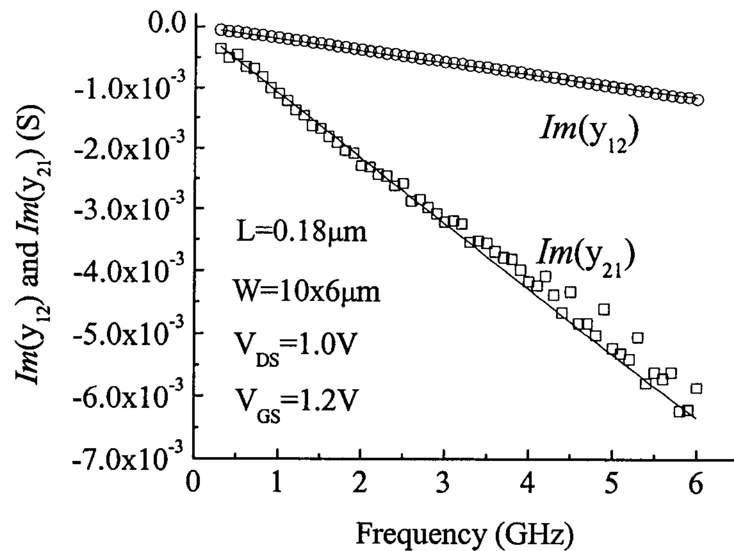

Fig. 5.21: Measured (symbols) and simulated (lines) imaginary parts of y_{12} and y_{21} versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.18 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

Figs. 5.22 to 5.25 show the extracted g_m, R_{DS}, C_{GS} and C_{GD} versus gate bias respectively, for devices with different channel lengths. These extracted parameters give similar fitting accuracies as that shown in figs. 5.18 to 5.21 of the y-parameters vs. frequencies at all the gate biases shown in figs. 5.22 to 5.25.

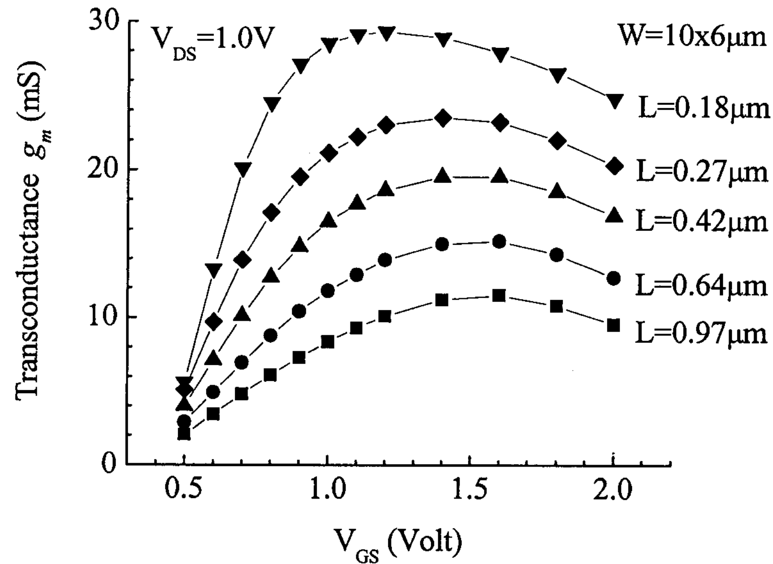

Fig. 5.22: Transconductance (g_m) versus V_{GS} characteristics obtained from the measured $Re(y_{21})$ at low frequencies for the n-type MOSFETs with W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

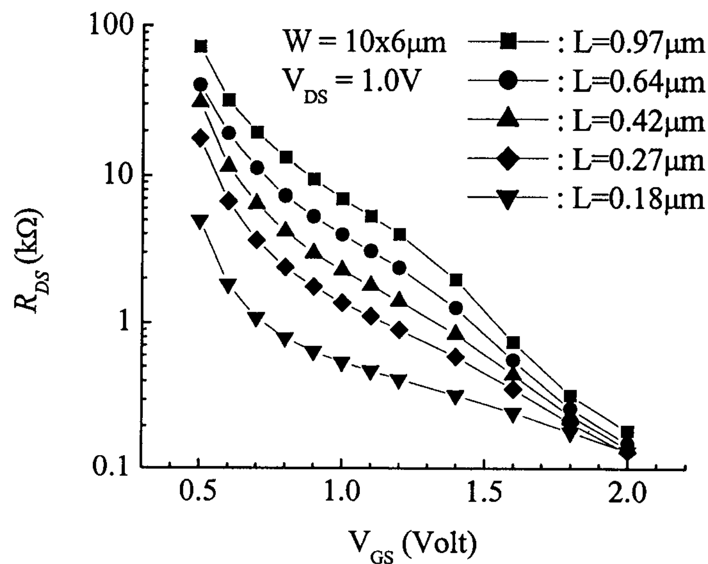

Fig. 5.23: Output resistance (R_{DS}) versus V_{GS} characteristics obtained from the measured $Re(y_{22})$ at low frequencies for the n-type MOSFETs with W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

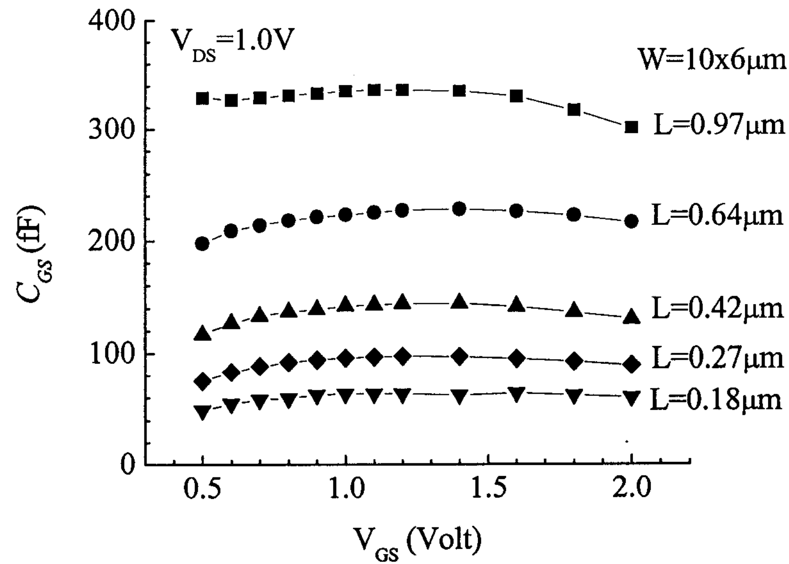

Fig. 5.24: Gate-to-source capacitances (C_{GS}) versus V_{GS} characteristics extracted from the $Im(y_{11})$ at low frequencies for the n-type MOSFETs with W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

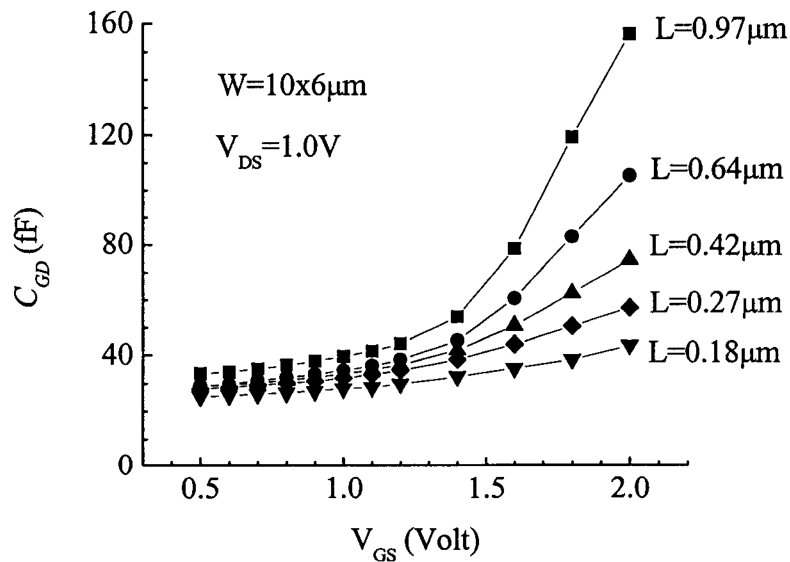

Fig. 5.25: Gate-to-drain capacitances (C_{GD}) versus V_{GS} characteristics extracted from the $Im(y_{12})$ at low frequencies for the n-type MOSFETs with W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

The gate resistance (R_G) used in the simulation for different channel lengths is obtained from

$$R_G = \frac{R_{GSH} \cdot W}{3 \cdot n^2 \cdot L} \tag{5.28}$$

where $R_{GSH} = 5.17\ \Omega$ and n is the number of fingers. In fig. 5.22, the V_{GS} bias for the peak g_m decreases as the channel length is reduced and this results in the shift of the peak f_T shown in fig. 5.26. Although the peak value of g_m increases when the channel length is reduced, the output resistance (R_{DS}) in fig. 5.23 decreases at the same time, and this results in the amplification factor μ_f ($\mu_f = g_m \times R_{DS}$) being approximately the same at the V_{GS} where the peak value of g_m occurs.

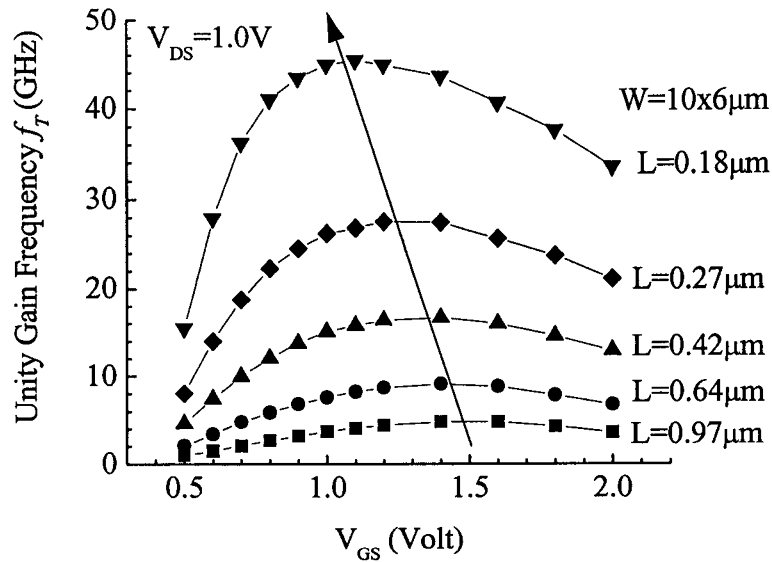

Fig. 5.26: Unity gain frequency (f_T) versus V_{GS} characteristics obtained from the measured intrinsic $|h_{21}|$ at 0 dB for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

Based on the element values extracted from the y-parameters and the measured noise parameters, fig. 5.27 shows the extracted channel noise versus frequency characteristics for n-type MOSFETs with different channel lengths biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V. It is shown that the channel noise, in general, is frequency independent and increases when the channel length decreases. The solid lines in fig. 5.27 are the extracted channel noise based on the method in [16] which provides an alternative way to verify the channel noise extracted by the proposed method. The small increase in the channel noise at low frequencies for deep submicron devices might be caused by the inaccuracy of the measurement system at low frequencies.

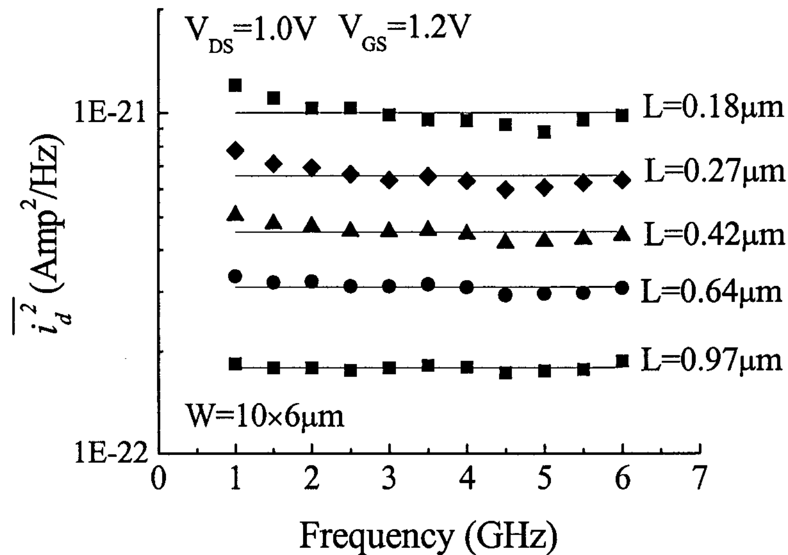

Fig. 5.27: Extracted channel noise ($\overline{i_d^2}$) versus frequency characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V. The solid lines are the extracted channel noise based on the method in [16].

Figs. 5.28 and 5.29 show that the induced gate noise $\overline{i_g^2}$ and the correlation noise $\overline{i_g i_d^*}$ are proportional to f^2 and f, respectively where f is the operating frequency (solid lines in the figures). In addition, when channel length decreases, both the induced gate noise and the correlation noise also decrease because of the decrease of C_{GS}, as shown in fig. 5.24.

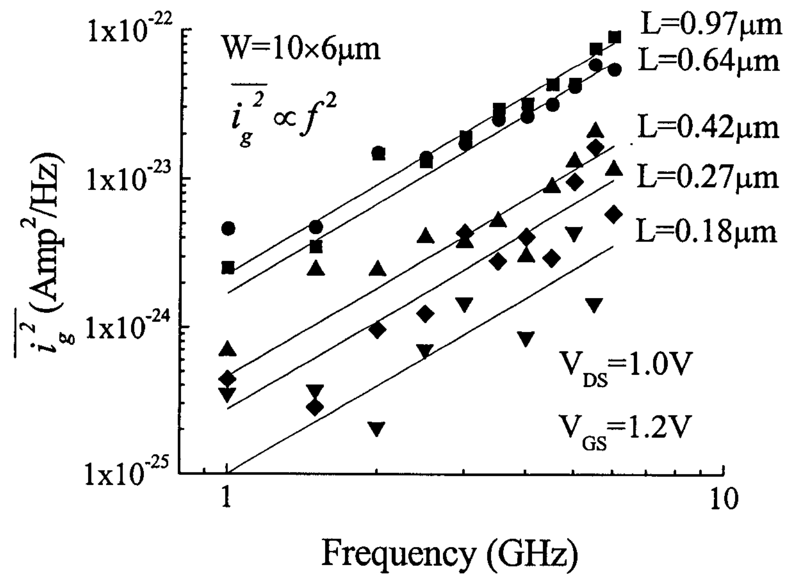

Fig. 5.28: Extracted induced gate noise ($\overline{i_g^2}$) versus frequency characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

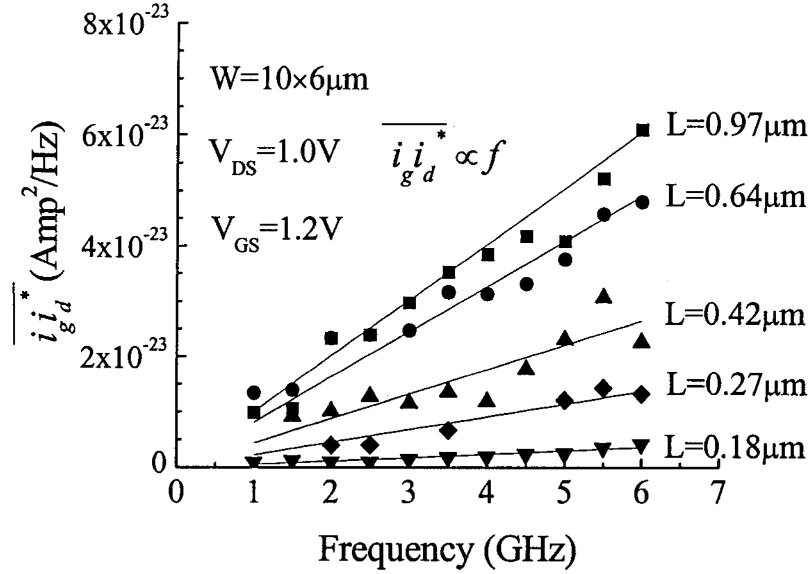

Fig. 5.29: The correlation between $\overline{i_g^2}$ and $\overline{i_d^2}$ ($\overline{i_g i_d^*}$) versus frequency characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

Another useful parameter that is used to describe the relationship between the channel noise, induced gate noise and their correlation is the cross-correlation coefficient *c*, which is defined as

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}. \tag{5.29}$$

Fig. 5.30 shows the extracted cross-correlation coefficient *c* versus frequency characteristics for the devices with different channel lengths. In general, *c* is frequency independent and decreases when the channel length decreases. This is an opposite trend to the simulated results in [46],[61].

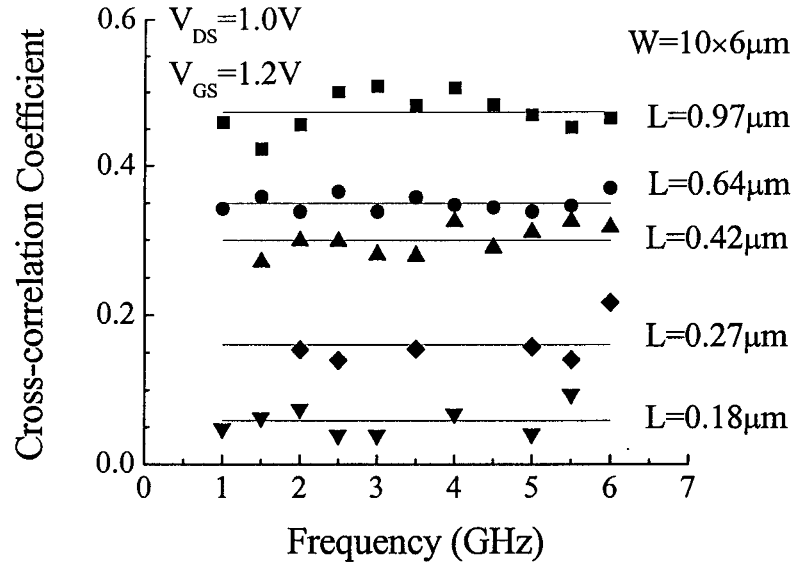

Fig. 5.30: The cross-correlation coefficient c versus frequency characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

In order to verify the accuracy of the extracted noise sources and compare the simulation results against the measured data and those based on van der Ziel's model [38] which is suggested for long channel devices, figs. 5.31 to 5.34 show the measured (symbols) and simulated (lines) noise parameters versus frequency characteristics by using the direct calculation technique described in Chapter 3. These results are for the n-type MOSFET with the channel width W = 10 × 6 μm and length L = 0.97 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V. In these figures, the solid lines are the simulated results based on the extracted noise sources (solid lines in figs. 5.27 - 5.29) and the dashed lines are the simulated results based on van der Ziel's model in which the power spectral density of the noise sources are given by

$$\overline{i_d^2} = \gamma_{satn} 4kTg_{do} \tag{5.30}$$

$$\overline{i_g^2} = \delta_{satn} 4kT\frac{\omega^2 C_o^2}{g_{do}} \tag{5.31}$$

and

$$\overline{i_g i_d^*} = \varepsilon_{satn} 4kTj\omega C_o \tag{5.32}$$

where g_{do} = 12.5 mS, γ_{satn} = 2/3, δ_{satn} = 16/135, ε_{satn} = 1/9, $C_o = 3C_{GS}/2$ and $\omega = 2\pi f$.

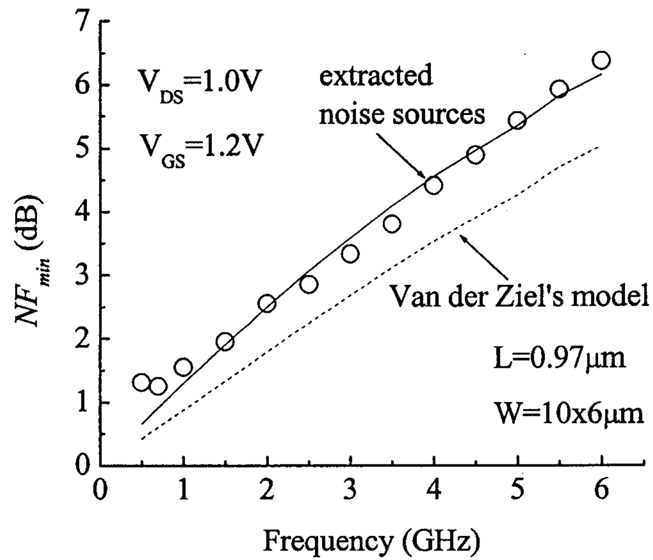

Fig. 5.31: Measured (symbols) and simulated (lines) minimum noise figure (NF_{min}) versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.97 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V. The solid line is calculated with all the extracted noise sources and the dashed line is calculated using the Van der Ziel's model.

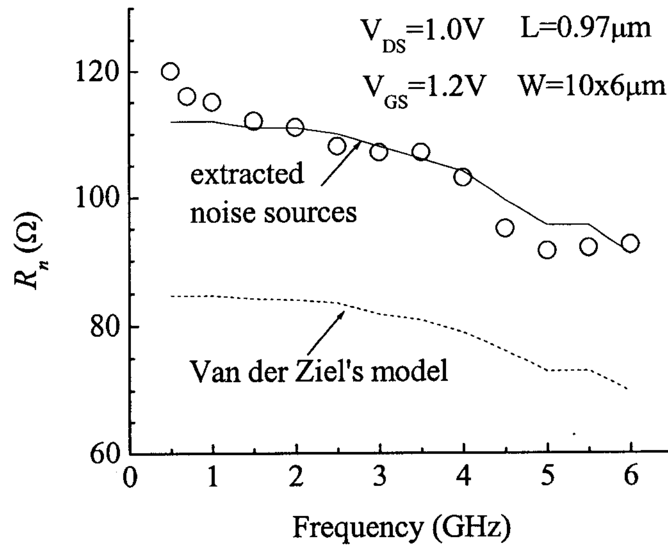

Fig. 5.32: Measured (symbols) and simulated (lines) equivalent noise resistance (R_n) versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm and length L = 0.97 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

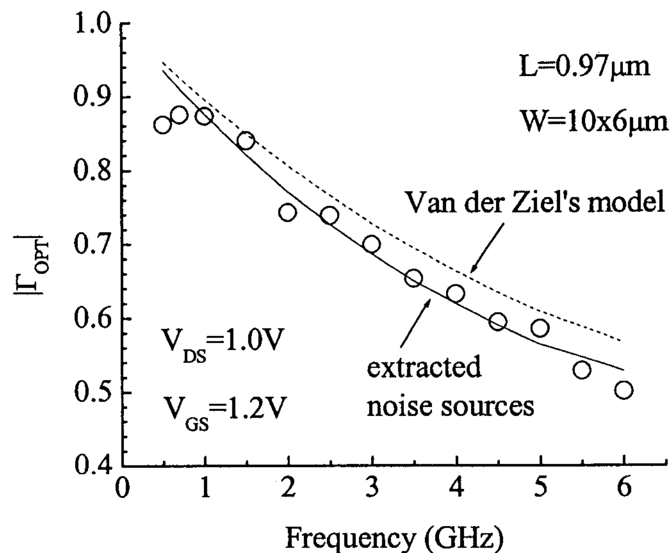

Fig. 5.33: Measured (symbols) and simulated (lines) magnitude of the optimized source reflection coefficient ($|\Gamma_{OPT}|$) versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm and length L = 0.97 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

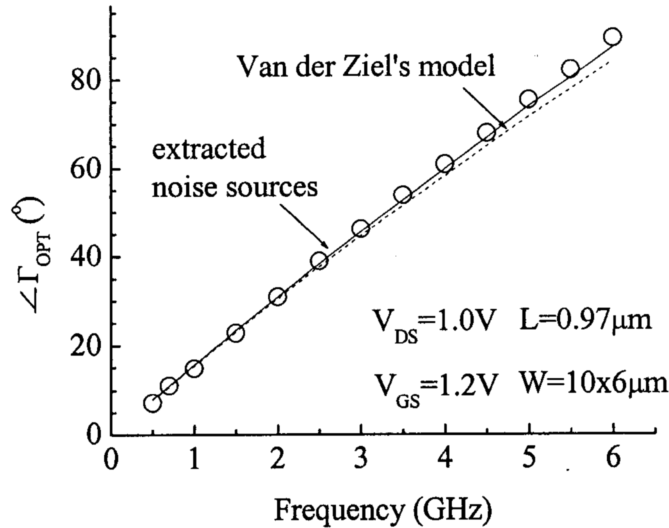

Fig. 5.34: Measured (symbols) and simulated (lines) angle of the optimized source reflection coefficient ($\angle\Gamma_{OPT}$) versus frequency characteristics for the n-type MOSFET with the channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.97 μm biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V. The solid line is calculated with all the extracted noise sources and the dashed line is calculated using the Van der Ziel's model.

It is shown that the extracted noise sources, in general, give a good noise prediction. However, van der Ziel's model predicts lower NF_{min} and R_n and this is caused by not including the enhancement of the local channel resistance which will be discussed in Chapter 6.

For the bias dependence of the extracted noise sources, figs. 5.35 to 5.38 show the $\overline{i_d^2}$, $\overline{i_g^2}$, $\overline{i_g i_d^*}$ and c versus bias characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm respectively, biased at V_{DS} = 1.0 V. It is shown that $\overline{i_d^2}$ and $\overline{i_g i_d^*}$ have a strong bias dependence and they increase then tend to saturate when V_{GS} increases, but $\overline{i_g^2}$ has a weak bias dependence. On the other hand, the cross-correlation coefficient c decreases when V_{GS} increases, and it follows the trend predicted in [31].

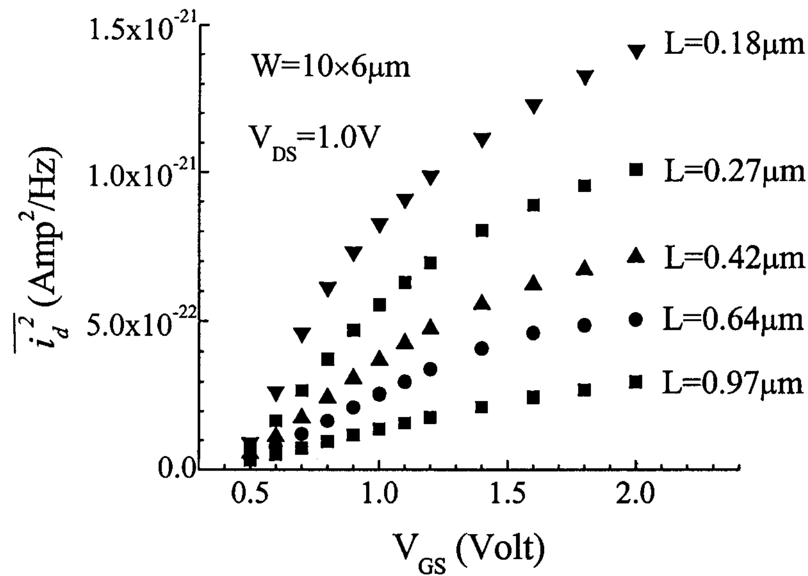

Fig. 5.35: Channel noise ($\overline{i_d^2}$) versus bias characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

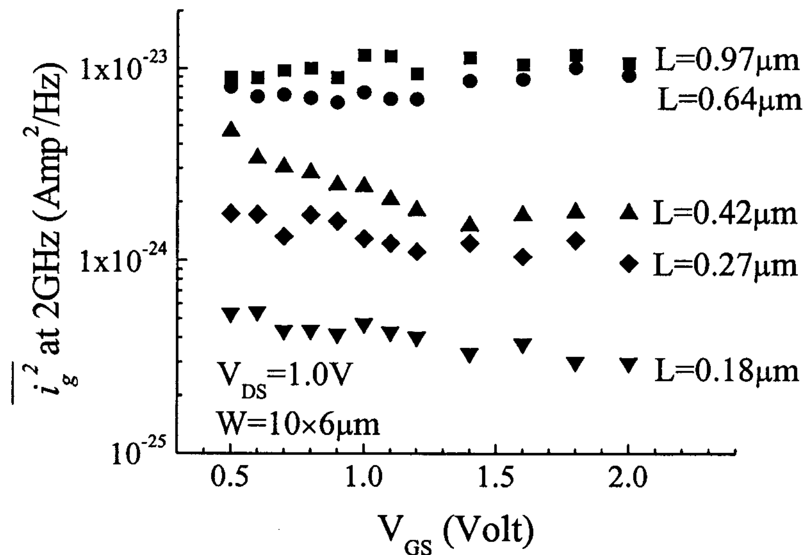

Fig. 5.36: Induced gate noise ($\overline{i_g^2}$) versus bias characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

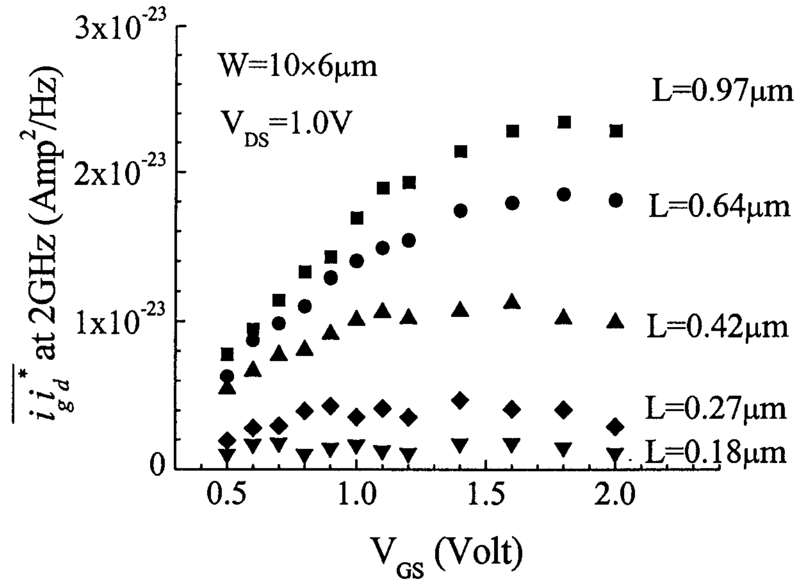

Fig. 5.37: The correlation between $\overline{i_g^2}$ and $\overline{i_d^2}$ ($\overline{i_g i_d^*}$) versus bias characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

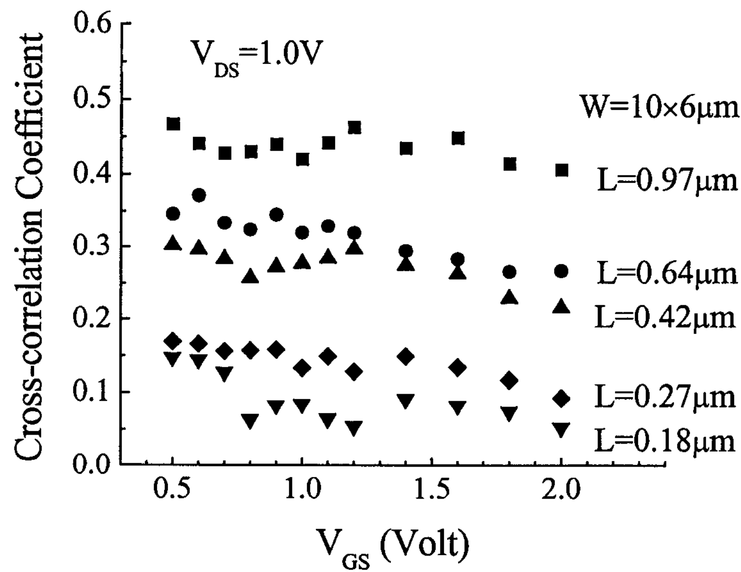

Fig. 5.38: The cross-correlation coefficient c versus bias characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V.

Finally, figs. 5.39 and 5.40 show the extracted $\overline{i_d^2}$ and $\overline{i_g^2}$ versus V_{GS} characteristics of a 0.97 μm n-type MOSFET biased at V_{DS} = 1.0 V, 1.2 V, 1.5 V, 1.8 V and 2.0 V, respectively. It is shown that both noise sources have a weak V_{DS} dependence in the V_{DS} region discussed, and this might be because the weak channel length modulation (CLM) effect in these devices, as shown in fig. 5.17. For short-channel devices, fig. 5.41 shows the extracted $\overline{i_d^2}$ versus V_{GS} characteristics of a 0.18 μm n-type MOSFET biased at V_{DS} = 1.0 V, 1.2 V, 1.5 V, 1.8 V and 2.0 V, respectively. It is shown that the extracted $\overline{i_d^2}$ demonstrates some V_{DS} dependence in the V_{DS} region discussed, and this is because of the stronger impact from the CLM effect on the short channel devices. The proof of this statement will be discussed in detail in Chapter 6.

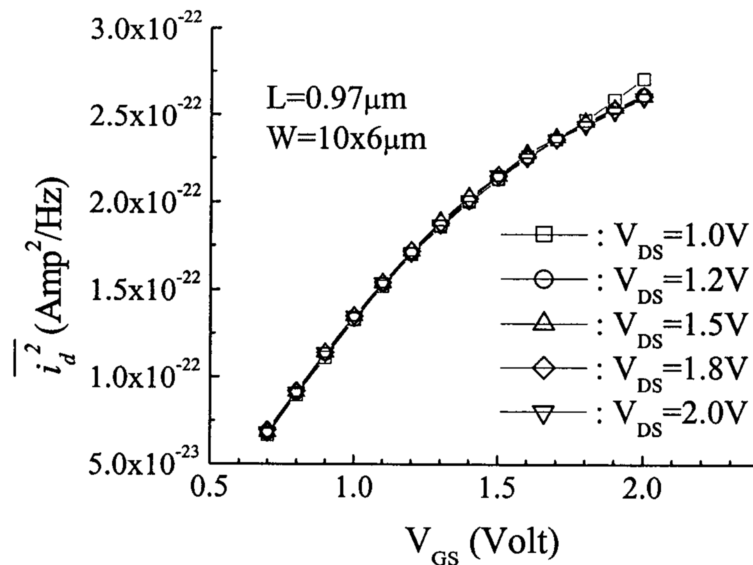

Fig. 5.39: Channel noise ($\overline{i_d^2}$) versus V_{GS} characteristics for the n-type MOSFET with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.97 μm biased at V_{DS} = 1.0 V, 1.2 V, 1.5 V, 1.8 V and 2.0 V, respectively.

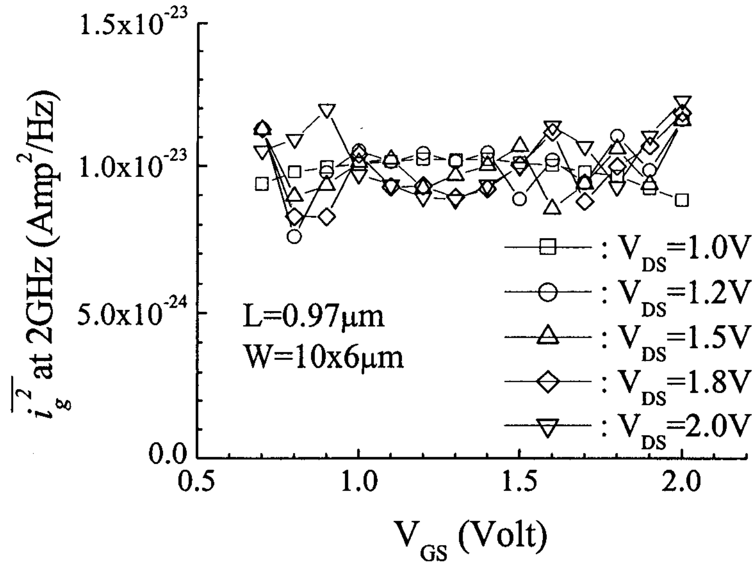

Fig. 5.40: Induced gate noise ($\overline{i_g^2}$) versus V_{GS} characteristics for the n-type MOSFET with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.97 μm biased at V_{DS} = 1.0 V, 1.2 V, 1.5 V, 1.8 V and 2.0 V, respectively.

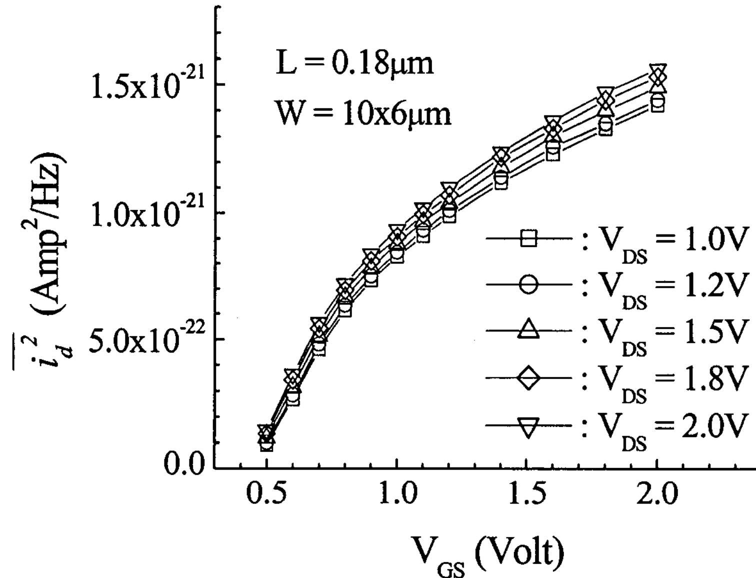

Fig. 5.41: Channel noise ($\overline{i_d^2}$) versus V_{GS} characteristics for the n-type MOSFET with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and length L = 0.18 μm biased at V_{DS} = 1.0 V, 1.2 V, 1.5 V, 1.8 V and 2.0 V, respectively.

Chapter 6

PHYSICS-BASED RF NOISE MODEL OF MOSFETS

6.1 CHANNEL NOISE IN MOSFETS

As discussed in Chapter 5, when working at high frequencies, the noise generated within the device itself will play an increasingly important role in the overall RF IC performance, especially in the noise performance of a front-end receiver. Therefore, a physics-based noise model which can accurately predict the noise characteristics of deep-submicron MOSFETs is crucial for the low noise, RF IC design.

To date, the noise model of the channel noise based on the Nyquist theory and the DC model of MOSFETs successfully predicted the channel noise of the devices working the linear region. However, for RF ICs, the short-channel MOSFETs usually operate in the saturation region for most applications, and it is often observed that the channel noise generated from the short-channel devices is higher than expected from the conventional channel noise theory for long-channel MOSFETs [34],[35]. Some approaches have been presented to explain the discrepancy by introducing the extra channel noise from the velocity saturation through either the hot-electron effect [34] or the diffusion noise [36],[37]. The noise from the saturation region proposed in these models is neither physical

nor proven by the measured noise data of deep-submicron MOSFETs. In this chapter, a new analytical noise model using the channel length modulation (CLM) effect to calculate the channel noise of deep sub-micron MOSFETs is presented and verified with the measured data obtained using the direct extraction method [8],[62]. In addition, the hot electron effect and the noise from the velocity saturation region are also discussed.

6.1.1 Derivation of the Channel Noise in MOSFETs

The approach used in this research to calculate the channel noise is based on a two-section channel model in which the channel of a MOSFET is divided into two regions - a gradual channel region of length $L_{elec} = L_{eff} - \Delta L$ (region I in fig. 6.1) and a velocity saturation region of length ΔL (region II in fig. 6.1) [34],[61],[63]. For the derivation of the channel noise in this work, ΔL is given by [64]

$$\Delta L = \frac{1}{\alpha}\ln\left(\frac{\alpha(V_{DS} - V_{DSsat}) + E_D}{E_{crit}}\right), \tag{6.1}$$

where

$$E_D = E_{crit}\sqrt{1 + \left(\frac{\alpha(V_{DS} - V_{DSsat})}{E_{crit}}\right)^2}, \tag{6.2}$$

and

$$\alpha = \lambda\sqrt{\frac{3}{2}\frac{C_{ox}}{x_j\varepsilon_{si}\varepsilon_o}}. \tag{6.3}$$

Here, E_{crit} is the critical lateral electric field at which carriers travel at their saturation velocity, x_j is the junction depth of the source and drain regions, C_{ox} is the gate-oxide

capacitance per unit area, and λ is a fitting parameter to adjust the channel length modulation and it is unity in this work. Based on this channel model, the total noise current shown at the drain terminal will be the sum of the noise current contributed from both regions in the channel.

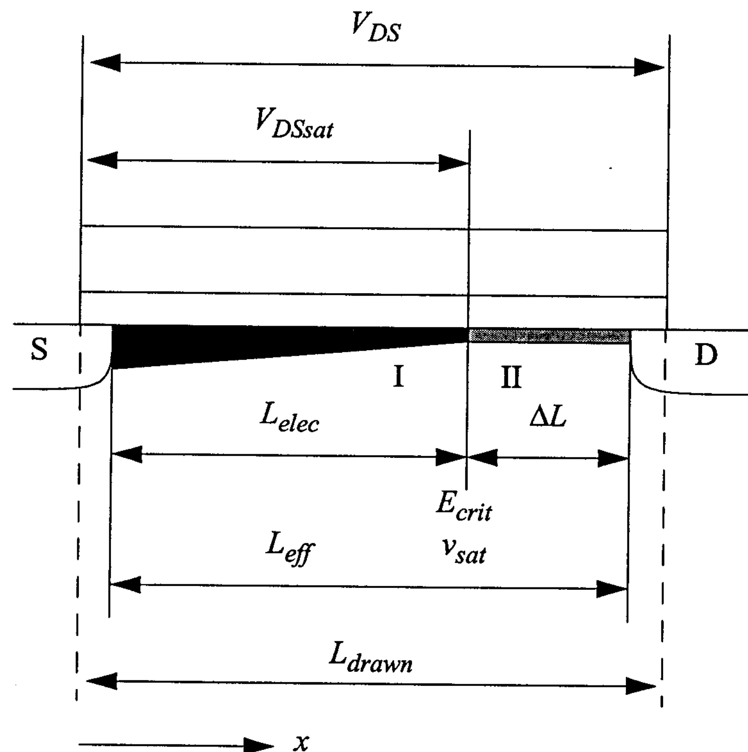

Fig. 6.1: Cross section of a MOSFET channel divided into a gradual channel region (I) and a velocity saturation region (II).

- **Channel noise from the gradual channel region (region I)**

In the derivation of the channel noise in the gradual channel region, we assume that the electric field in the x direction for most of the sections in the gradual channel region is much less than the critical field E_{crit} (for example, see fig. 6(b) in [65]). We will verify and discuss this assumption for the modeling of channel noise with the measured noise data

in the next section. Using this assumption and the DC model of MOSFETs, then the channel resistance ΔR of a section Δx at the position x_o in the gradual channel region is given by [66]

$$\Delta R(x_o) = \frac{\Delta x}{W\mu(x_o)(-Q(x_o))} \tag{6.4}$$

where $\mu(x_o)$ and $Q(x_o)$ are the mobility (cm^2/V.sec) and the electron concentration (C/cm^2), respectively at the position x_o. The term $-Q(x_o)$ is positive because of the negative charge $Q(x_o)$ for electrons. From the thermal noise theory (or Nyquist theory), the mean square value of the noise voltage generated from $\Delta R(x_o)$ is given by

$$\overline{\Delta v(x_o)^2} = 4kT(x_o)\Delta R(x_o)\Delta f = \frac{4kT(x_o)\Delta x \Delta f}{W\mu(x_o)(-Q(x_o))} \tag{6.5}$$

where k is Boltzmann's constant, $T(x_o)$ is the absolute temperature of the lattice at the position x_o and Δf is the bandwidth. If we treat the part of the channel in the gradual channel region as a single transistor with the channel length L_{elec}, then according to the channel noise derivation presented in [66] or Appendix D, the mean square value of the noise current $\overline{\Delta i(x_o)^2}$ delivered to the drain terminal from $\Delta R(x_o)$ is given by $\overline{\Delta v(x_o)^2}$ multiplied by the square of its local conductance $g(x_o)$, and it is

$$g(x_o) = \frac{W\mu(x_o)(-Q(x_o))}{L_{elec}}. \tag{6.6}$$

Assuming that the electric field in the x direction for most of the sections in the gradual channel region is much less than the critical field E_{crit}, then the local mobility $\mu(x_o)$ is about the same as the effective mobility μ_{eff}, which is given by [67]

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{BS})\left(\frac{V_{GS} + 2V_{TH}}{T_{ox}}\right) + U_b\left(\frac{V_{GS} + 2V_{TH}}{T_{ox}}\right)^2}, \tag{6.7}$$

where T_{ox} is the oxide thickness and V_{TH} the threshold voltage. Therefore, from (6.5) and (6.6), the mean square value of the noise current contributed from $\Delta R(x_o)$ is then [66]

$$\overline{\Delta i_d(x_o)^2} = g_{DS}^2(x_o) \cdot \overline{\Delta v(x_o)^2} = \frac{4kT(x_o)\Delta f W \mu_{eff} Q(x_o)\Delta x}{L_{elec}^2}. \tag{6.8}$$

Note that (6.8) is only true for the region where the carriers do not travel at their saturation velocity and it cannot be applied to the velocity saturation region (region II in fig. 6.1) because Nyquist's theory fails in that region [36].

There is also a debate about the temperature $T(x_o)$ in (6.8) - whether it is the electron temperature T_e or the lattice temperature T_o. Let's assume that $T(x_o)$ is the electron temperature. In this case, we can use the most commonly adopted equation for the electron temperature at the position x_o [68],

$$T_e(x_o) = T_o\left(1 + \delta\left(\frac{E(x_o)}{E_{crit}}\right)^2\right), \tag{6.9}$$

where δ is a fitting parameter and its value is in the range of 5 - 20 for values of E_{crit} in the range of 2 - 4 V/μm [68]. The total noise spectral density $S_{i_d^2}$ from region I is then given by the integration of (6.8) from $x = 0$ to $x = L_{elec}$ divided by Δf which is

$$S_{i_d^2} = \frac{\overline{i_d^2}}{\Delta f} = \frac{4kT_o}{L_{elec}^2}\int_0^{L_{elec}}\left(1 + \delta\left(\frac{E(x_o)}{E_{crit}}\right)^2\right) W \mu_{eff} Q(x_o) dx, \tag{6.10}$$

where $\overline{i_d^2}$ is the mean square value of the total noise current. After rearranging (6.10) as derived in Appendix C, the spectral density of the channel noise $S_{i_d^2}$ becomes

$$S_{i_d^2} = \frac{4kT_o}{L_{elec}^2}\mu_{eff}(-Q_{inv}) + \delta\frac{4kT_o I_{DS}}{L_{elec}^2 E_{crit}^2}V_{DSsat} \tag{6.11}$$

where $-Q_{inv}$ is the total inversion charge in gradual channel region (region I). Equation (6.11) is general and can be applied to any compact model. Different complexity and accuracy will be achieved depending on the models used to calculate the inversion charge Q_{inv} and the channel length modulation effect ΔL. Note that V_{DSsat} in (6.11) will become V_{DS}, and L_{elec} will become L_{eff} when the device operates in the linear mode. Equation (6.11) is similar to the equation (10) in [34], but it uses the L_{elec} instead of L_{eff} for the noise calculation.

- **Channel noise from the velocity saturation region (region II)**

For the noise current generated from the velocity saturation region (region II), several models were presented in [34],[37],[61],[69] for example, to calculate the noise current from this region. For the noise models in [34] and [69], the equation based on the (8.5.18) in [66] for the model derivation is only true in the absence of velocity saturation [66]. On the other hand, because the Ohm's law is not valid in the velocity saturation region, the local resistance ΔR in (6.4) is not defined and therefore the thermal noise (or Johnson noise) theory cannot be used in region II [36]. These reasons make the noise calculation in [61] questionable in region II.

The key question for the noise calculation in region II is what is the noise mechanism if the thermal noise theory fails? Different noise mechanisms - diffusion noise model [70],[71] and drifting dipole layer model [36],[37] have been proposed for the noise calculation in velocity saturation region. However, in this thesis, we will show that there is

no noise current generated from region II. This conclusion, which is justified in section 6.4, will also be checked with experimental data extracted from the RF noise measurements.

6.1.2 Measurements and Discussions

The device-under-tests (DUTs) are fabricated in a 0.18 μm CMOS technology with channel width W = 10×6 μm and channel length L = 0.18 μm, 0.42 μm and 0.97 μm, respectively. Fig. 6.2 shows the measured (symbols) and simulated (lines) DC current I_{DS} versus V_{GS} characteristics of the DUTs biased at V_{DS} = 1.5 V based on the DC current model shown in Appendix A. The parameter values used in the calculation are $T_{ox} = 38$ A, $N_{SD} = 2.3\times10^{17}$, $\mu_0 = 610$ cm^2/Vs, $U_a = 25.98\times10^{-10}$ m/V, $U_b = 1.12\times10^{-19}$ (m/V)^2, U_c = 4.84×10^{-11} m/V^2, $K_1 = 0.254$ V$^{1/2}$, $K_2 = 0.042$, $Nlx = 1.89\times10^{-7}$ m, and $V_{THO} = 0.42$ V, 0.41 V and 0.39 V for 0.97 μm, 0.42 μm and 0.18 μm devices, respectively. The threshold voltage reduction is taken care of by using different V_{THO} values instead of using the compact model for better data fitting. Therefore, V_{THO} is a fitting parameter for the devices with different channel lengths.

Fig. 6.3 shows the extracted (symbols) and simulated (lines) spectral density of the channel noise $S_{i_d^2}$ versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V and with $\delta = 0$. The inversion charge model in [67] is used to calculate the Q_{inv} in (6.11). The solid lines are obtained by using L_{elec} and the dashed lines are obtained by using L_{eff} in (6.11).

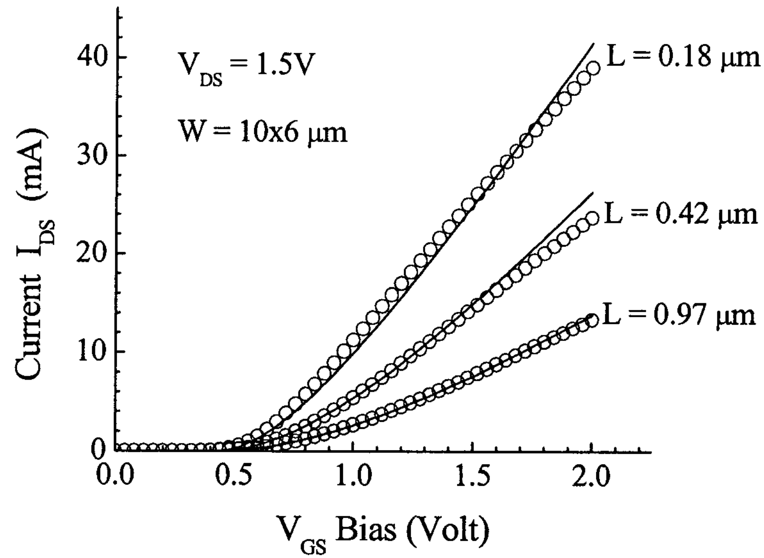

Fig. 6.2: Measured (symbols) and simulated (lines) DC current I_{DS} versus V_{GS} characteristics of NMOSFETs with channel width W = 10×6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V.

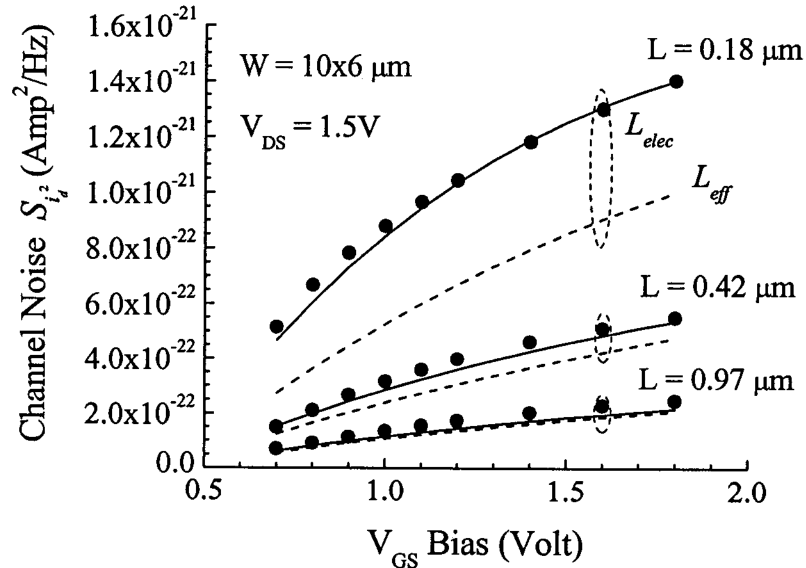

Fig. 6.3: Extracted (symbols) and simulated (lines) channel noise versus V_{GS} characteristics of NMOSFETs with channel width W = 10×6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V with δ = 0. The solid lines are obtained using L_{elec} and the dashed lines are obtained using L_{eff}.

It is shown that the CLM effect begins to have some impact on the channel noise when the channel length of the device is smaller than 0.5 μm, and that is why the simulated channel noise from region I in [34] predicts lower channel noise from 0.25 μm and 0.18 μm devices. Although [34] corrects this degradation by the introduction of the channel noise current caused by the hot electrons from the velocity saturation region, the equation used in the model derivation cannot be applied to the position where carriers do travel at their saturated velocity as discussed in section 6.1.1. Another observation from fig. 6.3 is that the hot electron effects suggested in [38],[72] and used in [34],[61],[73],[74] does not show any noticeable impact on the channel noise of deep sub-micron MOSFETs, and this agrees with the simulated results presented in [35].

For the V_{DS} dependence of the channel noise, fig. 6.4 shows extracted (symbols) and simulated (lines) spectral density of the channel noise $S_{i_d^2}$ versus V_{DS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{GS} = 1.0 V and without the hot electron effect (i.e. $\delta = 0$). The solid lines are obtained by using L_{elec} and the dashed lines are obtained by using L_{eff} in the noise calculation. It is shown that the calculated channel noise using L_{eff} in (6.11) predicts lower channel noise, and cannot match the increasing trend of the extracted channel noise caused by the CLM effect for the deep sub-micron devices. The slope of simulated lines in the channel noise versus V_{DS} characteristics will depend on the accuracy of the model calculating the channel length modulation ΔL.

Sometimes, the spectral density of the channel noise is expressed [38] as

$$S_{i_d^2} = \gamma \cdot 4kTg_{dso} \tag{6.12}$$

where g_{dso} is the output conductance at zero drain bias (i.e. $V_{DS} = 0$). Based on the noise theory for long channel devices, the value of γ is 2/3 [38]. However, when the channel length is reduced, the value of γ will be increased [18],[35],[56]. Fig. 6.5 shows the extracted (symbols) and simulated (lines) γ versus V_{GS} characteristics of n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 10 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V with $\delta = 0$. For the long channel devices, the calculated γ is 2/3 at V_{GS} = 1.8 V, which agrees with the theoretical value. When the channel length is decreased, the γ value will increase from 2/3 to 1.2 or 1.8 (depending on the V_{GS} bias), and the model agrees well with the data.

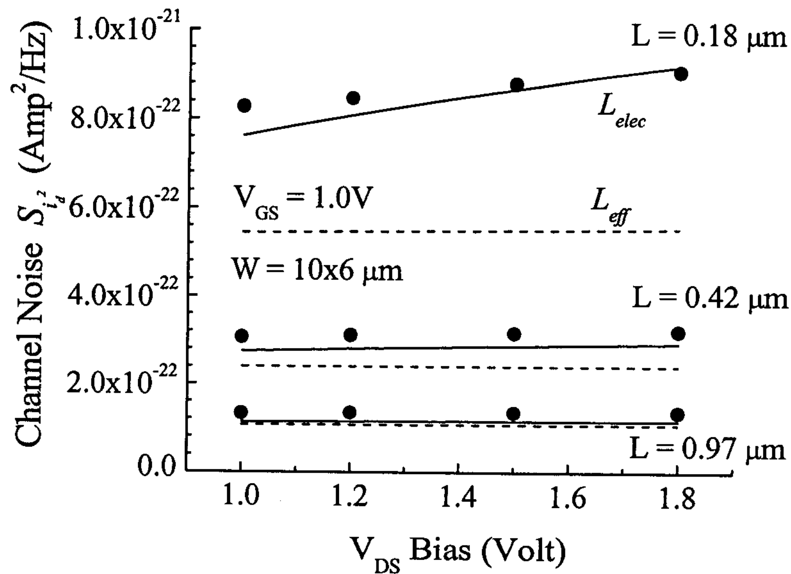

Fig. 6.4: Extracted (symbols) and simulated (lines) channel noise versus V_{DS} characteristics of NMOSFETs with channel width W = 10×6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{GS} = 1.0 V with $\delta = 0$. The solid lines are obtained using L_{elec} and the dashed lines are obtained using L_{eff}.

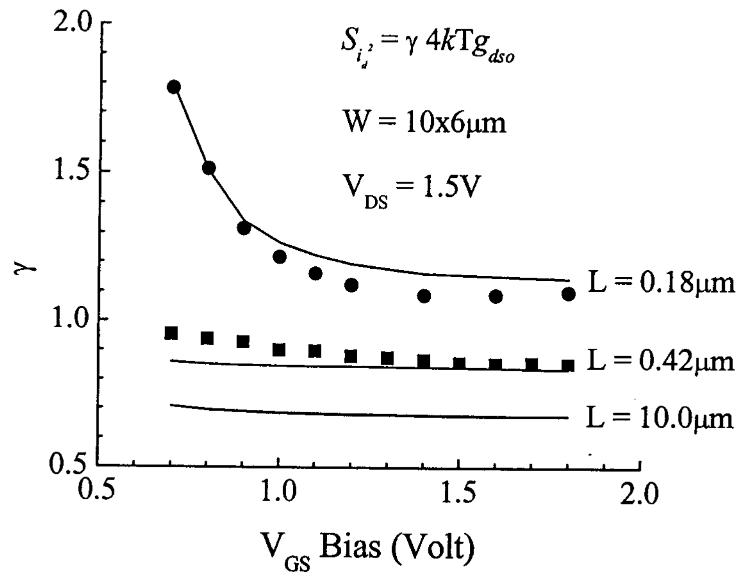

Fig. 6.5: Extracted (symbols) and simulated (lines) γ versus V_{GS} characteristics of NMOSFETs with channel width W = 10×6 μm and channel lengths L = 10 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V with $\delta = 0$.

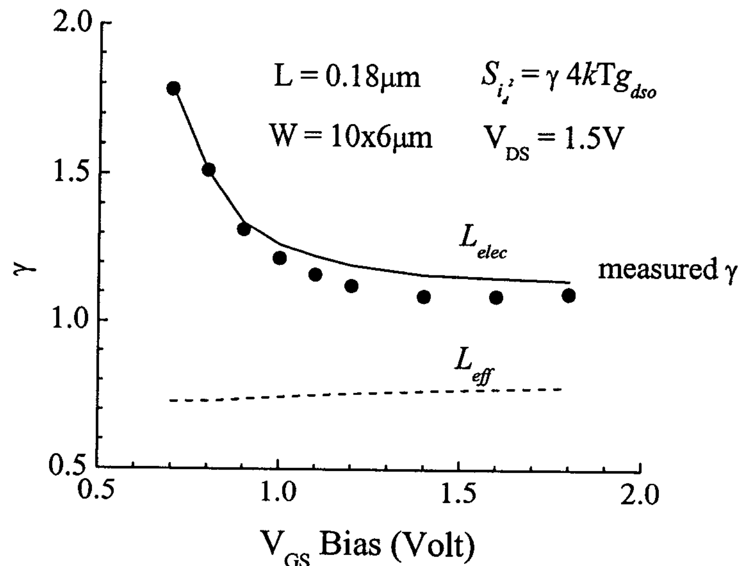

Fig. 6.6: Extracted (symbols) and simulated (lines) γ versus V_{GS} characteristics of NMOSFETs with channel length L = 0.18 μm and width W = 10×6 μm and biased at V_{DS} = 1.5 V with $\delta = 0$. The solid line is obtained using L_{elec} and the dashed line is obtained using L_{eff}.

Fig. 6.6 shows the extracted (symbols) and simulated (lines) γ versus V_{GS} characteristics of the n-type MOSFET with channel length L = 0.18 μm and width W = 10 × 6 μm and biased at V_{DS} = 1.5 V without the hot electron effect (i.e. $\delta = 0$). The solid line is obtained by using L_{elec} and the dashed line is obtained by using L_{eff}. It is shown again that the calculated γ using L_{eff} in (6.11) predicts lower γ value and cannot match the decreasing trend which is also reported in [35] when the V_{GS} bias is increased.

6.2 INDUCED GATE NOISE

At high frequencies, a MOSFET must be considered as an RC distributed network, with the capacitive coupling to the gate representing the distributed capacitance and the channel itself representing the distributed resistance. This means that the high-frequency gate admittance y_{GS} of the device contains a conductive component. To obtain the capacitive and conductive components, we start from the wave equation of the distributed line representing a MOSFET with a low conductivity substrate given by [75]

$$\frac{d}{dx}[\Delta I_{DS}(x)] = j\omega W_{eff} C_{ox} \Delta v(x) \tag{6.13}$$

where $\Delta v(x)$ is the AC voltage fluctuation along the channel caused by the small variation in gate voltage v_{GS}. Geurst [76] has solved this equation for long-channel transistors, and he expanded y_{GS} in terms of $j\omega$ to get

$$y_{GS} = g_{mo} \cdot \frac{\frac{2}{3}j\hat{\omega} + \frac{4}{45}(j\hat{\omega})^2 + \frac{2}{405}(j\hat{\omega})^3 + \frac{2}{13365}(j\hat{\omega})^4 + \ldots}{1 + \frac{4}{15}j\hat{\omega} + \frac{1}{45}(j\hat{\omega})^2 + \frac{4}{4455}(j\hat{\omega})^3 + \ldots} \tag{6.14}$$

where

$$g_{mo} = \frac{\mu_{eff} C_{ox} W_{eff}}{L_{eff}} (V_{GS} - V_{TH}), \tag{6.15}$$

$$\hat{\omega} = \omega \cdot \frac{L_{eff}^2}{\mu_{eff}(V_{GS} - V_{TH})}, \tag{6.16}$$

and $\omega = 2\pi f$. If we take the first order approximation of (6.14), and model y_{GS} by a capacitance C_{GS} in series with a resistance R_i, we may write, in saturation, that

$$y_{GS} = g_{mo} \cdot \left[\frac{2}{3} j\hat{\omega} + \frac{4}{45}\hat{\omega}^2\right] = \frac{1}{\frac{1}{j\omega C_{GS}} + R_i}. \tag{6.17}$$

For frequency at which $\omega^2 R^2 C^2 << 1$, we may solve for C_{GS} and R_i to get

$$C_{GS} = \frac{2}{3} g_{mo} \frac{\hat{\omega}}{\omega} = \frac{2}{3} C_{ox} W_{eff} L_{eff} \tag{6.18}$$

and

$$R_i = \frac{g_{mo} \cdot \frac{4}{45}\hat{\omega}^2}{\omega^2 C_{GS}^2} = \frac{1}{5 g_{mo}}. \tag{6.19}$$

From (6.18), we find that the maximum value of C_{GS} at saturation is 2/3 of the total oxide capacitance for long-channel transistors, and R_i will decrease with increasing $V_{GS,int}$ since g_{mo} is increasing with bias as shown in (6.15). The resistance R_i will have noise associated with it [66], and this is the physical cause of the induced gate noise. Therefore, when transistors operate in the GHz range, the random potential fluctuations in the channel resulting in the channel noise will be coupled to the gate terminal through the gate oxide capacitance and cause the induced gate noise, which is usually correlated with the channel noise [31],[32],[38],[66],[77],[78].

To evaluate the noise of R_i at higher frequencies, one must know the induced gate noise $\overline{i_g^2}$ and the its cross-correlation with the channel noise $\overline{i_g i_d^*}$. Let's use the two-section channel model again and the total noise current shown at the gate terminal will be the sum of the noise current contributed from both regions.

- **Induced gate noise from the gradual channel region (region I)**

As derived in Appendix D, the noise spectral density of the induced gate noise $\overline{\Delta i_g(x_o)\Delta i_g(x_o)^*}$ from a section Δx in the gradual channel region is

$$\overline{\Delta i_g(x_o)\Delta i_g(x_o)^*} = \left(\frac{\omega W C_{ox}}{I_{ds}}\right)^2 \cdot g(V_o)^2 \overline{\Delta v(x_o)^2}[V_{as} - V(x_o)]^2 \tag{6.20}$$

where

$$g(V_o) = W_{eff}\mu_{eff}C_{ox}(V_{GS} - V_{TH} - V_o), \tag{6.21}$$

$$V_{as} = V_{DS} - \frac{\frac{1}{2}(V_{GS} - V_{TH})V_{DS} - \frac{1}{6}V_{DS}^2}{V_{GS} - V_{TH} - \frac{1}{2}V_{DS}}, \tag{6.22}$$

and $\overline{\Delta v(x_o)^2}$ is defined in (6.5). Note that (6.20) is only valid in region I, and (6.5) for $\overline{\Delta v(x_o)^2}$ is only defined in region I. The total spectral density of the induced gate noise $S_{i_g^2}$ from the gradual channel region is then obtained by the integration of (6.20) from $x = 0$ to $x = L_{elec}$ divided by Δf, which is

$$S_{i_g^2} = \frac{\overline{i_g^2}}{\Delta f} = \frac{4kT_o\omega^2 W_{eff}^4 C_{ox}^4 \mu_{eff}^2}{I_{DS}^3} \times \Big(V_{GT}^2 V_{as}^2 V_{DS} - V_{GT}V_{as}(V_{GT} + V_{as})V_{DS}^2 + \frac{1}{3}(V_{GT}^2 + 4V_{GT}V_{as} + V_{as}^2)^2 V_{DS}^3 - \frac{1}{2}(V_{GT} + V_{as})V_{DS}^4 + \frac{1}{5}V_{DS}^5\Big) \tag{6.23}$$

where $V_{GT} = V_{GS} - V_{TH}$.

- **Induced gate noise from the velocity saturation region (region II)**

As shown in Appendix D, the induced gate noise and the channel noise are fully correlated. As discussed in previous section, there is no channel noise from region II because the local conductance is zero in region II. Therefore, it is assumed again that there is no induced gate noise generated from the velocity saturation region, as long as the impact ionization (i.e. the substrate current caused by hot carriers) in region II is negligible.

6.3 CORRELATION NOISE

As derived in Appendix D to obtain the induced gate noise, the noise spectral density of the noise correlation between the induced gate noise and the channel noise $\overline{\Delta i_g(x_o)\Delta i_d(x_o)^*}$ from a section Δx in the gradual channel region is

$$\overline{\Delta i_g(x_o)\Delta i_d(x_o)^*} = \frac{j\omega W C_{ox}}{I_{ds}} \cdot \frac{g(V_o)^2 \overline{\Delta v(x_o)^2}}{L_{elec}}[V_{as} - V(x_o)], \tag{6.24}$$

and again (6.24) is only valid in region I. Therefore, total spectral density of the correlation noise $S_{i_g i_d^*}$ from the gradual channel region is then obtained by the integration of (6.24) from $x = 0$ to $x = L_{elec}$ divided by Δf which is

$$S_{i_g i_d^*} = \frac{\overline{i_g i_d^*}}{\Delta f} = j\frac{4kT_o\omega W_{eff} C_{ox}}{L_{elec} \cdot I_{DS}^2} \times \left(V_{GT}^2 V_{as} V_{DS} - \frac{V_{GT}}{2}(V_{GT} + 2V_{as})V_{DS}^2 + \frac{1}{3}(2V_{GT} + V_{as})V_{DS}^3 - \frac{1}{4}V_{DS}^4 \right). \tag{6.25}$$

Because of no induced gate noise and channel noise generated from the velocity saturation region, the correlation noise between the channel noise and the induced gate noise generated from region II is zero.

6.4 REVIEW OF NOISE MODELS FOR SHORT-CHANNEL MOSFETS

In this section, physics-based RF noise models of the channel noise, induced gate noise and their correlation published in the literature [21],[34],[35],[37],[38],[61],[69],[74] for short-channel MOSFETs will be briefly reviewed and discussed.

6.4.1 Modeling of Channel Noise

To date, there are many publications on the high-frequency channel noise modeling of short-channel MOSFETs [21],[34],[35],[37],[38],[61],[69],[74]. The channel noise which is white (or frequency independent) and is included in the equivalent circuit model (as shown in fig. 5.15) by adding the noise current source $\overline{i_d^2}$ between the intrinsic drain and source terminals, but its value is not determined by the output resistance R_{DS}. The conventional noise model for long-channel MOSFETs [66] for $\overline{i_d^2}$ based on the Nyquist theory and the DC model of MOSFETs successfully predicted the channel noise of the short-channel devices working in the linear region. However, for RF ICs, the MOSFETs usually operate in the saturation region for most applications, and it is often observed that the channel noise generated from the short-channel devices working in the saturation region is higher than the prediction obtained from the conventional channel noise theory [21],[34],[35],[56]. Therefore, how to explain the noise enhancement in short-channel

MOSFETs becomes crucial in the channel noise modeling. In this section, the noise models [21],[34],[35],[37],[38],[61], [69],[74] will be briefly reviewed from three different aspects - the calculation method of the noise current, the model derivation of the channel noise, and the modeling of the conducting channel.

- **Noise current calculation**

The total noise current at the drain terminal is obtained by summing the noise contribution from each section in the channel. There have been two different calculation approaches presented in the literature to compute the total spectral density of the noise current $\overline{i_d^2}$. The first approach is to obtain the spectral density of the noise current at the drain terminal from each channel section and integrate each noise current density along the channel [21],[34],[35],[38],[69],[74]. The other approach is to integrate each noise voltage density along the channel and then multiply the total spectral density of the noise voltage by g_{DS}^2, where g_{DS} is the output conductance [37],[61]. The second approach is essentially not correct because it is assumed that a local noise source $\Delta v(x_0)$ can be translated into a terminal fluctuation Δv_{DS} which is correct for resistors, but not for MOSFETs. Therefore, from the model derivation in [38] and [66], the channel noise from each section in the channel should be calculated based on the first approach, i.e.

$$\overline{\Delta i_d(x_o)^2} = g^2(x_o) \cdot \overline{\Delta v(x_o)^2} \qquad (6.26)$$

where $g(x_o)$ and $\overline{\Delta v(x_o)^2}$ are the local conductance and the noise voltage fluctuation at the position x_o, respectively. Based on the Nyquist theory and the DC model of MOSFETs in the absence of velocity saturation, (6.26) can be simplified to [66]

$$\overline{\Delta i_d(x_o)^2} = -\frac{4kT(x_o)\Delta f W\mu(x_o)Q(x_o)\Delta x}{L^2} \tag{6.27}$$

where k is Boltzmann's constant, $T(x_o)$ is the absolute lattice temperature at the position x_o, Δf is the bandwidth, $\mu(x_o)$ is the local mobility (cm^2/V.sec), $Q(x_o)$ is the local electron concentration (C/cm^2) at the position x_o, W is the channel width and L is the channel length of the transistor. The term $-Q(x_o)$ is positive because of the negative charge $Q(x_o)$ for electrons.

- **Modeling of a MOSFET's channel**

After reviewing the calculation method of these proposed models, what is the physical cause of the enhanced noise spectral density in short-channel devices, and how to properly model the noise enhancement are two key issues to be solved in any proposed model [21],[34],[35],[38],[69],[74]. In general, the proposed models can be divided into two categories according to the modeling of the channel. The first approach [35],[38],[74] is based on a one-section channel model in which the channel (or the inversion charge) only exists in the gradual channel region which is from the intrinsic source terminal to the pinch-off point. The hot electron effect in this region is proposed as the physical cause of the noise enhancement, and it is included in the noise model by treating the $T(x_o)$ in (6.27) as the electron temperature.

The second approach [21],[34],[69] is to develop the noise model based on a two-section channel model in which the channel of a MOSFET is divided into two regions - a gradual channel region of length $L_{elec} = L_{eff} - \Delta L$ (region I in fig. 6.1) and a velocity saturation region of length ΔL (region II in fig. 6.1). When a transistor works in the linear

region, L_{elec} is the same as L_{eff}. There are two main physical causes proposed to explain the noise enhancement based on this approach - extra noise from region II due to the hot electron effect [34],[69] and the channel length modulation (CLM) effect in region I [21]. However, the noise models presented in [34] and [69] are not correct because the equation used to calculate the noise contribution from the sections in region II is based on (6.27), which is only true in the absence of velocity saturation [66]. Therefore, the channel noise expressions from these proposed models [34],[69] are questionable. On the other hand, because the Ohm's law is not valid in the velocity saturation region, the local resistance ΔR usually used in the noise models [38],[66] is not defined, and therefore the thermal noise (or Johnson noise) theory cannot be applied in region II [36].

- **Noise from the velocity saturation region**

The key question for the noise modeling in region II is what is the noise mechanism if the thermal noise theory fails? Different noise mechanisms - drifting dipole layer model [36],[37] and diffusion noise model [70],[71] have been proposed for the noise calculation in velocity saturation region. However, as proposed in [21], it is assumed that there is no noise current generated from region II based on the following "thought" experiment. Let's assume that there exists a noise mechanism that generates a finite voltage fluctuation at a local position x_o in region II. Because the carriers in region II travel at their saturated velocity, the carriers will not respond to the local change of the electric field caused by the noise voltage fluctuation, i.e. $g_{DS}(x_o) = 0$. Therefore, based on (6.26), there will be no noise current (or current fluctuation) generated by the finite noise voltage at the position x_o in the velocity saturation region. This applies to all the sections in region II, and

therefore, it is assumed that the noise current from region II is zero (or negligible) as long as the impact ionization (i.e. the substrate current caused by hot carriers) in region II is negligible.

How to explain the enhancement of the noise current in short-channel MOSFETs assuming zero noise current from region II? Let's examine the derivation of (6.27) again based on the two-section channel model. If we treat the part of the channel in the gradual channel region as a single transistor with the channel length L_{elec}, then the local conductance $g(x_o)$ will become

$$g(x_o) = \frac{W\mu(x_o)(-Q(x_o))}{L_{elec}}. \tag{6.28}$$

According to the channel noise derivation in [19] and [38], the mean square value of the noise current $\overline{\Delta i_d(x_o)^2}$ delivered to the drain terminal from $\Delta R(x_o)$ is given by $\overline{\Delta v(x_o)^2}$ multiplied by the square of its local conductance $g(x_o)$, and it becomes [21]

$$\overline{\Delta i_d(x_o)^2} = -\frac{4kT(x_o)\Delta f W\mu_{eff}Q(x_o)\Delta x}{L_{elec}^2}. \tag{6.29}$$

Therefore, because of the local $g_{DS}(x_o)$ enhancement caused by the CLM effect in short-channel MOSFETs, more noise current $\overline{\Delta i(x_o)^2}$ will be delivered to the drain terminal from the same the local noise fluctuation $\overline{\Delta v(x_o)^2}$. Therefore, it is believed that the enhancement of the delivering capability of the channel, instead of extra noise sources in region I or II by hot electron effects, is the main reason causing the enhancement of the noise current in short-channel MOSFETs [21]. In addition, as proposed in [21] to obtain (6.29), it is assumed that the electric field in the x direction for most of the sections in the

gradual channel region is much less than the critical field E_{crit}, then the local mobility $\mu(x_o)$ is about the same as the effective mobility μ_{eff}. The impact of neglecting the velocity saturation effect in region I on the modeling of the channel noise will be discussed next.

- **Velocity saturation effect in gradual channel region**

As discussed before, the derivation of (6.29) is based on the assumption that the electric field in the longitudinal direction for most of the sections in the gradual channel region is much less than the critical field E_{crit}, i.e. the velocity saturation effect for sections in region I close to the boundary of regions I and II is ignored. As suggested in [38] and [74], the velocity saturation effect should be included in the channel noise modeling, especially for short-channel devices. If the velocity saturation effect in region I is included by modeling the local mobility with the empirical relation [38],[66]

$$\mu(x_o) = \frac{\mu_{eff}}{1 + E(x_o)/E_{crit}} \tag{6.30}$$

where $E(x_0)$ is the local electric field at the position x_0 and μ_{eff} is the effective mobility depending on the vertical field only, the DC drain current I_{ds} becomes

$$I_{ds} = \frac{W\mu_{eff}(-Q(x_o))}{1 + E(x_o)/E_{crit}} \cdot \frac{dV(x_o)}{dx} = \frac{\Delta V(x_o)}{\Delta R_{loc}(x_o)} \tag{6.31}$$

where $\Delta R_{loc}(x_o)$ is the local channel resistance at the position x_0. It is difficult to derive an analytical expression for $\Delta R_{loc}(x_o)$ from (6.31), but it can be observed quantitatively that the local channel resistance is increased due to the velocity saturation effect (i.e. $\Delta R_{loc}(x_o) > \Delta R(x_o)$), where $\Delta R(x_o)$ is the local resistance without the velocity saturation effect. This

implies that a higher thermal noise voltage is generated from the section at the position x_o close to L_{elec}.

However, as can be seen from (6.6), the local conductance $g_{loc}(x_o)$ at position x_o including the velocity saturation effect will be decreased because the local mobility $\mu(x_o)$ is reduced (i.e. $g_{loc}(x_o) < g(x_o)$). Therefore, the product $g_{loc}(x_o)^2 \bullet \Delta R_{loc}(x_o)$ is approximately about the same as $g(x_o)^2 \bullet \Delta R(x_o)$ or the difference between these two products is negligible [21]. This means that the impact of the velocity saturation effect in region I on the channel noise modeling is not as pronounced as that on the modeling of DC current, and it can be considered as a secondary effect compared to the CLM effect in the channel noise modeling of short-channel devices. If the noise model only takes care of the impact of the velocity saturation effect on the conductance reduction but not on the enhancement of the local resistance, it will predict a lower noise spectral density. The noise model including the CLM effect can achieve a good noise prediction without including the hot electron effect [21], and it is believed that the enhancement of the local conductance by the CLM effect is the main physical cause of the noise enhancement in short-channel MOSFETs. The noise equations of the models [21],[38],[66],[74] are summarized in Table 6.1.

Table 6.1: Summary of the channel noise equations in [21],[38],[66] and [74] used in the model verification.

Tsividis [66]	$\overline{i_d^2} = \frac{4kT_o\Delta f}{L_{eff}^2}\mu_{eff}(-Q_{inv})$
van der Ziel [38]	$\overline{i_d^2} = \frac{4kT_o\Delta f}{L_{eff}^2 I_{DS}}\int_0^{V_{DS}}\left(1+\frac{E}{E_{crit}}\right)^n g(V)^2 dV$
Klein [74]	$\overline{i_d^2} = \frac{4kT_o\Delta f}{L_{eff}^2}\mu_{eff}(-Q_{inv}) + \frac{8}{3}qv_{sat}\tau_e\frac{I_{DS}}{L_{eff}}\Delta f$
Chen and Deen [21]	$\overline{i_d^2} = \frac{4kT_o\Delta f}{L_{elec}^2}\mu_{eff}(-Q_{inv}) + \delta\frac{4kT_o I_{DS}\Delta f}{L_{elec}^2 E_{crit}^2}V_{DS}$

6.4.2 Induced Gate Noise and its Correlation with the Channel Noise

The proposed models in [32] and [38] are similar to the channel noise modeling, and they can be characterized into two categories according to the channel model used - one-section channel model [38] or two-section channel model [32]. The model proposed in [32] assumes that there is induced gate noise generated in the velocity saturation region (region II). However, as can be seen in [38], the induced gate noise is fully correlated with the channel noise. As discussed in section 6.2, the induced gate noise and its correlation with the channel noise from one section in region I can be obtained from

$$\begin{aligned}\overline{\Delta i_g(x_o)\Delta i_g(x_o)^*} &= \left(\frac{\omega W L_{elec} C_{ox}}{I_{ds}}\right)^2 \cdot \frac{g(V_o)^2\overline{\Delta v(x_o)^2}}{L_{elec}^2}[V_{as} - V(x_o)]^2 \\ &= \frac{\omega^2 C_{GS}^2 \Delta f}{I_{ds}^2}\cdot\overline{\Delta i_d(x_o)^2}[V_{as} - V(x_o)]^2\end{aligned} \quad (6.32)$$

and

$$\overline{\Delta i_g(x_o)\Delta i_d(x_o)^*} = \frac{j\omega W L_{elec} C_{ox}}{I_{ds}} \cdot \frac{g(V_o)^2 \overline{\Delta v(x_o)^2}}{L_{elec}^2}[V_{as} - V(x_o)] \tag{6.33}$$
$$= \frac{j\omega C_{GS}\Delta f}{I_{ds}} \cdot \overline{\Delta i_d(x_o)^2}[V_{as} - V(x_o)]$$

where $g(V_o)$ and V_{as} are defined in (6.21) and (6.22), respectively. Again, (6.32) and (6.33) are obtained by assuming that the velocity saturation effect for sections in region I close to the boundary of regions I and II can be ignored, and V_{DS} becomes V_{DSsat} when transistors operate in saturation. Based on the two-section channel model and neglecting the perturbation of L_{elec} caused by $\overline{\Delta v(x_o)^2}$ in region I, it is expected that the induced gate noise is only generated in region I because $\overline{\Delta i_d(x_o)^2} = 0$ in region II as discussed before. Therefore, the proposed induced gate noise from region II in [32] should not exist. In addition, the equation to calculate the induced gate noise from region II in [32] is not correct because it is based on the thermal noise theory which is only valid in region I and it cannot be applied to region II [36]. Therefore, the induced gate noise and its correlation with the channel noise should be obtained by integrating $\overline{\Delta i_g(x_o)\Delta i_g(x_o)^*}$ and $\overline{\Delta i_g(x_o)\Delta i_d(x_o)^*}$ over region I only, as discussed previously in sections 6.2 and 6.3.

6.4.3 Measurements and Discussions

To compare the best fitting from different noise models [38] and [74] including the hot electron effect, fig. 6.7 shows the extracted (symbols) and simulated (lines) spectral density of the channel noise $S_{i_d^2}$ versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm,

respectively biased at V_{DS} = 1.5 V. The solid lines are obtained by using the channel noise model in [21], the dotted-dashed lines are obtained based on the noise model in [38] with the hot electron effect factor n = 2.6, and the dashed lines are based on the noise model in [74] with the fitting parameter $\tau_e = 8\times10^{-10}$ second. It is shown that the noise models based on including the hot electron effect predict different slopes in the $S_{i_d^2}$ versus V_{GS} characteristics when compared to the measured data.

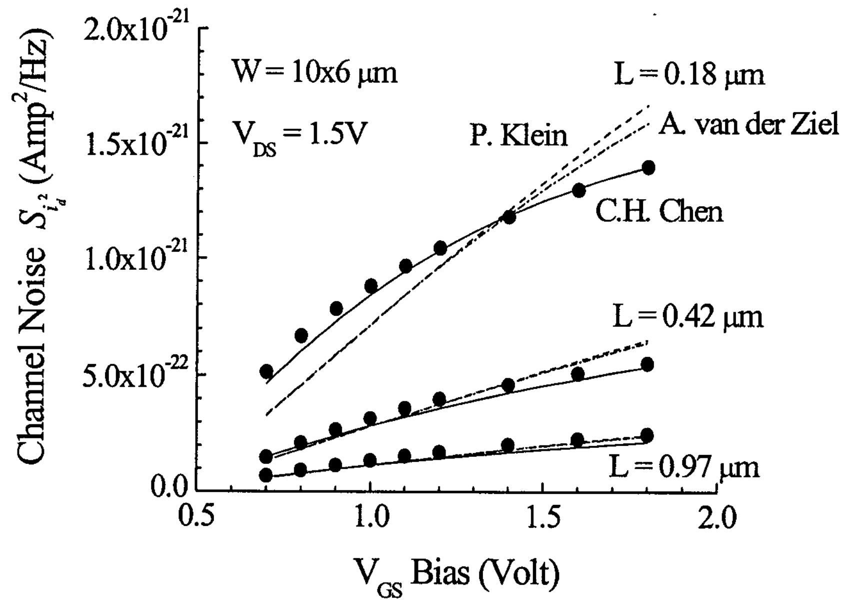

Fig. 6.7: Extracted (symbols) and simulated (lines) spectral density of the channel noise versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V including the hot electron effect in the proposed models in [38] and [74].

For the induced gate noise and its correlation with the channel noise, figs. 6.8 and 6.9 show the extracted (symbols) and simulated (lines) spectral densities of the induced gate noise $S_{i_g^2}$ and the correlation noise $S_{i_g i_d^*}$ versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm

and 0.18 μm, respectively biased at V_{DS} = 1.5 V based on the proposed noise model in [38] with/without the velocity saturation effect and the hot electron effect. The solid lines are obtained by using the channel noise model in [38] without including the hot electron effect and the velocity saturation effect. The dotted-dashed and the dashed lines are obtained based on the noise model in [38] with (n = 2.6) and without (n = 0) the hot electron effect, respectively. Similar to what has been discussed in the modeling of the channel noise, the model with the velocity saturation effect predicts lower $S_{i_g^2}$ and $S_{i_g i_d^*}$ because it neglects the local resistance enhancement.

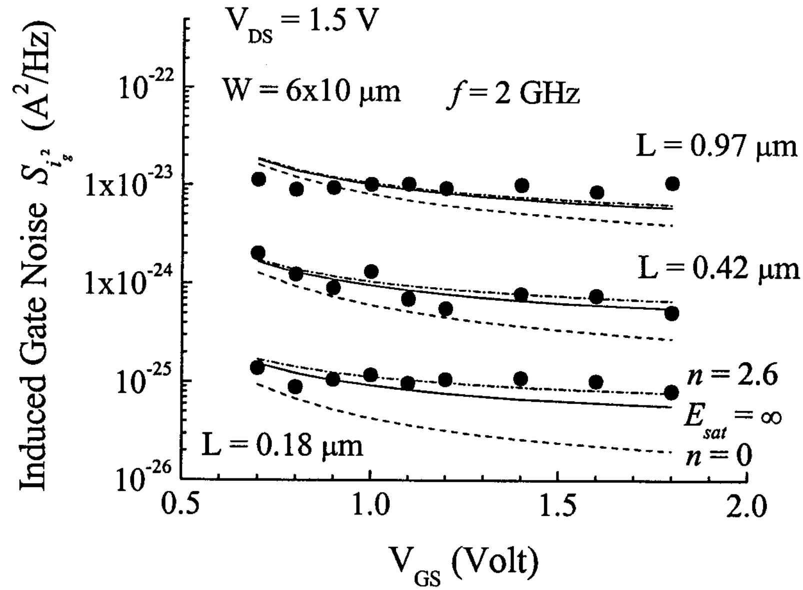

Fig. 6.8: Extracted (symbols) and simulated (lines) spectral density of the induced gate noise versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V based on the proposed noise model in [38] with/without the velocity saturation effect and the hot electron effect.

On the other hand, including the hot electron effect can reasonably solve the discrepancy in $S_{i_g^2}$, but degrade the prediction of $S_{i_g i_d^*}$. This is because the hot electron term in [38] enhances the negative value caused by the term V_{as} - V_o when V_o is close to V_{DSsat}. Finally, from (6.32) and (6.33), and figs. 6.8 and 6.9, the CLM effect does not affect $S_{i_g^2}$ and $S_{i_g i_d^*}$ too much because the net effect of the L_{elec} appears in the numerator of (6.32), not in the denominator as shown in (6.29) for channel noise. Using the channel noise model with the CLM effect [21] and the induced gate noise in [38] without the hot-electron effect and the velocity saturation effect, then the high-frequency noise performance of a MOSFET can be accurately calculated if the element values in the AC small-signal model and its DC characteristics are known.

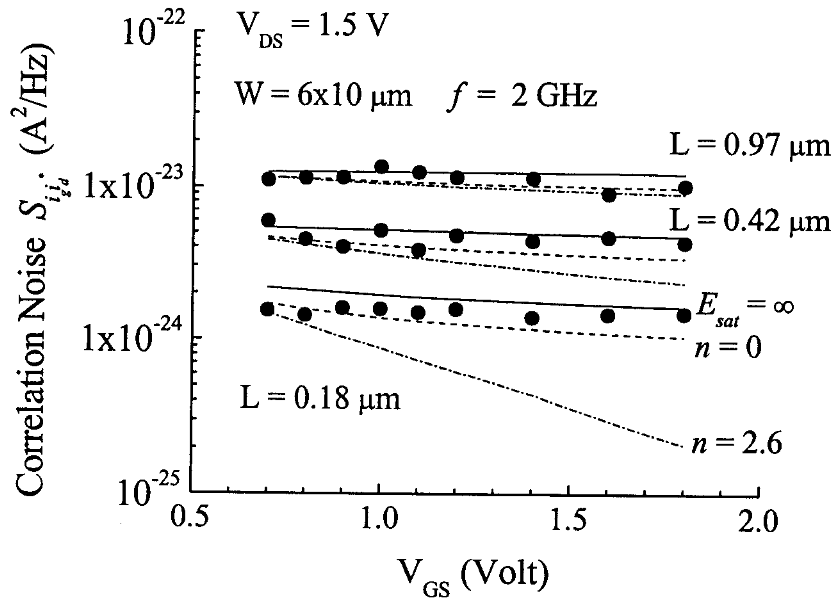

Fig. 6.9: Extracted (symbols) and simulated (lines) spectral density of the correlation noise versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V based on the proposed noise model in [38] with/without the velocity saturation effect and the hot electron effect.

Chapter 7

DESIGN OF LOW NOISE AMPLIFIERS

7.1 DESIGN CONSIDERATION FOR LOW NOISE CIRCUITS

Before going into the design of a low noise amplifier in detail, the most general questions being asked by the circuit designers are how to properly choose the device size, select the bias conditions (V_{GS} and V_{DS}), and design the device geometry to achieve the best noise performance for their RF circuits. In this section, the noise behavior of MOSFETs will be explained qualitatively based on the extracted noise sources and noise parameters, and this leads to the proper selection of the device size and the determination of the bias conditions.

7.1.1 Selection of Bias Conditions

Figs. 5.26 and 7.1 show the unity gain frequency (f_T) and the minimum noise figure (NF_{min}) versus gate bias V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V. The V_{GS} biases for the peak f_T and the lowest NF_{min} are reduced (arrows in the figures) when the channel length is reduced. This trend makes MOSFETs very attractive for low power, low noise RF circuit

designs. The measured peak f_T of the 0.18 μm devices is about 50 GHz at the specified V_{DS} = 1.0V and the lowest NF_{min} is about 0.5 dB at 2 GHz.

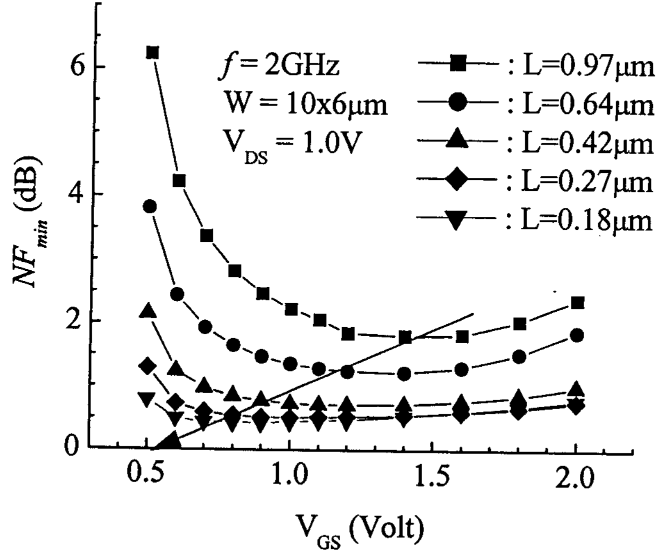

Fig. 7.1: Simulated intrinsic minimum noise figure (NF_{min}) versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V using new noise models presented in Chapter 6.

In general, as shown in fig. 7.1, the minimum noise figure NF_{min} decreases when V_{GS} increases at low V_{GS} region, and it increases in the high V_{GS} region. This can be understood by comparing the measured transconductance g_m (shown in fig. 5.31) and the extracted channel noise $\overline{i_d^2}$ (shown in fig. 5.43) versus V_{GS} characteristics. In general, NF_{min} is mainly determined by these two factors - g_m and $\overline{i_d^2}$ [8]. In the low V_{GS} region, the increasing rate of g_m (or the first order derivative of g_m with respect to V_{GS}) is greater than that of $\overline{i_d^2}$ and therefore it causes the drop of NF_{min}. However, in the high V_{GS} region, since g_m decreases but $\overline{i_d^2}$ keeps increasing, this causes NF_{min} to increase.

There are two observations that can be made from this explanation. First, as shown in fig. 7.1, the V_{GS} value for the lowest NF_{min} becomes lower when the channel length is reduced, and this is because of the faster increase of g_m for the short channel devices. Second, from figs. 5.31 and 7.1, it is shown that the lowest NF_{min} actually happens before the peak g_m instead of at the peak g_m. This is because the derivative of g_m with respect to V_{GS} is zero at the peak g_m.

As for the V_{DS} dependence, figs. 7.2 to 7.4 show the measured intrinsic transconductance g_m, minimum noise figure NF_{min} and equivalent noise resistance R_n versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm biased at V_{DS} = 1.0 V 1.5 V and 2.0 V, respectively. It is shown that at higher V_{DS}, because of the increase of g_m in the high V_{GS} region, this causes NF_{min} and R_n drop for these high V_{GS}. Therefore, a higher V_{DS} bias will make the noise performance of the transistor less sensitive to the V_{GS} variation, but then the power consumption will be higher.

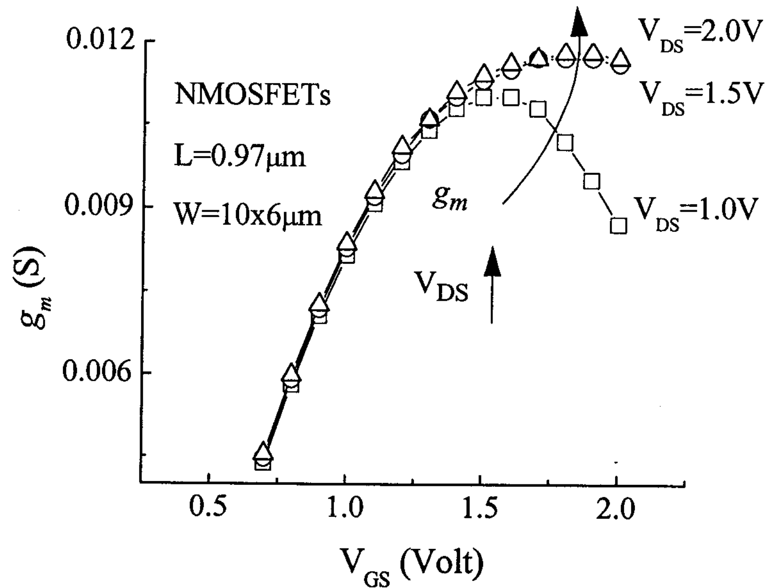

Fig. 7.2: Measured intrinsic transconductance (g_m) versus V_{GS} characteristics extracted from the measured $Re(y_{21})$ at the low frequency region for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm biased at V_{DS} = 1.0 V 1.5 V and 2.0 V, respectively.

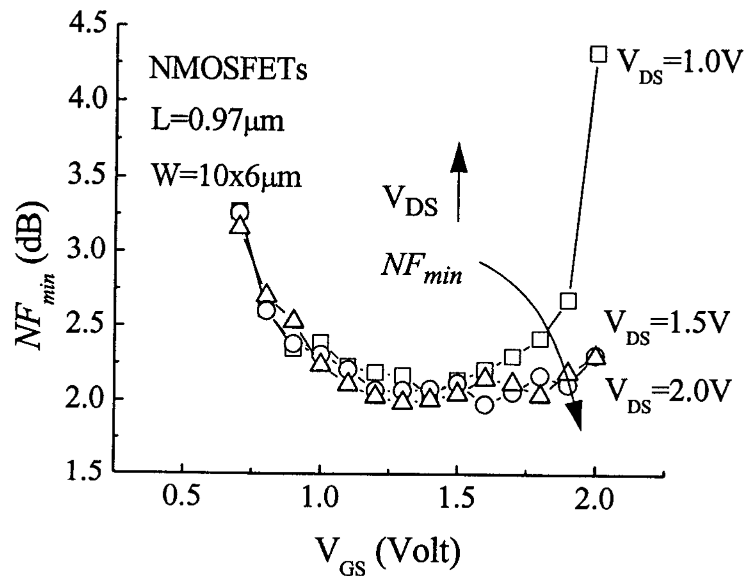

Fig. 7.3: Measured intrinsic minimum noise figure (NF_{min}) versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm biased at V_{DS} = 1.0 V 1.5 V and 2.0 V, respectively.

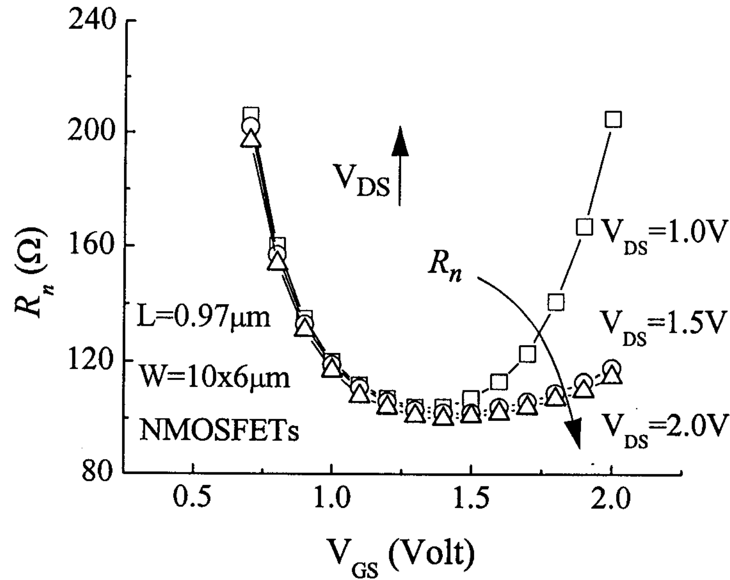

Fig. 7.4: Measured intrinsic equivalent noise resistance (R_n) versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm biased at V_{DS} = 1.0 V 1.5 V and 2.0 V, respectively.

7.1.2 Consideration of Device Geometry - Multi-Finger Gate Design

In general, the effective gate resistance R_G of a single finger device with the input signal from one side of the transistor as shown in fig. 7.5(a) can be modeled [84] as

$$R_G = \frac{1}{3} \times R_{gsh} \times \frac{W}{L} \tag{7.1}$$

where 1/3 is used to model the distributed effects of the gate resistance, R_{gsh} is the sheet resistance, W and L are the channel width and length, respectively.

In order to improve the noise performance by reducing the gate resistance R_G, two approaches were investigated. One involves metal-reinforced gates [85],[86] and the other employs the multi-finger design technique. The first approach reduces the R_{gsh} so as to reduce R_G. This approach can achieve the goals of reducing the overall noise level, but it

requires a change to the fabrication process. The multi-finger gate design [87] shown in fig. 7.5(b) in which some narrower devices are connected in parallel to reduce R_G based on the existing technology can improve the overall noise performance as well. In general, as shown in fig. 7.5(b), because the signal path is reduced by a factor of $1/n$ when there are n narrower transistor connected in parallel, where n is the number of fingers, then the effective gate resistance R_G will then be reduced by a factor of n^2.

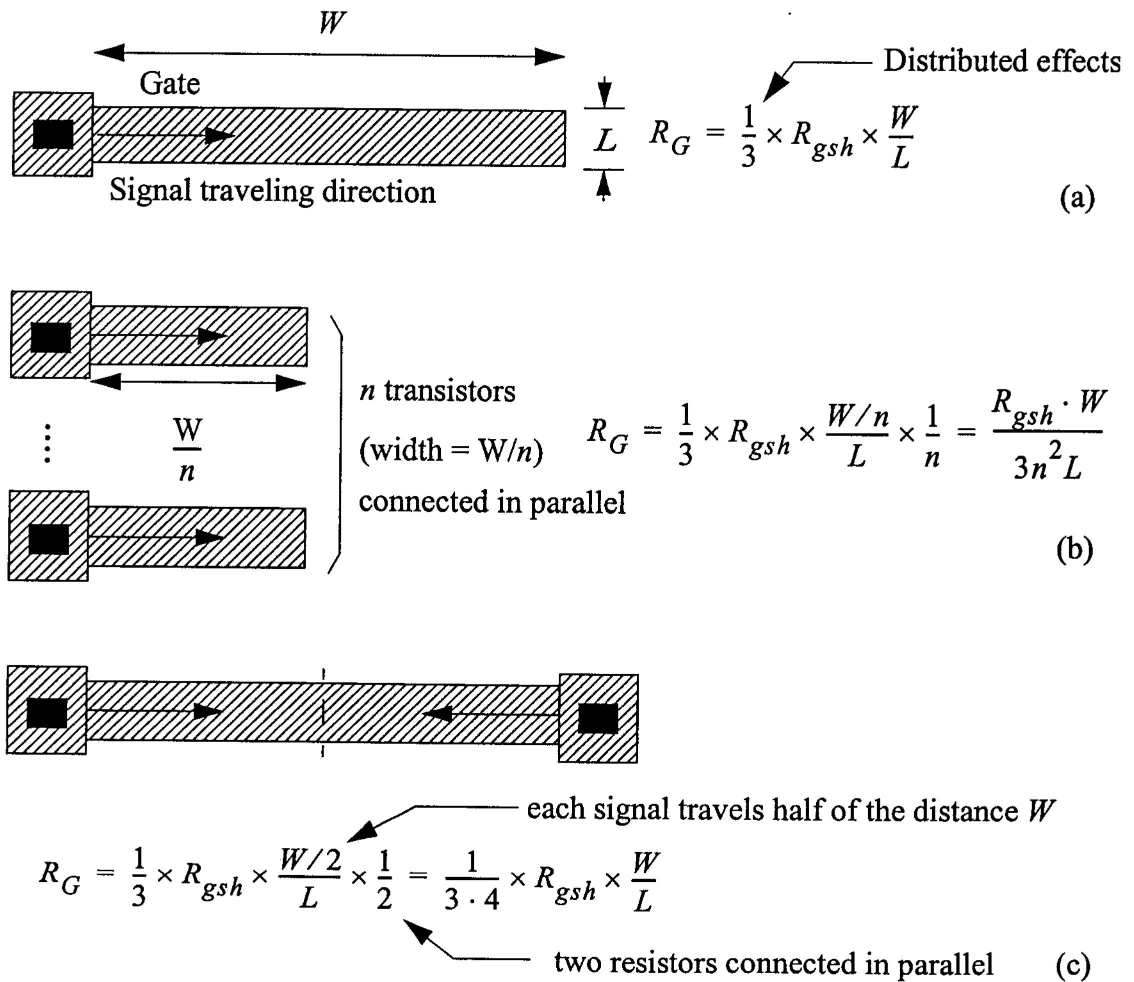

Fig. 7.5: Effective gate resistance (R_G) of (a) a single finger design with the input signal from one side of the transistor, (b) a multi-finger design with the input signal from one side of the transistor and (c) a single finger design with the input signal from both sides of the transistor.

Fig. 7.6 shows the measured NF_{min} (symbols) of a 60 μm transistor and a multi-finger gate design in which there are six 10 μm wide transistors connected in parallel. The calculated NF_{min} (dashed lines) for the 1 × 60 μm transistor is based on R_G = 175 Ω and the R_G value for the calculation of NF_{min} for the 6 × 10 μm transistor is 175 Ω/36. It is shown that the multi-finger gate design will decrease the overall noise performance by decreasing the gate resistance R_G. Also, good agreement between the measured and calculated NF_{min} of multi-finger gate design is obtained.

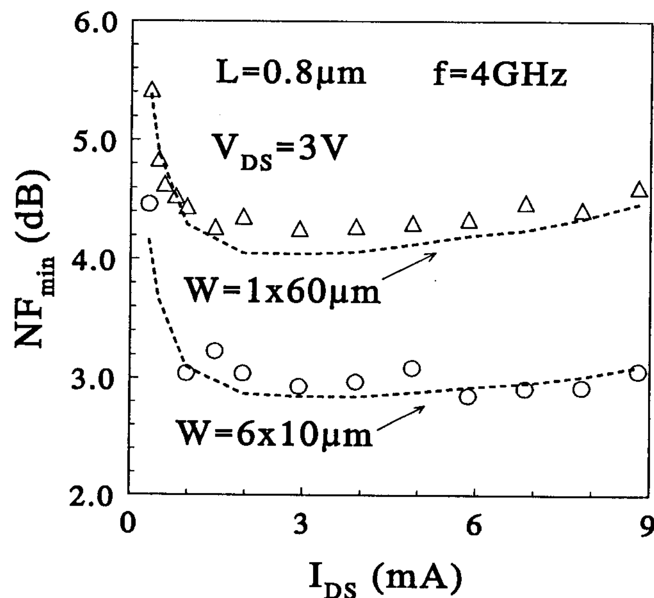

Fig. 7.6: The measured (symbols) and calculated (dashed lines) NF_{min} of a single 60 μm transistor (triangle) and a multi-finger gate design (circle) with six 10 μm wide transistors connected in parallel. The calculated data for multi-finger gate design is obtained by changing R_G to R_G/n^2 (n = 6 in this calculation) and the rest of model parameters are the same as those used in the noise calculation for the single 60 μm transistor [57].

An additional way to reduce the gate resistance is to apply the input signal from both ends of a transistor, as shown in fig. 7.5(c). In this case, since the signal path for the signal to travel is reduced by a half and there are two half-width transistors connected in

parallel, therefore the effective gate resistance can be reduced by another factor of 4 in this configuration.

7.2 DESIGN OF LOW NOISE AMPLIFIERS

For the design of a low noise amplifier (LNA), in addition to the selection of the device size and bias condition, spiral inductors are often used in the design of an LNA. This section will briefly discuss the inductor model for the spiral inductor on a silicon substrate, and the element values in the inductor model will be obtained from the measurements. Based on the noise models presented in Chapter 6, the design strategies discussed in the section 7.1 and the inductor model, the impact of the accuracy of the noise models on the simulated circuit performance will also be discussed.

7.2.1 Model of Spiral Inductors

An example of a rectangular planar spiral inductor is shown in fig. 7.7. For the key device geometry parameters shown in fig. 7.7, L_1 is the length of first segment, L_2 is the length of second segment, L_3 is the length of third segment, L_n is length of last segment, W is conductor width, and S is the spacing between the conductors. For the layout of a spiral inductor, the objective is to obtain the desired inductance value with the smallest area, while keeping the parasitic capacitance low. In addition, the Q-factor is a very important parameter in the design of the inductor, and it is a function of frequency and inductor geometry. By changing the geometry, the Q-factor can be optimized to the highest value for the frequency range at which the inductor will be used.

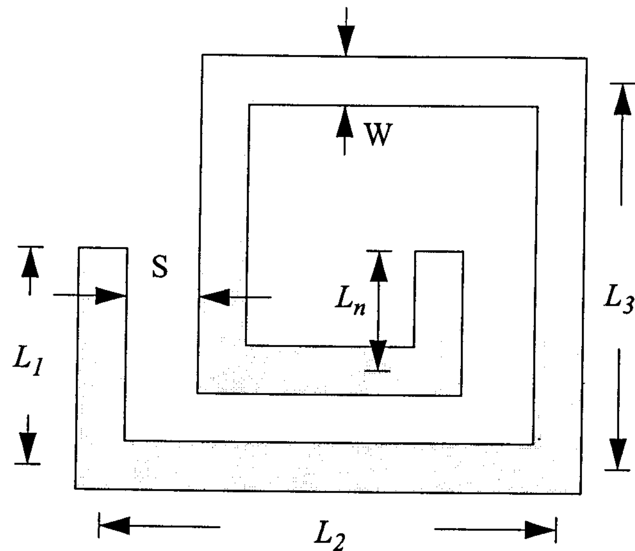

Fig. 7.7: Example of microstrip rectangular inductor (1 1/2-turn) [88].

- **Inductor circuit model**

In general, the spiral inductor is a distributed structure. There are capacitive and inductive couplings between each of the microstrip lines, and the series resistance is distributed over the entire microstrip structure. These complicated distributed effects of the spiral inductor can be ignored up to the inductor's first self-resonance frequency, and the distributed model of the spiral inductor can be reduced to a lumped one. A basic lumped element representation of the spiral inductor is shown in fig. 7.8. In this model, L_s represents the series inductance of the structure, R_s represents the series resistance of the metal, C_i models the inter-turn capacitance between the metal traces, C_{sub1} and C_{sub2} represent the capacitance from the metal layer to the ground plane, and R_{sub1} and R_{sub2} are the substrate resistance.

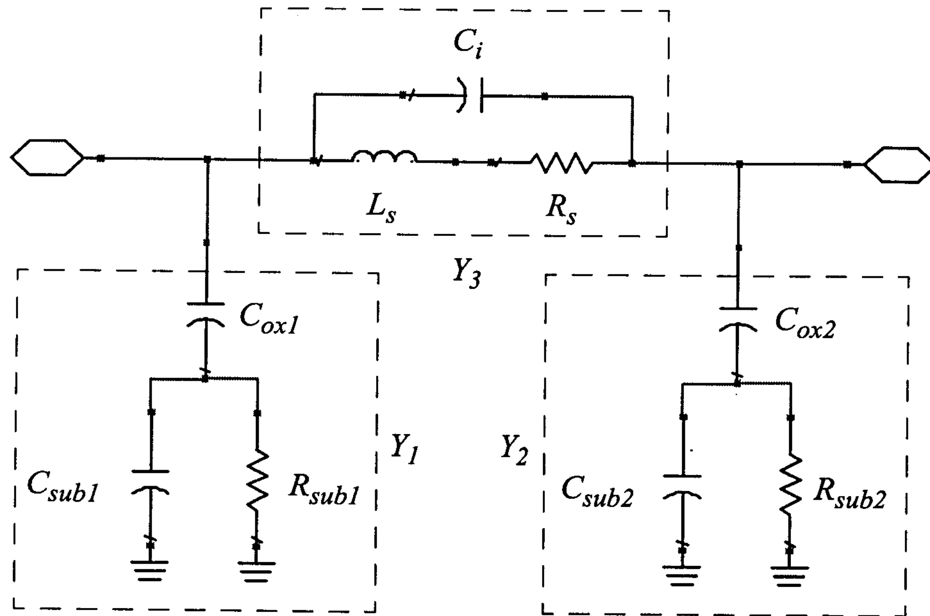

Fig. 7.8: Equivalent circuit of a spiral inductor on silicon substrate.

- **Extraction of element values**

After the circuit model is developed, element values in the circuit model must be obtained. A general technique is developed to extract lumped element values of the model from measured *s*-parameters. After removing the parasitic effects from the probe pads, the three-step extraction procedure is now described in the following [89].

1. Convert the measured s-parameters to their y-parameters using (4.2) in Chapter 4.
2. Y_1, Y_2 and Y_3 in the two port π-network shown in fig. 7.8 can be obtained by

$$Y_2 = -Y_{12} \ (or \ -Y_{21}), \tag{7.2}$$

$$Y_1 = Y_{11} + Y_{12}, \tag{7.3}$$

and

$$Y_3 = Y_{22} + Y_{21}. \qquad (7.4)$$

In addition, from the equivalent circuit model, Y_1, Y_2 and Y_3 can be expressed as

$$Y_1 = \frac{j\omega C_{ox1} \cdot (1/R_{sub1} + j\omega C_{sub1})}{1/R_{sub1} + j\omega(C_{ox1} + C_{sub1})}, \qquad (7.5)$$

$$Y_2 = \frac{j\omega C_{ox2} \cdot (1/R_{sub2} + j\omega C_{sub2})}{1/R_{sub2} + j\omega(C_{ox2} + C_{sub2})}, \qquad (7.6)$$

$$Y_3 = j\omega C_i + \frac{1}{j\omega L_s + R_s}, \text{ and} \qquad (7.7)$$

$$R_s = R_{sdc} \cdot \left(1 + \sqrt{\frac{f}{15 \cdot 10^9}}\right). \qquad (7.8)$$

3. Perform parameter optimization on (7.5) to (7.7) to get the element values.

To verify the inductor model, a 2.5 turn square spiral inductor is designed in a 0.18 μm CMOS technology with the geometrical parameters shown in Table 7.1. The extracted element values are shown in Table 7.2.

Table 7.1: Geometrical parameters of 2.5 turn spiral inductor [89].

Number of terms	number of segments	W (μm)	S (μm)	L_1 (μm)	L_2 (μm)	L_3 (μm)	L_n (μm)
2.5	7	30	1.5	180	320	300	90

Table 7.2: Extracted element values of the 2.5 turn square spiral inductor [89].

L_s (nH)	R_{sdc} (Ω)	C_f (fF)	C_{ox1} (fF)	C_{ox2} (fF)	C_{sub1} (fF)	C_{sub2} (fF)	R_{sub1} (Ω)	R_{sub2} (Ω)
3.56	4.396	2.17	188	192	145	161	225	213

Based on the element values shown in Table 7.2 and (7.8), the measured and simulated S_{11}, S_{12}, Q-factor and the inductance value L are shown in figs. 7.9 and 7.10.

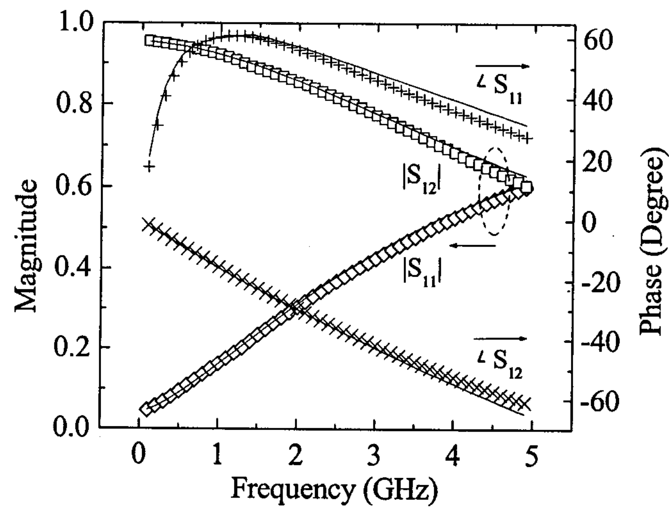

Fig. 7.9: Measured (symbols) and simulated (lines) S_{11} and S_{12} of inductor 1 (Ind1) based on the equivalent circuit model shown in fig. 7.8 and the element values shown in Table 7.2 [89].

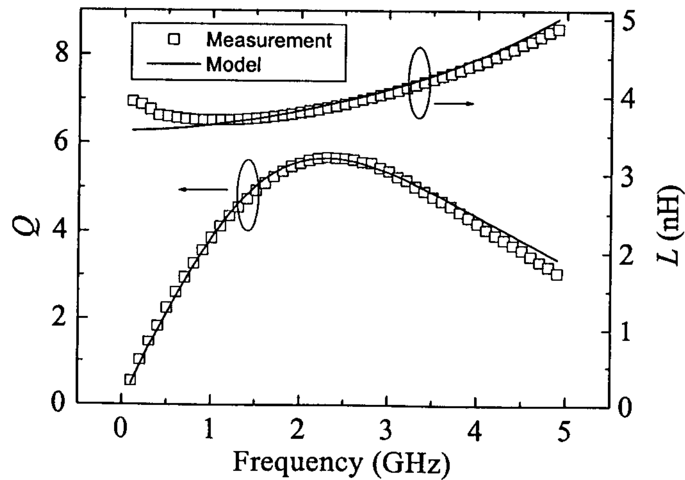

Fig. 7.10: Measured (symbols) and simulated (lines) quality factor Q and the inductance L of 2 2.5-turn inductor (Ind1) based on the equivalent circuit model shown in fig. 7.8 and the element values shown in Table 7.2 [89].

After the inductor model and the element values are obtained, they are used in the simulation of a low noise amplifier to find the impact of the noise models on the circuit simulation.

7.2.2 Impact of Noise Models on the Design of an LNA

In order to find out the impact of the noise models on the design of an LNA, a two-stage amplifier is proposed and shown in fig. 7.11.

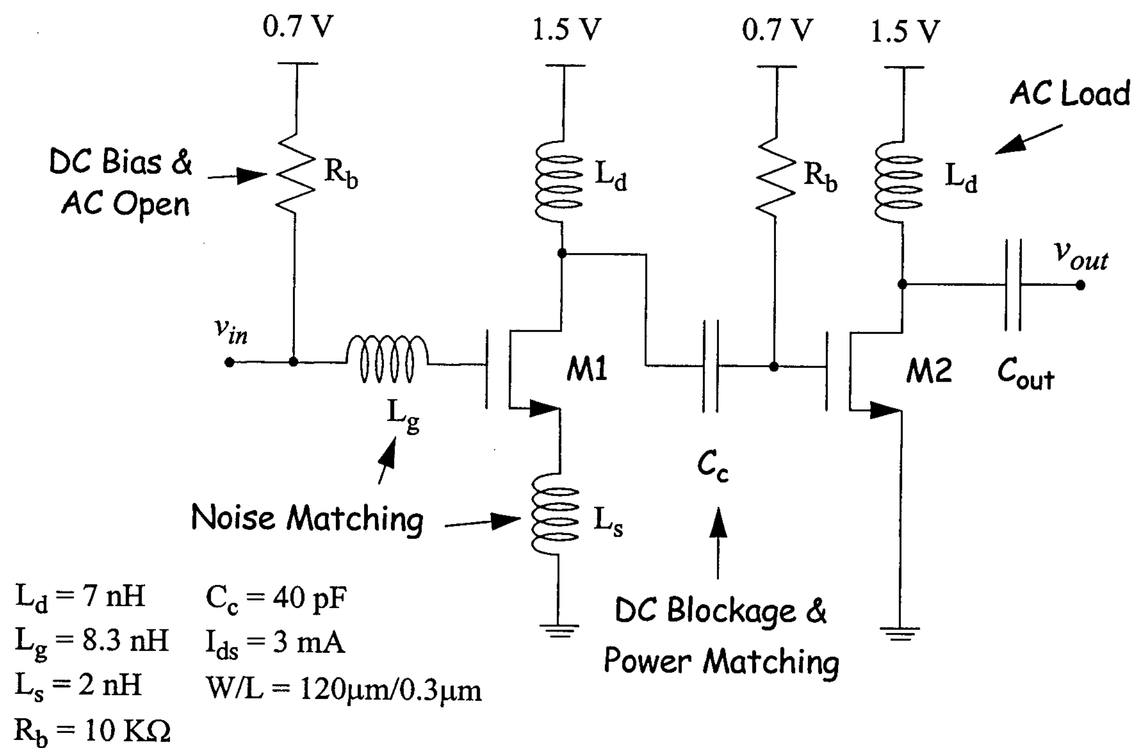

Fig. 7.11: Two-stage low noise amplifier to verify the impact of noise models on the simulated noise figure.

In fig. 7.11, the transistor M_1 is the first stage to minimize the noise figure and M_2 is the second stage to boost the power gain. The inductors L_g and L_s are used to provide the noise

matching, and L_d acts as an AC load. The capacitor C_c is to provide an DC blockage and a power matching between two stages. R_b is used as an element for DC bias and serves as an AC open at high frequency. Based on the element values shown in fig. 7.11 and the inductor model shown in fig. 7.8, fig. 7.12 shows the simulated noise figure (*NF*) versus frequency characterization based on the noise model using L_{elec}, L_{eff} (solid lines) and L_{elec} without the induced gate noise $\overline{i_g^2}$ and the correlations $\overline{i_g i_d^*}$ (dashed line). It is shown that using L_{eff} to calculate $\overline{i_d^2}$, the *NF* is underestimated about 0.3 dB and the optimized frequency is underestimated about 0.1 GHz (from 1.72 GHz to 1.62 GHz). As for the impact of $\overline{i_g^2}$ and $\overline{i_g i_d^*}$, the error in *NF* is about 0.1 dB and the optimized frequency is overestimated about 0.1 GHz. Figs. 7.13 and 7.14 show the power gain S_{21} of the two-stage low noise amplifier.

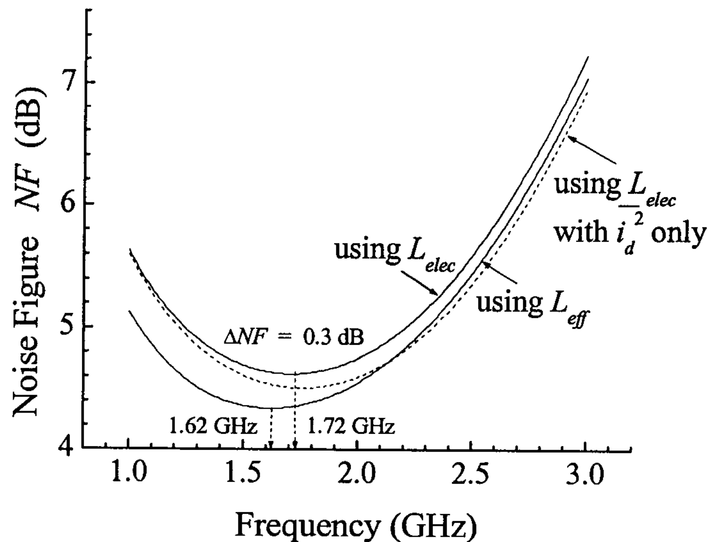

Fig. 7.12: Simulated noise figure (*NF*) versus frequency characterization for the circuit shown in fig. 7.11 based on the noise model using L_{elec}, L_{eff} (solid lines) and L_{elec} without the induced gate noise $\overline{i_g^2}$ and the correlations $\overline{i_g i_d^*}$ (dashed line).

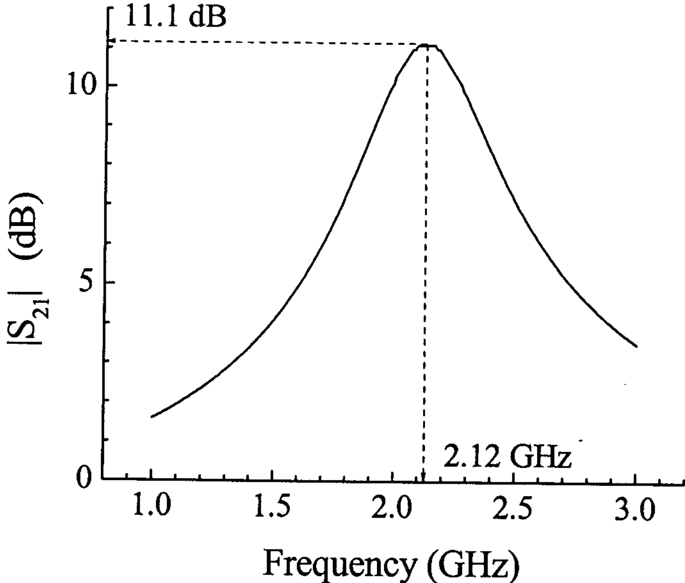

Fig. 7.13: Simulated magnitude of the power gain S_{21} for the design of the low noise amplifier shown in fig. 7.11.

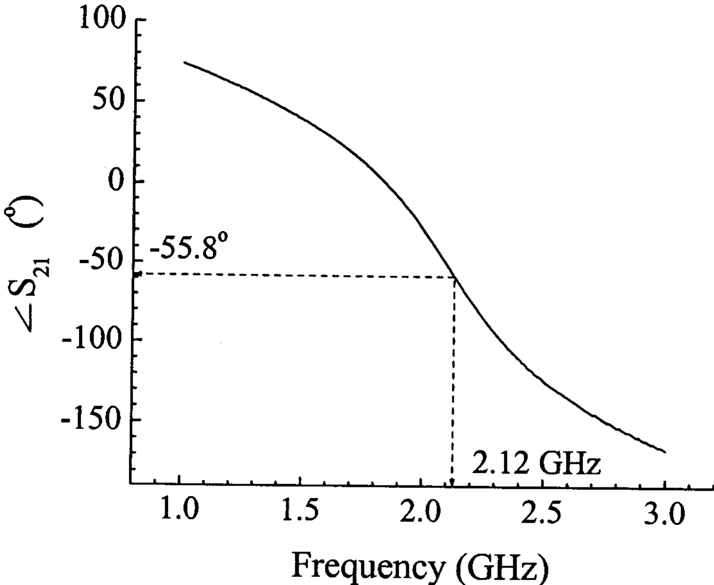

Fig. 7.14: Simulated phase of the power gain S_{21} for the design of the low noise amplifier shown in fig. 7.11.

Chapter 8

CONCLUSIONS AND RECOMMENDATIONS

8.1 CONCLUSIONS

This thesis presents a systematic framework for the RF noise characterization of MOSFETs. The systematic procedure to calculate the noise parameters of MOSFETs, the new, innovative noise and s-parameter de-embedding procedures, the noise source extraction methods to obtain the spectral density of the channel noise, induced gate noise and their correlation directly from the intrinsic RF noise and scattering parameters, and the new physics-based noise models to calculate the channel noise for low noise, wireless applications are the main contributions of this thesis. For the two calculation methods using matrix analysis and circuit simulator to calculate the four noise parameters of MOSFETs, the advantage of the direct matrix analysis is that it easily allows to characterize the noise sources in the model if there is any correlation existing between the noise sources. This analysis can serve as a tool to develop proper noise models and to verify their implementation in compact models used in circuit simulators.

The accuracy of the de-embedding procedure which removes the parasitic effects from the probe pads and the metal interconnections to obtain the intrinsic noise and RF performance of transistors is the first concern for the high-frequency characterization of

any active device. A general de-embedding procedure of noise parameters based on the cascade configuration for on-wafer RF measurements of MOSFETs has been presented in detail and was verified with measurements. This method improves the accuracy of de-embedded results at high frequencies by properly taking into account the distributed capacitive effect of metal interconnections without lumping it with the bonding pads. Therefore this de-embedding procedure is more suitable for the scattering or noise parameters measured at higher frequencies or for DUTs with long or wide metal interconnections.

After the intrinsic noise parameters are obtained, two extraction methods to obtain the spectral densities of the channel noise, induced gate noise and their correlation from these noise parameters to serve as a direct target were presented. The first method using the extrapolation method down to DC or low frequencies only extracts the channel noise, and it is shown that among the noise parameters - NF_{min}, R_n, R_{opt} and X_{opt}, only the equivalent noise resistance R_n at low frequencies provides a direct insight of the channel noise. Therefore, any proposed channel noise model should compare the calculated and measured R_n versus frequency characteristics for the model verification, instead of just comparing NF_{min} which will be affected by $\overline{i_g^2}$ as well. The other direct extraction procedure to obtain the induced gate noise, channel noise and their correlation noise in MOSFETs directly from the intrinsic scattering and noise parameters is also presented in detail and verified with measurements. In general, the channel noise $\overline{i_d^2}$ is frequency independent which confirms the assumption used in the first extraction method, and it increases when the channel length decreases for all bias conditions at a fixed V_{DS} because of higher local output conductance

g_{DS}. On the other hand, the induced gate noise $\overline{i_g^2}$ and its correlation with the channel noise $\overline{i_g i_d^*}$ are proportional to f^2 and f, respectively, and they both decrease when the channel length decreases because of the decrease of C_{GS}. In the case of the cross-correlation coefficient c, it is frequency independent and decreases when the channel length decreases. It was found that $\overline{i_d^2}$ and $\overline{i_g i_d^*}$ have a strong V_{GS} bias dependence and first they increase, then tend to saturate when V_{GS} increases, but $\overline{i_g^2}$ has a weak V_{GS} dependence. In addition, both $\overline{i_d^2}$ and $\overline{i_g^2}$ have a weak V_{DS} dependence for devices in which channel length modulation by the drain bias is weak. The extracted channel noise, induced gate noise and their correlation can be used as a direct target for the verification of the physics-based noise models of sub-micron MOSFETs.

The channel length modulation (CLM) effect begins to impact the channel noise for the devices with channel length shorter than 0.5 μm. For deep sub-micron MOSFETs, if the CLM effect is not included, the calculated spectral density of the channel noise will be much lower than the experimental results. On the other hand, the noise contributions from the velocity saturation region and from the hot electron effect seems to be negligible in the channel noise modeling of deep sub-micron MOSFETs down to 0.18 μm. Different noise models published in the literature are reviewed from both theoretical and experimental point of view. In this thesis, it is shown that the impact of the velocity saturation effect in the gradual channel region on the channel noise modeling is not as pronounced as that on the modeling of DC current, and it can be considered as a secondary effect compared to the CLM effect in the channel noise modeling of short-channel devices. If a noise model only takes care of the impact of the velocity saturation effect on the

conductance reduction but not on the enhancement of the local resistance, it will predict a lower noise spectral density and can compensate this discrepancy by introducing the hot electron effect. The noise model including the CLM effect can achieve a good noise prediction without including the hot electron effect, and it is believed that the enhancement of the local output conductance by the CLM effect is the main physical cause of the noise enhancement in short-channel MOSFETs. In addition, the model with the velocity saturation effect predicts lower $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ because of the neglect in the local resistance enhancement. On the other hand, including the hot electron effect can reasonably solve the discrepancy in $\overline{i_g^2}$, but degrade the prediction of $\overline{i_g i_d^*}$.

Based on the measured noise parameters and extracted noise sources, some design strategies for the low noise circuits were discussed. First, the lowest NF_{min} happens before the peak g_m instead of at the peak g_m. This is because the derivative of g_m with respect to V_{GS} is zero at the peak g_m. Therefore, the transistor should be biased right before the peak g_m for the best noise performance. Second, for the V_{DS} bias, it is shown that at higher V_{DS}, the increase of g_m at high V_{GS} region causes NF_{min} and R_n drop at high V_{GS} region. Therefore, higher V_{DS} bias will cause the noise performance of the transistor to be less sensitive to the V_{GS} variation, but then the power consumption will be higher. Third, multi-finger designs with the signal sent into both gate ends will improve the noise performance of the transistors by reducing the effective gate resistance R_G. For the impact of accuracy of the noise models on the circuit design, it is shown that using the effective channel length L_{eff} to calculate the channel noise, the noise figure NF is underestimated about 0.3 dB and the optimized frequency is underestimated about 0.1 GHz for the chosen amplifier design.

Neglect of the induced gate noise and its correlation with the channel noise results in an error about 0.1 dB in *NF*. The optimized frequency for the chosen amplifier design is overestimated about 0.1 GHz.

8.2 RECOMMENDATIONS

Based on the results obtained and experience gained during the course of the research, the following recommendations for future research can be made. First, there is a tremendous push to operate reduced channel length FETs at lower voltages for lower power circuit applications. In some cases, the transistors operate in moderate or even weak inversion. Therefore, a natural extension of this work is to study how to model the DC, AC and noise behaviour of MOSFETs in moderate and weak inversion regions. This presents a lot of challenges since the transistor changes its conduction mode from drift to drift and diffusion in moderate inversion and predominantly diffusion in weak inversion.

Second, for devices with sufficiently small dimensions, quantum effects will begin to play a role. How to include this effect in device models will become a serious research issue.

Third, MOSFET technology continues to dominate the electronics industry. However, for practical uses, these devices must be characterized over the commercial or industrial temperature range of -65 to 85°C. Therefore, extending the research results by considering temperature effects is another extension of this work.

Fourth, in this work, an indirect discussion of dimensional scaling issues was initiated. An important extension of this work is to discuss rigorously scaling issues of the

noise parameters or noise sources. In this way, predictive capabilities can be developed before devices are actually fabricated so that the cost-benefit analysis can be properly performed.

Lastly, several of the techniques and algorithms presented in this thesis are general and can be applied to other transistors, such as BJTs or HEMTs. It would be relatively easy to extend the noise modeling and extraction techniques discussed in the thesis to other two or three-terminal active devices. In this way, accurate and predictive capabilities can be developed for other active devices similar to what was achieved in this research.

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Appendix A

DC CURRENT MODEL OF MOSFETS

This appendix lists the models for the DC current, threshold voltage, carrier mobility and the inversion charge of a MOSFET channel used in this thesis.

- **DC current of MOSFETs**

In general, the drain current of a MOSFET at any section in the gradual channel region biased in strong inversion is given by

$$I_{DS} = g(V)\frac{dV}{dx} \tag{A.1}$$

where

$$g(V) = W_{eff}\mu_{eff}C_{ox}(V_{GS} - V_{TH} - V), \tag{A.2}$$

W_{eff} is the effective channel length, μ_{eff} is the effective mobility, C_{ox} is the gate-oxide capacitance per unit area, V_{TH} is the threshold voltage, and V is the potential in the channel.

- **Threshold and mobility models**

The threshold and mobility models used are [67]

$$V_{TH} = V_{THO} - K_1 \cdot (\sqrt{\Phi_s} - \sqrt{\Phi_s - V_{bs}}) - K_2 \cdot V_{bs} + K_1 \cdot \left(\sqrt{1 + \frac{Nlx}{L_{eff}}} - 1\right)\sqrt{\Phi_s} \tag{A.3}$$

and

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bs})\left(\frac{V_{gs} + 2V_{th}}{T_{ox}}\right) + U_b\left(\frac{V_{gs} + 2V_{th}}{T_{ox}}\right)^2} \quad (A.4)$$

where T_{ox} is the oxide thickness, V_{TH} the threshold voltage, K_1, K_2, Nlx, μ_o, U_a, U_b and U_c are the fitting parameters, and Φ_s is given by

$$\Phi_s = 2 \cdot \frac{kT}{q} \ln\left(\frac{N_{SD}}{n_i}\right). \quad (A.5)$$

- **Inversion charge models**

There are three inversion charge models proposed in BSIM4 [67] and EKV [90] compact models, and by Tsividis [66] referenced in this thesis.

For BSIM4 model [67], Q_{inv} is

$$Q_{inv} = -W_{eff} L_{eff} C_{ox} \cdot NF \cdot \left(V_{gteff} - \frac{A_b V_{dseff}}{2} + \frac{A_b^2 V_{dseff}^2}{12 \cdot \left(V_{gteff} - \frac{A_b V_{dseff}}{2} \right)} \right). \quad (A.6)$$

For Tsividis's simplified model [66], Q_{inv} is

$$Q_{inv} = -W_{eff} L_{eff} C_{ox} \cdot (V_{GS} - V_T) \cdot \frac{2}{3} \cdot \frac{1 + \eta + \eta^2}{1 + \eta} \quad (A.7)$$

where η and V_{DS}' are given by

$$\eta = \begin{cases} 1 - \frac{V_{DS}}{V_{DSsat}}, & V_{DS} \le V_{DSsat} \\ 0, & V_{DS} > V_{DSsat} \end{cases} \quad (A.8)$$

and

$$V_{DSsat} = \frac{V_{GS} - V_T}{A_b}. \tag{A.9}$$

For EKV model [90], Q_{inv} is calculated from

$$Q_{inv} = -nU_T C_{ox} \cdot \left(\frac{4}{3}\frac{x_f^2 + x_f x_r + x_r^2}{x_f + x_r} - 1\right) \tag{A.10}$$

where U_T is the thermal voltage which is kT/q and the parameters n, x_f and x_r are defined in [90].

$$\Delta L = \frac{1}{\alpha}\ln\left(\frac{\alpha(V_{ds} - V_{dssat}) + E_D}{E_{crit}}\right) \tag{A.11}$$

where

$$E_D = E_{crit}\sqrt{1 + \left(\frac{\alpha((V_{ds} - V_{dssat}))}{E_{crit}}\right)^2}, \tag{A.12}$$

$$\alpha = \lambda\sqrt{\frac{3}{2}\frac{C_{ox}}{x_j \varepsilon_{si} \varepsilon_o}}, \tag{A.13}$$

x_j is the junction depth of the source and drain region, C_{ox} is the gate-oxide capacitance, and λ is a fitting parameter to adjust the channel length modulation.

Appendix B

DISCUSSION OF NOISE CALCULATION

In this section, the general approach for the calculation of channel noise in MOSFETs is derived.

- **Equivalent noise current of a partitioned resistance**

From thermal noise theory, if we examine the term $\sqrt{4kTR\Delta f}$ associated with a resistance R, it has the unit of "volt". Therefore, for two resisters connected in series, it is so easy to make the mistake by using the superposition principle to add the noise voltage from each resistor as the total noise voltage ($2\sqrt{4kTR\Delta f}$) which is not the expected value $\sqrt{4kT(2R)\Delta f}$. This is because the value $\sqrt{4kTR\Delta f}$ is the R.M.S. value of the associated noise voltage. The question is what is the right way to calculate the total noise current from several resistors connected in series? This is a fundamental skill in the noise modeling of channel noise. Assuming that there are two resistors connected in series with their noise voltage sources as shown in fig. B.1, and imagining that there is a load resistance R_L connected at the output port, the square of the output voltage can be obtained through the average power $\overline{P_L}$ by

$$\overline{v_{out}^2} = \overline{P_L} \cdot R_L = \sum_{i=1}^{n} \frac{\left(\sqrt{4kTR\Delta f} \cdot \frac{R_L}{n \cdot R + R_L}\right)^2}{R_L} \cdot R_L . \tag{B.1}$$

If $R_L = \infty$, it will become

$$\overline{v_{out}^2} = 4kT(nR)\Delta f \tag{B.2}$$

In addition, the short-circuited noise current at the output port is given by

$$\overline{i_{out}^2} = \frac{\overline{P_L}}{R_L} = \sum_{i=1}^{n} \frac{\left(\sqrt{4kTR\Delta f} \cdot \frac{R_L}{n \cdot R + R_L}\right)^2}{R_L} \cdot \frac{1}{R_L} = \sum_{i=1}^{n} \frac{(\sqrt{4kTR\Delta f})^2}{(n \cdot R + R_L)^2} \tag{B.3}$$

If $R_L = 0$, it becomes

$$\overline{i_{out}^2} = \left(\sqrt{\frac{4kT\Delta f}{nR}}\right)^2. \tag{B.4}$$

One important observation from (B.3) is that the square of total short-circuited noise current at the output port is the summation of the square of the noise current at the output port from each individual noise source.

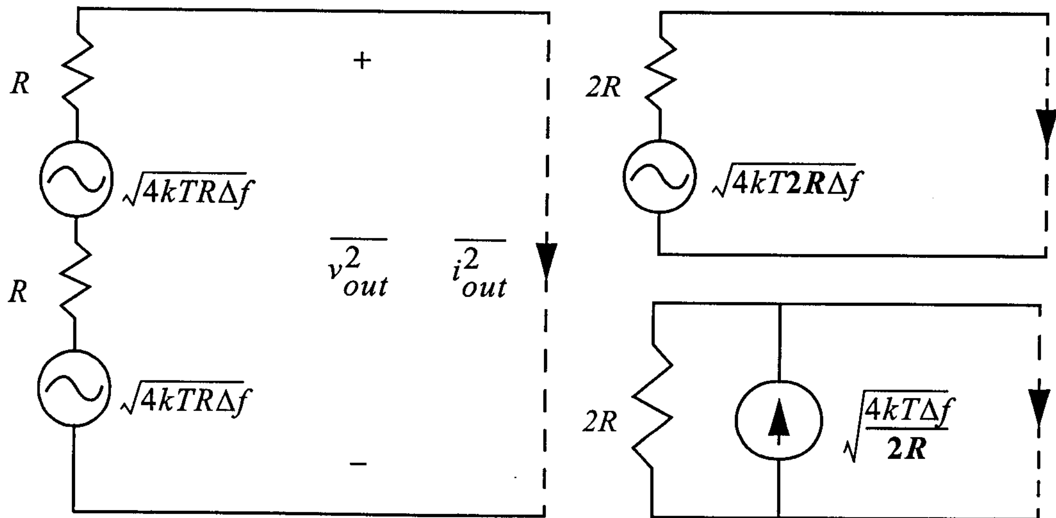

Fig. B.1: Equivalent circuit of two resistors with noise voltage source connected in series.

Appendix C

DERIVATION OF CHANNEL THERMAL NOISE

As shown in Appendix A, the drain current I_D at the position x_o in the channel of a MOSFET working in the linear region can be written as

$$I_D = -W\mu(x_o)Q(x_o)E(x_o) \tag{C.1}$$

or

$$I_D = -W\mu(x_o)Q(x_o)\frac{dV}{dx} \tag{C.2}$$

where V is the voltage along the x direction. Now we rearrange (C.1) and (C.2) to have

$$E(x_o) = \frac{I_D}{-W\mu(x_o)Q(x_o)} \tag{C.3}$$

and

$$\frac{1}{-W\mu(x_o)Q(x_o)}dx = \frac{dV}{I_D} \tag{C.4}$$

where V_o is the local voltage at the position x_o. From (6.9), we can obtain the following

$$S_{i_d^2} = \frac{4kT_o\Delta f}{L_{eff}^2}\int_0^{L_{eff}} W\mu_{eff}(-Q(x_o))dx + \delta\frac{4kT_o\Delta f}{L_{eff}^2 E_{crit}^2}\int_0^{L_{eff}} E(x_o)^2 W\mu_{eff}(-Q(x_o))dx\,. \tag{C.5}$$

The first term in (6.11) can be directly obtained from the first term in (C.5) where

$$Q_{inv} = \int_0^{L_{eff}} WQ(x_o)dx \tag{C.6}$$

and its analytical expression will be different for different DC models. For the second term in (C.5), if we replace $E(x_o)$ by (C.3) and use (C.4), the second integration term on the right of (C.5) will become

$$\begin{aligned}\int_0^{L_{eff}} E(x_o)^2 W\mu_{eff}(-Q(x_o))dx &= \int_0^{L_{eff}} \left(\frac{I_D}{-W\mu(x_o)Q(x_o)}\right)^2 \cdot W\mu(x_o)(-Q(x_o))dx \\ &= \int_0^{V_{DS}} I_D^2 \cdot \frac{dV}{I_D} \\ &= I_D V_{DS}\end{aligned} \tag{C.7}$$

where V_{DS} will be V_{DSsat} if the device works in the saturation region. From (C.6) and (C.7), we can obtain (6.11).

Appendix D

DERIVATION OF INDUCED GATE NOISE

If a noise voltage source Δv_{xo} is generated within the section between x_o and (x_o + Δx) in the channel as shown in fig. D.1, then the local voltage $v(x)$ and current i_{DS} which is continuous and independent of position x anywhere along the channel in the gradual channel region will become

$$v(x_o) = V(x_o) + \Delta v(x_o) \quad \text{(D.1)}$$

and

$$i_{DS} = I_{DS} + \Delta i_d \quad \text{(D.2)}$$

where $\Delta v(x_o)$ is the voltage fluctuation at the position x_o and Δi_d is the current fluctuation caused by the Δv_{xo} generated at x_o. Note that $\Delta v(x_o)$ is the voltage difference at the position x_o before and after the noise voltage source Δv_{xo} is generated within the section between x_o and (x_o + Δx), and therefore, $\Delta v(x_o)$ is different from Δv_{xo}. According to [31], the function $\Delta v(x)$ follows the following conditions:

1. $\Delta v(x) = 0$ at $x = 0$, and $x = L_{eff}$ (or L_{elec} when the device is in saturation) since the channel potential at source (ground) and the channel potential V_{DS} (or V_{DSsat}) at drain (or L_{elec}) are fixed. L_{elec} fluctuation caused by channel noise is negligible.
2. $\Delta v(x_o + \Delta x)$ - $\Delta v(x_o) = \Delta v_{xo}$, i.e. after the noise voltage Δv_{xo} generated between x_o and (x_o + Δx), if $\Delta v(x_o)$ is the voltage fluctuation at x_o, then the voltage fluctuation $\Delta v(x_o$ +

Δx) at ($x_o + \Delta x$) is Δv_{xo} higher than that at x_o. This condition causes the drain current to be smaller, i.e. Δi_d in equation (D.2) is negative if we define Δi_d as flowing from source to drain. This is because of the smaller local electrical field in the channel section from $x_o = x_o + \Delta x$ to $x_o = L_{eff}$ (or L_{elec}) as shown in fig. 8.35 in [66].

One thing which has to be addressed here is that the noise voltage Δv_{xo} generated between x_o and ($x_o + \Delta x$) will cause the voltage fluctuation along the gate from $x = 0$ to $x = L_{eff}$ (or L_{elec}) as shown in fig. D.1. Therefore the total noise current coupled to the gate from the channel section Δx with the noise voltage source Δv_{xo} generated between x_o and ($x_o + \Delta x$) will be the integration of the gate noise current from $x = 0$ to $x = L_{eff}$ (or L_{elec}).

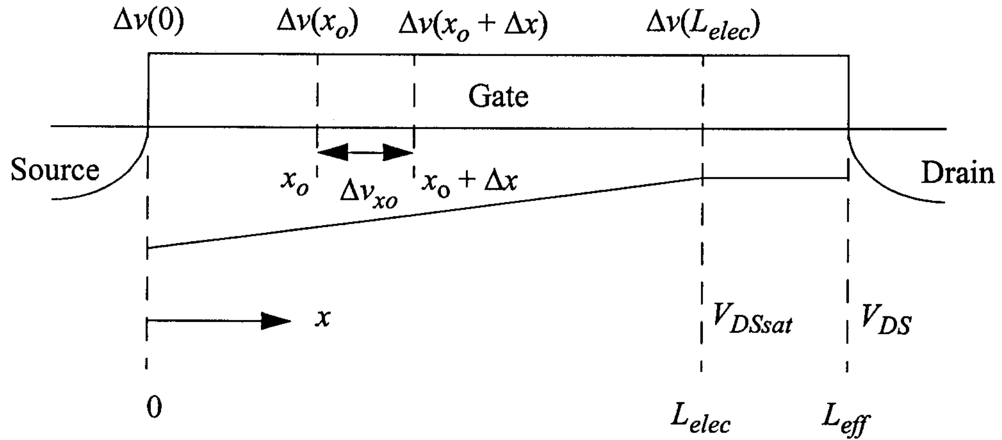

Fig. D.1: Cross-section of a MOSFET channel.

To derive the induced gate noise from one section in the gradual channel region, let's start from the DC current of a MOSFET. In general, the drain current of a MOSFET at any section in the gradual channel region under strong inversion is given by

$$I_{DS} = g(V)\frac{dV}{dx} \tag{D.3}$$

where

$$g(V) = W_{eff}\mu_{eff}C_{ox}(V_{GS} - V_{TH} - V), \tag{D.4}$$

and V is the potential in the channel. If a noise voltage source Δv_{xo} is generated within the section between x_o and $(x_o + \Delta x)$, according to (D.1) to (D.4), and the second feature of the $\Delta v(x)$ function, the drain current with the current fluctuation becomes

$$\begin{aligned} I_{DS} - \Delta i_d &= g(V+\Delta v)\frac{d(V+\Delta v)}{dx} \\ &= \left(g(V) + \frac{1}{1!}\cdot\frac{dg(V)}{dV}\Delta v + \frac{1}{2!}\cdot\frac{d^2g(V)}{dV^2}(\Delta v)^2 + \ldots\right)\cdot\frac{d(V+\Delta v)}{dx}. \end{aligned} \tag{D.5}$$

If we neglect the second order and the higher terms in the expansion, then (D.5) can be simplified to

$$\begin{aligned} I_{DS} - \Delta i_d &= \left(g(V) + \frac{dg(V)}{dV}\Delta v\right)\cdot\frac{d(V+\Delta v)}{dx} \\ &= g(V)\frac{dV}{dx} + g(V)\frac{d\Delta v}{dx} + \frac{dg(V)}{dV}\Delta v\frac{dV}{dx} + \frac{dg(V)}{dV}\Delta v\frac{d\Delta v}{dx}. \end{aligned} \tag{D.6}$$

If we neglect the last term in (D.6), and apply the chain rule to the third term, then (D.6) will become

$$I_{DS} - \Delta i_d = g(V)\frac{dV}{dx} + \frac{d}{dx}(g(V)\Delta v). \tag{D.7}$$

Therefore, the equation governing Δv is given by the solution of

$$\frac{d}{dx}(g(V)\Delta v) = -\Delta i_d \tag{D.8}$$

where Δi_d flows from source to drain. The solution of this differential equation [31] is

$$g(V)\Delta v(x) = -\Delta i_d \cdot x \qquad for \qquad 0 < x < x_o \tag{D.9}$$

which satisfies the condition $\Delta v(x) = 0$ at $x = 0$, and

$$g(V)\Delta v(x) = -\Delta i_d \cdot (x - L_{elec}) \qquad for \qquad x_o + \Delta x_o < x < L_{elec} \tag{D.10}$$

which satisfies the condition $\Delta v(x) = 0$ at $x = L_{elec}$. According to the second feature of the $\Delta v(x)$ function, i.e. $\Delta v(x_o + \Delta x) - \Delta v(x_o) = \Delta v_{xo}$, and (D.9) and (D.10), the channel noise current Δi_d is given by

$$\Delta i_d = \frac{g(V_o)}{L_{elec}} \Delta v_{xo} \tag{D.11}$$

where V_o is the DC potential at x_o. Equation (D.11) agrees with the result derived in [66], and it is only valid in the gradual channel region.

Next we will evaluate the induced noise current at the gate from this section Δx between x_o and $(x_o + \Delta x)$ in the channel. By capacitive coupling to the gate, $\Delta v(x_o)$ will produce a gate noise current along the gate from $x = 0$ to $x = L_{elec}$. The total gate noise current Δi_g flowing out of the gate, as discussed before, is found by integrating along the channel, and it is

$$\Delta i_g = j\omega W_{eff} \cdot \int_0^{L_{elec}} C_{ox} \Delta v(x) dx . \tag{D.12}$$

Based on (D.9), (D.10) and (D.12), Δi_g is given by

$$\begin{aligned} \Delta i_g &= j\omega W_{eff} C_{ox} \Delta i_d \cdot \left[-\int_0^{x_o} \frac{x}{g(V)} dx - \int_{x_o + \Delta x}^{L_{elec}} \frac{x}{g(V)} dx + \int_{x_o + \Delta x}^{L_{elec}} \frac{L_{elec}}{g(V)} dx \right] \\ &\approx j\omega W_{eff} C_{ox} \Delta i_d \cdot \left[-\int_0^{L_{elec}} \frac{x}{g(V)} dx + \int_{x_o}^{L_{elec}} \frac{L_{elec}}{g(V)} dx \right]. \end{aligned} \tag{D.13}$$

Because $dx = g(V)dV/I_{DS}$,

$$x = \int_0^V \frac{g(u)}{I_{DS}}du = \frac{\mu_{eff}W_{eff}C_{ox}\left[(V_{GS}-V_{TH})V-\frac{1}{2}V^2\right]}{I_{DS}}, \tag{D.14}$$

$$\begin{aligned}\int_0^{L_{elec}} \frac{x}{g(V)}dx &= \int_0^{V_{DSsat}} \frac{x}{g(V)}\cdot\frac{g(V)}{I_{DS}}dV \\ &= \frac{\mu_{eff}W_{eff}C_{ox}}{I_{DS}^2}\left[\frac{(V_{GS}-V_{TH})V_{DSsat}^2}{2}-\frac{V_{DSsat}^3}{6}\right],\end{aligned} \tag{D.15}$$

and

$$\int_{x_o+\Delta x}^{L_{elec}} \frac{L_{elec}}{g(V)}dx = \int_{V_o}^{V_{DSsat}} \frac{L_{elec}}{g(V)}\cdot\frac{g(V)}{I_{DS}}dV = \frac{L_{elec}}{I_{DS}}(V_{DSsat}-V_o). \tag{D.16}$$

Substituting (D.11), (D.15) and (D.16) into (D.13), then the induced gate noise Δi_g becomes

$$\Delta i_g = \frac{j\omega W_{eff}C_{ox}}{I_{DS}}\cdot g(V_o)\Delta v_{xo}[V_{as}-V(x_o)] \tag{D.17}$$

where

$$V_{as} = V_{DSsat}-\frac{\frac{1}{2}(V_{GS}-V_{TH})V_{DSsat}-\frac{1}{6}V_{DSsat}^2}{V_{GS}-V_{TH}-\frac{1}{2}V_{DSsat}}. \tag{D.18}$$

Appendix E

MATLAB PROGRAM FOR PARAMETER DE-EMBEDDING

- **Parallel-Series Configuration**

```
%########################################################################################
%#
%# Function Name: noise_deembed_ps.m
%#
%# Purpose: This function de-embeds the parasitic effects of probe-pads from measured scattering and
%#          noise parameters.
%#
%# Author: Chih-Hung Chen
%#
%# Date: July 7, 2000
%#
%# Syntax:
%#  []=noise_deembed_ps(fn_dut, fn_open, fn_short, temperC, Rcon1, Rcon2, Zo)
%#
%# Intput:
%#  fn_dut    - file name of measured DUT data from ATN NP5
%#  fn_open   - file name of measured s-parameters of OPEN dummy pads
%#  fn_short  - file name of measured s-parameters of SHORT dummy pads or "N" if not used
%#  temperC   - temperature in Celsius
%#  Rcon1     - contact resistance at the input port (or port 1) (in Ohm)
%#  Rcon2     - contact resistance at the output port (or port 2) (in Ohm)
%#  Zo        - system characteristic impedance (optional)
%#
%# Output:
%#  De-embedded s-parameter and noise parameter files with file extensions .noise_intr and .sparm_intr.
%#
%# Note:
%#  1. fn_short is optional. If 'N' specified, only fn_open will be used.
%#  2. Zo is optional. If not specified, Zo=50.
%#
%########################################################################################
function []=noise_deembed_ps(varargin)
```

```
%##########
%# Constants
%##########
k_boltz = 1.38066E-23;

%#############
%# Control Flags
%#############
express_RI = 0;    % output format - real and imaginary for GAMMA only

%#################
%# Read in file names
%#################
Zo = 50;
use_of_short = 1;

nargin =length(varargin);

if(nargin < 6 | nargin > 7)
 eval('help noise_deembed_ps');
 return;
end

fname_dut   = varargin{1};
fname_open = varargin{2};
fname_short = varargin{3};
temperC     = varargin{4};
Rcon1       = varargin{5};
Rcon2      = varargin{6};

if(nargin == 7)
 Zo=varargin{7};
end

if(strcmpi(fname_short,'n')),
 use_of_short = 0;
end

%##################
% Absolute Temperautre
%##################
Temp = 273.15 + temperC;

%##################
% Obtain Bias Condition
%##################
[vd,id,vg,ig] = seekbias(fname_dut,'A');

%##################
%# Converting data format
```

```
%####################
convert_dut(fname_dut);
convert_dummy(fname_dut,fname_open);
if(use_of_short == 1)
  convert_dummy(fname_dut,fname_short);
end

%#####################################
%# Read in the noise parameters of DUT,
%# s-parameters of DUT, OPEN and SHORT
%#####################################

%# Prepare input file names
fsdut = [strtok(fname_dut,'.'),'.sparm_extr'];
fndut = [strtok(fname_dut,'.'),'.noise_extr'];
fsopen = [strtok(fname_open,'.'),'.sparm'];
if(use_of_short == 1)
  fsshort = [strtok(fname_short,'.'),'.sparm'];
end

%# Read parameters into buffers
buffer_sdut = seekdata(fsdut,1);
buffer_ndut = seekdata(fndut,1);
buffer_open = seekdata(fsopen,1);
if(use_of_short == 1)
  buffer_short = seekdata(fsshort,1);
end

%# Convert data from ASCII to numbers for all frequencies
[data,nsdut] = sscanf(buffer_sdut,'%f',[9 inf]);
data = data';
freq_sdut = data(:,1);                  %# frequencies
data_dut(:,1) = data(:,2)+i*data(:,3);  %# S11
data_dut(:,2) = data(:,4)+i*data(:,5);  %# S12
data_dut(:,3) = data(:,6)+i*data(:,7);  %# S21
data_dut(:,4) = data(:,8)+i*data(:,9);  %# S22

[data,nndut] = sscanf(buffer_ndut,'%f',[5 inf]);
data = data';
freq_ndut = data(:,1);
NFmin = 10.^(data(:,2)/10);
GAMMA_opt = data(:,3).*cos(data(:,4)/180*pi)+i*data(:,3).*sin(data(:,4)/180*pi);
Rn = data(:,5)*Zo;
Yopt = (1-GAMMA_opt)./(1+GAMMA_opt)/Zo;

[data,nopen] = sscanf(buffer_open,'%f',[9 inf]);
data = data';
freq_open = data(:,1);
data_open(:,1) = data(:,2)+i*data(:,3);
data_open(:,2) = data(:,4)+i*data(:,5);
data_open(:,3) = data(:,6)+i*data(:,7);
```

```
data_open(:,4) = data(:,8)+i*data(:,9);

if(use_of_short == 1)
 [data,nshort] = sscanf(buffer_short,'%f',[9 inf]);
 data = data';
 freq_short = data(:,1);
 data_short(:,1) = data(:,2)+i*data(:,3);
 data_short(:,2) = data(:,4)+i*data(:,5);
 data_short(:,3) = data(:,6)+i*data(:,7);
 data_short(:,4) = data(:,8)+i*data(:,9);
end

%##################################################
%# Noise parameter de-embedding - based on the frequency
%# points of available noise parameters
%# S-parameters of DUT: data_dut
%# Noise parameters of DUT: NFmin, Rn, and Yopt
%# S-parameters of OPEN pads: data_open
%# S-parameters of SHORT pads: data_short (if there exists)
%##################################################

%# Noise parameter de-embedding
for k = 1 : size(freq_ndut)

 if (Rcon1 ~= 0 | Rcon2 ~= 0)

  %##################
  %# Rcon de-embedding
  %##################

  %# 1.1: Convert s-parameters of DUT, OPEN and SHORT to their
  %# corresponding y-parameters for all frequencies
  S21Limit = 0;          % lower limit of s21 of measured OPEN to perform the s2a transformation
  S21OPEN = data_open(k,3);

  %# 1.2: Calculate the ABCD parameters [A_RCON] of the contact resistors Rcon1 and Rcon2
  A_RCON1 = [1, Rcon1; 0, 1];
  A_RCON2 = [1, Rcon2; 0, 1];

  %# 1.4: Convert the s-parameters of DUT, OPEN and SHORT to their ABCD parameters,
  %# performing Rcon de-embedding and convert them to their Y parameters
              [A_DUT_MEA(1,1),A_DUT_MEA(1,2),A_DUT_MEA(2,1),A_DUT_MEA(2,2)]              =
   s2a(data_dut(k,1),data_dut(k,2),data_dut(k,3),data_dut(k,4),Zo);
  A_DUT = inv(A_RCON1)*A_DUT_MEA*inv(A_RCON2);
                      [Y_DUT(1,1),Y_DUT(1,2),Y_DUT(2,1),Y_DUT(2,2)]                      =
   a2y(A_DUT(1,1),A_DUT(1,2),A_DUT(2,1),A_DUT(2,2),Zo);

  if(S21OPEN > S21Limit)
   [A_OPEN_MEA(1,1),A_OPEN_MEA(1,2),A_OPEN_MEA(2,1),A_OPEN_MEA(2,2)] = ...
    s2a(data_open(k,1),data_open(k,2),data_open(k,3),data_open(k,4),Zo);
   A_OPEN = inv(A_RCON1)*A_OPEN_MEA*inv(A_RCON2);
```

```
                [Y_OPEN(1,1),Y_OPEN(1,2),Y_OPEN(2,1),Y_OPEN(2,2)] =
  a2y(A_OPEN(1,1),A_OPEN(1,2),A_OPEN(2,1),A_OPEN(2,2),Zo);
else
                [Y_OPEN(1,1),Y_OPEN(1,2),Y_OPEN(2,1),Y_OPEN(2,2)] =
  s2y(data_open(k,1),data_open(k,2),data_open(k,3),data_open(k,4),Zo);
end

if (use_of_short == 1)
 [A_SHORT_MEA(1,1),A_SHORT_MEA(1,2),A_SHORT_MEA(2,1),A_SHORT_MEA(2,2)] = ...
  s2a(data_short(k,1),data_short(k,2),data_short(k,3),data_short(k,4),Zo);
 A_SHORT = inv(A_RCON1)*A_SHORT_MEA*inv(A_RCON2);
                [Y_SHORT(1,1),Y_SHORT(1,2),Y_SHORT(2,1),Y_SHORT(2,2)] =
  a2y(A_SHORT(1,1),A_SHORT(1,2),A_SHORT(2,1),A_SHORT(2,2),Zo);
end

%# 2. Noise parameters obtained from measurements

%# 3. Calculate the correlation matrix [CA] of the DUT at one frequency
CA_DUT_MEA(1,1) = Rn(k);
CA_DUT_MEA(1,2) = (NFmin(k)-1)/2 - Rn(k)*conj(Yopt(k));
CA_DUT_MEA(2,1) = (NFmin(k)-1)/2 - Rn(k)*Yopt(k);
CA_DUT_MEA(2,2) = Rn(k)*abs(Yopt(k))^2;
CA_DUT_MEA = 2*k_boltz*Temp*CA_DUT_MEA;    %# [CA_DUT] is 4x4 for one frequency

%# 1.5: Convert [A_RCON] to its Y parameters [Y_RCON] (not [Z_RCON] because of the singularity
  problem)
                [Y_RCON1(1,1),Y_RCON1(1,2),Y_RCON1(2,1),Y_RCON1(2,2)] =
  a2y(A_RCON1(1,1),A_RCON1(1,2),A_RCON1(2,1),A_RCON1(2,2),Zo);
                [Y_RCON2(1,1),Y_RCON2(1,2),Y_RCON2(2,1),Y_RCON2(2,2)] =
  a2y(A_RCON2(1,1),A_RCON2(1,2),A_RCON2(2,1),A_RCON2(2,2),Zo);

%# 1.6: Calculate the correlation matrix CYs of at input and output ports at one frequency
CY_RCON1 = 2*k_boltz*Temp*real(Y_RCON1);   %# [CY_RCON1] is 4x4 at one frequency
CY_RCON2 = 2*k_boltz*Temp*real(Y_RCON2);   %# [CY_RCON2] is 4x4 at one frequency

%# 1.7: Convert [CY_RCON] to [CA_RCON]
T_RCON1 = [0, A_RCON1(1,2); 1, A_RCON1(2,2)];
CA_RCON1= T_RCON1*CY_RCON1*T_RCON1';       %# [CA_RCON1] is 4x4 at one frequency
T_RCON2 = [0, A_RCON2(1,2); 1, A_RCON2(2,2)];
CA_RCON2= T_RCON2*CY_RCON2*T_RCON2';       %# [CA_RCON2] is 4x4 at one frequency

%# 1.8: Calculate the correlation matrix [CA] with Rcon de-embedded
      CA_DUT = inv(A_RCON1)*(CA_DUT_MEA - CA_RCON1)*inv(A_RCON1') -
  A_DUT*CA_RCON2*A_DUT';

else

%# 1. Convert s-parameters of DUT, OPEN and SHORT to their
%# corresponding y-parameters for one frequency
                [Y_DUT(1,1),Y_DUT(1,2),Y_DUT(2,1),Y_DUT(2,2)] =
  s2y(data_dut(k,1),data_dut(k,2),data_dut(k,3),data_dut(k,4),Zo);
```

```
                                [Y_OPEN(1,1),Y_OPEN(1,2),Y_OPEN(2,1),Y_OPEN(2,2)]       =
  s2y(data_open(k,1),data_open(k,2),data_open(k,3),data_open(k,4),Zo);
 if(use_of_short == 1)
                              [Y_SHORT(1,1),Y_SHORT(1,2),Y_SHORT(2,1),Y_SHORT(2,2)]     =
  s2y(data_short(k,1),data_short(k,2),data_short(k,3),data_short(k,4),Zo);
 end

 %# 2. Noise parameters obtained from measurements

 %# 3. Calculate the correlation matrix [CA] of the DUT at one frequency
 CA_DUT(1,1) = Rn(k);
 CA_DUT(1,2) = (NFmin(k)-1)/2 - Rn(k)*conj(Yopt(k));
 CA_DUT(2,1) = (NFmin(k)-1)/2 - Rn(k)*Yopt(k);
 CA_DUT(2,2) = Rn(k)*abs(Yopt(k))^2;
 CA_DUT = 2*k_boltz*Temp*CA_DUT;      %# [CA_DUT] is 4x4 for one frequency

end

%# 4. Convert [CA_DUT] to [CY_DUT] at one frequency
T_DUT = [-Y_DUT(1,1), 1; -Y_DUT(2,1), 0];
CY_DUT = T_DUT*CA_DUT*T_DUT';   %# [CY_DUT] is 4x4 for one frequency

%# 5. Calculate the correlation matrix CYs of OPEN and SHORT at one frequency
CY_OPEN = real(Y_OPEN);
CY_OPEN = 2*k_boltz*Temp*CY_OPEN;     %# [CY_OPEN] is 4x4 for one frequency

if(use_of_short == 1)
 CY_SHORT = real(Y_SHORT);
 CY_SHORT = 2*k_boltz*Temp*CY_SHORT;  %# [CY_SHORT] is 4x4 for one frequency
end

%# 6. Substract parallel parasitics from [Y_DUT] and [Y_SHORT] at one frequency
Y_DUT_I = Y_DUT - Y_OPEN;
if(use_of_short == 1)
 Y_SHORT_I = Y_SHORT - Y_OPEN;
end

%# 7. De-embed the parallel parasitics from [CY_DUT] at one frequency
CY_DUT_I = CY_DUT - CY_OPEN;

if(use_of_short == 0)              %# Only OPEN dummy pads used

 %# 8. Convert the [Y_DUT_I] of an intrinsic transistor to its [A] matrix
 [A(1,1), A(1,2), A(2,1), A(2,2)] = y2a(Y_DUT_I(1,1), Y_DUT_I(1,2), Y_DUT_I(2,1), Y_DUT_I(2,2),
  Zo);

 %# 9. Convert [CY_DUT_I] of an intrinsic transistor to [CA]
 TA = [0, A(1,2); 1, A(2,2)];
 CA = TA*CY_DUT_I*TA';

 %# Convert the [Y_DUT_I] of an intrinsic transistor to its [S] matrix
```

```
    [S(1,1), S(1,2), S(2,1), S(2,2)] = y2s(Y_DUT_I(1,1), Y_DUT_I(1,2), Y_DUT_I(2,1), Y_DUT_I(2,2),
    Zo);

  else

    %# 8. Convert [Y_DUT_I] and [Y_SHORT_I] to [Z_DUT_I] and [Z_SHORT_I] at one frequency
    [Z_DUT_I(1,1), Z_DUT_I(1,2), Z_DUT_I(2,1), Z_DUT_I(2,2)] = y2z(Y_DUT_I(1,1), Y_DUT_I(1,2),
     Y_DUT_I(2,1), Y_DUT_I(2,2), Zo);
    [Z_SHORT_I(1,1), Z_SHORT_I(1,2), Z_SHORT_I(2,1), Z_SHORT_I(2,2)] = y2z(Y_SHORT_I(1,1),
     Y_SHORT_I(1,2), Y_SHORT_I(2,1), Y_SHORT_I(2,2), Zo);

    %# 9. Convert [CY_DUT_I] to [CZ_DUT_I]
    CZ_DUT_I = Z_DUT_I*CY_DUT_I*Z_DUT_I';

    %# 10. Calculate the correlation matrix [CZ_SHORT_I] of the SHORT dummy pads
    CZ_SHORT_I = 2*k_boltz*Temp*real(Z_SHORT_I);

    %# 11. Substract series parasitocs from [Z_DUT_I]
    Z = Z_DUT_I - Z_SHORT_I;

    %# 12. De-embed the serious parasitics from [CZ_DUT_I]
    CZ = CZ_DUT_I - CZ_SHORT_I;

    %# 13. Convert the [Z] of an intrinsic transistor to its [A] matrix
    [A(1,1), A(1,2), A(2,1), A(2,2)] = z2a(Z(1,1), Z(1,2), Z(2,1), Z(2,2), Zo);

    %# 14. Convert [CZ] of an intrinsic transistor to [CA]
    TA = [1, -A(1,1); 0, -A(2,1)];
    CA = TA*CZ*TA';

    %# Convert the [Z] of an intrinsic transistor to its [S] matrix
    [S(1,1), S(1,2), S(2,1), S(2,2)] = z2s(Z(1,1), Z(1,2), Z(2,1), Z(2,2), Zo);

  end

  %# 10./15. Calculate NFmin, Rn, and GAMMA_opt of an intrinsic transistor
  nfmin = 1 + (real(CA(1,2)) + sqrt(real(CA(1,1))*real(CA(2,2)) - imag(CA(1,2))^2))/(k_boltz*Temp);
  rn = real(CA(1,1))/(2*k_boltz*Temp);
  yopt = (sqrt(real(CA(1,1))*real(CA(2,2)) - imag(CA(1,2))^2) + i*imag(CA(1,2)))/real(CA(1,1));
  zopt = 1./yopt;
  gamma_opt = (zopt - Zo)./(zopt + Zo);

  %# Convert NFmin to dB and normalize Rn to Zo
  nfmin = 10*log10(nfmin);
  rn = rn/Zo;

  %# Collect de-embedded noise parameters to data_intr
  data_intr(k,1) = freq_ndut(k);
  data_intr(k,2) = nfmin;
  if(express_RI == 1)
   data_intr(k,3) = real(gamma_opt);
```

```
    data_intr(k,4) = imag(gamma_opt);
  else
    data_intr(k,3) = abs(gamma_opt);
    data_intr(k,4) = angle(gamma_opt)/pi*180;
  end
  data_intr(k,5) = rn;

end

%########################################
%# Output de-embedded noise parameters to file
%########################################
fnintr = [strtok(fname_dut,'.'),'.noise_intr'];

if (use_of_short == 0)
  fname_dummy = [' and ',fname_open];
else
  fname_dummy = [', ',fname_open,' and ',fname_short];
end

header1=['!De-embedded noise parameters from ',fname_dut,fname_dummy,' on ',date];
header2=['!VD = ',num2str(vd),' V  ID = ',num2str(id),...
      ' mA  VG = ',num2str(vg),' V  IG = ',num2str(ig),' uA'];
if(express_RI == 1)
    header3=['!FREQ(GHz)          ','NFMIN(dB)          ','GAMMA(REAL)        ','GAMMA(IMAG)
    ','Rn(NORMALIZED)   '];
else
    header3=['!FREQ(GHz)          ','NFMIN(dB)          ','GAMMA(MAG)         ','GAMMA(ANG)
    ','Rn(NORMALIZED)   '];
end

savedata(fnintr,'new',data_intr,header1,header2,header3);

return
```

- **Cascade Configuration**

```
%##########################################################################################
%#
%# Function Name: noise_deembed_ca.m
%#
%# Purpose: This function deembeds the parasitic effects of probe-pads from measured scattering and
%#            noise parameters based on cascade configuations.
%#
%# Author: Chih-Hung Chen
%#
%# Date: July 7, 2000
%#
%# Syntax:
```

```
%#  [] = noise_deembed_ca(fn_dut, fn_open, fn_thru1, fn_thru2, temperC, Rcon1, Rcon2, Zo)
%#
%# Intput:
%#  fn_dut   - file name of measured DUT data from ATN NP5
%#  fn_open  - file name of measured s-parameters of OPEN dummy pads
%#  fn_thru1 - file name of measured s-parameters of THRU1 dummy pads or "N" if not used.
%#  fn_thru2 - file name of measured s-parameters of THRU2 dummy pads or "N" if not used.
%#  temperC - temperature in Celsius
%#  Rcon1    - contact resistance at the input port (or port 1) (in Ohm)
%#  Rcon2    - contact resistance at the output port (or port 2) (in Ohm)
%#  Zo       - system characteristic impedance (optional)
%#
%# Output:
%#  Deembeded noise parameter files with fil extensions .noise_intr.
%#
%# Note:
%#  1. fn_thru1 and fn_thru2 are optional. If 'N' specified, only fn_open will be used.
%#  2. Zo is optional. If not specified, Zo=50.
%#
%##########################################################################################

function []=noise_deembed_ca(varargin)

%##########
%# Constants
%##########
k_boltz = 1.38066E-23;

%##############
%# Control Flags
%##############
express_RI = 0;   % output format - real and imaginary for GAMMA only

%##################
%# Read in file names
%##################
Zo = 50;
use_of_thru1 = 1;
use_of_thru2 = 1;

nargin =length(varargin);

if(nargin < 7 | nargin > 8)
 eval('help noise_deembed_ca');
 return;
end

fname_dut   = varargin{1};
fname_open  = varargin{2};
fname_thru1 = varargin{3};
fname_thru2 = varargin{4};
```

```
temperC     = varargin{5};
Rcon1       = varargin{6};
Rcon2       = varargin{7};

if(nargin == 8)
  Zo = varargin{8};
end

if(strcmpi(fname_thru1,'n')),
  use_of_thru1 = 0;
end
if(strcmpi(fname_thru2,'n')),
  use_of_thru2 = 0;
end

%###################
% Absolute Temperautre
%###################
Temp = 273.15 + temperC;

%###################
% Obtain Bias Condition
%###################
[vd,id,vg,ig] = seekbias(fname_dut,'A');

%##########################
%# Converting format of data file
%##########################
convert_dut(fname_dut);
convert_dummy(fname_dut,fname_open);
if(use_of_thru1 == 1)
  convert_dummy(fname_dut,fname_thru1);
end
if(use_of_thru2 == 1)
  convert_dummy(fname_dut,fname_thru2);
end

%####################################
%# Read in the noise parameters of DUT,
%# s-parameters of DUT, OPEN, THRU1 and
%# THRU2
%####################################
%# Prepare input file names
fsdut = [strtok(fname_dut,'.'),'.sparm_extr'];
fndut = [strtok(fname_dut,'.'),'.noise_extr'];
fsopen = [strtok(fname_open,'.'),'.sparm'];
if(use_of_thru1 == 1)
  fsthru1 = [strtok(fname_thru1,'.'),'.sparm'];
end
if(use_of_thru2 == 1)
  fsthru2 = [strtok(fname_thru2,'.'),'.sparm'];
```

```
end

%# Read parameters into buffers
buffer_sdut = seekdata(fsdut,1);
buffer_ndut = seekdata(fndut,1);
buffer_open = seekdata(fsopen,1);
if(use_of_thru1 == 1)
  buffer_thru1 = seekdata(fsthru1,1);
end
if(use_of_thru2 == 1)
  buffer_thru2 = seekdata(fsthru2,1);
end

%# Convert data from ASCII to numbers for all frequencies
[data,nsdut] = sscanf(buffer_sdut,'%f',[9 inf]);
data = data';
freq_sdut = data(:,1);                  %# frequencies
data_dut(:,1) = data(:,2)+i*data(:,3);  %# S11
data_dut(:,2) = data(:,4)+i*data(:,5);  %# S12
data_dut(:,3) = data(:,6)+i*data(:,7);  %# S21
data_dut(:,4) = data(:,8)+i*data(:,9);  %# S22

[data,nndut] = sscanf(buffer_ndut,'%f',[5 inf]);
data = data';
freq_ndut = data(:,1);
NFmin = 10.^(data(:,2)/10);
GAMMA_opt = data(:,3).*cos(data(:,4)/180*pi)+i*data(:,3).*sin(data(:,4)/180*pi);
Rn = data(:,5)*Zo;
Yopt = (1-GAMMA_opt)./(1+GAMMA_opt)/Zo;

[data,nopen] = sscanf(buffer_open,'%f',[9 inf]);
data = data';
freq_open = data(:,1);
data_open(:,1) = data(:,2)+i*data(:,3);
data_open(:,2) = data(:,4)+i*data(:,5);
data_open(:,3) = data(:,6)+i*data(:,7);
data_open(:,4) = data(:,8)+i*data(:,9);

if(use_of_thru1 == 1)
  [data,nthru1] = sscanf(buffer_thru1,'%f',[9 inf]);
  data = data';
  freq_thru1 = data(:,1);
  data_thru1(:,1) = data(:,2)+i*data(:,3);
  data_thru1(:,2) = data(:,4)+i*data(:,5);
  data_thru1(:,3) = data(:,6)+i*data(:,7);
  data_thru1(:,4) = data(:,8)+i*data(:,9);
end

if(use_of_thru2 == 1)
  [data,nthru2] = sscanf(buffer_thru2,'%f',[9 inf]);
  data = data';
```

```
 freq_thru2 = data(:,1);
 data_thru2(:,1) = data(:,2)+i*data(:,3);
 data_thru2(:,2) = data(:,4)+i*data(:,5);
 data_thru2(:,3) = data(:,6)+i*data(:,7);
 data_thru2(:,4) = data(:,8)+i*data(:,9);
end

%##################################################
%# Noise parameter de-embedding - based on the available
%# frequency points of noise parameters
%# S-parameters of DUT          : data_dut
%# Noise parameters of DUT      : NFmin, Rn, and Yopt
%# S-parameters of OPEN pads    : data_open
%# S-parameters of THRU1 pads   : data_thru1 (if there exists)
%# S-parameters of THRU2 pads   : data_thru2 (if there exists)
%##################################################

%# 1. S-parameters of DUT, OPEN, THRU1 and THRU2 are obtained
%# and stored in data_dut, data_open, data_thru1 and data_thru2

%# Noise Parasitics De-embedding
for k = 1 : size(freq_ndut)

 %# 2. Noise parameters obtained from measurements and
 %# stored in NFmin, Yopt and Rn. Calculate the correlation
 %# matrix [CA] of the DUT at one frequency
 CA_DUT(1,1) = Rn(k);
 CA_DUT(1,2) = (NFmin(k)-1)/2 - Rn(k)*conj(Yopt(k));
 CA_DUT(2,1) = (NFmin(k)-1)/2 - Rn(k)*Yopt(k);
 CA_DUT(2,2) = Rn(k)*abs(Yopt(k))^2;
 CA_DUT = 2*k_boltz*Temp*CA_DUT;      %# [CA_DUT] is 4x4 at one frequency

 %# Rcon de-embedding
 S21Limit = 0; % lower limit of s21 of measured OPEN to perform the s2a transformation
 S21OPEN = data_open(k,3);
 if (Rcon1 ~= 0 | Rcon2 ~= 0)
  %#2.2: Calculate the ABCD parameters [A_RCON] of the contact resistors Rcon1 and Rcon2
  A_RCON1 = [1, Rcon1; 0, 1];
  A_RCON2 = [1, Rcon2; 0, 1];

  %#2.4: Convert the s-parameters of OPEN, THRU1 and THRU2 to their ABCD parameters
  %# and performing Rcon de-embedding
  if(S21OPEN > S21Limit)
            [A_OPEN_MEA(1,1),A_OPEN_MEA(1,2),A_OPEN_MEA(2,1),A_OPEN_MEA(2,2)] =
   s2a(data_open(k,1),data_open(k,2),data_open(k,3),data_open(k,4),Zo);
   A_OPEN_I = inv(A_RCON1)*A_OPEN_MEA*inv(A_RCON2);
  end

  if (use_of_thru1 == 1)
         [A_THRU1_MEA(1,1),A_THRU1_MEA(1,2),A_THRU1_MEA(2,1),A_THRU1_MEA(2,2)] =
   s2a(data_thru1(k,1),data_thru1(k,2),data_thru1(k,3),data_thru1(k,4),Zo);
```

```
   A_THRU1_I = inv(A_RCON1)*A_THRU1_MEA*inv(A_RCON2);
  end

  if (use_of_thru2 == 1)
         [A_THRU2_MEA(1,1),A_THRU2_MEA(1,2),A_THRU2_MEA(2,1),A_THRU2_MEA(2,2)] =
   s2a(data_thru2(k,1),data_thru2(k,2),data_thru2(k,3),data_thru2(k,4),Zo);
   A_THRU2_I = inv(A_RCON1)*A_THRU2_MEA*inv(A_RCON2);
  end

end

%# 3. Convert the s-parameters of OPEN to its Y parameters [Y_OPEN]
if ( (Rcon1+Rcon2) == 0 | S21OPEN <= S21Limit)
                          [Y_OPEN(1,1),Y_OPEN(1,2),Y_OPEN(2,1),Y_OPEN(2,2)]        =
   s2y(data_open(k,1),data_open(k,2),data_open(k,3),data_open(k,4),Zo);
else
                          [Y_OPEN(1,1),Y_OPEN(1,2),Y_OPEN(2,1),Y_OPEN(2,2)]        =
   a2y(A_OPEN_I(1,1),A_OPEN_I(1,2),A_OPEN_I(2,1),A_OPEN_I(2,2),Zo);
end
YPAD1 = Y_OPEN(1,1) + Y_OPEN(1,2);
YPAD2 = Y_OPEN(2,2) + Y_OPEN(2,1);
%# calculate the ABCD parameters [A_PAD1] and [A_PAD2] of pads
A_PAD1 = [1, 0; YPAD1, 1];
A_PAD2 = [1, 0; YPAD2, 1];

%# 4. Convert [S_THRU1] and [S_THRU2] to [A_THRU1] and [A_THRU2] at one frequency
if (use_of_thru1 == 1)
 if ((Rcon1+Rcon2) == 0 | S21OPEN <= S21Limit)
                        [A_THRU1(1,1),A_THRU1(1,2),A_THRU1(2,1),A_THRU1(2,2)]      =
   s2a(data_thru1(k,1),data_thru1(k,2),data_thru1(k,3),data_thru1(k,4),Zo);
 else
   A_THRU1 = A_THRU1_I;
 end
end
if (use_of_thru2 == 1)
 if ((Rcon1+Rcon2) == 0 | S21OPEN <= S21Limit)
                        [A_THRU2(1,1),A_THRU2(1,2),A_THRU2(2,1),A_THRU2(2,2)]      =
   s2a(data_thru2(k,1),data_thru2(k,2),data_thru2(k,3),data_thru2(k,4),Zo);
 else
   A_THRU2 = A_THRU2_I;
 end
end

%# 5. Calculate the ABCD parameters [A_IN] and [A_OUT]
if (use_of_thru1 == 1)
 A_IN = A_THRU1 * inv(A_PAD2);
else
 A_IN = A_PAD1;
end
if (use_of_thru2 == 1)
 A_OUT = inv(A_PAD1) * A_THRU2;
```

```
else
  A_OUT = A_PAD2;
end

%# 5.5: Update A_IN and A_OUT if Rcon1 or Rcon2 is not zero
if (Rcon1 ~= 0 | Rcon2 ~= 0)
  A_IN  = A_RCON1*A_IN;
  A_OUT = A_OUT*A_RCON2;
end

%# 6. Convert [S_DUT] to its ABCD parameters [A_DUT]
                                    [A_DUT(1,1),A_DUT(1,2),A_DUT(2,1),A_DUT(2,2)]          =
    s2a(data_dut(k,1),data_dut(k,2),data_dut(k,3),data_dut(k,4),Zo);
%# calculate the ABCD parameters [A_TRANS] of the intrinsic device
A_TRANS = inv(A_IN) * A_DUT * inv(A_OUT);

%# 7. Convert [A_IN] and [A_OUT] to their Z parameters [Z_IN] and [Z_OUT]
[Z_IN(1,1),Z_IN(1,2),Z_IN(2,1),Z_IN(2,2)] = a2z(A_IN(1,1),A_IN(1,2),A_IN(2,1),A_IN(2,2),Zo);
                                    [Z_OUT(1,1),Z_OUT(1,2),Z_OUT(2,1),Z_OUT(2,2)]          =
    a2z(A_OUT(1,1),A_OUT(1,2),A_OUT(2,1),A_OUT(2,2),Zo);

%# 8. Calculate the correlation matrix CZs of at input and output ports at one frequency
CZ_IN  = 2*k_boltz*Temp*real(Z_IN);   %# [CZ_IN]  is 4x4 at one frequency
CZ_OUT = 2*k_boltz*Temp*real(Z_OUT);  %# [CZ_OUT] is 4x4 at one frequency

%# 9. Convert [CZ_IN] and [CZ_OUT] to [CA_IN] and [CA_OUT]
T_IN = [1, -A_IN(1,1); 0, -A_IN(2,1)];
T_OUT = [1, -A_OUT(1,1); 0, -A_OUT(2,1)];
CA_IN = T_IN*CZ_IN*T_IN';            %# [CA_IN]  is 4x4 at one frequency
CA_OUT = T_OUT*CZ_OUT*T_OUT';        %# [CA_OUT] is 4x4 at one frequency

%# 10. Calculate the correlation matrix [CA] of the intrinsic device
CA = inv(A_IN)*(CA_DUT - CA_IN)*inv(A_IN') - A_TRANS*CA_OUT*A_TRANS';

%# Convert the [A_TRANS] of the intrinsic device to its [S] matrix
[S(1,1),S(1,2),S(2,1),S(2,2)] = a2s(A_TRANS(1,1),A_TRANS(1,2),A_TRANS(2,1),A_TRANS(2,2), Zo);

%# 11. Calculate NFmin, Rn, and GAMMA_opt of an intrinsic transistor
nfmin = 1 + (real(CA(1,2)) + sqrt(real(CA(1,1))*real(CA(2,2)) - imag(CA(1,2))^2))/(k_boltz*Temp);
rn = real(CA(1,1))/(2*k_boltz*Temp);
yopt = (sqrt(real(CA(1,1))*real(CA(2,2)) - imag(CA(1,2))^2) + i*imag(CA(1,2)))/real(CA(1,1));
zopt = 1./yopt;
gamma_opt = (zopt - Zo)./(zopt + Zo);

%# Convert NFmin to dB and normalize Rn to Zo
nfmin = 10*log10(nfmin);
rn = rn/Zo;

%# Collect de-embedded noise parameters to data_intr
data_intr(k,1) = freq_ndut(k);
data_intr(k,2) = nfmin;
```

```
  if(express_RI == 1)
    data_intr(k,3) = real(gamma_opt);
    data_intr(k,4) = imag(gamma_opt);
  else
    data_intr(k,3) = abs(gamma_opt);
    data_intr(k,4) = angle(gamma_opt)/pi*180;
  end
  data_intr(k,5) = rn;

end

%########################################
%# Output de-embedded noise parameters to file
%########################################
fnintr = [strtok(fname_dut,'.'),'.noise_intr'];

if (use_of_thru1 == 1)
  fname_dummy = [', ',fname_open,' and ',fname_thru1];
end
if (use_of_thru2 == 1)
  fname_dummy = [', ',fname_open,' and ',fname_thru2];
end
if (use_of_thru1 == 1 & use_of_thru2 == 1)
  fname_dummy = [', ',fname_open,', ',fname_thru1,' and ',fname_thru2];
end
if (use_of_thru1 == 0 & use_of_thru2 == 0)
  fname_dummy = [' and ',fname_open];
end

header1=['!De-embedded noise parameters from ',fname_dut,fname_dummy,' on ',date];
header2=['!VD = ',num2str(vd),' V  ID = ',num2str(id),...
       ' mA  VG = ',num2str(vg),' V  IG = ',num2str(ig),' uA'];
if(express_RI == 1)
    header3=['!FREQ(GHz)        ','NFMIN(dB)          ','GAMMA(REAL)        ','GAMMA(IMAG)
    ','Rn(NORMALIZED)   '];
else
    header3=['!FREQ(GHz)        ','NFMIN(dB)          ','GAMMA(MAG)         ','GAMMA(ANG)
    ','Rn(NORMALIZED)   '];
end

savedata(fnintr,'new',data_intr,header1,header2,header3);

return
```

Appendix F

MATLAB PROGRAM FOR NOISE SOURCE EXTRACTION

```
%#####################################################################################
%#
%# Function name: JCmosNoiseExtr.m
%#
%# Purpose:  This function extracts the channel thermal noise id^2, induced gate noise ig^2 and
%#           their correlation igid* as a function of frequency.
%#
%# Author:   Chih-Hung Chen
%#
%# Date:  May 8, 2000
%#
%# Syntax:
%#   [ididDC,igig,igid,idid,Cigig,Cigid,Cidid] = JCmosNoiseExtr(fname,Param,freq,Pconst,Option)
%#
%# Intput:
%#   fname  - file name of the intrinsic noise parameters
%#   Param - element values of the RF transisotr model
%#   freq    - frequency interested (in GHz)
%#   Pconst - constant values => Pconst = [Temp; q; k_boltz; Zo; kt4 = 4*k_boltz*Temp]
%#   Option - 0: save the extracted noise data; 1: not save the extracted data
%#
%# Output:
%#     Extracted id^2, ig^2 and igid* vs. frequencies will be saved in "fname.nprn"
%#
%# Note: 1. ididDC is the extracted channel thermal noise assuming that id^2 is frequency
%#          independent and extracted based on the algorithm published in ICMTS2000 by C.H.Chen
%#
%#####################################################################################

function [ididDC,igig,igid,idid,Cigig,Cigid,Cidid] = JCmosNoiseExtr(fname,Param,Pconst,Option)

%#########
%# Constants
%#########
```

```
To     = 290;
Temp   = Pconst(1,1);
q      = 1.60218E-19;
k_boltz = 1.38066E-23;
Zo     = Pconst(2,1);
kt4    = 4*k_boltz*Temp;

%###############
% Model elements
%###############
gmdc = Param(1,1);
gmbdc= Param(2,1);
gmddc= Param(3,1);
Rg   = Param(4,1);
Rd   = Param(5,1);
Rs   = Param(6,1);
Rds  = Param(7,1);
Rdbi = Param(8,1);
Rsbi = Param(9,1);
Rdb  = Param(10,1);
Rsb  = Param(11,1);
Ri   = Param(12,1);
Rgd  = Param(13,1);
Cgs  = Param(14,1);
Cgd  = Param(15,1);
Cgb  = Param(16,1);
Cdb  = Param(17,1);
Csb  = Param(18,1);
tau  = Param(19,1);

%############
%# Initialization
%############
NFmin = [];
Rn = [];
Gamma = [];
Gamma_m = [];
Gamma_p = [];
Y = [];
igig = [];
igid = [];
idid = [];
igigcal = [];
igidcal = [];
ididDCcal = [];

%###################
% Prepare input file names
%###################
fsdev = [strtok(fname,'.'),'.sparm_intr'];
fndev = [strtok(fname,'.'),'.noise_intr'];
```

```
%###################
% Obtain Bias Condition
%###################
[vd,id,vg,ig] = seekbias(fsdev,'C');

%######################
% Read in noise parameters
%######################
%# Read parameters into buffers
buffer = seekdata(fndev,1);

%# Convert data from ASCII to numbers for all frequencies
[data,nndut] = sscanf(buffer,'%f',[5 inf]);
data = data';
freqn = data(:,1);
NFmin = 10.^(data(:,2)/10);
GAMMA_opt = data(:,3).*cos(data(:,4)/180*pi)+i*data(:,3).*sin(data(:,4)/180*pi);
Rn = data(:,5)*Zo;
Yopt = (1-GAMMA_opt)./(1+GAMMA_opt)/Zo;

%###################
% Read in s-parameters
%###################
%# Read parameters into buffers
buffer = seekdata(fsdev,1);

%# Convert data from ASCII to numbers for all frequencies
[data,ndut] = sscanf(buffer,'%f',[9 inf]);
data = data';

freqs = data(:,1);              %# frequencies
p11  = data(:,2)+i*data(:,3);   %# S11
p12  = data(:,4)+i*data(:,5);   %# S12
p21  = data(:,6)+i*data(:,7);   %# S21
p22  = data(:,8)+i*data(:,9);   %# S22

[p11, p12, p21, p22] = s2y(p11, p12, p21, p22,Zo);

ymeas(:,1) = p11;
ymeas(:,2) = p12;
ymeas(:,3) = p21;
ymeas(:,4) = p22;

% Choose proper frequency points
next = 1;
index = 1;
nums = length(freqs);
numn = length(freqn);
Ydev = [];
while (index <= nums & next <= numn)
```

```
  if (freqs(index) == freqn(next))
    Ydev = [Ydev ; ymeas(index,:)];
    next = next + 1;
  end
  index = index + 1;
end

%###########
% Frequencies
%###########
freq = freqn * 1E+9;

%########################################################
% Extraction of the channel thermal noise based on the DC approach
%########################################################
y = Rn(1:4);
x = freqn(1:4);
coeff = polyfit(x,y,0);
Rsub = (Rdbi + Rdb)/2;
ididDC = kt4.*( (coeff(1) - Rg - Rs)*gmdc^2 - (Rsub + Rs)*gmbdc^2 - 2*Rs*gmdc*gmbdc - 2*Rs*(gmdc +
    gmbdc)/Rds - (Rd + Rs)/Rds^2 );

if (0)

  for f = 1 : size(freq)

    S = i*2*pi*freq(f);

    igig = [igig; -kt4*(4*Ri/3)*(S*Cgs)^2];
    igid = [igid; kt4*S*Cgs/6];
    idid = [idid;ididDC];

    igigcal = [igigcal; -kt4*(4*Ri/3)*(S*Cgs)^2];
    igidcal = [igidcal; kt4*S*Cgs/6];
    ididDCcal = [ididDCcal; ididDC];

  end

else

%##############################
%# Calculate Y and noise parameters
%##############################
for f = 1 : size(freq)

  S = i*2*pi*freq(f);

  gm  = gmdc*(1 - S*tau);
  gmb = gmbdc*(1 - S*tau);
  gmd = gmddc*(1 - S*tau);
```

```
%####################################################
%# Define element values at a certain frequency for one bias
%####################################################
Y1  = 1/Rg;
Y2  = 1/Rd;
Y3  = 1/Rs;
Y4  = 1/Rds;
Y5  = 1/Rdbi;
Y6  = 1/Rsbi;
Y7  = 1/Rdb;
Y8  = 1/Rsb;
Y9  = 1/(Ri + 1/(S*Cgs));
Y10 = 1/(Rgd + 1/(S*Cgd));
Y11 = S*Cgb;
Y12 = S*Cdb;
Y13 = S*Csb;

%######################################################
%# Define noise source values at a certain frequency for one bias
%######################################################
igg  = 0;
igd  = 0;
idd  = 0;
idg  = conj(igd);
iGG  = kt4/Rg;
iDD  = kt4/Rd;
iSS  = kt4/Rs;
idbi = kt4/Rdbi;
isbi = kt4/Rsbi;
idb  = kt4/Rdb;
isb  = kt4/Rsb;

%######################################################
%# 5. Calculate the correlation matrix [CAdev] of the transistor
%# based on de-embedded noise parameters at one frequency
%######################################################
CAdev(1,1) = Rn(f);
CAdev(1,2) = (NFmin(f)-1)/2 - Rn(f)*conj(Yopt(f));
CAdev(2,1) = (NFmin(f)-1)/2 - Rn(f)*Yopt(f);
CAdev(2,2) = Rn(f)*abs(Yopt(f))^2;
CAdev     = 2*k_boltz*To*CAdev;       %# [CAdev] is 4x4 at one frequency

%############################################################
%# 6. Calculate the four port admittance matrix Yextr of the extrinsic part
%# in the RF transistor model.
%############################################################
m = 8;   % number of nodal equations (number of rows and colums in Y, number of rows in A and C)

% Y4, Y9, Y10, gm and gmd are taken away from the Ymm to get Yex
Yex=[ Y1,  0,   -Y1,   0,    0,    0,     0,    0; ...
      0,   Y2, 0,   -Y2,    0,    0,     0,    0; ...
```

```
    -Y1,    0,  Y1+Y11,     0,      0,  -Y11,   0,      0; ...
      0, -Y2,      0, Y2+Y12,  -gmb,   gmb,    -Y12,     0; ...
      0,   0,      0,    0,Y3+Y13+gmb,-gmb,       0,  -Y13; ...
      0,   0,   -Y11,    0,      0,Y5+Y6+Y11,   -Y5,   -Y6; ...
    0,   0,  0,  -Y12,    0,    -Y5,Y5+Y7+Y12,       0; ...
    0,   0,  0,     0,  -Y13,   -Y6,       0,   Y6+Y8+Y13 ];

%# Node Elimination
YAex(1:m,1:m) = Yex;

% Node elemination until 5 nodes remained
for k = 1 : (m-5)
 YAex(1:m-k, 1:m-k) = YAex(1:m-k, 1:m-k) - YAex(1:m-k, m+1-k)*YAex(m+1-k, 1:m-k)./YAex(m+1-k,
   m+1-k);
end

% Change veriables - V3 = V3' - V5'and V4 = V4' - V5'
YAex(:,5) = YAex(:,3) + YAex(:,4) + YAex(:,5);

% Add row 3 and row 4 of YAextr to its row 5 because I3 + I4 = -I5 => I3 + I4 + I5 = -I5 + I5 = 0
YAex(5,:) = YAex(3,:) + YAex(4,:) + YAex(5,:);

% Eliminate node 5 (or V5)
for k = (m-4) : (m-4)
 YAex(1:m-k, 1:m-k) = YAex(1:m-k, 1:m-k) - YAex(1:m-k, m+1-k)*YAex(m+1-k, 1:m-k)./YAex(m+1-k,
   m+1-k);
end

% Calculate the four port admittance matrix Yextr which is defined in YAex(1:4,1:4)
Yextr = YAex(1:4,1:4);

% Partition Yextr
Yee = Yextr(1:2,1:2);
Yei = Yextr(1:2,3:4);
Yie = Yextr(3:4,1:2);
Yii = Yextr(3:4,3:4);

%##############################################################
%# 7. Calculate the two port admittance matrix Yintr of the intrinsic part
%# in the RF transistor model.
%##############################################################
Yintr = [Y9+Y10,-Y10;gm-Y10,Y4+Y10+gmd];

%############################
%# 8. Calculate the matrix D
%############################
D = -Yei*inv(Yii + Yintr);

%##################################################################
%# 9. Convert CAdev to CYdev by using the measured intrinsic Y parameters
%##################################################################
```

```
TY = [-Ydev(f,1), 1; -Ydev(f,3), 0];
CYdev = TY*CAdev*TY';   %# [CYdev] is 2x2 for one frequency


%################################################
%# 10. Calculate the noise correlation CYextr from Yextr
%################################################
CYextr = 2*k_boltz*Temp*real(Yextr);    %# [CYextr] is 4x4 for one frequency

% Partition CYextr
Cee = CYextr(1:2,1:2);
Cei = CYextr(1:2,3:4);
Cie = CYextr(3:4,1:2);
Cii = CYextr(3:4,3:4);

%################################################
%# 11. Calculate the correlation admittance matrix CYintr
%################################################
Di = inv(D);
CYintr = Di*(CYdev - Cee)*Di' - Cie*Di' - Di*Cei - Cii;

%#########################
%# 12. Convert Yintr to Aintr
%#########################
[Aintr(1,1), Aintr(1,2), Aintr(2,1), Aintr(2,2)] = y2a(Yintr(1,1), Yintr(1,2), Yintr(2,1), Yintr(2,2), Zo);

%###########################
%# 13. Convert CYintr to CAintr
%###########################
TA = [0, Aintr(1,2); 1, Aintr(2,2)];
CAintr = TA*CYintr*TA';   %# [CAintr] is 2x2 for one frequency

%################################
%# 14. Calculate the noise parameters
%################################
NFmin_intr = 1 + (real(CAintr(1,2)) + sqrt(real(CAintr(1,1))*real(CAintr(2,2)) - imag(CAintr(1,2))^2))/
   (k_boltz*To);
 Rn_intr = real(CAintr(1,1))/(2*k_boltz*To);
 Yopt_intr = (sqrt(real(CAintr(1,1))*real(CAintr(2,2)) - imag(CAintr(1,2))^2) + i*imag(CAintr(1,2)))/
   real(CAintr(1,1));

%######################################################
%# 15. Calculate the power spectral dendity of the noise sources
%######################################################
kt4Rn = kt4*Rn_intr;
Ycor = (NFmin_intr - 1)/2/Rn_intr - Yopt_intr;
i2i2 = kt4Rn*abs( Yintr(2,1) )^2;
i1i1 = kt4Rn*( abs(Yopt_intr)^2 - abs(Yintr(1,1))^2 + 2*real( (Yintr(1,1) - Ycor)*conj(Yintr(1,1)) ) );
i1i2 = kt4Rn*(Yintr(1,1)-Ycor)*conj(Yintr(2,1));

igig = [igig;i1i1];
```

```
 igid = [igid;i*imag(i1i2)];
 idid = [idid;i2i2];

 igigcal = [igigcal; -kt4*(4*Ri/3)*(S*Cgs)^2];
 igidcal = [igidcal; kt4*S*Cgs/6];
 ididDCcal = [ididDCcal; ididDC];

end

end

%####################
% Calculate the coefficients
%####################
y = igig;
x = freqn;
coeff = polyfit(x,y,2);
if (coeff(1) < 0)
  coeff(1) = 0;
end
Cigig = coeff(1)./(1E+18);

y = imag(igid);
x = freqn;
coeff = polyfit(x,y,1);
if (coeff(1) < 0)
  coeff(1) = 0;
end
Cigid = coeff(1)./(1E+9);

y = idid;
x = freqn;
coeff = polyfit(x,y,0);
if (coeff(1) < 0)
  coeff(1) = 0;
end
Cidid = coeff(1);

%Correlation Coefficient
Cc = imag(igid) ./ real(sqrt(igig.*idid));

%############################################
% Write extracted noise sources to file.nprn
%############################################
if (Option == 0)
  data_noise(:,1) = freqn;
  data_noise(:,2) = igig;
  data_noise(:,3) = imag(igid);
  data_noise(:,4) = idid;

  %data_noise(:,3) = igigcal;
```

```
  %data_noise(:,6) = imag(igidcal);
  %data_noise(:,4) = real(igid);
  %data_noise(:,8) = ididDC;

  fout = [strtok(fname,'.'),'.nprn'];
  header1=['!Extracted noise sources from ',fndev,' on ',date];
  header2=['!VD = ',num2str(vd),' V  ID = ',num2str(id),...
      ' mA  VG = ',num2str(vg),' V  IG = ',num2str(ig),' uA'];
  header3=['!FREQ(GHz)   ','igig(A^2/Hz) ','igid(A^2/Hz) ','idid(A^2/Hz)'];

  fprintf('Writting extracted noises to file .... %s\n\n', fout);

  savedata(fout,'new',data_noise,header1,header2,header3);
end

return
```

Appendix G

MATLAB PROGRAM FOR NOISE CALCULATION

```
%##########################################################################################
%#
%# Function: MOSFETNoise.m
%#
%# Purpose: This function calculates the channel noise, induced gate noise and their
%#          correlation as a function of bias and frequency
%#
%# Author: Chih-Hung Chen
%#
%# Date: September 30, 2001
%#
%# Syntax: [Ids,Sidid,Sigig,Sigid,c] = MOSFETNoise(model_param,[L;W],[Vd;Vg;Vs;Vb],freq);
%#
%# Input:
%#        L  : channel length (um)
%#        W : channel width (um)
%#        Vd, Vg, Vs and Vb : drain, gate, source and body bias (volt)
%#        freq : operating frequency (GHz)
%#
%# Output:
%#        Ids   : DC current Ids (A)
%#        Sidid : spectral density of the channel noise (A^2/Hz)
%#        Sigig : spectral density of the induced gate noise (A^2/Hz)
%#        Sidid : spectral density of the correlation noise (A^2/Hz)
%#        c     : noise correlation coefficient
%#
%##########################################################################################

function [Ids, Sidid, Sigig, Sigid, c]=MOSFETNoise(varargin)

model_param = varargin{1};
device_geo  = varargin{2};
device_bias = varargin{3};
freq        = varargin{4};
```

```
%#################
% Physical Parameters
%#################
k_boltz = 1.38066E-23;        % J/K - Boltzmann constant
tempC = 27;                   % Celcus - room temperature
q_charge = 1.60218E-19;       % C - electronic charge
epsilon_o = (8.854E-14)*100;  % (F/cm)*100 - free space permittivity
rel_epsilon_si = 11.8;        % relative permittivity of Si
rel_epsilon_ox = 3.9;         % relative permittivity of SiO2
vsat = (8E+6)*1E-2;           % (cm/sec)*1e-2 - saturated velocity
ni = (1.45E+10)*1E+6;         % (1/cm^3)*1e+6 - intrinsic concentration of Si
phim_Al = 0.6;                % V - contact potential of Al
d = 1E-8;                     % watts for silicon

%Derived physical parameters
tempAbs = 273.15 + tempC;             % K - absolute temperature
Vtm=k_boltz*tempAbs/q_charge;         % volt - thermal voltage, p.7, (1.2.8) - Tsividis
epsilon_si = rel_epsilon_si * epsilon_o;   % F/m - permittivity of Si
epsilon_ox = rel_epsilon_ox * epsilon_o;  % F/m - permittivity of SiO2
kTo4 = 4*k_boltz*tempAbs;

%################
% Model Parameters
%################
tox   = model_param(1,1)*1E-10;       % angstrom*1e-10 = m - oxide thinkness
Nsd   = model_param(2,1)*1E+6;        % (1/cm^3)*1e+6 - doping concentration
xj    = model_param(3,1)*1E-6;        % (um)*1e-6 - source/drain junction depth
Qo    = model_param(4,1)*1E+4*q_charge; % (1/cm^2)*1e+4*q - oxide trapped charge
Vtho  = model_param(5,1);             % V - threhold voltage for Vbs = 0 in the linear region
u0    = model_param(6,1)*1E-4;     % (cm^2/V.s)*1e-4 - mobility at low field, p.3-7, (3.2.1) - Bsim3v3
Ua    = model_param(7,1);          % fitting parameter for effective mobility, p.3-7, (3.2.1) - Bsim3v3
Ub    = model_param(8,1);          % fitting parameter for effective mobility, p.3-7, (3.2.1) - Bsim3v3
Uc    = model_param(9,1);          % fitting parameter for effective mobility, p.3-7, (3.2.1) - Bsim3v3
delta = model_param(10,1);         % fitting parameter for Vdeff, p73, (4.82) - Lim
cplum = model_param(11,1);         % fitting parameter for CLM, p0, (4.108) - Lim
Rds   = model_param(12,1);         % Ohm - sum of source and drain resistances
laumda = 1;                        % fitting parameter for lchar
delta_hot = 0.2;                   % fitting parameter for hot electron effect

% Derived device parameters
Cox = epsilon_ox/tox;                  % F/m^2 - oxide capacitance, p.55, (2.2.4) - Tsividis
%lchar = sqrt(xj*epsilon_si/Cox);        % m - characteristic length, p75, (4.86) - Lim
lchar = laumda*sqrt(2*xj*epsilon_si/Cox/3); % m - characteristic length, p75, (4.86) - Lim
cclm = cplum/lchar^2;

%###################
% Geometry Information
%###################
L = device_geo(1,1)*1E-6;       % m
W = device_geo(2,1)*1E-6;       % m
```

```
Leff = L;
Weff = W;


%############
% Bias Conditions
%############
Vd = device_bias(1,1);
Vg = device_bias(2,1);
Vs = device_bias(3,1);
Vb = device_bias(4,1);
Vds = Vd - Vs;
Vgs = Vg - Vs;
Vbs = Vb - Vs;

%###################
% Calculated Parameters
%###################

% Flatband voltage (checked OK)
phim = phim_Al;
phiF = Vtm * log(Nsd/ni);   % p.21, (1.4.2) - Tsividis
phims = -phiF - phim;       % p.53, (2.2.2) - Tsividis
VFB = phims - Qo/Cox;       % p.55, (2.2.6) - Tsividis

% Threhold voltage
gamma = 2*q_charge*epsilon_si*Nsd;
%Vth = VFB + 2*phiF + gamma*sqrt(2*phiF-Vbs)/Cox;
Vth = Vtho + gamma*sqrt(2*phiF-Vbs)/Cox;
Vgt = Vgs - Vth;
if Vgt < 0
  Vgt = 0;
end

% Bulk-charge factor
phiB = 2*phiF;                                     % p.54 - Lim
Ab = 1 + 0.5*gamma/sqrt(phiB-Vbs)*(1-Vds/3);      % p.63, (4.54) - Lim

% Mobility
const_Eeffv = (Vgs+2*Vth)/tox;                                    % p.3-7, (3.2.1) - Bsim3v3
ueff = u0/(1+(Ua+Uc*Vbs)*const_Eeffv+Ub*const_Eeffv^2);  % modified p.3-7, (3.2.1) - Bsim3v3
Esat = 2*vsat/ueff;

% Saturation voltage
Vdsat = Esat*Leff*Vgt/(Vgt+Ab*Esat*Leff);         % p.71, (4.73) - Lim

% Effective drain voltage
Vdseff = Vdsat-0.5*(Vdsat-Vds-delta+sqrt((Vdsat-Vds-delta)^2+4*delta*Vdsat));

% Velocity saturation region
const_deltaVds = Vds - Vdseff;
```

```
const_ratioVds = const_deltaVds /lchar/Esat;
hclm = cclm*(1+sqrt(1+const_ratioVds^2))/(sqrt(1+const_ratioVds^2) - cclm*const_deltaVds);
Esatn = Esat*(1+hclm*const_deltaVds);                    % Esatn should be larger than Esat => vh > v

% Voltage and electrical field in the velocity saturation region (II)
const_EsatII = const_deltaVds/lchar;
Em = sqrt(const_EsatII^2 + Esat^2);
deltaL = lchar*log((const_EsatII+Em)/Esat);

% Effective Early Voltage
if Vdseff == 0
 Vdseff = 1E-12;
end
VAeff = (Esat*Leff*(1+hclm*const_deltaVds)+Vdseff)/hclm/Vdseff;  % p.81, (4.112) - Lim
gclm = 1 + const_deltaVds/VAeff;                                  % p.81, (4.111) - Lim

% Finial equivalent mobility;
const_uequ=0.5;
uequ = ueff/(1+const_uequ*Vdseff/(Leff*Esat));                    % p.66, (4.61) - Lim
Idso = Weff/Leff*uequ*Cox*(Vgt*Vdseff-0.5*Ab*Vdseff^2);
Idson = gclm*Idso;              % DO NOT use Esat = Esatn if using this equation, p.81, (4.111) - Lim

% Drain current
if Vgs > Vth
 Ids = Idson/(1+Rds*Idson/Vdseff);
 %Ids = Idso;    % Use Esat = Esatn if using this equation
else
 Ids = 0;
end

%######################
% Channel Noise Calculation
%######################

%####################
% C. H. Chen's noise model
%####################
% Model 1 for Qinv
%if Vds <= Vdsat
%  eta = 1 - Vds/Vdsat;
%else
%  eta = 0;
%end
%SidI = kTo4*Weff*ueff*Cox*Vgt*2*(1+eta+eta^2)/3/(Leff-deltaL)/(1+eta); % Tividis

% Model 2 for Qinv
const_VgtAb = Vgt - Ab*Vdseff/2;
Qinv = Weff*Cox*(const_VgtAb + (Ab*Vdseff)^2/12/const_VgtAb);
SidI = kTo4*ueff*Qinv/(Leff-deltaL);        % one Lelec = Leff-deltaL is cancelled with one Lelec in Qinv

% Channel noise caused by hot electron
```

```
SidI_hot = delta_hot*kTo4*Ids*Vdseff/(Leff-deltaL)^2/Esat^2;
SidI_hot = 0;

% Calculating noise voltage of channel noise in region II
SidII = Ids^3*kTo4*ueff*lchar*tanh(deltaL/lchar)/vsat/Esat^2/cplum^2;
SidII = 0;

%####################
% Peter Klien's oise model
%####################
if (0)
 taue = 0.1E-12      % second
 %Eta = Ab*(Vd-Vs)/Vgt;
 %Qi = Weff*Cox*Vgt*(1+Eta^2/3-Eta)/(1-Eta/2); %<=== negative value obtained!!!
 SidI = kTo4*ueff*Qinv/Leff; % 1. one L is cancelled with one L in Qi 2. negative value obtained for Qi, =>
    use Qinv!!!
 SidI_hot = 8*q_charge*vsat*taue*Ids/Leff/3*0;
 SidII = 0;
end

%#########################
% A. van der Ziel's noise model
%#########################
if (0)
 n = 2.6;     % hot electron coefficient
 Vstep = 0.001;
 V = 0 : Vstep : Vdseff;
 gofV = ueff.*Weff.*Cox.*(Vgt - V) - Ids./Esat;
 FoverFc = ueff.*Weff.*Cox.*(Vgt - V)./gofV;
 Zielnoise = sum(FoverFc.^n.*gofV.^2*Vstep);
 SidI = kTo4/Ids/Leff^2*Zielnoise;
 SidI_hot = 0;
 SidII = 0;
end

%#########################
% H. E. Halladay's noise model
%#########################
if (0)
 Cgg = Weff*Leff*Cox;
 eta = 1 - Vdseff/Vgt;
 SidI = kTo4*2/3*ueff*Cgg*Vgt*(1+eta+eta^2)/(1+eta)/Leff^2;
 SidI_hot = 0;
 SidII = 0;
end

% Total Noise Current at Drain Terminal
Sidid = SidI + SidI_hot + SidII;

Sidid = Sidid.*ones(1,length(freq));
```

```
%###########################
% Induced Gate Noise Calculation
%###########################
Vas = Vdseff - (0.5*Vgt*Vdseff - Vdseff^2/6)/(Vgt - 0.5*Vdseff);
Pgg = (Vgt*Vas)^2*Vdseff - Vgt*Vas*(Vgt+Vas)*Vdseff^2 + (Vgt^2+4*Vgt*Vas+Vas^2)*Vdseff^3/3 ...
     -0.5*(Vgt+Vas)*Vdseff^4 + 0.2*Vdseff^5;

%freq = [0.5:0.5:6];
fop = freq.*1e+9;
SigI = kTo4*(2*pi*fop).^2*Cox^4*Weff^4*ueff^2/Ids^3*Pgg;

%#########################
% A. van der Ziel's noise model
%#########################
if (0)
 n = 2.6;     % hot electron coefficient
 Vstep = 0.001;
 V = 0 : Vstep : Vdseff;
 Vas = Vdseff + Vdseff^2/2/Esat/Leff - (Vgt*Vdseff/2-Vdseff^2/6)/(Vgt-Vdseff/2)*(1+Vdseff/Esat/Leff);
 gofV = ueff*Weff*Cox*(Vgt - V) - Ids/Esat;
 FoverFc = ueff*Weff*Cox*(Vgt - V)./gofV;
 Zielgatenoise = sum(FoverFc.^n.*gofV.^2.*(Vas-V).^2*Vstep);
 SigI = kTo4*(2*pi*fop).^2*Cox^2*Weff^2/Ids^3*Zielgatenoise;
end

%#########################
% H. E. Halladay's noise model
%#########################
if (0)
 Cgg = Weff*Leff*Cox;
 eta = 1 - Vdseff/Vgt;
          SigI      =      16*kTo4*(2*pi*fop).^2*Leff^2*Cgg*(1+5*eta+13*eta^2+5*eta^3+eta^4)/
    (135*ueff*Vgt*(1+eta)^5);
end

Sigig = SigI;

%#########################
% Correlation Noise Calculation
%#########################
Pgd = Vgt^2*Vas*Vdseff - 0.5*Vgt*(Vgt+Vas)*Vdseff^2 + Vgt*Vdseff^3/3 ...
    - 0.5*Vgt*Vas*Vdseff^2 + (Vgt+Vas)*Vdseff^3/3 - 0.25*Vdseff^4;

Sigid = kTo4*(2*pi*fop)*Weff^3*Cox^3*ueff^2*Pgd/Leff/Ids^2;

%#########################
% A. van der Ziel's noise model
%#########################
if (0)
 n = 2.6;     % hot electron coefficient
 Vstep = 0.01;
```

```
  V = 0 : Vstep : Vdseff;
  %Vas = Vdseff - (Vgt*Vdseff/2-Vdseff^2/6)/(Vgt-Vdseff/2);
  %gofV = ueff*Weff*Cox*(Vgt - V);
  Vas = Vdseff + Vdseff^2/2/Esat/Leff - (Vgt*Vdseff/2-Vdseff^2/6)/(Vgt-Vdseff/2)*(1+Vdseff/Esat/Leff)
  gofV = ueff*Weff*Cox*(Vgt - V) - Ids/Esat;
  FoverFc = ueff*Weff*Cox*(Vgt - V)./gofV;
  Zielcolnoise = sum(FoverFc.^n.*gofV.^2.*(Vas-V)*Vstep);
  Sigid = kTo4*(2*pi*fop)*Cox*Weff/Ids^2/Leff*Zielcolnoise;
end

%########################
% H. E. Halladay's noise model
%########################
if (0)
  Cgg = Weff*Leff*Cox;
  eta = 1 - Vdseff/Vgt;
  Sigid = kTo4*(2*pi*fop)*Cgg*(1-eta^2)*(1+4*eta+eta^2)/(9*(1+eta)^4);
end

%###################
% Correlation Coefficient
%###################
c = Sigid ./ sqrt(Sigig.*Sidid);

return
```