.

THE DESIGN, FABRICATION AND CHARACTERIZATION OF SILICON OXIDE NITRIDE OXIDE SEMICONDUCTOR THIN FILM GATES FOR USE IN MODELING SPIKING ANALOG NEURAL CIRCUITS

THE DESIGN, FABRICATION AND CHARACTERIZATION OF SILICON OXIDE
NITRIDE OXIDE SEMICONDUCTOR THIN FILM GATES FOR USE IN MODELING
SPIKING ANALOG NEURAL CIRCUITS

By RICHARD PETER WOOD, B. ENG., M.A Sc.
A Thesis Submitted to the School of Graduate Studies in Partial Fulfillment of the
Requirements for
The Degree Doctor of Philosophy

.

McMaster University Doctor of Philosophy (2012) Hamilton, Ontario (Engineering Physics)

TITLE: The Design, Fabrication and Characterization of Silicon Oxide Nitride Oxide

Semiconductor Thin Film Gates for Use in Modeling Spiking Analog Neural Circuits

AUTHOR: Richard Peter Wood, B.Eng., M.A.Sc. (McMaster University)

SUPERVISORS: Dr. Peter Mascher and Dr. Ian Bruce

NUMBER OF PAGES: xii, 118.

.

ABSTRACT

This Thesis details the design, fabrication and characterization of organic semiconductor field effect transistors with silicon oxide-nitride-oxide-semiconductor (SONOS) gates for use in spiking analog neural circuits. The results are divided into two main sections. First, the SONOS structures, parallel plate capacitors and field effect transistors, were designed, fabricated and characterized. Second, these results are used to model spiking analog neural circuits. The modeling is achieved using PSPICE based software.

The initial design work begins with an analysis of the basic SONOS structure. The existence of the ultrathin layers of the SONOS structure is confirmed with the use of Transmission Electron Microscopy (TEM) and Energy Dispersive Spectroscopy (EDS) scans of device stacks. Parallel plate capacitors were fabricated prior to complete transistors due to the significantly less processing required. The structure and behaviour of these capacitors is similar to that of the transistor gates which allows for the optimization of the structures prior to the fabrication of the transistors. These capacitors were fabricated using the semiconductor materials of; crystalline silicon, amorphous silicon, Zinc Oxide, copper phthalocyanine (CuPc) and tris 8-hydroxyquinolinato aluminium (AlQ3). These devices are then subjected to standard capacitance voltage (C-V) analysis. The results of this analysis demonstrate that the inclusion of SONOS structures in the capacitors (and transistors) result in a hysteresis which is the result of charge accumulation in the nitride layer of the SONOS structure.

.

This effect can be utilized as an imbedded memory. Standard control devices were fabricated and analysed and no significant hysteresis effect was observed. The hysteresis effect is only observed after the SONOS devices are subject to high voltages (approximately 14 volts) which allows tunneling through a thin oxide layer into traps in the silicon nitride layer. This analysis was conducted to confirm that the SONOS structure causes the memory effect, not the existence of interface states that can be charged and discharged.

The next step was to design and fabricate amorphous semiconductor field effect transistors with and without the SONOS structure. First FETs without the SONOS gates were fabricated using amorphous semiconductor materials; Zinc Oxide, CuPc and AlQ3 and then the devices were characterized. This initial step confirmed the functionality of these basic devices and the ability to fabricate working control samples. Next, SONOS gate TFTs were fabricated using CuPc as the semiconductor material. The characterization of these devices confirmed the ability to shift the transfer characteristics of the devices through a read and write mechanism similar to that used to shift the C-V characteristics of the parallel plate capacitors. Split gate FETs were also produced to examine the feasibility of individual transistors with multiple gates.

The results of these characterizations were used to model spiking analog neural circuits. This modeling was carried out in four parts. First, representative transfer and

.

output characteristics were used to replicate analog spiking neural circuits. This was carried out using standard PSPICE software with the modification of the discrete TFT device characteristics to represent the amorphous CuPc organic transistors. The results were found to be comparable to circuits using crystalline silicon transistors. Second, the SONOS structures were modeled closely matching the characterized results for charge and voltage shift. Third, a simple Hebbian learning circuit was designed and modeled, demonstrating the potential for imbedded memories. Lastly, split gate devices were modeled using the device characterizations.

.

ACKNOWLEDGMENTS

TABLE OF CONTENTS

TABLE OF FIGURES

PREFACE

This Thesis contains 6 chapters. Chapter 1 provides an introduction. Chapter 2 provides relevant background information and Chapter 3 presents the experimental details. Chapters 4 and 5 present the main findings of this work. Chapter 6 provides a summary.

As part of the background research outlined in Chapter 2, several digital neural networks were developed on FPGAs. This work has been accepted for Publication in the SPIE Photonics North 2012 Proceedings.

The investigation of SONOS capacitors as discussed in Chapter 4, was presented at Nano Ontario 2011.

Material from Chapters 4 and 5 covering the use of organic transistors in spiking analog circuits has been accepted for publication in the Springer Series, ICANN 2012, Part I, Lecture Notes in Computer Science 7552.

Material from Chapters 4 and 5 has been accepted for publication in the journal Organic Electronics.

The main concept of this work, the identification of a novel circuit element for use in Analog Spiking Neural Circuits was my own. The development of the digital neural networks was done by me. The fabrication and testing of the SONOS devices and the transistors was conducted by me. The modeling of the Spiking Analog circuits was also conducted by me.

PUBLICATIONS AND PRESENTATIONS

Wood, R., Moon, C.-B., Kim, W. Y., Wilson, P.R.J. , Wojcik, J. and Mascher, P. Comparison of Silicon Oxide Nitride Oxide Semiconductor (SONOS) Capacitors Using Silicon and Organic (AlQ3) Semiconductor Materials. (Poster Presentation at Nano Ontario 2011).

Wood, R., Bruce, I. and Mascher, P. Modeling of Spiking Analog Neural Circuits with Hebbian Learning, Using Amorphous Semiconductor Thin Film Transistors with Silicon Oxide Nitride Semiconductor Split Gates. (Accepted for publication in ICANN 2012, Part I, Lecture Notes in Computer Science 7552).

Wood, R., Bruce, I., Moon, C.-B., Kim, W. Y and Mascher, P. Modeling of Spiking Analog Neural Circuits Using Organic Semiconductor Thin Film Transistors with Silicon Oxide Nitride Semiconductor Gates. (Accepted for publication in Organic Electronics).

Wood, R., McGlashan, Alex, Yatulis, J., Mascher, P. and Bruce, I. Digital Implementation of a Neural Network for Imaging. (Accepted for Publication in SPIE Photonics North 2012 Proceedings).

Young Kim, Woo Kim, You-Hyun; Jhun, Chul-Gyu; Wood, R.; Mascher, P.; Moon, C.-B. Spectroscopic study of white organic light-emitting devices with various thicknesses of emissive layer. Journal of Applied Physics, v 111, n 1, January 1, 2012

Song, Wook Meng, Mei; Kim, You Hyun; Moon, Chang-Bum; Jhun, Chul Gyu; Lee, Sang Youn; Wood, Richard; Kim, Woo-Young. High efficient and color stable WOLED using double white emissive layer. Journal of Luminescence, v 132, n 8, p 2122-2125, August 2012

Lee, Sang Youn, Kim, You Hyun; Song, Wook; Mei, Meng; Wood, Richard; Kim, Woo Young. White organic light-emitting diodes using red-fluorescent and blue-phosphorescent emitters with inducer layer. Japanese Journal of Applied Physics, v 50, n 6 PART 1, June 2011

Wood, Richard, Cheuk, Roger; Woo, Young Kim. High performance active matrix TOLED. Proceedings of International Meeting on Information Display, v 2006, p 117-118, 2006, Proceedings of 2006 6th International Meeting on Information Display and the 5th International Display Manufacturing Conference - Digest of Technical Papers

Wood, Richard, Cheuk, Roger; Kim, Woo Young. High contrast top emission active matrix RGB OLED. IDW/AD'05 - Proceedings of the 12th International Display Workshops in Conjunction with Asia Display 2005, n 1, p 665-666, 2005, IDW/AD'05 - Proceedings of the 12th International Display Workshops in Conjunction with Asia Display 2005

1 INTRODUCTION

1.1 Overview

The subject of artificial neural networks is an intense field of study with the bulk of the work being conducted in digital representations, either indirectly through software that runs on digital computers or directly in the use of digital devices such as the field programmable gate array. Study of analog devices that emulate neural networks, or discrete neurons, has been around for many years. A resurgence of this subfield is likely due to increases in the ease, including cost, of device fabrication. This work focuses on the design, fabrication and characterization of discrete analog circuit elements and the application of these elements to analog neuron models. The discrete elements of interest are a type of memory device that can be imbedded directly into the gates of transistors. These are silicon oxide-nitride-oxide-semiconductor (SONOS) gates. These devices have been studied using standard crystalline silicon processes. The fundamental mechanism of these gates, which provides them with a quasi-static memory, is tunneling of electrons (or holes) from a semiconductor material through a thin tunneling oxide and into a charge storage material. This tunneling occurs during the application of applied voltages that are above the normally operating voltage of the device. The charge in this layer then acts to shift the operating characteristics of the transistor. This provides the quasi-static memory.

In the current work, we examine the feasibility of using these structures in transistors fabricated using amorphous materials such as copper phthalocyanine (CuPc) and tris 8-hydroxyquinolinato aluminium (AlQ3). The use of these amorphous materials allows

for the fabrication of stacked devices, essentially three dimensional circuits, that will produce a high interconnection density, such as in a biological neural network. In this work, we also examine the feasibility of split gate transistors which can also be used to represent multiple synaptic connections.

The results of the characterizations of these discrete devices are then used to model analog spiking neural circuits.

1.2   Contributions to the Field

This work has several novel contributions. The first contribution is the analysis of SONOS devices using organic amorphous semiconductor materials and the comparison to silicon based semiconductor devices. The second contribution is the use of the results of the characterizations of organic transistors to model spiking analog circuits. The results indicate that organic transistors can be used to effectively replicate neural circuits. This is important in the context of the ease of manufacture of stacked organic transistors. The third contribution is the demonstration of the feasibility of using organic SONOS transistors in spiking analog circuits. This includes the demonstration of a basic working Hebbian learning circuit.

1.3   Thesis Outline

The following is a brief outline of the thesis structure. Chapter 2 provides a background to the work which includes an overview of neural modeling, SONOS devices and organic electronics. Chapter 3 provides the experimental procedure with

an overview of the high vacuum deposition of various thin film layers to produce the capacitors and transistors characterized. Chapters 4 and 5 outline the results and discussion. Chapter 4 covers the characterization of the SONOS capacitors and the transistors. Chapter 5 outlines the use of the results of these characterizations in the modeling of spiking analog circuits. Chapter 6 concludes the thesis with a summary of the key results and suggestions for future work.

2 BACKGROUND

2.1 Introduction

This chapter provides a brief overview of the background of this research. The first sections outline the relevant points of current research, and understanding, in modeling neurons and their inclusion in neural networks. The overriding objective is to develop beneficial neural models and circuits. There are several approaches; weighted networks, stochastic firing rate models, spiking models, that can be represented in digital, analog or mixed mode. The focus of this current work is on analog representation of biological neurons in analog spiking circuits. The background section of this thesis attempts to outline the relevance of this approach in the greater context of neural research. To do this, we outline the approaches, noting that many researchers use software implementations which are inherently digital as they are implemented on digital hardware. There are also attempts to model neurons directly on field programmable gate arrays (FPGAs) [1-12], which are also digital implementations. There are also some researchers working in the field of analog FPGAs [13, 14]. Sections 2.3 and 2.4 give overviews of SONOS devices and organic electronics.

2.2 Neural Models

2.2.1 Biological Neurons

A brief overview of biological neurons is included, with more extensive explanations available in literature. [15-17]. Biological neurons are an electro-chemical system in which the electrical state of the neuron is determined by the difference between the

interior charge and the charge of the extracellular fluid. These charges are the result of ion densities. The neuron produces electrical signals on through the ratio of these ion densities (positive and negative charge). At rest, the system has dynamic stability with ions being pumped into the system through channels in the cell membrane, to balance any leakage. If the total membrane potential of the neuron is raised above a threshold level, a positive feedback process starts and the neuron generates an action potential, an electrical spike. The ability of the neuron to produce a second spike after the first is time constrained by the bio-chemical nature of the system and results in a refractory period, during which time, a second spike is unlikely. In a neural system, information is contained within the firing rate and the spike timing. Information between any 2 neurons is carried through chemical signals across the synapse. Learning and memory result from activity dependent synaptic plasticity. The basic Hebbian rule stipulates that if a neuron contributes to the firing of a second neuron then this synapse is strengthened. The nature of strengthening (or weakening) of the synapse is complex but is the result of changes in pre and post synaptic biochemical reactivity.

2.2.2   Overview of Neural Networks and Digital Implementations

A basic artificial neural network is a system that attempts to functionally represent biological neural networks. Typically, the artificial network connects a system of individual neurons and integrates these inputs. The result of this integration is then filtered through a threshold function. As the behaviour of a real biological neural system can be extremely complex, artificial systems out of necessity model the functionality by reducing the complexity. A simple form follows the configuration

shown in Figure 2-1. In this case, the inputs are factored by individual weights, which are defined by the connection path between the input layer and the hidden layer. These factored inputs are then integrated at each neuron. The output can then be dependent on some form of threshold function.

The basic neural network is implemented in various ways. The most relevant in the present context (as the present work focuses on the development of analog hardware) are hardware implementations, with digital implementations being the most common.
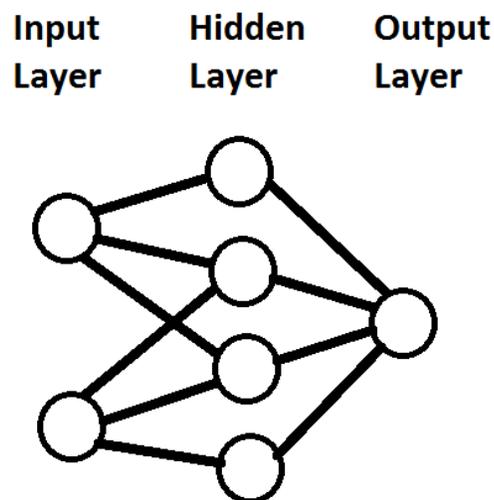
Figure 2-1:   Basic Neural Network.
An input layer is connected to an output layer through a hidden layer. Shown is a two neuron input layer, a four neuron hidden layer and a single output neuron. The straight lines represent the weights. In a more complex system, interconnections can exist between neurons in each layer.

The field programmable gate array (FPGA) is a useful prototyping device in general for digital designs and is ideal for the development of a neural network based devices.

The FPGA is a digital electronic prototyping device in which complex digital circuits can be rapidly implemented through non-volatile programming of gates in the device. The device can be reprogrammed many times, allowing for the iterative development of these complex circuits. Neural networks have been designed in FPGAs with many examples available [1-12]. The nature of the FPGA development boards and chips, such as the DE2 Educational Development board using the Cyclone III FPGA chip, manufactured by Altera, allows for the development of firing rate based neural networks or standard weight based matrices (a combination of the two is also possible).

A typical system structure follows that proposed by Savran et al. [1], as shown in Figure 2-2. Here, a state machine controls the mode that the system is in (learning, operating, etc.). It also controls the timing between network units (between aspect and decision space for example). This timing control is critical due to the overall system architecture. That is, this system uses the advantages of the digital FPGA by converting a parallel neural network into a sequential system. Although a true parallel system could be designed, it would be cumbersome and very difficult to implement as the nature of digital prototyping devices is inherently serial. In the system shown in Figure 2-2, in normal operating mode, each input is sequentially modified by a given synaptic weight with the result added to an accumulator. The output of the accumulator is then filtered through a thresholding function such as a sigmoid function as in Figure 2-3 [2]. All the data and the weights are digitized and will have a limited resolution based on this digitization.

Only when the entire layer is modified, can the system switch to the next layer. This makes the existence of the state machine and its control over timing, critical. This conversion to a sequential mode is feasible due to the high clock speed, in the GHz regime, of digital processors.
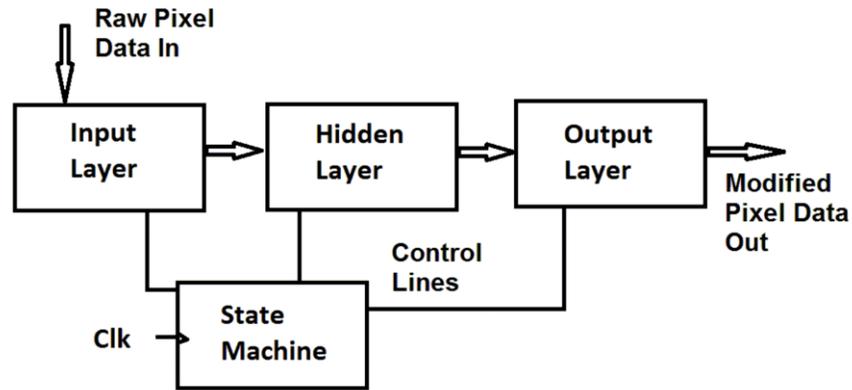
Figure 2-2: **Representative System Architecture for a Digital Neural Network. A state machine controls the sequencing of data and neural weights into individual neurons and between layers.**
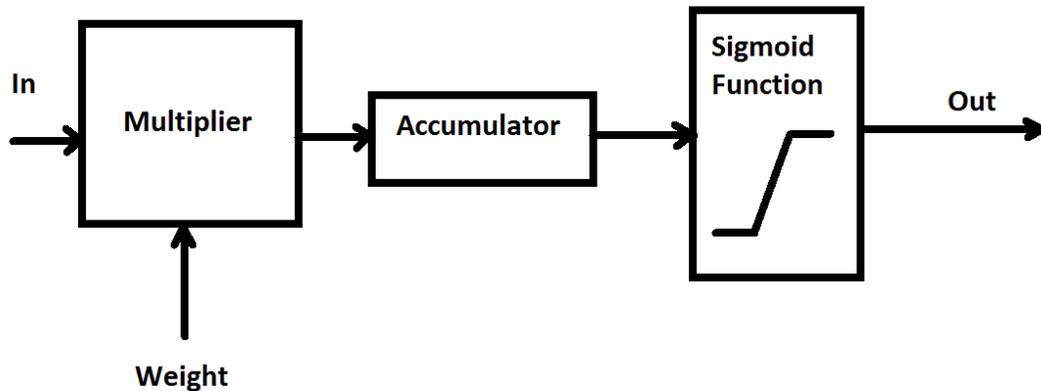
Figure 2-3: **Filtering through a Sigmoid Thresholding Function. After the state machine controls the accumulation of all the weight modified inputs to a single neuron, the result is filtered through the thresholding function, determining the output of the neuron.**

A schematic of a single neuron is shown in Figure 2-4.
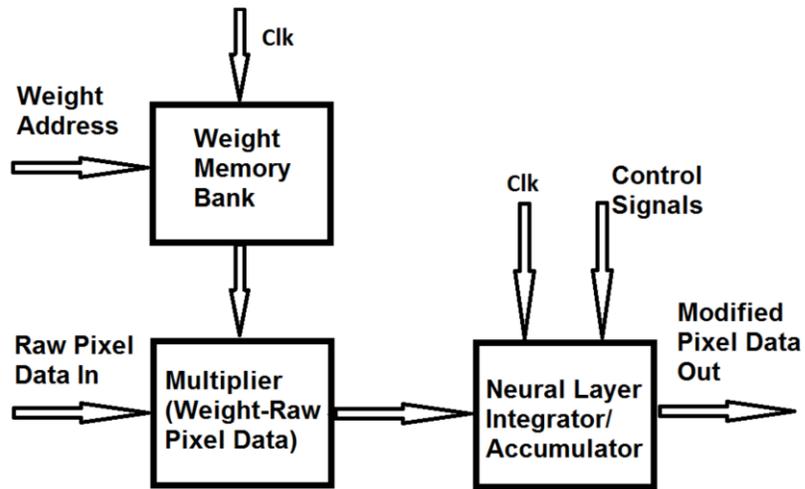
Figure 2-4:   **Single Neuron Schematic.**
Each pixel is modified by the weights and is integrated in an accumulator.

The digital neural network can be implemented in the form so far discussed which converts the parallel neural processor design into a sequential design. In this form of the design, the program will create virtual neurons and sequence through each with the use of some form of central processing unit and a memory controller. The memory controller will control the location of the weights and each neuron and is controlled by the state machine. However, the FPGA can also be used to design truly parallel designs. This is simple to design but highly inefficient for the compiler. A parallel system of three neurons is shown in Figure 2-5 which illustrates that individual neurons can be created in real space.
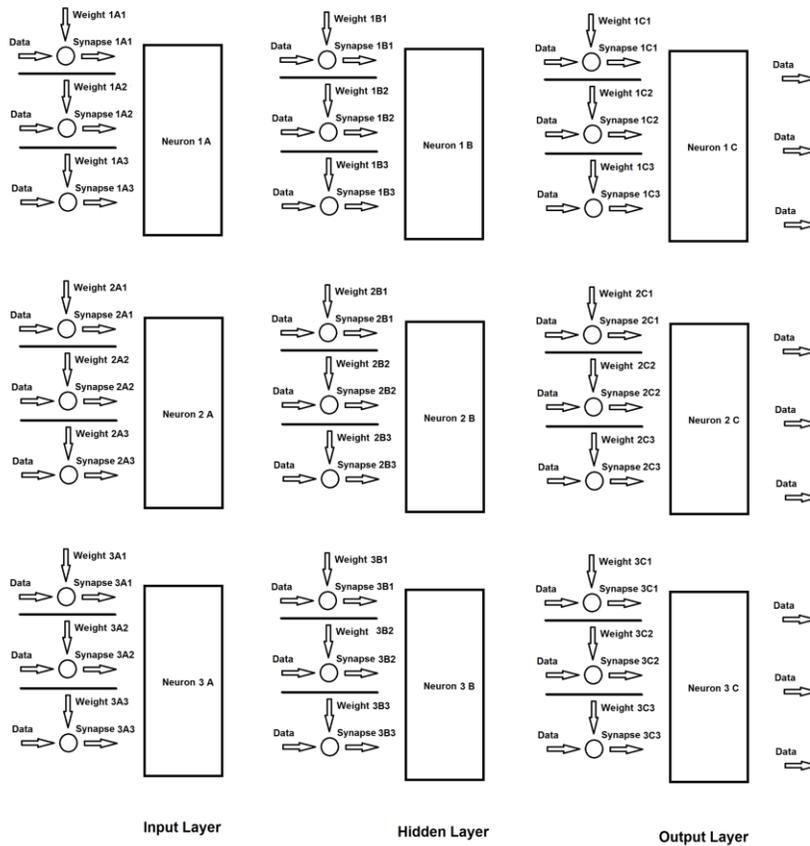
Figure 2-5:   Three-Neuron System with Three Layers in True Parallel Form. The complexity of this simple model can be seen with the neural interconnect routing being extremely difficult.

A basic learning configuration is shown in Figure 2-6 [4]. Here a separate module exists to modify the synaptic weights. This unit must also be controlled by the state machine, which can enable the learning cycle and back propagation. As shown in Figure 2-6, teaching signals can be taken from an external source. Unsupervised learning can also be used without the teaching signals. In this case an autocorrelation function of the output (and/or input) signals can be generated in the learning unit.
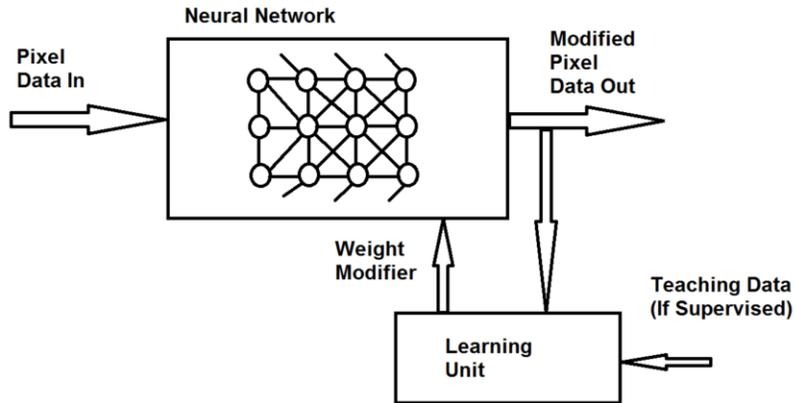
Figure 2-6:   Learning Configuration.
A learning unit controls the weight modification through control of teaching data (for supervised learning) or through control of the output data and an autocorrelation function (for unsupervised learning).

As part of the background examination of digital neural networks, several digital versions were generated for the current analysis. In particular, a simple visual neural field was created that was able to identify simple objects, such as letters and numbers, using the serial implementation of a weighted neural matrix. This artificial network was implemented in the DE2 Altera FPGA Development Board.

2.2.3   Overview of Spiking Models and Analog Neural Networks

The present work focuses on analog artificial neurons with significant information available in the timing of the output signals, either discretely in each pulse, or in the firing rate. These can be found in several specific references [18-21] and also in extended references [22-65]. One strain of artificial neural network research contends that the important properties of a neural network can be predominantly described by

the firing rate. In these configurations, the average firing rate response of a neuron to its inputs and the average effect of this firing rate on the inputs to other neurons is the dominant property. Note that the neuron is said to fire if the sum of its inputs exceeds some threshold with the output being essentially digital (but analog in time as the spike train is analyzed.) A schematic representation is shown below in Figure 2-7.
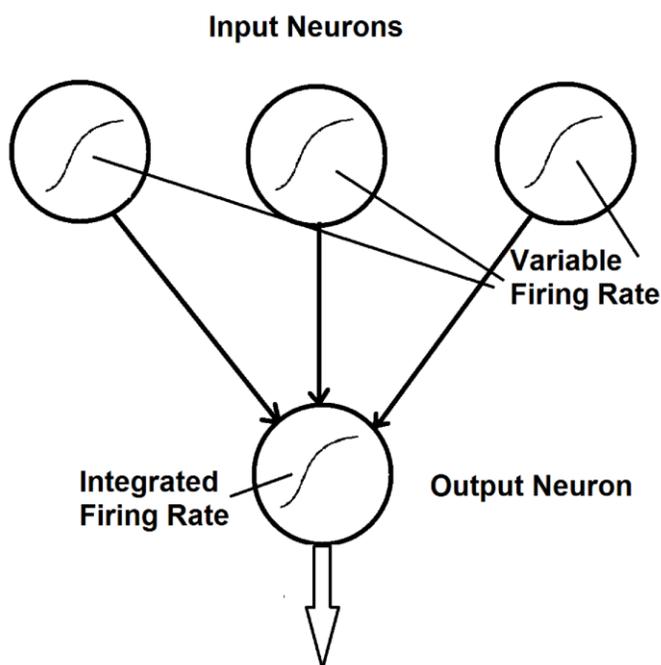
Figure 2-7:   Firing Rate Model.
The various input firing rates of the input neurons are combined in the output neuron and a new firing rate is produced and output.

2.2.4   Spiking Neural Models

It is believed that networks of spiking neurons may gain more computational power than traditional neural networks. A simple model is shown in Figure 2-8 [18]. Each input neuron emits a series of spikes. The weighted sum of decayed potentials is then computed. If the sum exceeds the threshold then an output spike is generated and over

time, a new series of output spikes results. In the simplest form, these spiking models follow the "integrate and fire" configuration as shown in Figure 2-9. Shown is a single neuron with a synaptic current that is integrated with capacitance C. Then, if the potential on C exceeds a threshold voltage, the neuron 'fires'. These models can become complicated when the intrinsic characteristics of the neuron are considered. An example of this is shown in Figure 2-10 [19], a circuit developed by Indiveri.
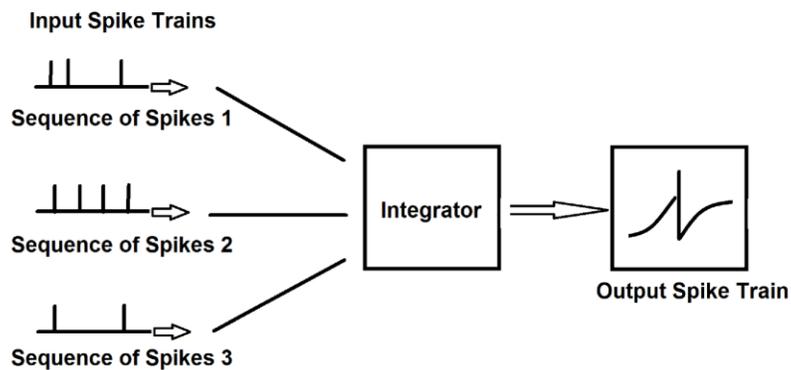
Figure 2-8:   Spiking Neural Model.
Shown are three spike trains which are then integrated and processed to produce a resulting output spike train.
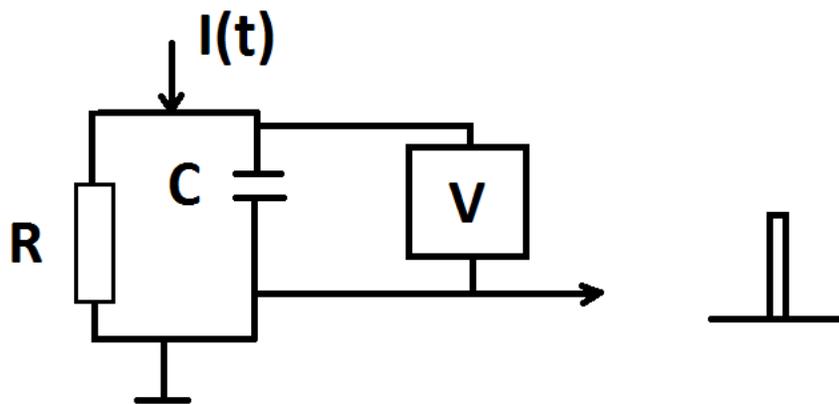
Figure 2-9: **"Integrate and Fire" Neural Model.**
An input current I(t) is integrated on capacitor C, with leakage R. The output spike is created if the voltage across C exceeds some comparative voltage.
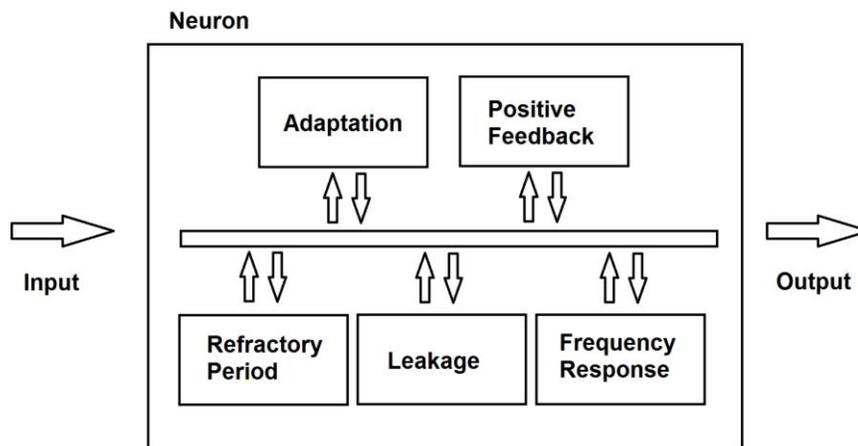
Figure 2-10: **Analog Neural Circuit Compartmental Model.**
Each functional unit (Refractory period, Adaptation, Positive Feedback, Leakage, Frequency Response) can be segmented within the circuit.

In this design, the functionality of the circuit has been divided into clear subgroups

(frequency response, leakage, adaptation, refractory period, positive feedback).

2.2.5 Learning

There are various aspects to neural learning. A brief description is included here to illustrate the relevant aspects of Hebbian learning. In the simplest form, Hebbian learning will occur when a neuron fires and in turn a connected neuron fires in sequence, then the synapse between these neurons is strengthened, Figure 2-11. In the matrix shown in Figure 2-11, the weights are modified by the relation $\tau_w \, dw/dt = vu$ where the rate of change of the weights depends on whether the output neuron fires in time with the given input vu. The learning rate is controlled by the constant τ_w.

$$\tau_w \frac{dw}{dt} = vu$$

Weight A1B1

Neuron A1

Neuron B1

Weight A2B1
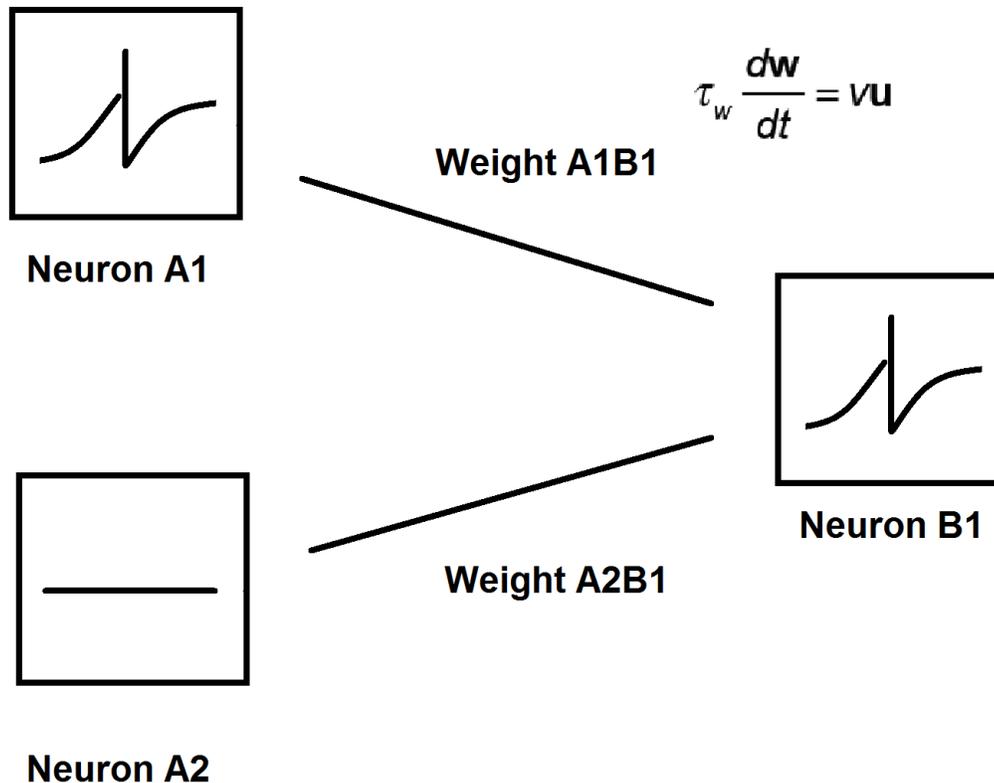
Neuron A2

Figure 2-11. **Simple neuron system with the Hebbian learning formula τ_w dw/dt = vu.**
Shown is one output neuron, B1, and 2 input neurons, A1 and A2. Neuron B1 fires as a result of A1, so the weight between these, A1B1, is increased while weight A2B1 remains unchanged.

In a modified Hebbian system, synapses can also be weakened between neurons that do not fire. In a system of neurons, the synapses will require some form of normalization to prevent a synaptic overload. Unsupervised learning for self-organization is possible with this basic premise. This will require the system to operate under four simple rules, as shown in Figure 2-12. First, the system follows the basic

Hebbian premise. Second, the system follows a "winner take all" scenario. Third, there is cooperative interaction between neurons. Lastly, structured information is required in the training process.
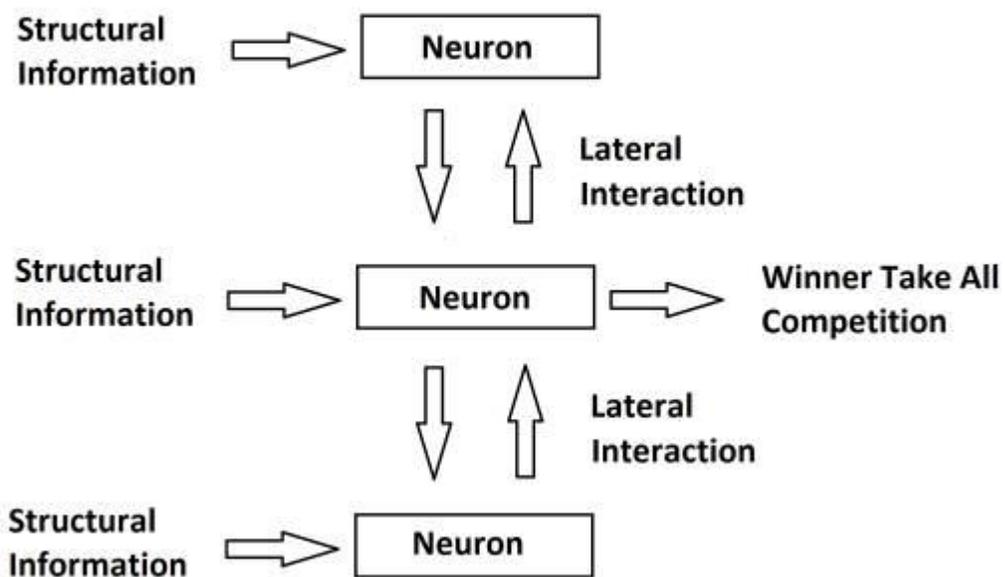
Figure 2-12.   Self Organization.
Requires structural information, lateral interaction and a winner take all system with Hebbian learning.

2.3 SONOS Devices

Silicon oxide nitride oxide semiconductor (SONOS) circuit elements have been previously studied [66-87] and found to be potentially useful structures for memory storage. As shown in Figure 2-13 [66], the devices are a thin film stack comprised of; a semiconductor substrate, followed by an oxide that is thin enough to allow electron or

hole tunneling. Next, there is a charge storage layer that has predominantly been made of silicon nitride. This is a matter of process convenience as this material is deposited in the same systems as the standard silicon semiconductor layer and the silicon based oxides but other materials can be used as the charge storage layer. Then there is a blocking oxide layer to prevent tunneling out of the charge storage layer. This is followed by a contact metal layer.

These structures can be used as quasi-permanent memory devices simulating synaptic plasticity through a non-volatile memory structure that utilizes charge tunneling through a thin gate oxide and a quasi-permanent charge storage layer (SiN). When a high positive bias is applied to the top electrode, electrons tunnel from the bulk semiconductor into the SiN layer. When the applied bias is removed, the negative internal charge remains and there is a shift to depletion/inversion in the semiconductor. This causes a shift to the right in the CV curve of an n-type semiconductor capacitor as higher positive voltages are required to overcome the effects of the negative internal charge and to achieve accumulation. The opposite effect occurs with the introduction of a positive trapped charge in the SiN layer using an applied negative bias. This causes a shift to the left in the CV curve of an n-type semiconductor capacitor. These effects can also be regarded as write or erase mechanisms.
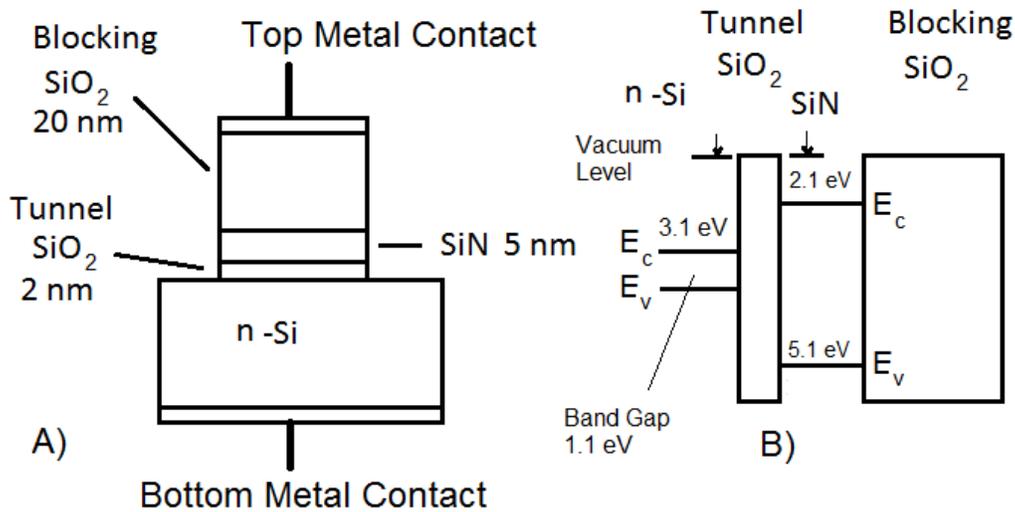
Figure 2-13.   SONOS Gate Structure.
A) A cross sectional view of a SONOS gate. This device uses n-type crystalline silicon as the semiconductor material. The blocking oxide is shown as 20 nm and the tunneling oxide is 2 nm. A SiN charge storage layer of 5 nm is used. B) The energy band diagram shows the approximate band alignment between the SiN and n-Si layers.

The basis of the SONOS structure is the tunneling effect through the ultra thin silicon dioxide layer. This mechanism has been previously characterized [88-98]. Tunneling in this structure can actually be described as three separate processes, as shown in Figure 2-14 [88]. The first is electron tunneling from the conduction band (ECB). The second is electron tunneling from the valence band (EVB). The third is hole tunneling from the valence band (HVB). The following formula is used to calculate tunneling currents (A/cm^2);

$$J_n = A\left(\frac{\emptyset_b}{V_{ox}}\right)\left(\frac{2\emptyset_b}{V_{ox}} - 1\right) E^2 \ * \ exp \left(\frac{-B\left[1 - \left(1 - \frac{V_{ox}}{\emptyset_b}\right)^{\frac{3}{2}}\right]}{E_{ox}}\right)$$

(2.1)

Where, coefficient A is,

$$A = \left(\frac{q^3}{8\pi h \emptyset_b}\right)$$
(2.1.1)

Coefficient B is,

$$B = \left(8\pi\sqrt{2m_{ox}} \ \emptyset_b^{3/2}/3hq\right)$$
(2.1.2)

E_{ox} is the electric field across the oxide defined as,

$$E_{ox} = (V_{ox}/T_{ox})$$
(2.1.3)

Where,

T_{ox} is the oxide thickness,

M_{ox} is the effective mass in the oxide,

$\acute{\emptyset}_b$ is the barrier height.
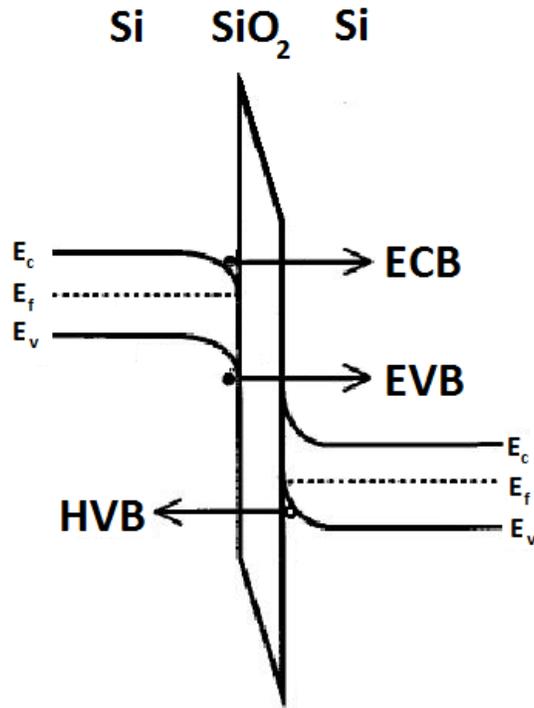
Figure 2-14. Tunneling Processes.
Shown is a system of Si-SiO₂-Si. tunneling proceeds through the thin oxide layer.
Shown are 3 possible tunneling processes, electrons from the conduction band to
the conduction band (ECB), electrons from the valence band to the conduction
band (EVB), and holes from the valence band to valence band.

In the proposed organic semiconductor based SONOS structure shown in Figure 2-15,

electrons will tunnel through a thin tunnel oxide from the copper phthalocyanine

(CuPc) Lowest Unoccupied Molecular Orbital (LUMO) level into traps in the SiN

layer. The band alignment is important as this will determine the tunneling rates at

given applied voltages. In the case shown with CuPc, the LUMO level is located at 3.2

eV and the Highest Occupied Molecular Orbital (HOMO) level at 4.95 eV. Ideally, to

act as an n-type device, efficient injection of electrons into the LUMO level of the

CuPc from a contact layer is required. In this case, calcium is shown, with a work

function of 2.87 eV, which closely matches the CuPc LUMO level. This will be discussed further in the section below on organic electronics.
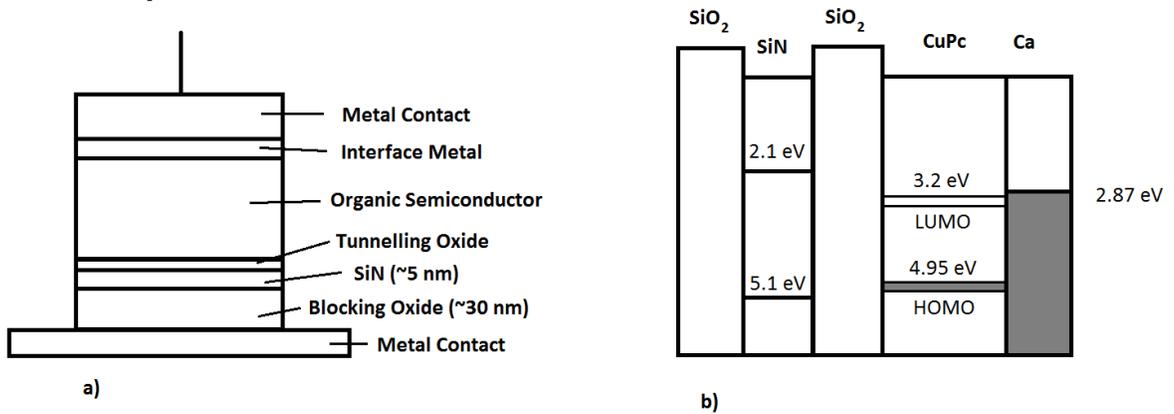
Figure 2-15. Proposed SONOS Gate Structure.
a) Cross section representation of the SONOS gate structure with an organic semiconductor. b) Energy band diagram for reference if the alignment of the conduction and valence bands of SiN to CuPc, and Calcium.

2.4 Organic electronics

The organic transistor differs from the standard silicon transistor in several ways, which has been previously analysed [99-111]. Of primary importance is the band alignment between the fermi level of contact metals and the LUMO or HOMO level of the organic semiconductor. The energy band structures for p and n-type devices made with the organic materials tris 8-hydroxyquinolinato aluminium (AlQ3) and CuPc, along with the amorphous material ZnO, are shown in Figure 2-16.

The semiconductor is regarded as p or n-type according to the band alignment of the injecting contact to the semiconductor. A p-type device is defined as one that has high injection efficiency of holes into the HOMO level of the organic semiconductor.

Appropriate selection of contact metals will allow for the design of either an n or p-type device.

Although both carrier types will be present, the injection barriers will dictate that one carrier will dominate the device characteristics at reasonably low source-drain source voltages. At high voltages, this injection barrier will be reduced. Real devices have been shown to exhibit ambipolar behaviour.

Of the devices shown, the most promising for the design of CMOS circuits are the CuPc devices. Here, we can get good alignment with the LUMO level using calcium as the contact metal to produce an n-type device, the only issue being the high reactivity of Ca. Using gold as the contact metal, we get good alignment with the HOMO level to produce a p-type device. In addition, the electron and hole mobilities of CuPc (7×10^{-4} and 2×10^{-3} cm^2/V s, respectively) are higher than Alq3 (5×10^{-7} and 1×10^{-7} cm^2/V s) [102].

For Alq3, we can also produce 'n' type devices using calcium as the metal contact but the alignment is not as close. The HOMO level is deeper than that of CuPc at 6.2 eV and requires gold contacts for closer band alignment. As mentioned, the mobility is also low.

For ZnO, we can produce reasonable 'n' type devices using aluminum contacts. The extreme depth of the valence band makes alignment with the metal Fermi level difficult, and 'p' type devices are not efficient. ZnO oxide is a rugged material and is relatively easy to produce. Unfortunately the depth of the valence band makes the production of CMOS circuits difficult.

Doping of the organic devices is possible. However, in the field of organic electronics, doping typically refers to the creation of a dopant-host system and the creation of new energy bands due to high doping concentrations rather than the creation of carriers.
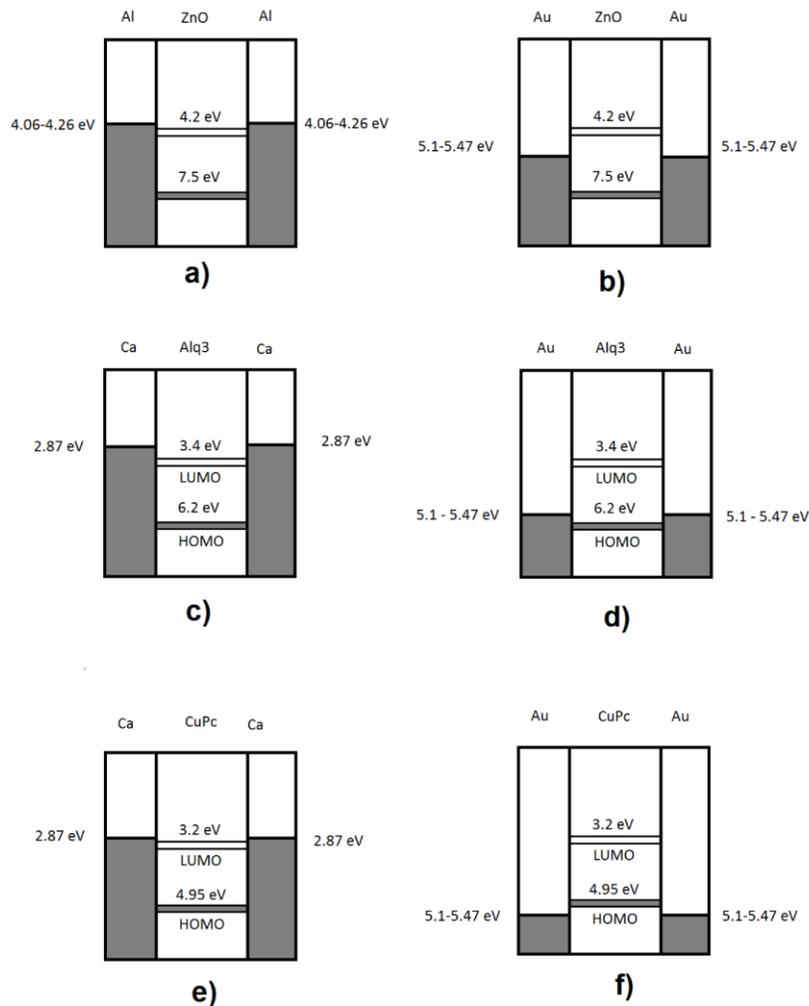
Figure 2-16. Energy Band Structures
of a) ZnO with aluminum contacts forming an n-type device. b) ZnO with gold contacts forming a p-type device. c) Alq3 with calcium contacts forming an n-type device. d) Alq3 with gold contacts forming a p-type device. e) CuPc with calcium contacts forming an n-type device. f) CuPc with gold contacts forming a p-type device.

The resulting transistor transfer characteristics will depend on the band alignment as well as the mobilities of the two carrier types. It will also depend on the internal fields created by the gates and will vary depending on the gate oxide thickness and materials and the gate metal. The expected transfer characteristics of the CuPc devices are shown in Figure 2-17. Due to the differences in electron and hole mobilities, to obtain balanced drain-source currents, either the applied voltages must differ or the gate lengths must be adjusted between the n and p-type transistors. The bias voltages of the devices must also be kept low to reduce the injection of 'unwanted' electrons and holes. At higher applied voltages, we will observe ambipolar behaviour as the minority carrier concentration will become significant.
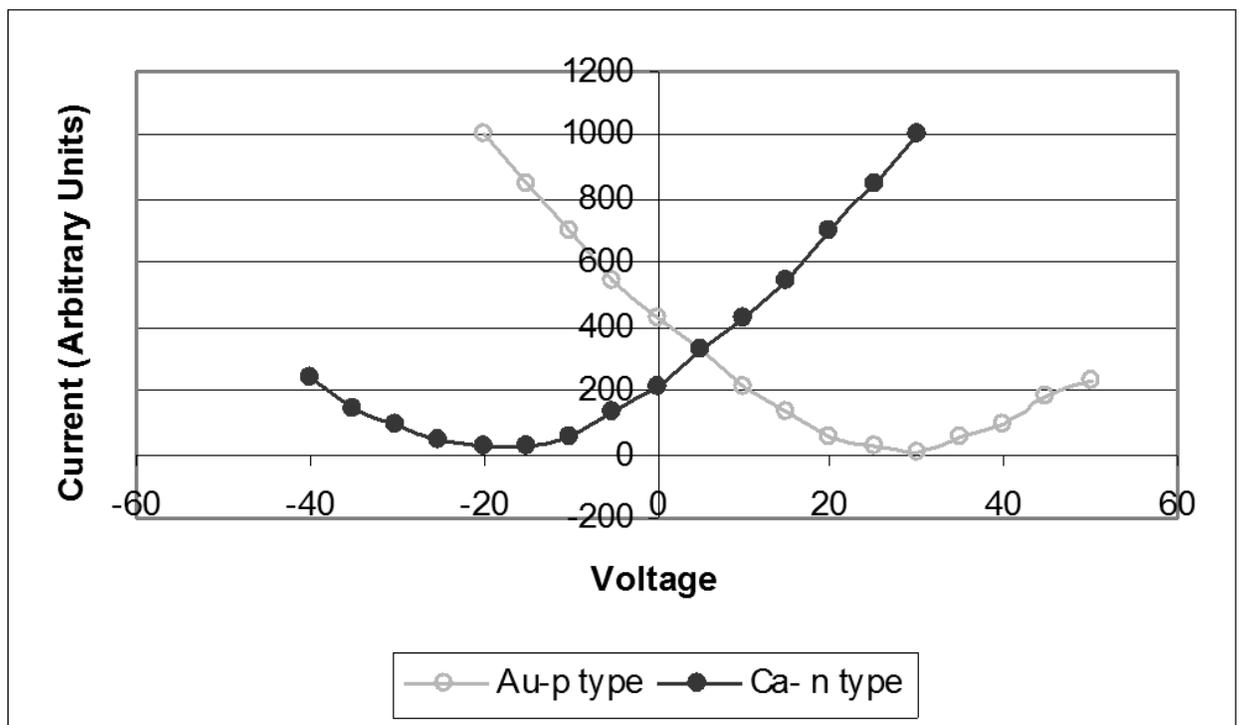
Figure 2-17: CuPc TFT with gold contacts and CuPc TFT with Calcium contacts.

The interface states of organic devices are of particular interest. Of concern is the formation of dipoles when the organic materials are deposited. When the organics are deposited on top of metals, the electric field at the metal surface causes the formation of the organic dipoles, Figure 2-18 [99]. As shown, a dipole barrier can form. The dipole will form as a result of the electric field that will extend beyond a metal layer. When the organic is deposited after the metal, it will deposit in the presence of this field and may form a dipole. This barrier is of concern if it can form charging sites that will mimic the behaviour of the SONOS (charge/discharge). In the current work, the organic materials are always deposited on oxides.
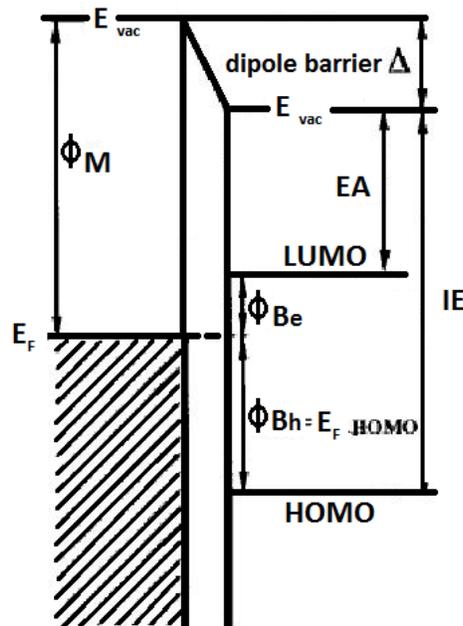
Figure 2-18.   Band Structure of theoretical metal-organic semiconductor interface. The dipole layer can form as the organic molecules will align to the field that extends beyond the surface of the metal layer. This dipole layer will act to shift the alignment of the LUMO and HOMO levels of the organic layer relative to the metal work function.

2.5 Split Gates

Split gate devices have also previously been studied [112-118] with an emphasis on dealing with short channel effects in silicon transistors. In this work, the split gate transistor is analyzed as applied to larger gates in amorphous semiconductor transistors. A schematic representation is shown in Figure 2-19. Here the device has 2 inputs (plus the source drain voltage). The devices could have more than 2 gates. A stacked gate configuration is shown in the Figure. Here the gates are separated with a spacer oxide. There will necessarily be gate-gate capacitance but this gate overlap is required as the mobility of the organic material is low and the devices cannot have spacing between the gates. The gate to gate capacitance in this case will occur due to the physical overlap of the gate metals which will create a parallel plate capacitor. This is necessary as any spaces that are not directly under a gate will not be subject to a field effect, resulting in extremely low conductivity in this area.
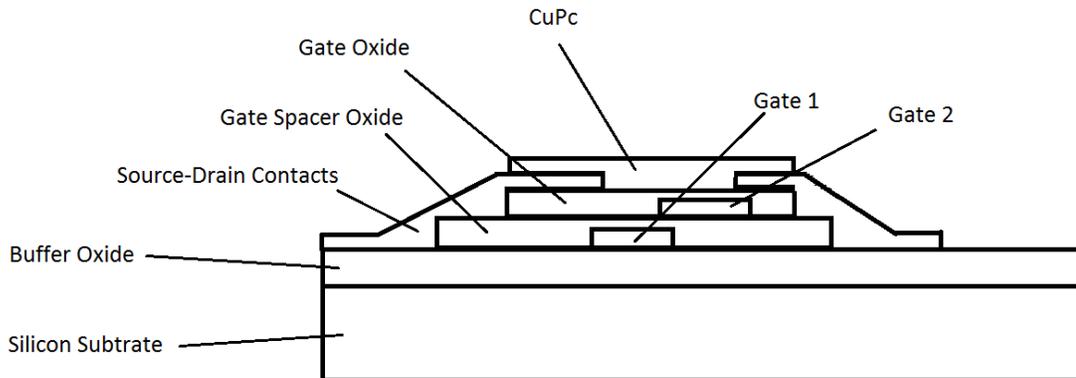
**Figure 2-19.   Split Gate Amorphous Semiconductor MOSFET.
Shown is a representative MOSFET structure with CuPc used as the
semiconductor material. Some overlap of the gates and source drain is required
to avoid 'dead zones' in the device that would otherwise be outside of the gate
field effect area.**

The SONOS gate structure shown in Figure 2-13 can be added to this amorphous

semiconductor split gate MOSFET

.

3   EXPERIMENTAL DETAILS

3.1   Introduction

This chapter provides the details on the fabrication of SONOS parallel plate capacitors and field effect thin film transistors. The devices were fabricated using standard high vacuum deposition techniques and semiconductor processing.

3.2   Fabrication of MOS Capacitors

Metal-Oxide Semiconductor (MOS) capacitors with the SONOS structure were designed, fabricated and characterized first due to the simpler processing requirements as compared to the fabrication of complete thin film transistors. For all device types, the SONOS layers were deposited using an Inductively Coupled Plasma Chemical Vapour Deposition (ICP CVD) high vacuum deposition system [119]. All devices utilized two-inch n-type silicon wafer substrates. Devices were made with several semiconductor materials; crystalline silicon, amorphous silicon, zinc oxide (ZnO), AlQ3, and CuPc. The SONOS structure was; 1. A tunneling layer of silicon dioxide in 3 thicknesses 1 nm, 2 nm and 3 nm; 2. A silicon nitride layer of 5 nm; and, 3. A blocking silicon dioxide of 20 nm. The tunneling oxide thickness was varied to examine the effect on tunneling.

3.2.1   Crystalline Silicon

For the crystalline silicon devices, the SONOS layers were deposited directly on the crystalline silicon substrate. The control oxide devices were produced with 20 nm

silicon dioxide only. Metal contacts were then deposited through a shadow mask to produce varying areas from 1 to 5 mm^2.

3.2.2 Amorphous Silicon

For the amorphous silicon devices, a thick amorphous silicon layer (200 nm) was first deposited on the silicon wafer followed by the SONOS layers. The control oxide devices were produced with 20 nm silicon dioxide only. Metal contacts were then deposited through a shadow mask to produce varying areas from 1 to 5 mm^2.

3.2.3 Zinc Oxide

Only control devices were produced for zinc oxide with a 30 nm silicon dioxide layer. Metal contacts were then deposited through a shadow mask to produce varying areas from 1 to 5 mm^2.

3.2.4 AlQ3 and CuPc

For the AlQ3 and CuPc devices, a thick buffer oxide was deposited on top of the crystalline silicon wafers. This was followed by the deposition of aluminium strip contact pads, followed by the SONOS layer deposition. Next, 200 nm AlQ3 or CuPc was deposited followed by top contacts of calcium followed by aluminium. The top metal contacts were deposited in strips at 90 degrees to the bottom contacts to give defined areas for the parallel plate capacitors. To reduce exposure to moisture and oxygen, the devices were then coated with a thick layer of a thermally deposited oxide using a silicon monoxide thermal source. These devices were then encapsulated in a nitrogen glove box using a cover glass and UV epoxy.

3.3   Transistors

Several transistor types were produced. 1. Single gate zinc oxide n-type. 2. AlQ3 single gate n-type. 3. CuPc single gate p and n-type. 4. CuPc single gate n-type with SONOS gates. 5. CuPc split gate p-type. The patterning of the metal contacts was achieved with standard positive photolithographic techniques. The gate lengths were varied from 10 μm to 50 μm. The organic materials were deposited through shadow masks.

3.3.1   Zinc Oxide Single Gate Transistors

Single gate n-type transistors were fabricated. Devices were fabricated on ultra flat glass substrates. The substrates were cleaned using an ultrasonic bath of acetone followed by methanol. The devices were transferred to a high vacuum system for the deposition of titanium. The titanium was patterned and etched to produce the gates. Next the gate dielectrics, 100 nm SiO_2, were deposited using the IPCVD system. Titanium was deposited using ebeam deposition, patterned and etched to produce the source drain contact pads. The devices were then pre-cleaned and etched and a 200 nm layer of ZnO was deposited using electron beam evaporation. The devices were then coated with a thick layer of thermally deposited silicon dioxide from a silicon monoxide source as a thin film encapsulant. The devices were then sealed in a nitrogen atmosphere using a glass cover plate and UV curable epoxy.

3.3.2 AlQ3 Single Gate p-Type Transistors

Single gate p-type transistors were fabricated. Devices were fabricated using the same method as the ZnO devices. Aluminium was deposited, patterned and etched to produce the source drain contact pads. The devices were then pre-cleaned and etched and a thin metal (5 Å) contact layer was deposited (Calcium for n-type) followed by the deposition of a 200 nm layer of AlQ3. The devices were then encapsulated using the method used for the ZnO transistors.

3.3.3 CuPc Single Gate Transistors

Single gate n and p-type transistors were fabricated to act as control devices (references points for standard device performance). Devices were fabricated as above. The devices were then pre-cleaned and etched and a thin metal (5 Å) contact layer was deposited (calcium for n-type and gold for p-type devices) followed by the deposition of a 200 nm layer of CuPc. The devices were then encapsulated using the method used for the ZnO transistors.

3.3.4 CuPc Transistors, p-Type, with Split Gates

Split gate devices were prepared as shown in Figure 2-19 above. Devices were fabricated as above. The intermediate gate dielectrics, 30 nm SiO2, were deposited using the IPCVD system. Titanium was deposited, patterned and etched to produce the second set of gates. The second gate dielectrics, 30 nm thick SiO2, were deposited using the IPCVD system. Titanium was deposited, patterned and etched to produce the source drain contact pads. The devices were then pre-cleaned and etched and a thin metal (5 Å) contact layer was deposited (gold for p-type devices) followed by the

deposition of a 200 nm layer of CuPc. The devices were then encapsulated using the method used for the ZnO transistors.

3.3.5 CuPc Transistors, p-type, with SONOS Gates

CuPc transistors, p-type, with SONOS gates were prepared as in 3.3.3, with the modification of the gate dielectric to include a SONOS structure of 30 nm SiO_2, 5 nm SiN, and 1 nm SiO_2.

4   RESULTS AND DISCUSSION

4.1   Introduction

The results of the measurement and analysis follow. The first section deals with the measurement procedures. The following sections cover the analysis of SONOS parallel plate capacitors. The initial analysis confirms the existence of the thin film stack through Transmission Electron Microscopy (TEM) and Energy Dispersive Spectroscopy (EDS). The CV analysis begins with the behaviour of crystalline and amorphous silicon which have been evaluated in literature. With the general SONOS behaviour demonstrated, AlQ3 and CuPc devices are analyzed. Field Emission Scanning Electron Microscope (FESEM) of an AlQ3 interface is examined. ZnO is included as a possible transistor semiconductor material as its amorphous nature would allow it to be deposited in three dimensional stacks. The last sections deal with the output and transfer characteristics of the transistors fabricated with AlQ3, ZnO, and CuPc.

4.2   Measurement Procedures

4.2.1   Capacitors

The parallel plate capacitors were measured using an HP 4280 Capacitance meter. The exact procedure was developed to examine the devices for hysteresis. Control devices without the SONOS structure, were examined to ensure that any future hysteresis could be attributed to the SONOS structure. The devices were mounted in an isolated probing station with contacts to the each side of the capacitors. The HP 4280 was then set to scan from positive or negative voltages. For all of the devices tested, the 14 volt

point was determined to be a consistent applied voltage that would allow charging through the tunneling oxide of the SONOS device. Below 6 volts, no SONOS behaviour was observed. For applied voltages between 6 and 14 volts, some behaviour was indicated depending on the exact device.

A description of the exact analysis follows. The device was set to scan from +14 volts to – 14 volts and the capacitance-voltage behaviour was recorded. This was repeated. Next, the device was scanned from +6 to -14 volts. This would examine a device for positive charging from the previous scan. The reverse procedure would be conducted to examine negative charging. The exact scan values changed depending on the exact device. This shift in the C-V characteristics is a result of several factors that serve to shift the device behaviour independently of the SONOS structure. These are primarily the contact potentials and charge imbedded in the oxides and the semiconductor materials.

A simple representation of the C-V scan is shown below, in Figure 4-1. Here, an observed shift of the capacitance is the result of the charging between scans. This charging, tunneling into the SiN layer, only occurs when the applied voltage exceeds 6 volts. The time for charge transfer is dependent on the tunneling current magnitude, so that lower applied charging voltages will still result in tunneling. The 14 V charging voltage was found to consistently result in maximum charge transfer into or out of the SiN layer.
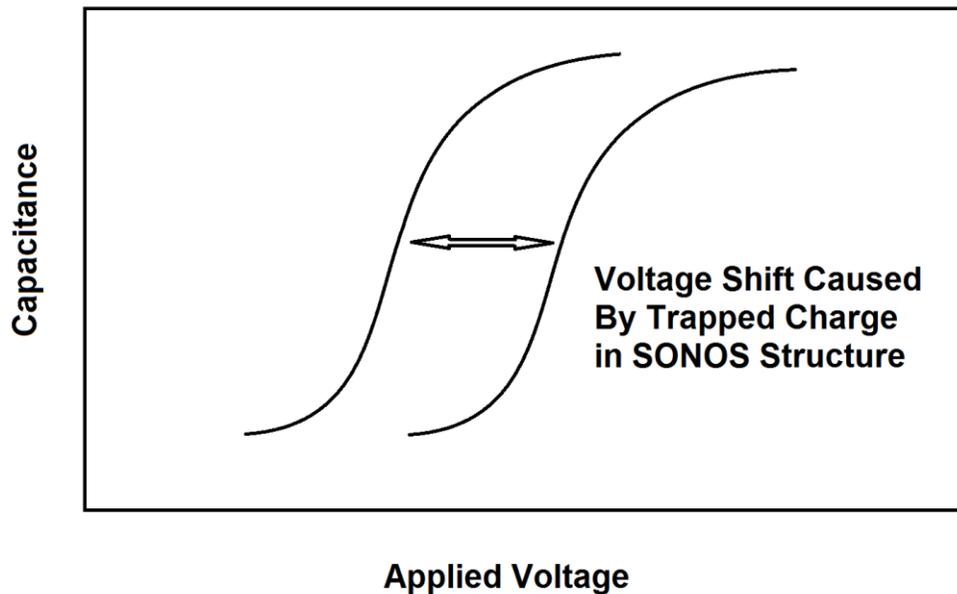
Figure 4-1.   Capacitance-Voltage Scan Illustration.
Charging voltages (positive and negative 14 volts) will allow for tunneling of
electrons or holes into or out of the charge storage layer. Charge in this layer will
shift the C-V characteristics of the device.

4.2.2   Transistor Measurement

The transistor characteristics were measured using an HP 6242 Semiconductor

Parameter Analyser. The output and transfer characteristics were examined. The

applied gate voltages and source drain voltages varied depending on the exact

transistor examined.

4.3   SONOS Parallel Plate Capacitors

TEM was conducted on a representative parallel plate capacitor sample to confirm the

existence of the separate SONOS layers and to verify the approximate layer

thicknesses. The TEM image of a calibration device is shown in Figure 4-2 below.

Here the target layers can be identified (30 nm amorphous silicon, 2 nm SiO_2, 5 nm

SiN, 1.5 nm SiO_2).
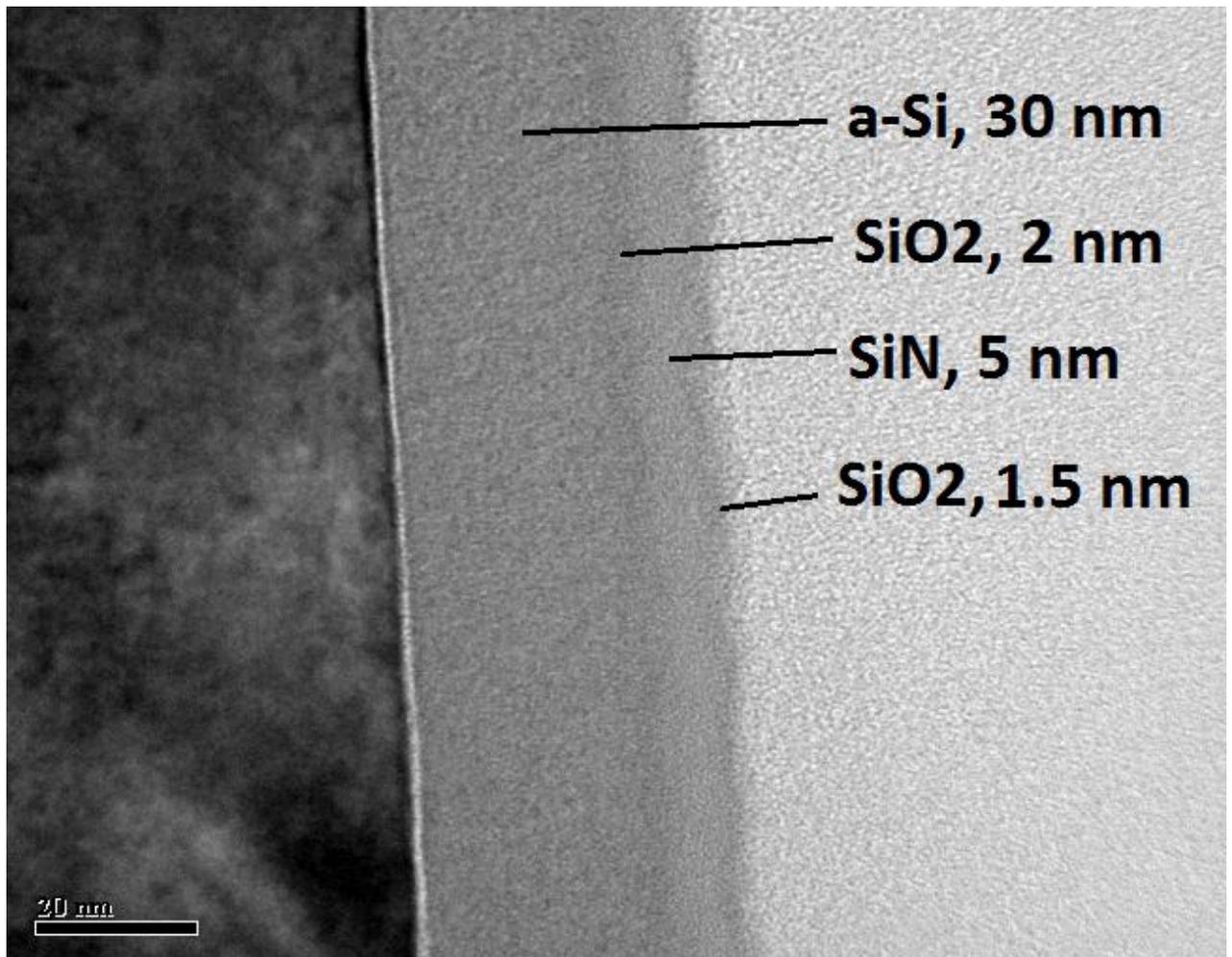
Figure 4-2: Transmission Electron Microscopy Image of SONOS Gate. Shown is a device with the structure (from left to right); crystalline silicon substrate, amorphous silicon (30 nm), silicon dioxide (2 nm), silicon nitride (5 nm), silicon dioxide (1.5 nm).

In addition, as shown in Figure 4-3, an Energy-dispersive X-ray spectroscopy (EDS) scan was performed. In this case, the oxygen content of the layers is shown as a function of depth. This scan also supports the existence of a distinct structure of SiO_2, SiN and SiO_2 as indicated by the dip in oxygen content at the expected depth of the SiN film.
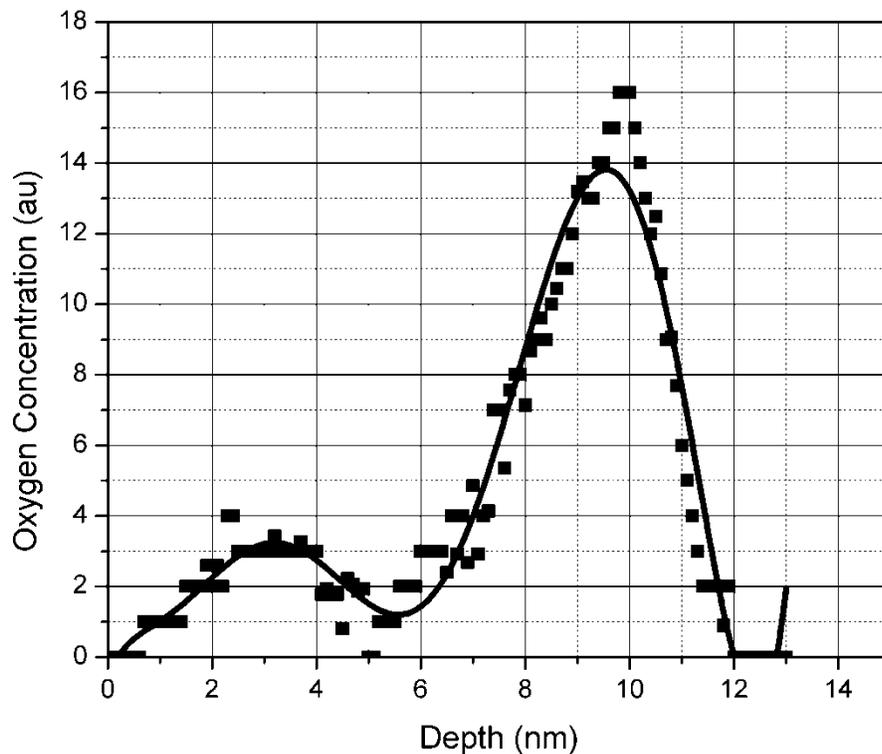
Figure 4-3:   Energy-Dispersive X-ray Spectroscopy Scan of the Oxygen Content of a Calibration Sample.
The scan shows (from left to right), an oxide layer to a depth of 4 nm, a low oxygen content layer from 4 nm to 6 nm, an oxide layer from 6 nm to 10 nm, and a low oxygen content layer from 10 nm. This corresponds to a structure grown as; 4 nm silicon dioxide, 2 nm silicon nitride, 4 nm silicon dioxide, on a crystalline silicon substrate.

The C-V results are separated into sections covering the behaviour of each of the 4 types of SONOS capacitors fabricated; crystalline silicon, amorphous silicon, AlQ3, and CuPc. A zinc oxide control sample is also included. The crystalline and amorphous silicon device behaviour is consistent with previous work on SONOS structures [61-82]. It must be noted that the measurements of high impedance transistor gate structures using this meter will be affected by the high RC time constants. The low mobility of the carriers in the organic materials will reduce the response time of carriers making high frequency capacitance measurements unstable in devices that are not parallel plates (such as making CV measurements on standard transistors). Lower frequency CV measurements could be conducted on other structures. This variation in behaviour can be seen in literature analysis of standard TFT gate capacitance.

4.3.1 Crystalline Silicon Capacitors

The CV characteristics of the crystalline silicon control sample (30 nm blocking oxide only) is shown in Figure 4-4 below and are compared to scans of a device with a 1 nm thick tunneling layer in Figure 4-5. Here the CV scans are shown before and after an applied bias charge of +-14 V. There is negligible shift/hysteresis in these control device scans, supporting the conclusion that the effects of interface state charging and oxide charges are minimal and will not result in the large shifts that will be observed in SONOS devices. The majority carrier density was found through a least squares curve fit to be 2×10^{19} cm^{-3} and is consistent with the expected density.

Figure 4-5 shows the CV scans of a 1 nm tunneling oxide SONOS device. The maximum shift in effective voltage due to charging of the SONOS device is approximately 3.5 volts. This is shown in the variation in the CV curves when the device was subjected to first a -14 volt charging voltage and then scanned to + 1V. Then the device was subjected to a +14 volt charging voltage and scanned from -6 Volts to +1 V. The devices were also examined for possible low voltage hysteresis. This was accomplished as follows. For the -14V charge behaviour, the device was scanned from -14 volts to 1 volt. This was repeated and the scans are shown as Neg 1 and Neg 2 in Figure 4-5. The device was then subjected to a +14 volt charging voltage and then scanned from -6 volts to +14 V. The scans are shown in Figure 4-5 as Pos 1 and Pos 2. No measureable shift in the threshold voltage was observed for this low voltage biasing. The control sample as shown in Figure 4-4 is included for reference.

The CV curves for the 2 nm device in Figure 4-6 illustrates the effect of varying the charging voltage from –8 V to +14 V. This supports the results of previous work [66, 71] that indicates that the threshold shifts can be controlled through variations in the applied charging bias voltages.

These CV characteristics of the crystalline SONOS parallel plate capacitors and control are consistent with results reported in the literature [85-87] and support the conclusion that the SONOS structure acts as a tunneling charge trap. This is evident in the voltage shift of the CV behaviour. When the charging voltage is reversed, the CV voltage shift is reversed. When low voltages are applied (below +/-14V), little to no

hysteresis is observed, suggesting that significant tunneling through the thin oxide

layer occurs only with high applied voltages.
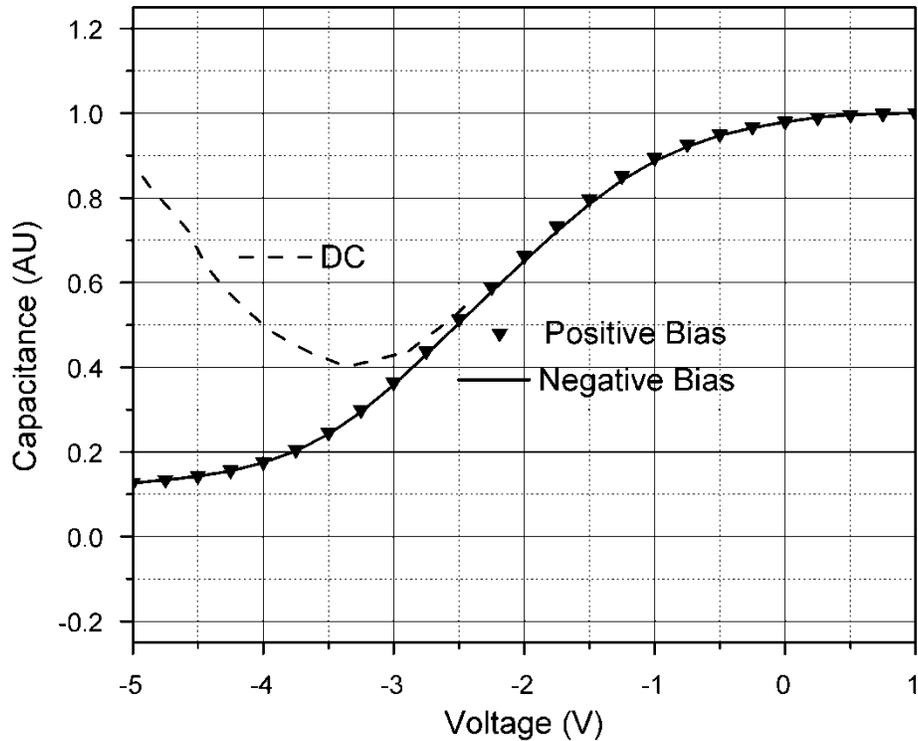
Figure 4-4: **CV Characteristics of a Crystalline Silicon Control Sample with DC,**
Scan After positive 14 V charging voltage, scan after negative 14 V charging
voltage.
The positive and negative scans are almost identical, indicating that no significant
charge storage occurs.
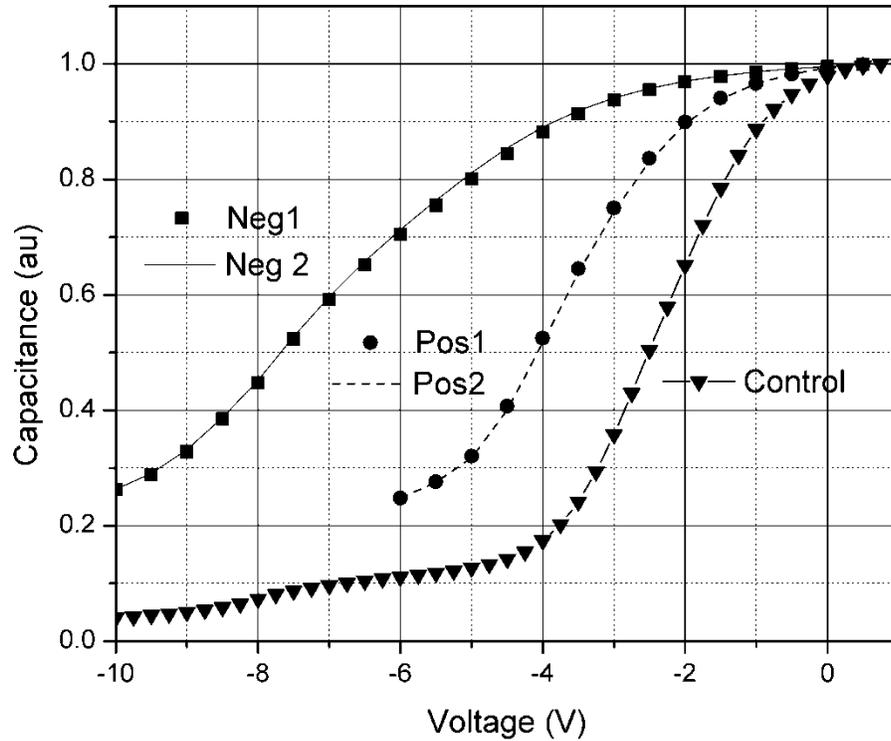
Figure 4-5:   CV Characteristics of a Crystalline Silicon Sample with 1 nm Tunneling Oxide Layer.
Includes: 2 sample scans after 14 V negative charging bias, 2 sample scans after 14 V positive charging bias, comparison to control scan.
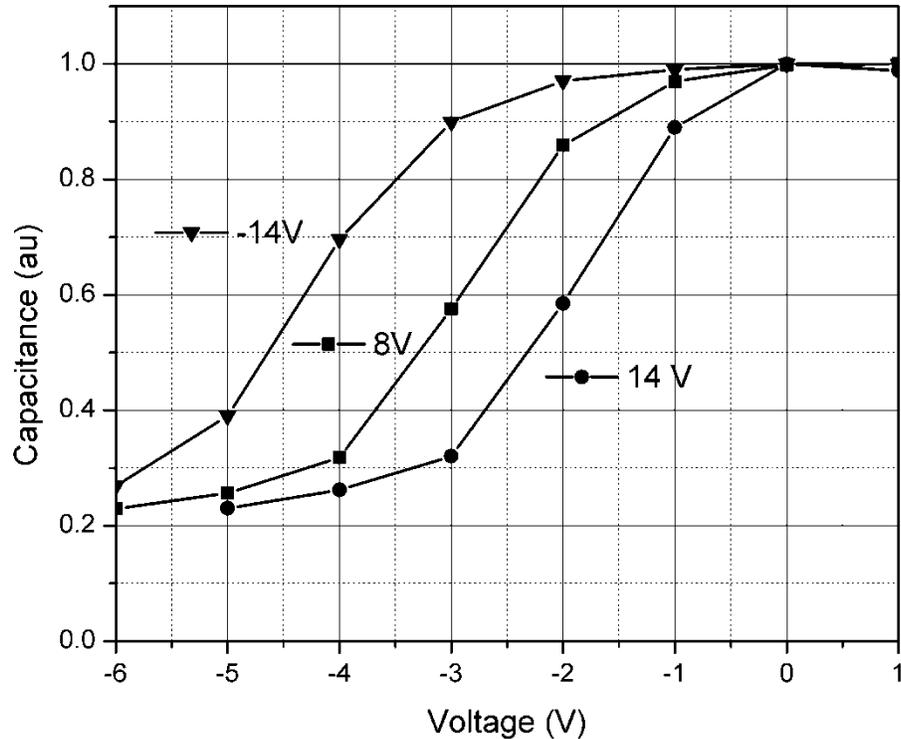
Figure 4-6: CV Characteristics of a Crystalline Silicon Sample with 2nm Tunneling Oxide Layer.
Scans after 14 V negative charging bias, 8 V negative charging bias, and 14 V positive charging bias. The C-V characteristics shift along the horizontal axis as a result of the charge trapped in the silicon nitride layer. The shifts are reversible.

4.3.2 Amorphous Silicon

The CV curves for the amorphous silicon control device are shown in Figure 4-7. As with the crystalline Si control device, there is negligible hysteresis between curves after the devices have been positively and negatively biased (at +14 V and − 14 V). Again, this suggests that there is little memory effect without the SONOS structure. Interface traps can from and will act to trap charge. These traps could result in hysteresis. The lack of any significant shift in the C-V curves suggests that interface

43

states will not produce the large shifts in behavior expected with the amorphous SONOS devices.

The shift in threshold voltage for the 1 nm *a*-Si:H device is shown in Figure 4-8. The device was subjected to a -14 volt charging voltage and then scanned from -14 volts to + 14 volts. The device was then scanned from zero to + 14 volts. The average shift in voltage behaviour is approximately 3 volts as seen between the curves when comparing the CV characteristics of the device having applied voltages of -14V to the device after an applied charging voltage of +14V. (There is a shift in the position of the C-V curves along the horizontal axis by 3 volts when measured at the 0.9 normalized capacitance points of the two curves). The hysteresis in the devices was examined by the following method. The device was subject to a negative 14 V bias and then scanned to positive 14V. The device was then reset and scanned from -14 V to + 14V. This is shown as the scans Neg 1 and Neg 2, in Figure 4-8. Then the device was subject to a positive applied voltage of +14 V. The devices were then scanned from zero to + 14V. This scan was then repeated. This is shown as the scans Pos 1 and Pos 2, in Figure 4-8. There is little observed shift as shown by the minimal variation in the first and second curves for each of the scan sets (Positive and negative charging voltages). There is a shift to the right of all of the curves with respect to the crystalline silicon devices (Figures 4-4 to 4-6). This shift is likely a result of the internal trapped charge in the amorphous Si layer. The devices also exhibit metastability when subjected to large applied voltages (above 30 V). (Metastability is a shift in the

threshold voltage caused by changes in the amount of trapped charge in the a-Si

caused by breaking and re-forming of bonds under high applied fields.)
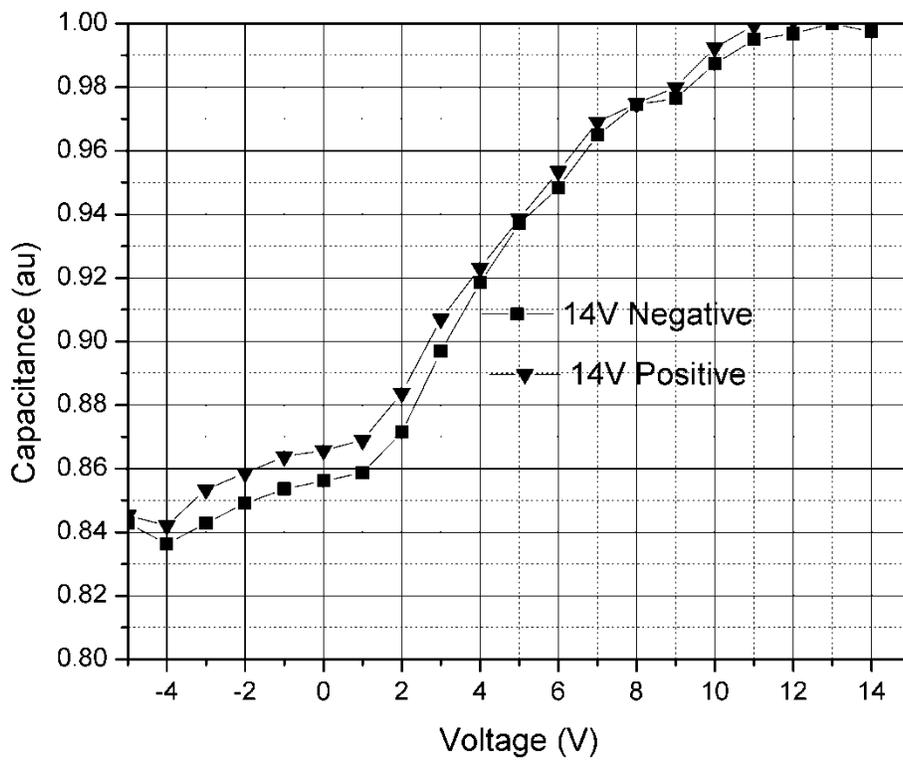
**Figure 4-7:   CV Characteristics of an Amorphous Silicon Control Sample.
Scans were obtained after 14 V negative charging voltage and after 14 V positive
charging voltage. There is little shift in the C-V characteristics along the
horizontal axis. This suggests that the SONOS structures are required to induce
the large shifts expected.**
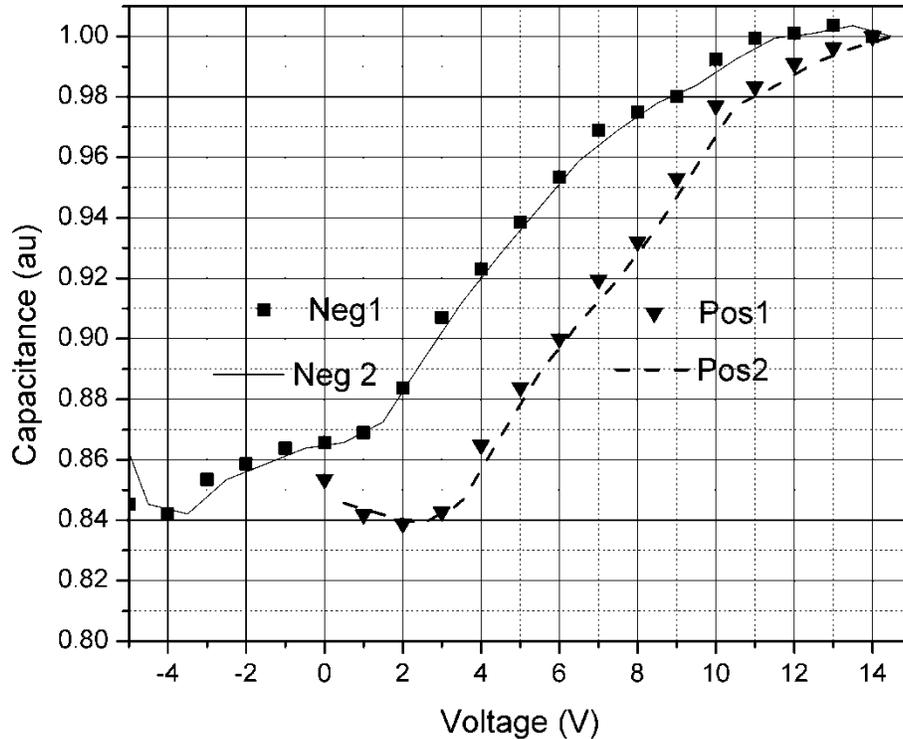
Figure 4-8: CV Characteristics of an Amorphous Silicon Sample with 1 nm thick Tunneling Oxide.
Two scans were taken after 14 V negative charging bias, and 2 scans after 14 V positive charging bias.

The CV characteristics of the 2 nm device are shown in Figure 4-9. Here, the shift in the curve is approximately 1.5 V (when measured at the 0.9 point of normalized capacitance), smaller than for the 1 nm devices due to the thicker tunneling oxide layer. Little hysteresis is evident when the scans are repeated after reversing the charge voltage. As previously noted, significant internal negative charge was observed in the a-Si layer. Significant parasitic capacitance was also observed through the high minimum capacitance observed in the inversion regime, a ratio of 0.85 compared to 0.20 for the silicon devices. This is likely due to the thin film nature of the devices,

which does not allow for the full depletion/inversion depth. The amorphous silicon semiconductor is only 300 nm thick as compared to a calculated penetration depth of 900 nm.
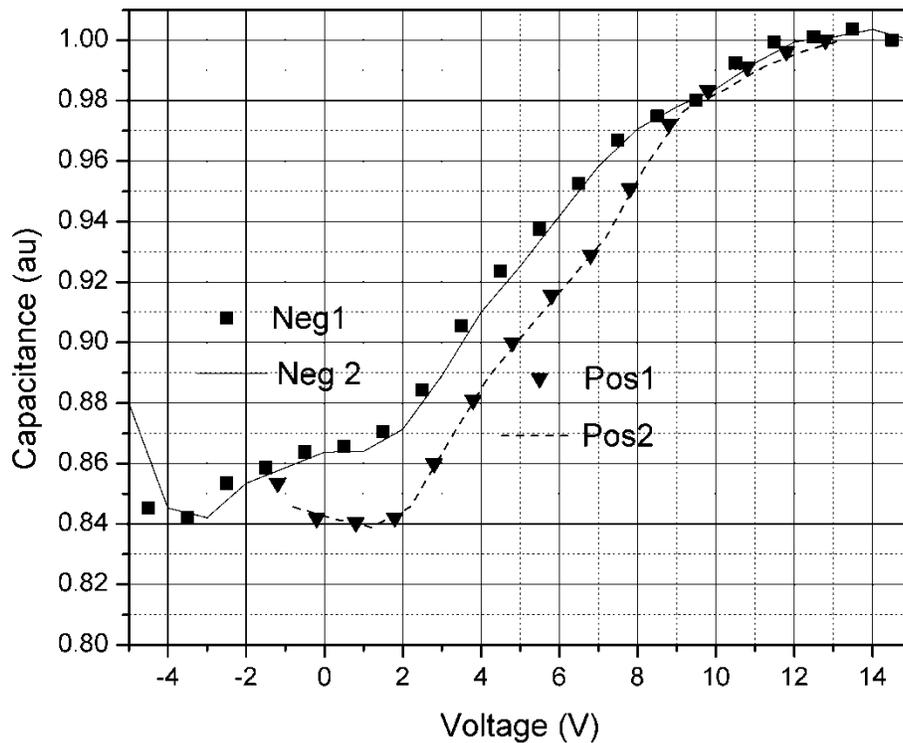
Figure 4-9:   CV Characteristics of an Amorphous Silicon Sample with 2 nm thick Tunneling Oxide.
Two scans were taken after 14 V negative charging bias, and 2 scans after 14 V positive charging voltage.

4.3.3   Alq3

The CV characteristics for the organic (Alq3) capacitor control device are shown in Figure 4-10. As with the other control devices, no significant shift in the curves is observed for applied charging voltages of ± 14 V. The results for the 1 nm tunneling

oxide organic device are shown in Figure 4-11. Here there is a clear average shift in the voltage behaviour of approximately 3.1 volts (at the 0.9 normalized capacitance points) between the two applied charging voltages of ± 14 V. The curve for the 2 nm Alq3 device is shown in Figure 4-12. Here the shift is approximately 1.8 volts. As with the amorphous Si devices, significant parasitic capacitance and internal fields were observed. Some hysteresis is observed as indicated by the dashed lines.
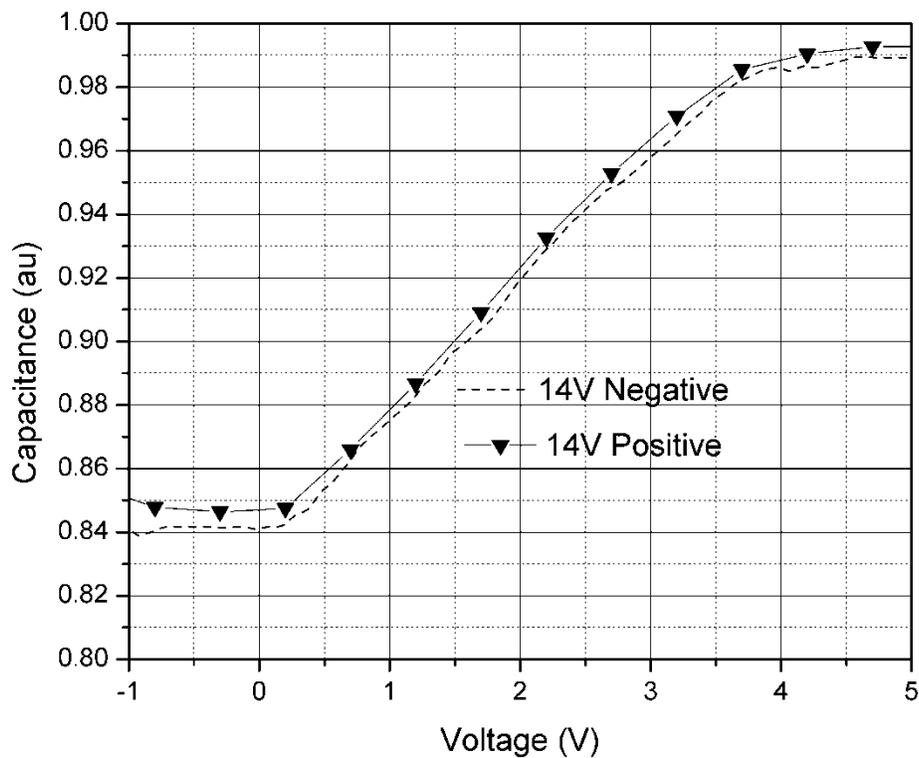
Figure 4-10: Alq3 Parallel Plate Capacitor Control Sample.
The solid line is the scan after a +14 volt applied voltage and the dashed line is the CV scan after a -14 volt applied voltage.
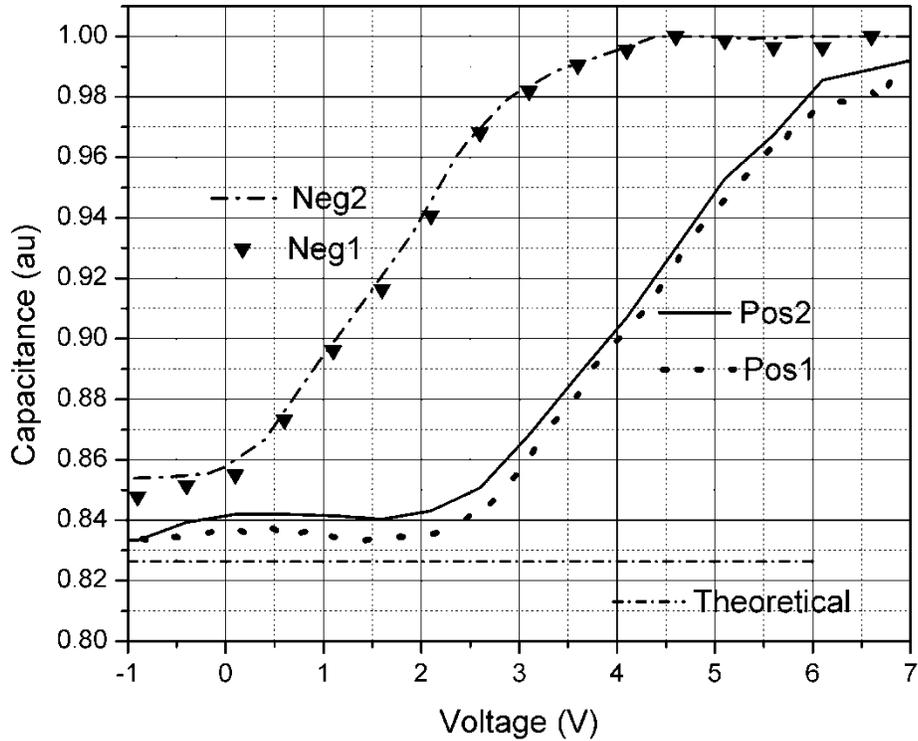
Figure 4-11: CV Characteristics of an Alq3 Sample with a 1 nm thick Tunneling Oxide Layer.
Two scans were taken after 14 V negative charging bias, 2 scans after 14 V positive charging voltage. Also shown is the theoretical minimum (dashed line) based on MOS capacitor characteristics. This theoretical minimum is defined as the point at which the depletion region extends all the way to the bottom of the AlQ3 layer (100 nm thick) to the interface with the bottom metal contact.

Figure 4-12: CV Characteristics of an Alq3 Device with a 2 nm thick Tunneling Oxide.
Two scans were taken after 14 V negative charging bias, and 2 scans after 14 V positive charging voltage.

The energy diagram for the SiN/Oxide/Alq3 system is shown in Figure 4-13. The lowest unoccupied molecular orbital (LUMO) level of the Alq3 (3.4 eV) is 1.3 eV below the conduction band of the SiN (2.1 eV). There is also a 1.0 eV separation between the Alq3 highest occupied molecular orbital (HOMO) level (6.2 eV) and the valence band of the SiN (7.2 eV). The applied charging voltage was varied from +/- 5V up to +/- 14 Volts. No charging/discharging of the SiN layer was observed for voltages below +/- 6V. The range of 6 to 14 volts corresponds to a V_{ox} across the

tunneling oxide of 230 to 540 meV. Based on this V_{ox} range, tunneling is likely into interfacial traps 500 meV below the SiN conduction band rather than directly into the SiN conduction band itself. Furthermore, the maximum entrapped charge in the SiN layer was found to be on the order of 0.1 C/m^2 (approximately 78 nC for the device shown). This was calculated using a simple capacitor model with the measured applied voltage shift of 3.1 V resulting from the charge imbedded in the SiN charge storage layer, and $Q = V/C$, where Q is the charge, V the voltage, and C the capacitance. At an effective V_{ox} of 540 meV, the theoretical maximum tunneling current density is on the order of 150 $\mu A/cm^2$, indicating that a 1 μm^2 TFT device has a charging time on the order of 1 ns.
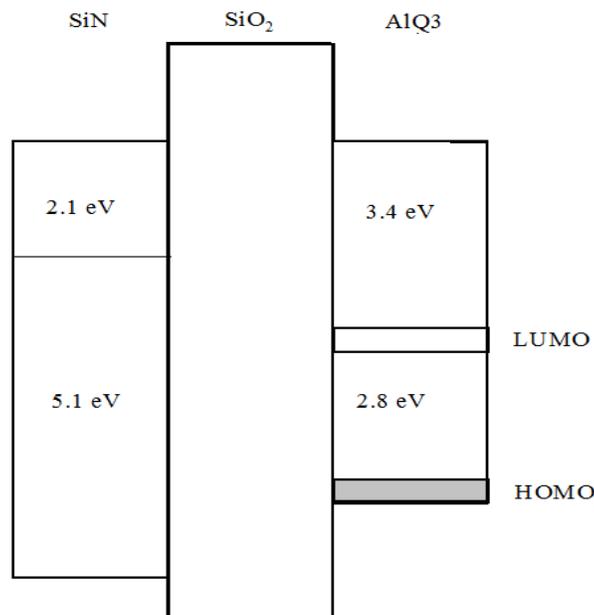
Figure 4-13: Energy Band Diagram for SiN-SiO$_2$-AlQ3 Structure.

The following series of figures (Figures 4-14 to 4-17) show FESEM images of the interface between an underlying oxide layer and a 200 nm Alq3 layer. The Alq3 was deposited on top of the oxide layer. This examination was conducted to investigate the possible presence of an interface zone between these two layers. From the images, no interface zone can be seen and the Alq3 appears to be amorphous throughout. This is consistent with the observed CV characteristics of the control parallel plate Alq3 capacitors shown in Figure 4-10 and also with literature reports [99] that indicate that a dipole region forms only when the organics are deposited on top of a metal layer.
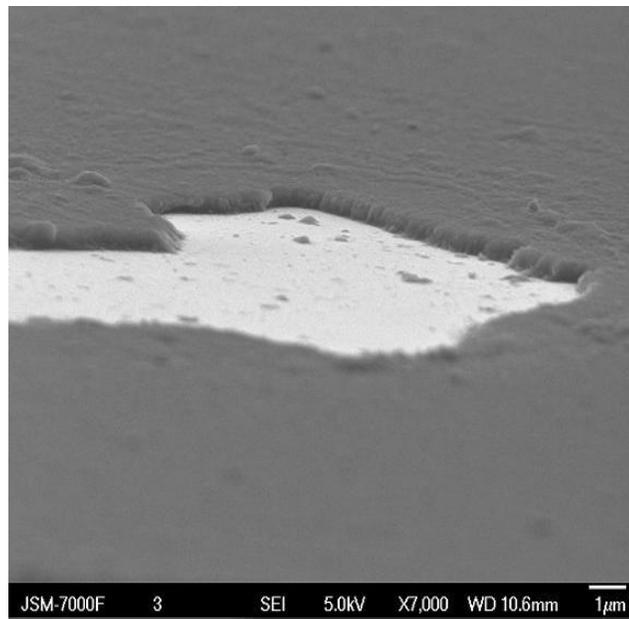
Figure 4-14: FESEM Image of Alq3 Deposited on SiN (x 7,000)
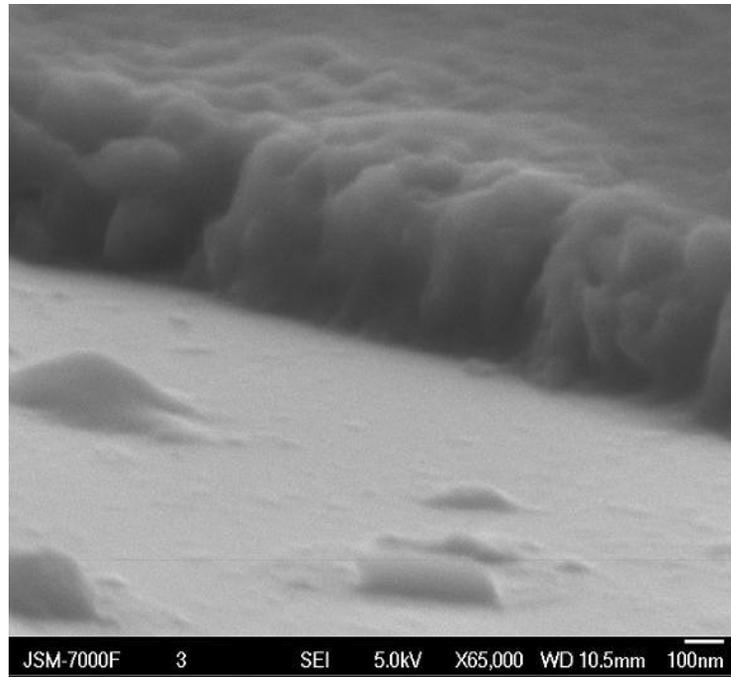
Figure 4-15: FESEM Image of Alq3 Deposited on SiN (x 65,000)
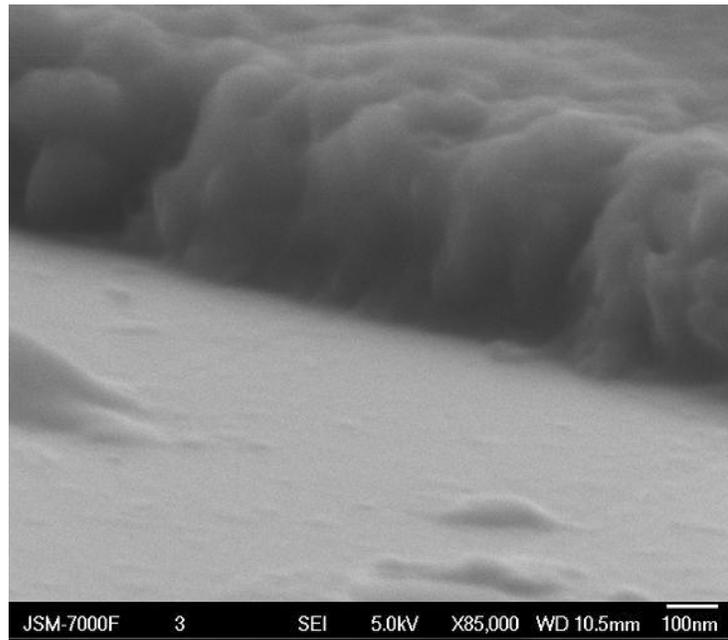
Figure 4-16: FESEM Image of Alq3 Deposited on SiN (x 85,000)
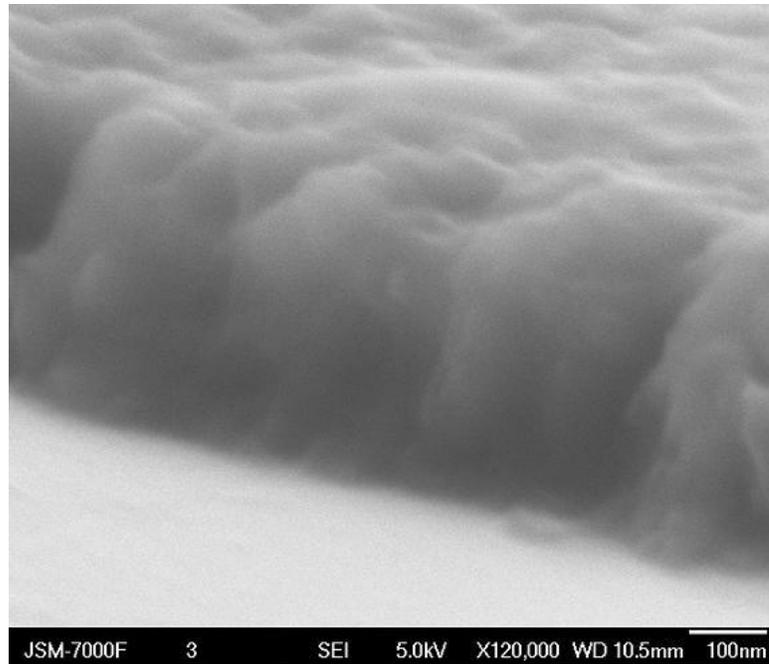
Figure 4-17: FESEM Image of Alq3 Deposited on SiN. (x 120,000)

The results of the capacitance-voltage measurements of the Alq3 parallel plate semiconductor capacitors demonstrate that Alq3 acts like a semiconductor material with minority and majority carriers. The SONOS devices also exhibit the same charge and discharge behaviour as shown in the silicon SONOS capacitors. This suggests that carriers are tunneling from the Alq3, through the thin tunnel oxide and into the silicon nitride layer.

4.3.4   CuPc

The CV characteristics for the organic (CuPc) capacitor control device are shown in Figure 2-18. As with the other control devices, no significant shift in the curves is observed for applied charging voltages of $\pm$ 14 V. The results for the 1 nm tunneling

oxide CuPc device are shown in Figure 4-19. Here there is a clear average shift in the

capacitance-voltage behaviour of approximately 4.6 volts (between the 0.9 normalized

capacitance points) between applied charging voltages of ± 14 V. The curve for the 2

nm CuPc device is shown in Figure 4-20. Here the shift is approximately 1.6 volts.
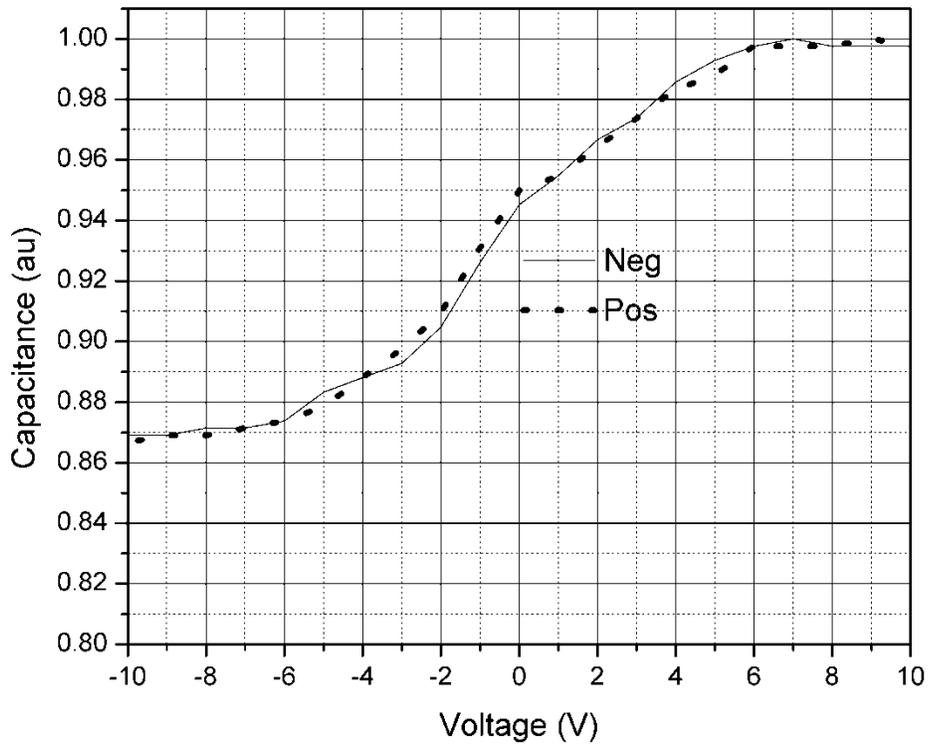
Figure 4-18: CV Characteristics of a CuPc Thin Film Parallel Plate Capacitor Control Sample (device without SONOS structure).
There is little observed hysteresis indicating that the SONOS structure is required for the large expected shifts.
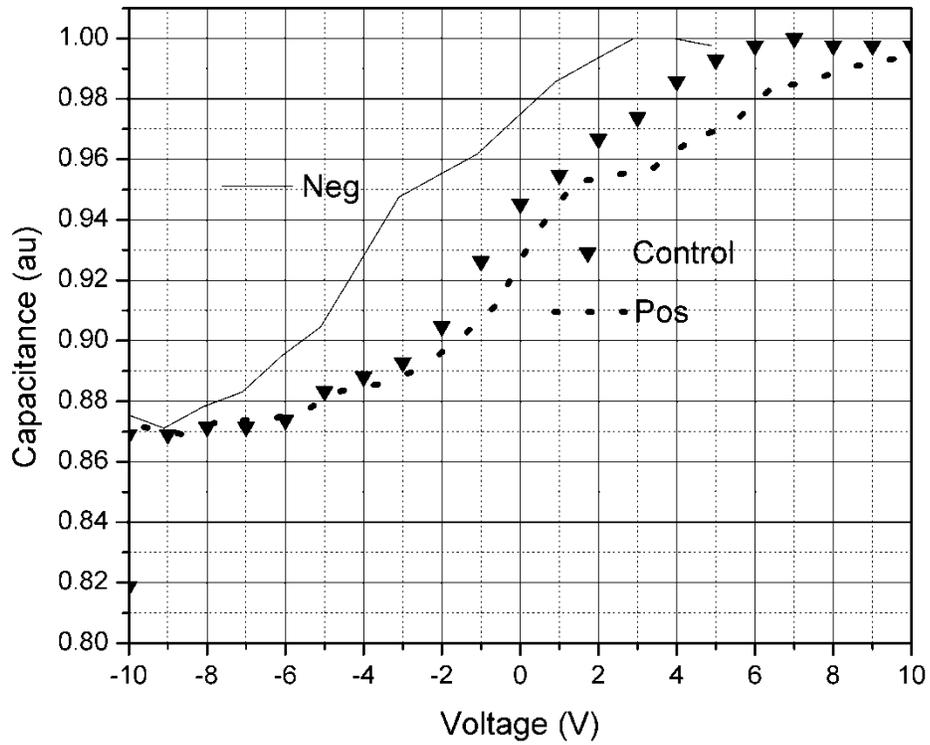
Figure 4-19: CV Characteristics of a CuPc Sample with 1 nm thick Tunneling Oxide.
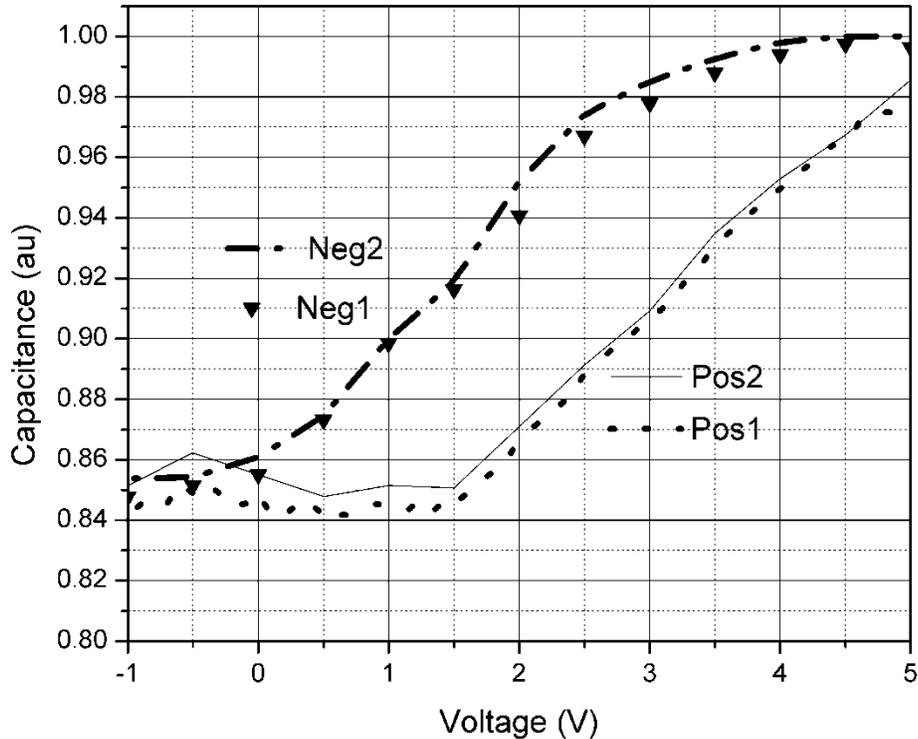**Scans are shown after 14 V negative charging bias and 14 V positive charging voltage, compared to a control sample.**
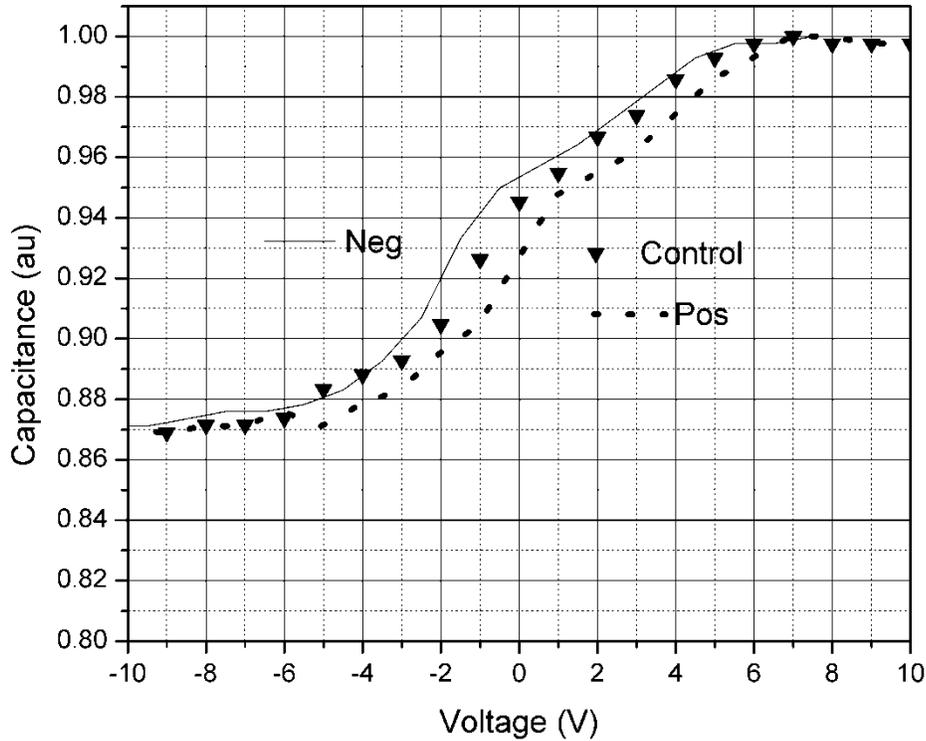
Figure 4-20: CV Characteristics of a CuPc Device with a 2 nm thick Tunneling Oxide.
Scans are shown after 14 V negative charging bias and after 14 V positive charging voltage, compared to a control sample.

As with the Alq3 devices, the results of the capacitance-voltage measurements of the CuPc parallel plate semiconductor capacitors demonstrate that CuPc acts like a semiconductor material with minority and majority carriers. The SONOS devices also exhibit the same charge and discharge behaviour as shown in the silicon SONOS capacitors. This suggests that carriers are tunneling from the CuPc layer, through the thin tunnel oxide and into the silicon nitride layer.

4.3.5   ZnO

ZnO devices have been tested as indicated in Figure 4-21. A scan of a control device is shown. There are significant shifts in the curves after positive and negative charging. In this case there is some interface or material effect that allows for charging at low applied voltages. This is in contrast to the control devices of crystalline silicon, amorphous silicon, Alq3 and CuPc. This is most likely a result of free charge in the form of mobile ions being present in the ZnO.
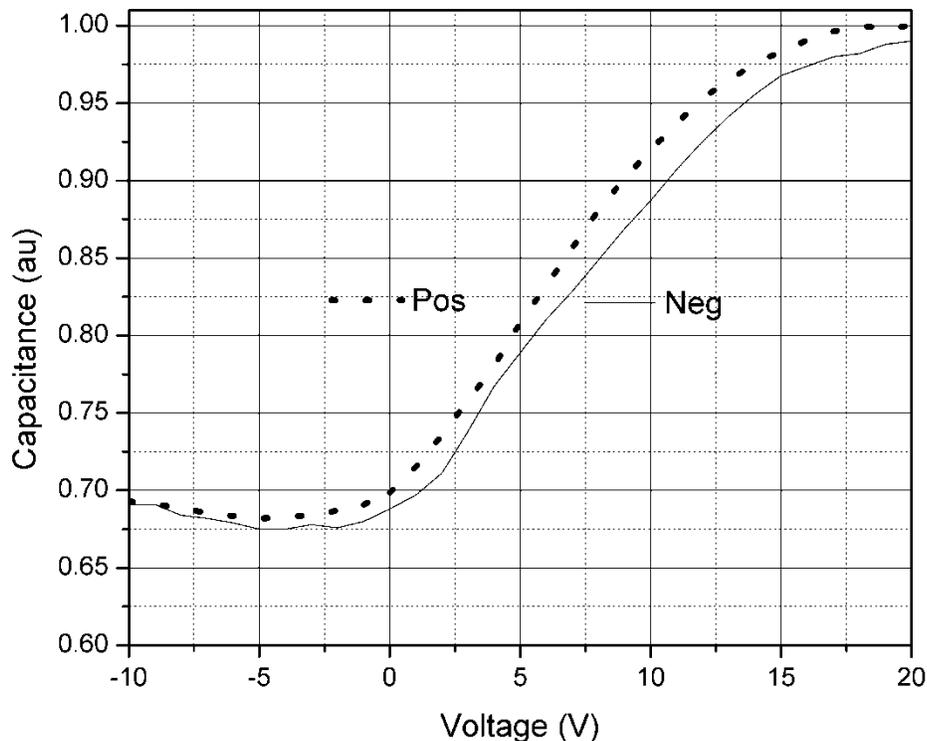
Figure 4-21: CV Characteristics of a ZnO MOS Capacitor.
Significant hysteresis is shown by the shift between the positive and negative charging cycle curves.
The shift is approximately 2 volts as measured at the 0.9 normalized capacitance point.

4.4   Thin Film Field Effect Transistors

The transistor characteristics were measured using an HP 6242 Semiconductor Parameter Analyser. The transfer and output characteristics are shown for Alq3, ZnO, and CuPc devices. Split gate and SONOS CuPc transistors are also shown. It should be noted that Alq3 and CuPc are not commonly used as semiconductor materials in thin film transistors. This is a result of the low mobility and low carrier density. The majority of research into organic transistors is focused on higher performance materials that will produce transistors with higher current carrying performance and higher on/off ratios. However, as will be shown in the modeling section, in the present case, the performance of these proof-of-concept devices is sufficient for the design of analog spiking circuit.

4.4.1   Alq3 Transistors

The output characteristics of the Alq3 control TFTs are shown in Figure 4-22. This is a single gate device with a single SiO_2 gate dielectric layer. The device shows low on/off characteristics; at 20 volts Vds, the current is 1 nA at a Vgs of -10 volts and drops to 0.2 nA at 0 volts Vgs. This is an on/off ratio of 5, or half an order of magnitude. The transfer characteristics are shown in Figure 4-23. For low voltage, and low current operation, the primary area of interest is in the linear regime (less than 10 volts) for gate voltages of –5V. In this particular device, there is a 'ledge' between +5 volts and -10 volts Vgs with a low slope and low on/off ratio. The Ids shifts from 0.1 nA to 0.9 nA over the 15 volt gate voltage shift. By comparison, the Ids shifts from .01 nA to 0.11 nA between +10 volts to + 5 volts. These initial results suggest that the Alq3

based transistor is suitable for low voltage analog neural circuits, which will be demonstrated is Chapter 5.
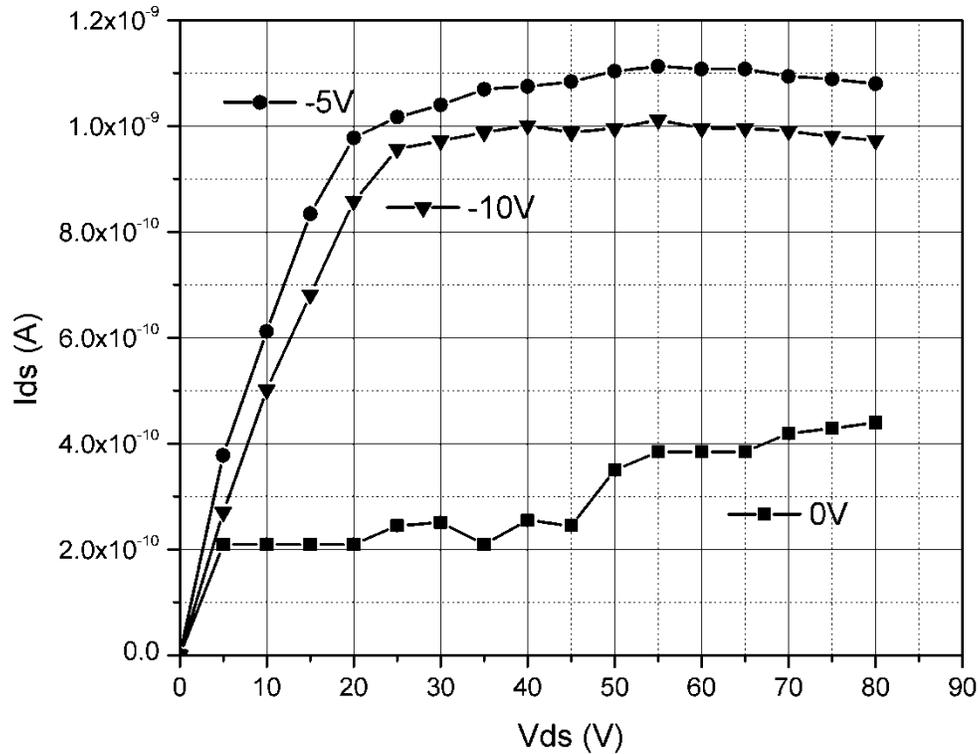
Figure 4-22: Output Characteristics of a p-type Alq3 transistor at V_{gs} = 0, 5, and 10 V.
The device shows low on/off characteristics; at 20 volts drain-source voltage (Vds), the drain source current (Ids) is 1 nA at a gate voltage (Vgs) of -10 volts and drops to 0.2 nA at 0 Vgs. This is an on/off ratio of 5, or half an order of magnitude.
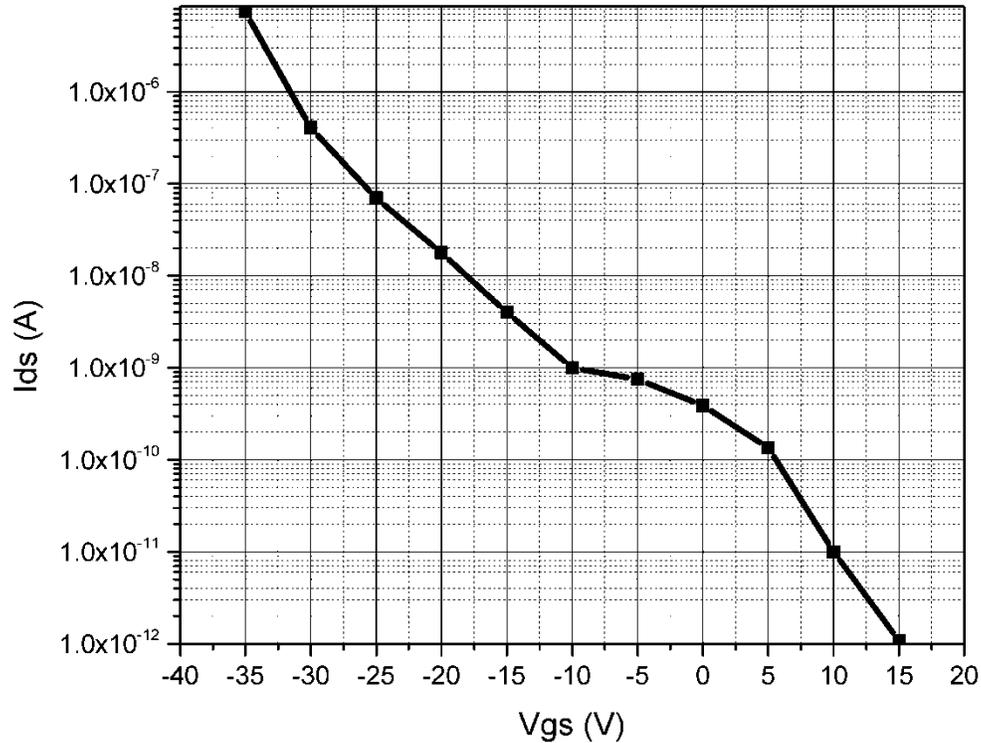
Figure 4-23: Transfer Characteristics of an Alq3 p-type TFT at Vds = 80 V. In this particular device, there is a 'ledge' between +5 volts and -10 volts Vgs with a low slope and low on/off ratio. The Ids shifts from 0.1 nA to 0.9 nA over the 15 volt gate voltage shift. By comparison, the Ids shifts from .01 nA to 0.11 nA between +10 volts to + 5 volts.

3.3.2   ZnO Transistors

The output characteristics of the control ZnO TFT are shown in Figure 4-24. At 30 V Vds, the drain-source (Ids) current is 20 uA at a gate voltage (Vgs) of 80 volts compared to 5 uA at 60 V Vgs. This represents an on/off ratio of 4.The transfer characteristics are shown in Figure 4-25. The slope of the Ids-Vgs curve is nearly

constant below 20 volts Vgs, with an approximate on/off ratio of 10 for every 10 volts Vgs.
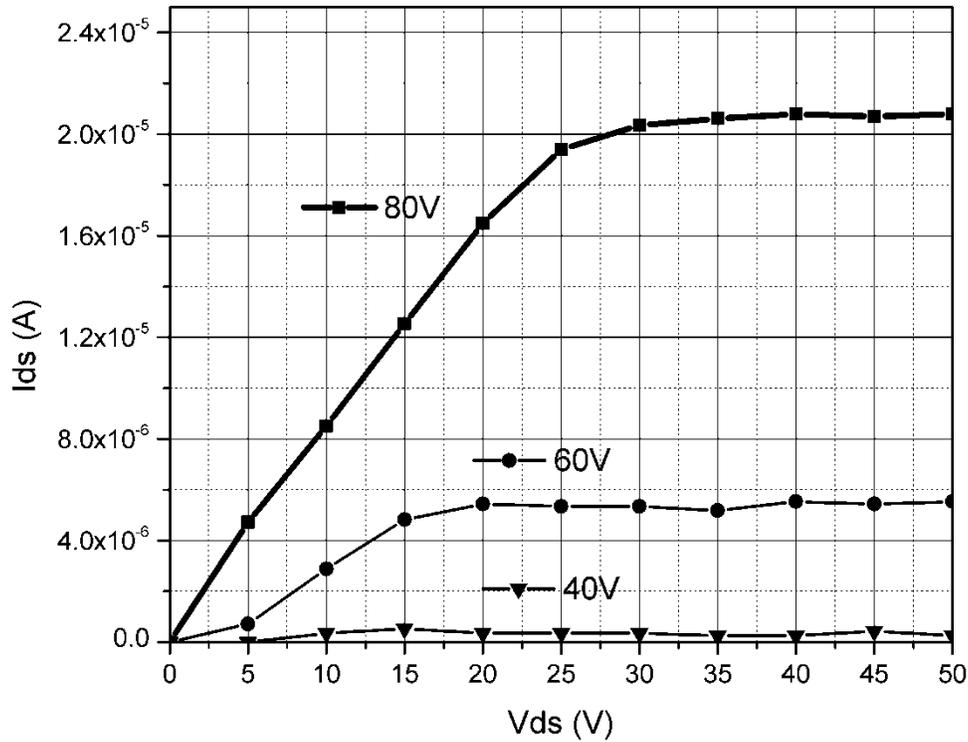
Figure 4-24: Output Characteristics of a ZnO n-type TFT at Vgs = 80, 60, and 40 V.
At 30 V Vds, the drain-source (Ids) current is 20 uA at a gate voltage (Vgs) of 80 volts compared to 5 uA at 60 V Vgs. This represents an on/off ratio of 4.
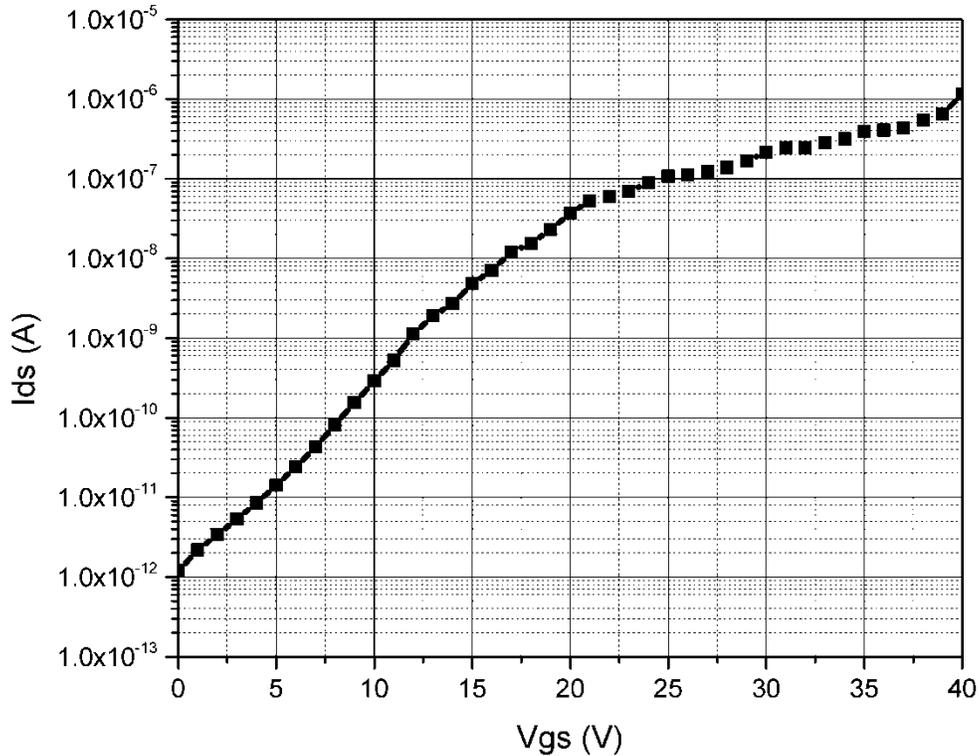
Figure 4-25: Transfer Characteristics of a ZnO n-type TFT at Vds = 40 V. Below 20 volts Vgs, the slope of the Ids-Vgs curve is nearly constant.

4.4.2   CuPc Single Gate Transistors

The output characteristics of the control n-type CuPc TFT are shown in Figure 4-26. At 25 volts drain source voltage (Vds), the drain source current (Ids) is 353 nA at a gate voltage (Vgs) of 10 volts. The Ids is 153 nA at 0 V Vgs. This is an on/off ratio of only 2.3. The transfer characteristics are shown in Figure 4-27. Between +10 volts and -10 volts Vgs, the drain-source current ranges from 340 nA to 140 nA. This is an on/off ratio of only 2.4. The output characteristics of the p-type CuPc TFT are shown in Figure 4-28. At 25 volts drain source voltage (Vds), the drain source current (Ids) is

25.2 nA at a gate voltage (Vgs) of -10 volts. The Ids is 10 nA at -5 V Vgs. This is an on/off ratio of only 2.5.The transfer characteristics are shown in Figure 4-29. Between -10 volts and 0 volts Vgs, the drain-source current ranges from 22 nA to 6.5 nA. An inflection point is observable at 10 volts Vgs. This is indicative of ambipolar behaviour as above 10 volts gate voltage, electrons (minority, negative carrier) begins to have an observable effect.
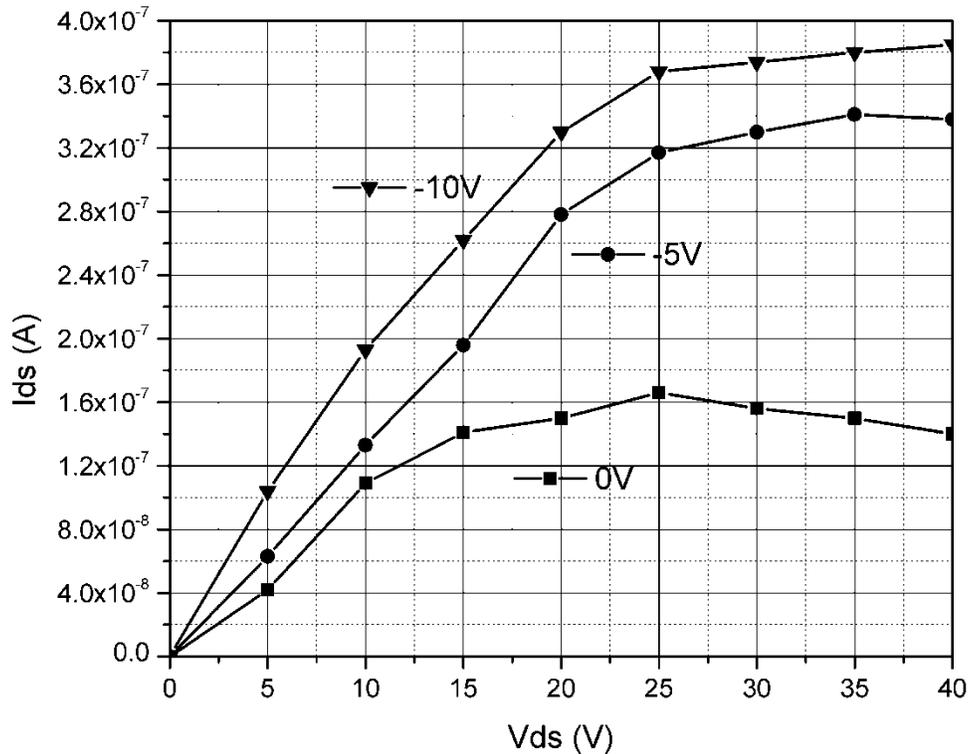
Figure 4-26: Output Characteristics of an n-type CuPc TFT at V_{gs} = 0, 5 and 10 V.
At 25 volts drain source voltage (Vds), the drain source current (Ids) is 353 nA at a gate voltage (Vgs) of 10 volts. The Ids is 153 nA at 0 V Vgs. This is an on/off ratio of only 2.3.
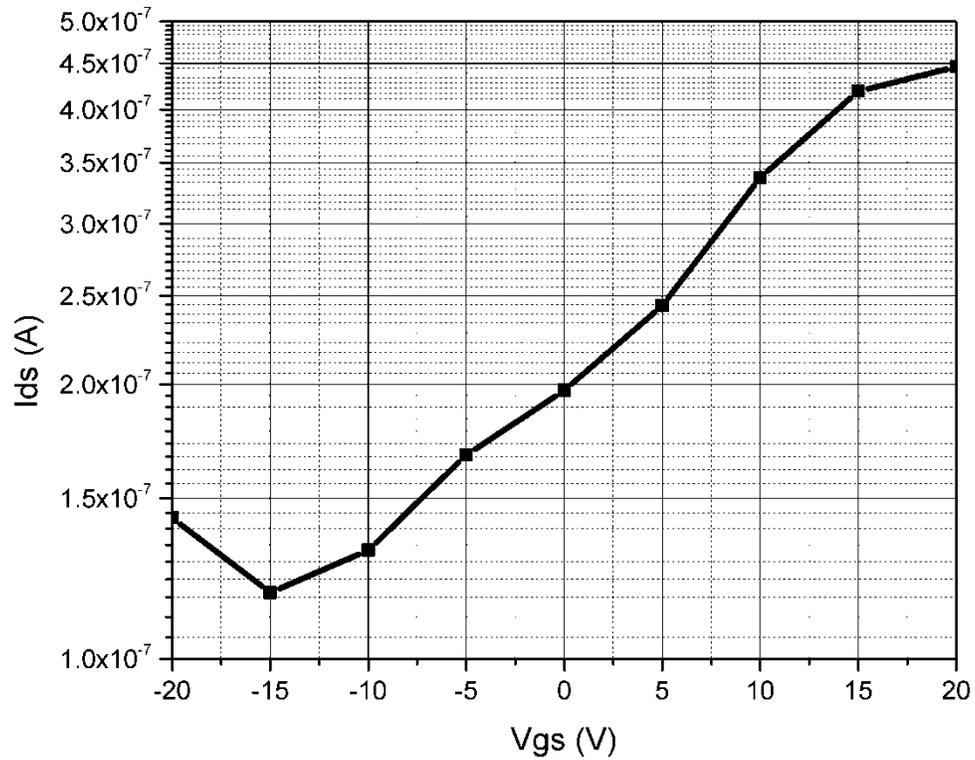
Figure 4-27: Transfer Characteristics of an n-type CuPc TFT at V_{ds} = 20 V. Between +10 volts and -10 volts Vgs, the drain-source current ranges from 340 nA to 140 nA.
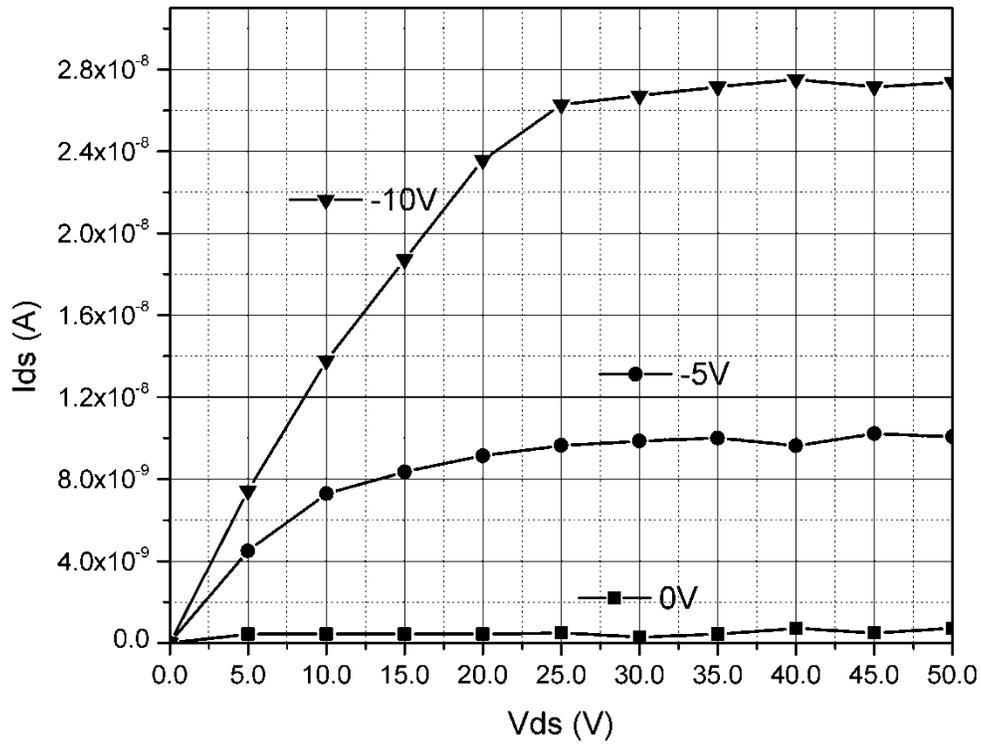
Figure 4-28: Output Characteristics of a p-type CuPc TFT at V_{gs} = 0, -5, and -10 Volts.
At 25 volts drain source voltage (Vds), the drain source current (Ids) is 25.2 nA at a gate voltage (Vgs) of -10 volts. The Ids is 10 nA at -5 V Vgs. This is an on/off ratio of only 2.5.
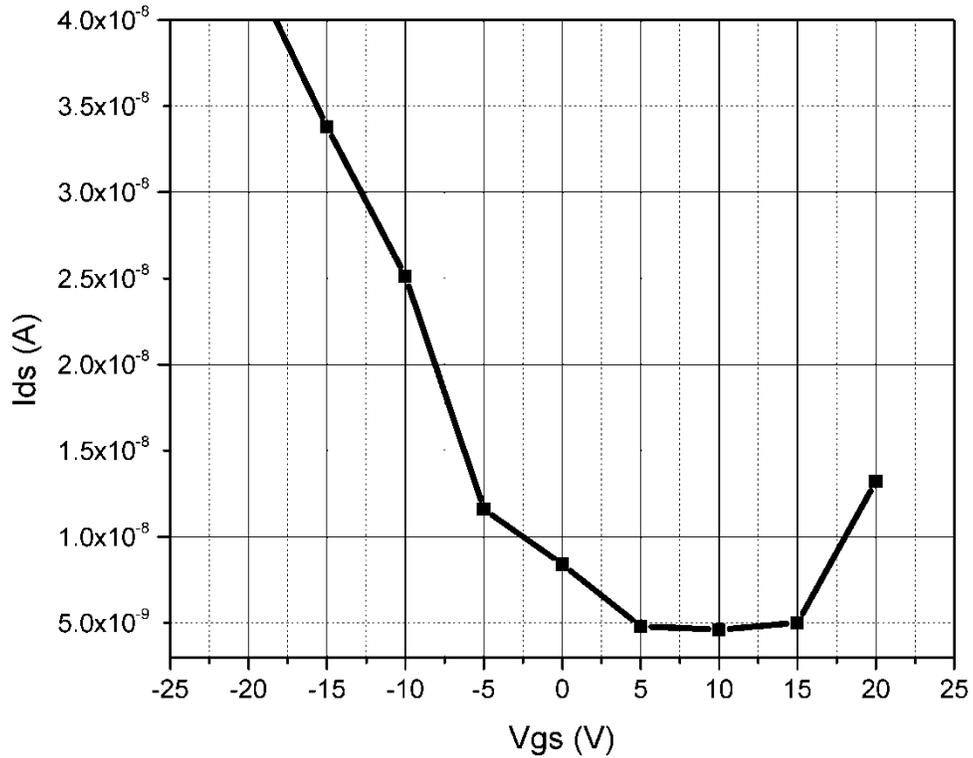
Figure 4-29: Transfer Characteristics of a p-type CuPc TFT at V_{ds} = 20 V. Between -10 volts and 0 volts Vgs, the drain-source current ranges from 22 nA to 6.5 nA.

4.4.3 Split Gate Transistors

The transfer characteristics of the split gate CuPc transistor is shown in Figure 4-30 below with V_{ds} at 20 V. The peak drain-source current of the device shown was measured at23 nA with both gates biased to -15 volts. This compares well to the single gate device produced and shown in Figure 4-29 which had a current of 22 nA at 20 V drain source voltage at a gate bias of -10 volts. This device requires further

optimization but the results are sufficient for the modeling which is reviewed in Chapter 5.
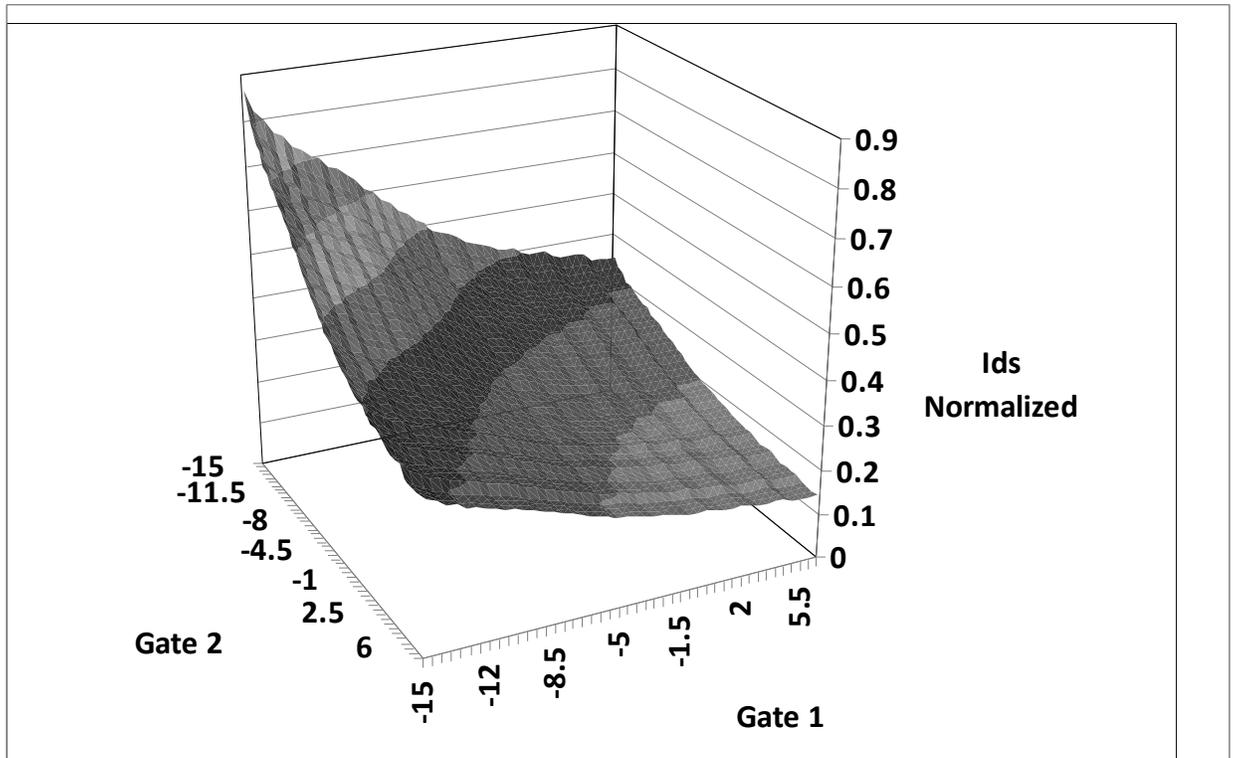
Figure 4-30: Split Gate Transfer Characteristics.
The normalized output current is shown, at 20 V, as a function of the Gate 1 and Gate 2 applied voltages. The peak current was found to be 23 nA at 20 Vds and with both gates biased at -15 volts.

4.4.4   SONOS TFTs

The transfer characteristics of a single gate TFT are shown in Figure 4-31 below before and after an applied gate voltage of + 14 and -14 V. The effective gate voltage is shifted by an average of 2.3 volts over the range shown, V_{gs} from 15 to –5 Volts. The shift between charging is the result of charge tunneling into and out of the SiN charge storage layer, effectively creating an imbedded memory in the transistor. In this

case, the effect on Ids is small due to the small on/off ratio inherent to the CuPc transistor. Looking at a vertical line at 10 volts Vgs, the shift is about 3×10^{-8} A, which is on the order of 14%.
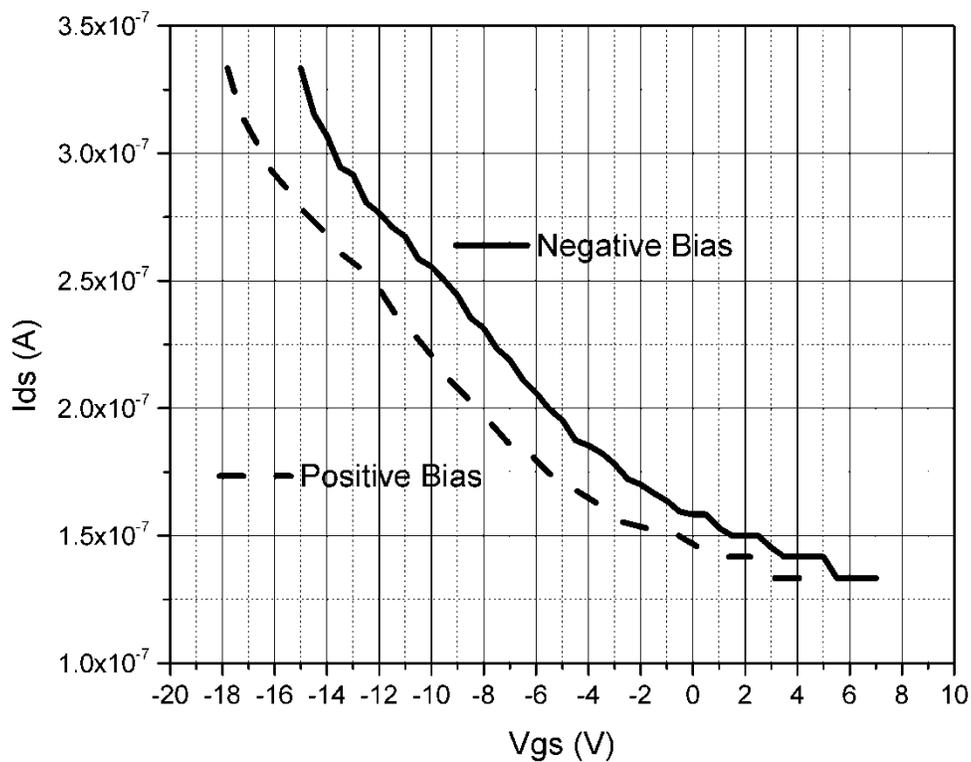
Figure 4-31: CuPc p-type SONOS FETFT Device Transfer Characteristics. Shown are the scans after a charging voltage of +14 volts and – 14 volts. The shift between charging is the result of chargetunneling into and out of the SiN charge storage layer, effectively creating an imbedded memory in the transistor. In this case, the effect on Ids is small due to the small on/off ratio inherent to the CuPc transistor. Looking at a vertical line at 10 volts, the shift is about 3 x 10 -8, which is on the order of 14%.

5   NEURAL SIMULATIONS

5.1   Introduction

This section gives the details on modeling of spiking analog neural circuits. The first stage was to reproduce a spiking circuit from literature. The circuit designed by van Schaik [20] was found to be a good starting point as it is a simple spiking circuit. Further modeling would develop the concepts identified by Indiveri [19] but the circuit is too complicated for initial analysis. This first circuit was developed (without the benefit of knowledge of component properties as these are not specified in the original work.) and was found to produce a spiking response to an input current. This procedure ensured that the base model used was working properly and would be an appropriate starting point for the development of a circuit using organic transistors with SONOS structures.

In the next step, the results of the characterization of the organic transistors, as covered in Chapter 4, were used to generate transistor models. These new transistor models were then used to replace the standard silicon transistors used in the literature models. This is significant as no previous work was identified that utilized organic transistors in this manner and is therefore a novel application of organic transistors. Lastly, the SONOS structures and the split gate transistors were used to further develop the spiking analog circuit model.

5.2 Base Spiking Model

The spiking analog circuit described by van Schaik [20] and shown in Figure 5-1 is used as a starting point to model a spiking circuit. The circuit used standard transistor properties. This circuit represents a single neuron and is an "integrate and fire" circuit. The current source, I1, represents a sum of synaptic currents. In a more detailed circuit model, the current source, I1, is replaced by many (100s to 1000s) of synaptic transistors. The response of each of these transistors will be similar to a synaptic weight.

In the circuit in Figure 5-1, the membrane potential (at C Mem) is compared (through circuit Q1, Q2, Q3, Q4) to a threshold voltage (V2) and sets a local output voltage, at Q3, to high or low. A following circuit (Q6 and Q5) inverts this voltage and drives a current (through Q10), that simulates a sodium current, that charges the membrane capacitor (C Mem). A second inverter (Q7, Q8) controls the current (through Q9) that discharges the membrane through a potassium-like current. This basic circuit has a variable threshold and a variable refractory period. A simulation of the membrane potential from this circuit is shown in Figure 5-2. Here, the general synaptic current is simulated by I1 which represents a resultant sum of synaptic currents. In the simulation shown in Figure 5-2, the input current is a broad, 1 second, 500 µA input current pulse. Here we can see a sloped charge of the membrane and then an abrupt spiking as the threshold voltage (at V2) is exceeded. This is caused by charging of the membrane with the current from Q10. This is followed by the quick activation of Q9 and the abrupt discharge of the membrane. The cycle then repeats as the input current

71

at I1 flows and the membrane recharges. Transistors Q12, Q 13, Q 14 and Q15 are current sources that control the current through the circuit and improve power efficiency.

In this version, the circuit is modeled with standard crystalline silicon MOSFETs which have fast response and low internal resistance. In designing and manufacturing a practical circuit, the manufacturing parameters of the transistors can be changed but the circuit performance can be realistically adjusted through changing the leakage resistance, R2, the membrane capacitance, C Mem, and the refractory capacitance, C2. The leakage resistance can be replaced by a transistor and varied dynamically. As previously mentioned, more complicated intrinsic properties can also be added (adaptation, frequency response, etc.) and have been modeled by Indiveri [19].
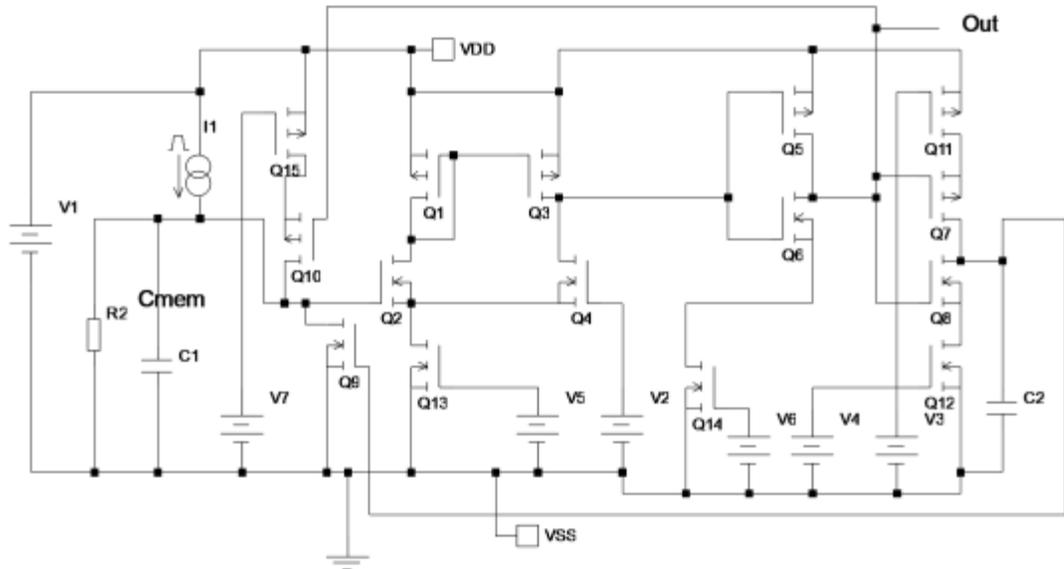
Figure 5-1: A van Schaik Circuit.
This is a basic circuit that models integrate and fire behaviour. The main composite synaptic input is represented by the current I1. The membrane capacitance is represented by C1 with R2 being the leakage resistance. The membrane capacitance is compared (comparator comprised of Q1, Q2, Q3, and Q4) to the voltage at V2. If the membrane potential exceeds the threshold voltage, V2, then Q10 turns on and the circuit spikes. Eventually Q9 turns on to discharge the membrane capacitance.
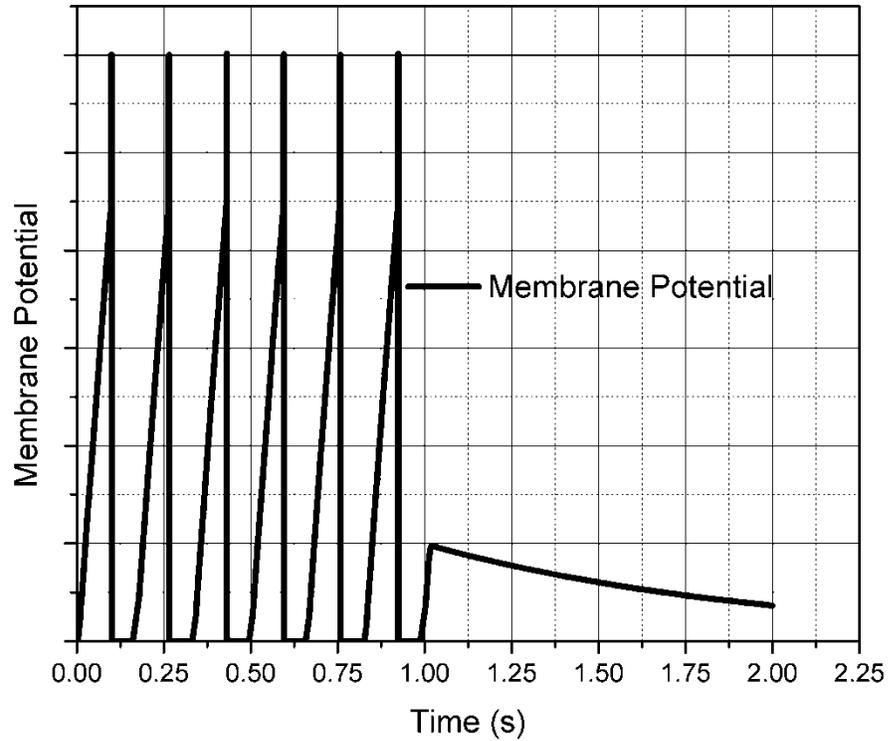
Figure 5-2:   Membrane Potential in Original van Schaik Circuit.
This is the output from the circuit shown in 5-1, with an input current at I1 of 500 µA for 1s. The circuit pulses until the input current stops and the membrane capacitance discharges. The spiking abrupt upward spike occurs as transistor Q10 turns on. The abrupt drop in membrane potential occurs when transitor Q9 turns on and discharges the membrane.

5.3   Organic Transistor Spiking Analog Neural Model

The first modification of the original van Schaik circuit is to reconfigure it to use

amorphous organic transistors with output and transfer characteristics that have been

extracted from real devices [100-103]. There is a large variation in amorphous

transistor characteristics depending on the design details. The gate length and width

can be varied and the selection of contact metals also has a significant effect on the

74

device performance. Proper selection of the semiconductor materials and contact metals can produce n or p-type MOSFETs. These transistors are typically fabricated to operate in the accumulation region. The transistors are n or p-type in the desired operating gate voltage range as a result of the band alignment between the organic semiconductor and the contact metal. CuPc has been shown to have reasonable current characteristics for both n and p-type devices in the desired gate voltage range (below 10 volts). Pentacene based devices are commonly studied and optimized due to the relatively high current control characteristics. However, the performance of CuPc transistors is sufficient for spiking analog neural circuits. Representative transfer characteristics are shown in Figure 5-3 and represent the TFTs that were used for the modeling in this paper. As shown, these devices have extremely low current carrying characteristics. Representative output characteristics of an n-type device are shown in Figure 5-4.
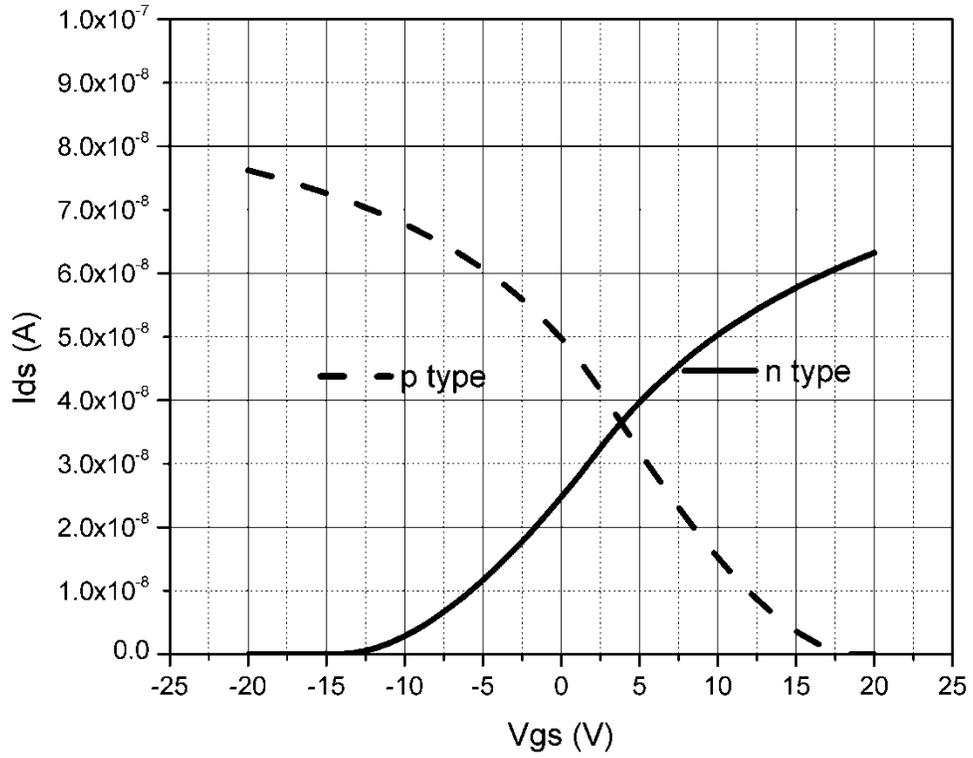
Figure 5-3: Modeled V_{gs} Characteristics of an Amorphous TFT. (Open circles for n-type material, closed squares for p-type material).
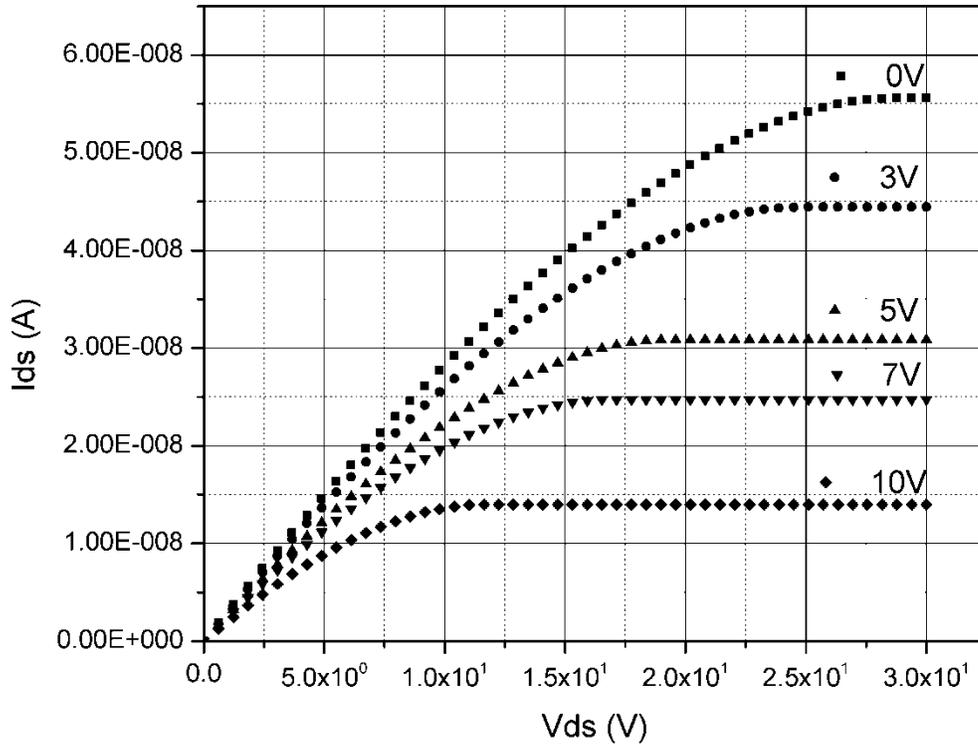
Figure 5-4: Modeled Generic p-Type Organic Transistor Output Characteristics for Applied Gate Voltages from 0 to 10 volts.

The transistors with transfer and output characteristics shown in Figure 5-3 and 5-4 were used to replace the transistors in the circuit designed by van Schaik. For this circuit a level 11 transistor model was used with the following parameters; zero bias threshold voltage (VTO) 3.0 volts, source resistance (RS) 100 K ohm, transconductance (KP) 0.543e-4 amps/volts^2, drain resistance (RD) 100 K ohm, gate resistance (RG) 7.5 ohms, bulk saturation current (IS) 1e-64 amps, gate drain capacitance (CGD) 1.70e-9 Farads/meter. The modified circuit is shown in Figure 5-5. The current regulating transistors have been removed due to the low currents in the

amorphous TFTs. A typical output is shown in Figure 5-6, together with an example of the variation in the refractory period. As in the test of the original circuit, the synaptic input sum is represented by current source I1. In the simulation shown in Figure 5-6, the input current is a broad, 1 second, 500 µA input current pulse. Again we can see a sloped charge of the membrane and then an abrupt spiking as the threshold voltage (at V2) is exceeded. The slope of the charging profile is shallow compared to the original simulation due to the internal resistance of the charging transistor, Q9. This is followed by the activation of Q10 and the discharge of the membrane. The cycle then repeats as the input current at I1 continues to flow and the membrane recharges. The shoulders that appear in Figure 5-6 are a result of the timing of the on/off of the charge/discharge transistors, Q9 and Q10 in Figure 5-5. The ledge occurs as Q9 stays on, charging the membrane while Q10 starts to discharge the membrane. The final ledge/drop off occurs when Q9 shuts off, and stops charging the membrane capacitor, and Q10 stays on and continues to discharge the membrane capacitor. At the peaks, Q9 has turned on, to charge the membrane but there is a delay in the turn on of Q10. Once Q10 turns on, the discharge begins and the membrane voltage drops abruptly. This is shown in Figure 5-7. Shown are the charge and discharge currents and the membrane potential. The ledge in the membrane potential aligns with the final shut off of Q9, the charging transistor.

The shape of the membrane potential can be further refined by adjustment of the TFT structure (for example, a shift of the TFT threshold voltages). Modifications of the

membrane capacitance, the leakage resistance and the input current I1 in the circuit result in a modified membrane potential pulse shape and response as shown in Figure 5-8. The duration of the shoulder has been reduced. The output behaviour more closely matches that of the original circuit shown in Figure 5-2.
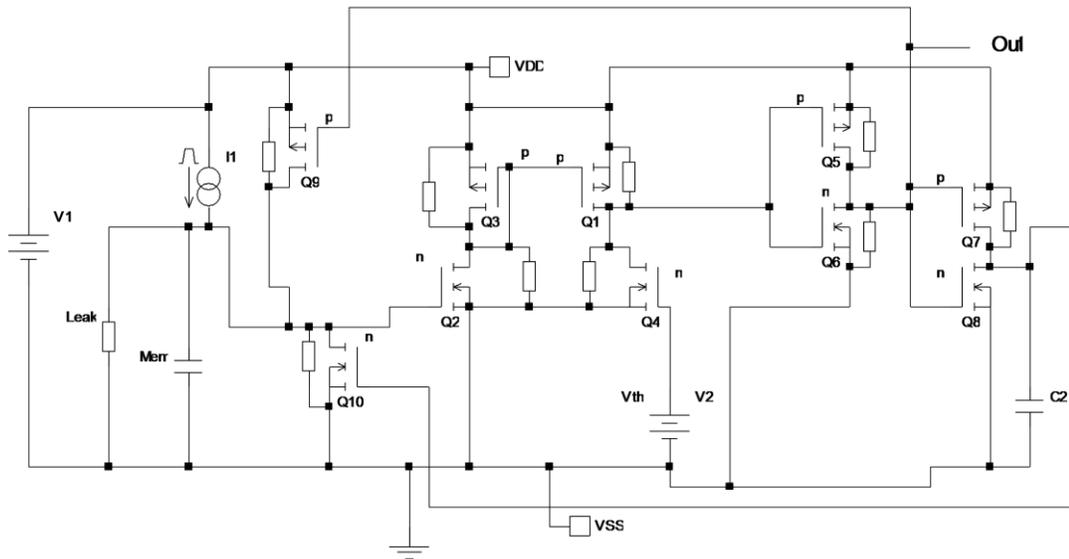
Figure 5-5:   Modified Neuron Circuit with Amorphous TFTs.
The current regulating transistors, Q12, Q13, Q14 and Q15 are removed (as shown in Figure 5-1). The standard transistors have been replaced with models of the organic transistors as defined by the properties in Figures 5-3 and 5-4.
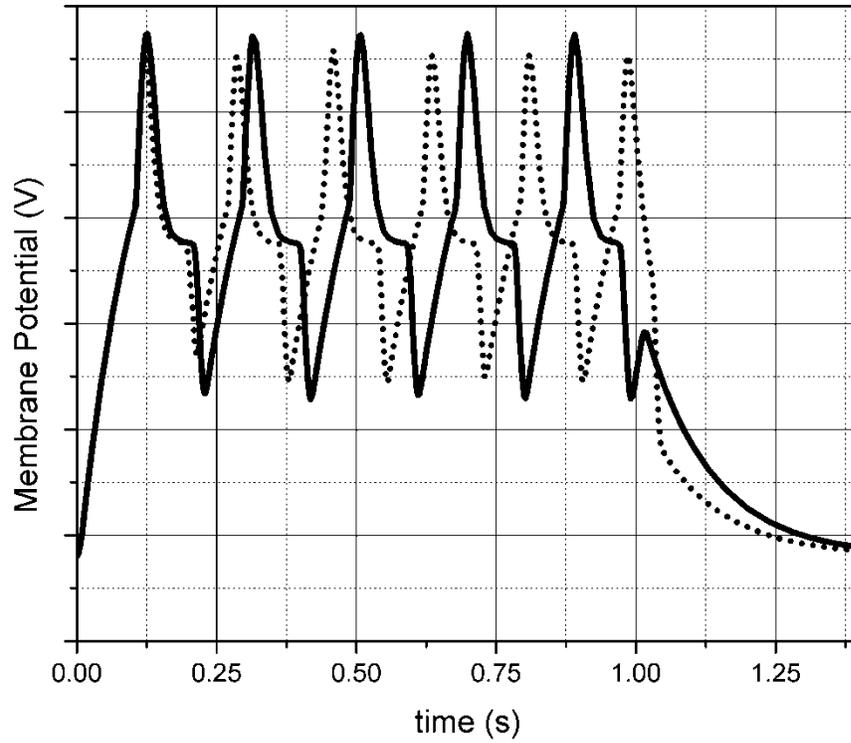
Figure 5-6: **Output of the Modified Circuit with Variable Refractory Period. Two differing Refractory Periods are Shown (Solid and Dashed Lines).**
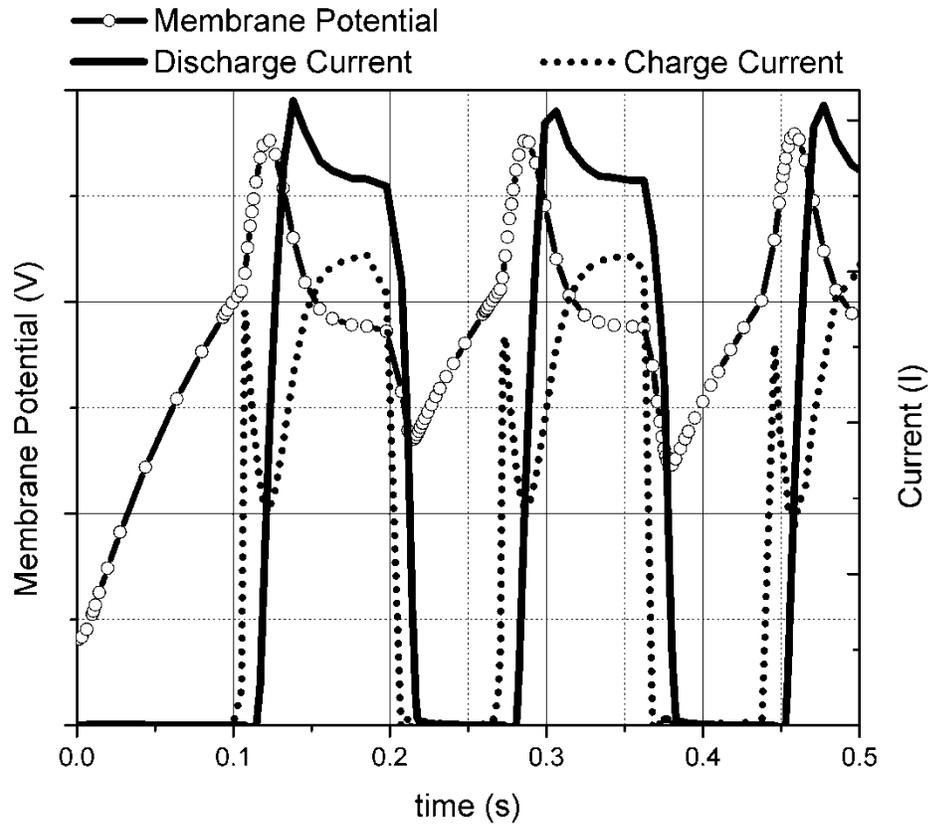
Figure 5-7.   Analysis of Shoulder Effect.
Shown are the membrane potential, and the charge and discharge currents.
The shoulder at 0.2 s results when as the charge transistor turns on at 0.11 s, but
does not turn off until 0.2 s, opposing the discharge current. Only when the
charge current is turned off (Q9) does the membrane potential drop to a
minimum.
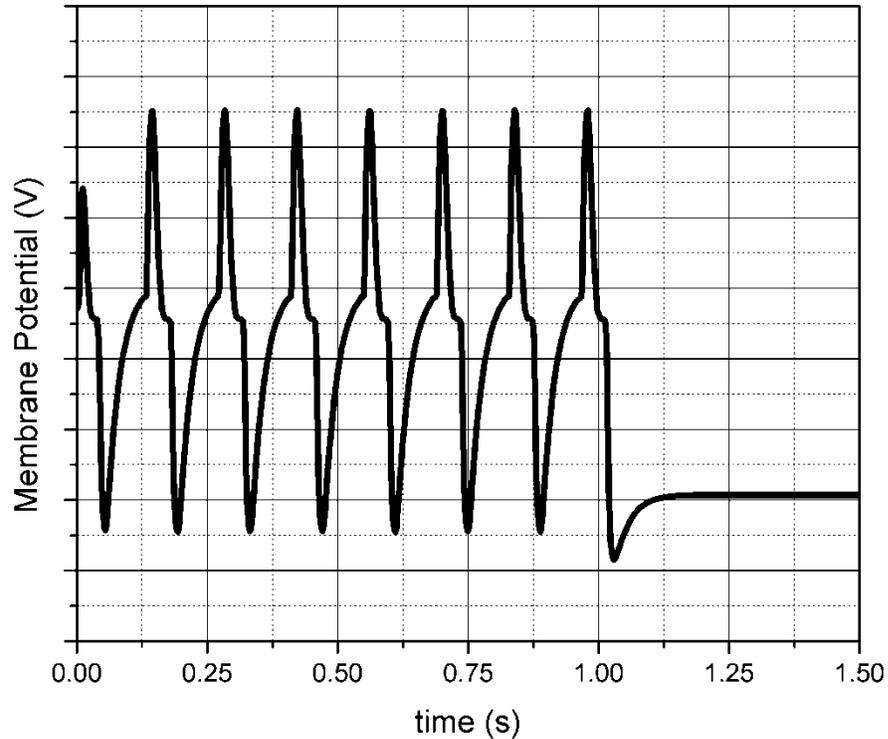
Figure 5-8: Modified Membrane Response of the Organic Transistor-based Spiking Analog Neural Circuit.
The element properties of the circuit shown in Figure 5-5 have been modified from the output shown in Figure 5-6. The duration of the shoulder has been reduced. The behaviour more closely matches that of the original circuit shown in Figure 5-2.

5.4   SONOS Model

A model of the SONOS gate is shown in Figure 5-9. The primary components are modeled by the opposed Zener diodes (D3 and D4) and the charge storage layer (C2).

The diode parameters used are; saturation current (IS) 9.19e-16 Amps, zero bias junction capacitance (CJO) 300 Pico Farads, and ohmic resistance (RS) 0.57 ohms.

This simple model was developed based on the measured behaviour of the SONOS

gates outlined in Chapter 4. Although further optimization of devices is required, the initial results support the development of this model. The properties of the Zener diodes and the charge storage capacitor can be further modified to reflect these optimizations. The ability to store charge is shown in Figure 5-10 which represents a functional simulation of the SONOS circuit model. Here, there is an imposed voltage across the SONOS gate capacitor (C2) resulting from an applied negative voltage (8 volts, pulse width 5 ms, at t=430 ms) pulse. This pulse is provided by source V5. Source V4 is the source of the input signal, a square wave pulse of period 50 ms. This quasi-permanent voltage is the result of stored charge in the capacitor and acts to shift the threshold of the transistor as it shifts the effective applied gate voltage (1 volt in the case shown). The gate potential of Q1 is shown and can be seen to shift after the learning pulse is applied at 420 ms. This shift mimics a shift in synaptic response of the neuron model. A decay in the charge/voltage is also evident as the gate potential decays from 430 ms to 1 s. This decay results from leakage through the diodes and can be adjusted through the design of the tunneling and blocking layers in actual devices.
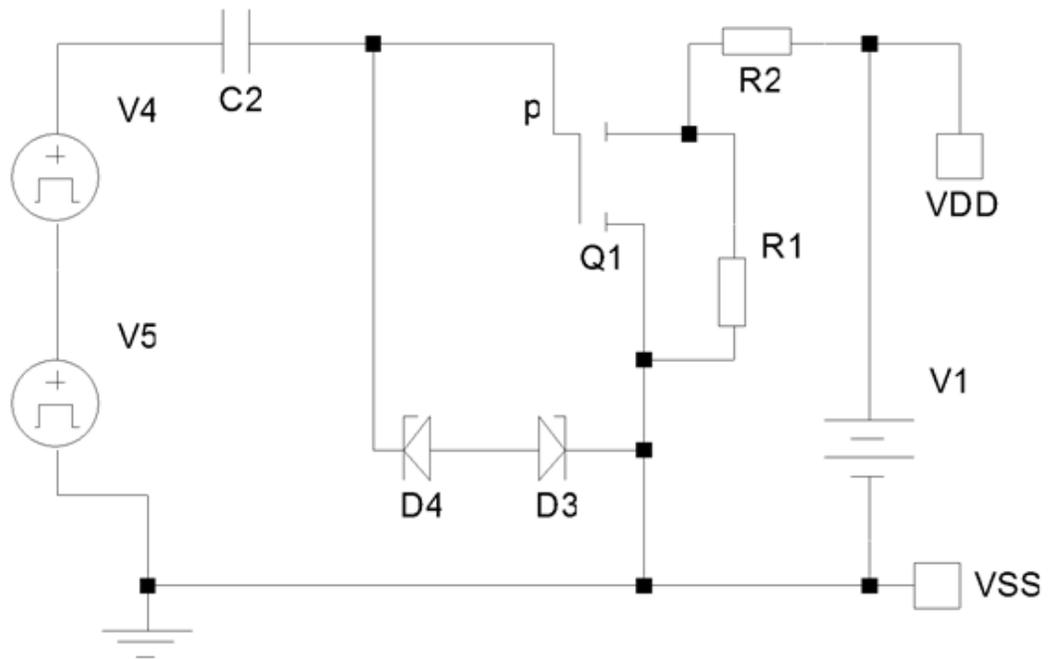
Figure 5-9: SONOS Gate Model.
The circuit represents a single transistor, Q1, with the SONOS gate modeled by the capacitor C2 and diodes D4 and D3. The high voltage learning pulse is provided by source V5. Source V4 provides the input signal.
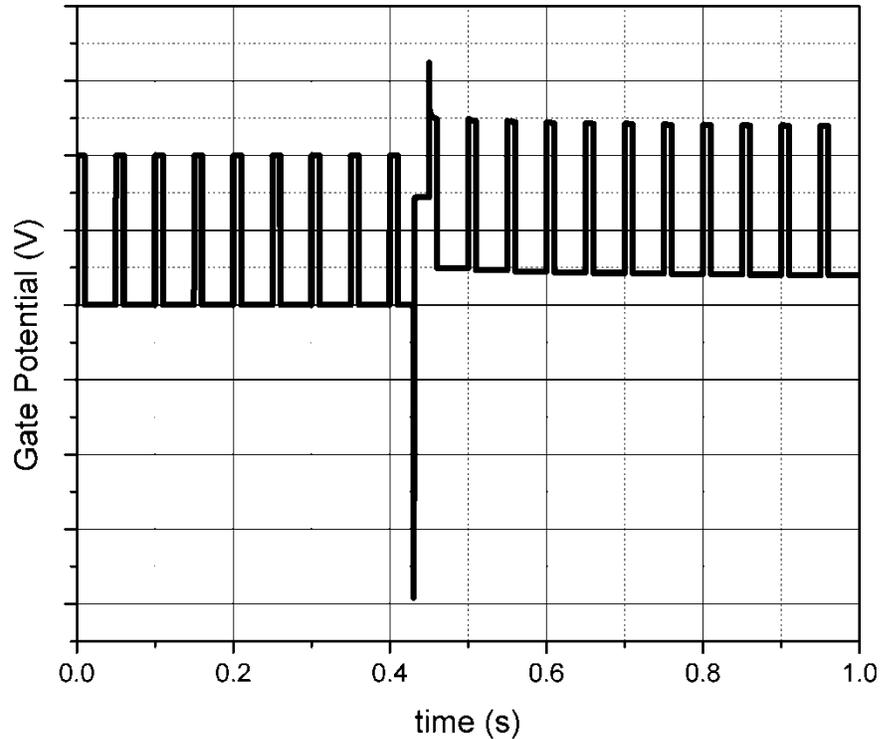
Figure 5-10: SONOS Gate Charging Behavior.
The gate potential is shown with an applied input square wave with a 50 ms
period (20 pulses shown). A learning pulse is imposed at 430 ms. The gate
potential shifts after the learning pulse as a result of charge storage in the
SONOS gate capacitor. The gate potential is increased by the charge storage after
the learning pulse and then decays as the charge leaks out of the storage capacitor
through the diodes.

5.5   Hebbian Learning Model

A schematic representation of a learning circuit for the SONOS TFT is shown in

Figure 5-11. Shown is a single transistor representing a single synapse. The single

transistor feeds into a main neuron which integrates a series of other synaptic inputs

provided by other transistors (not shown). If the main neuron fires, a pulse is seen at

the Output. If this output occurs within a specified time as the Input pulse, then an AND circuit with a time delay will apply a 14 volt learning pulse to the SONOS transistor.

The learning circuit model for the SONOS TFT is shown in Figure 5-12. In this simple circuit, an output pulse from the neuron combines with the 'synaptic' input pulse to drive an AND circuit which in turn drives a learning pulse. This can be seen to be a Hebbian-like modification process. The learning rate (charging rate) is adjustable either from the pulse height or width. This charge behavior mimics the tunneling current charging behavior in the SONOS device. The learning circuit can be modified to add a propagation delay as required. In this circuit, the propagation/timing circuitry is not shown but is imposed by the voltage sources V6 and V7. These voltage sources model the synaptic input and output of the single neuron. Each drives one input of an AND gate, so that when both are activated, the AND operates and will apply a large negative voltage to the gate (C2) of SONOS transistor Q2. A residual charge is left on across the gate capacitor, C2. The functionality of the circuit is shown in Figure 5-13. A negative learning pulse results when the input and output pulses are simultaneously present on the learning control circuit, the AND gate. These circuits show only induction of potentiation. Induction of depression can be achieved through the design of a circuit with positive pulses (or changing the synaptic transistors to n-type).
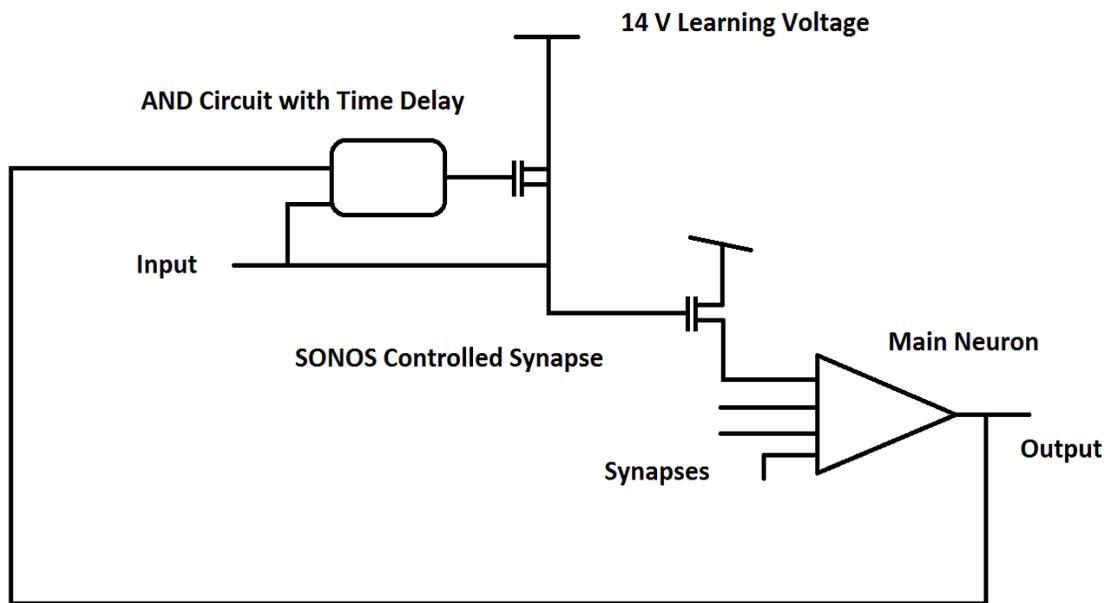
Figure 5-11: Schematic of Learning Circuit.
Shown is a single transistor representing a single synapse. The single transistor feeds into a main neuron which integrates a series of other synaptic inputs provided by other transistors (not shown). If the main neuron fires, a pulse is seen at the Output. If this output occurs within a specified time as the Input pulse, then an AND circuit with a time delay will apply a 14 volt learning pulse to the SONOS transistor.

Figure 5-12: SONOS Learning Circuit.
A single SONOS transistor is shown (Q1, D4, D3 and C2). An AND circuit is provided by Q12, Q13, Q14 and Q15. The input signal, V6, is combined with the simulated output signal, V7. When both are present, a learning pulse (magnitude set by V1) is applied to the SONOS gate at C2.
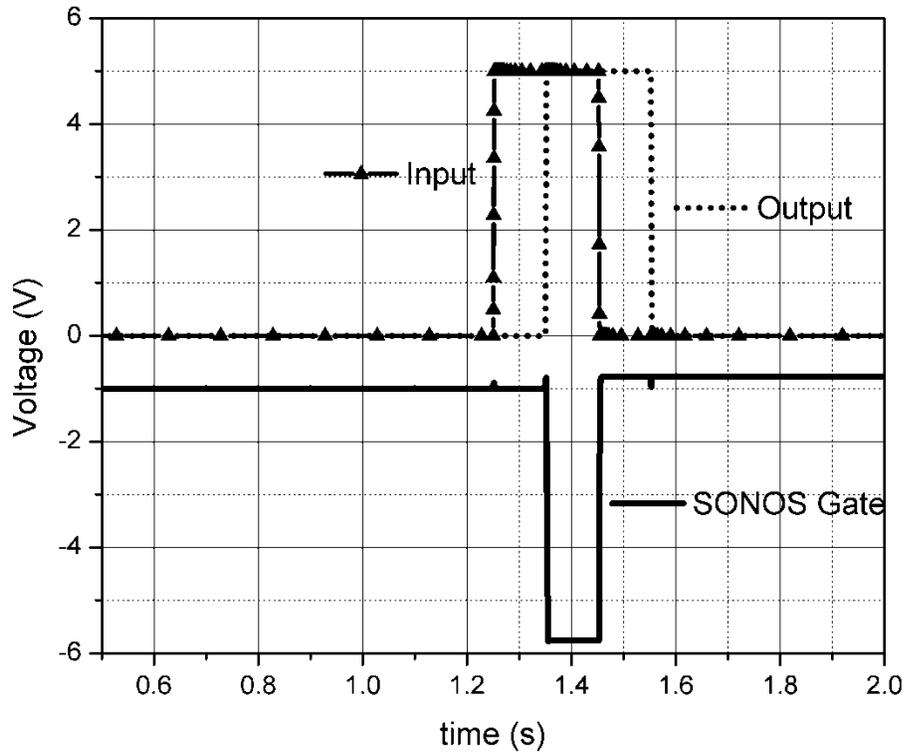
Figure 5-13.   Input and Output of Learning Circuit.
Shown is the control of the learning circuit (AND gate). When the Gate input pulse (V6 in the circuit in 5-12) and the output signal (simulated by V7) are simultaneously present, a learning pulse (magnitude set by V1) is applied to the gate.

5.6   SONOS Split Gate

The SONOS split gate learning circuit is shown in Figure 5-14. Shown is a two-gate configuration. This circuit can be combined with the learning circuit shown in Figure 5-12. Each gate is controlled by a separate learning circuit.
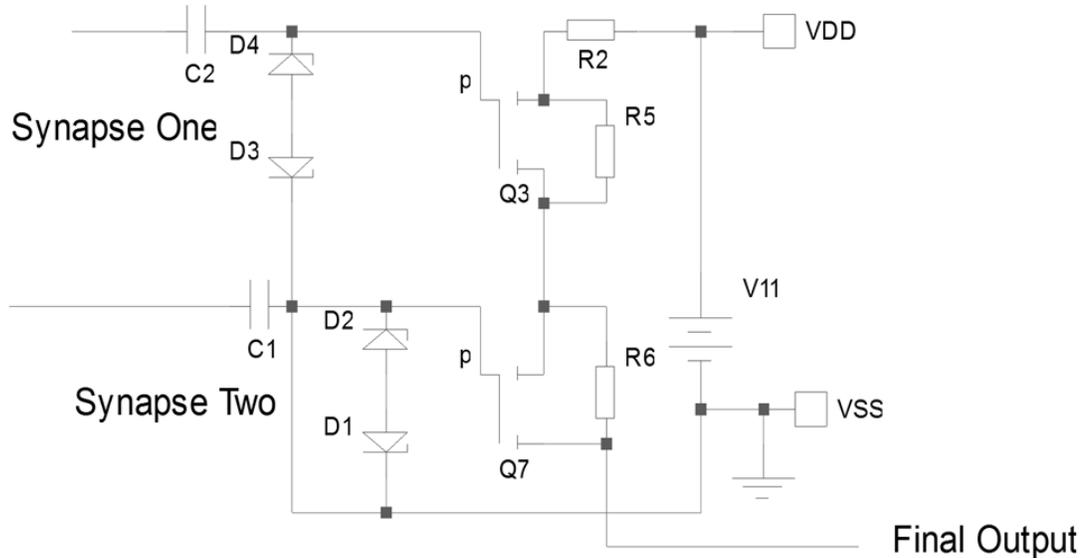
Figure 5-14: Split Gate SONOS with Learning Circuit.
Shown is a two gate configuration represented by two separate transistors, Q3 and Q7 (with SONOS 2 sets of SONOS circuitry, C1, C2, D1, D2, D3, D4). The transistors are models of organic TFTs.

5.7   Single Synapse SONOS Circuit Model

The circuit shown in Figure 5-15 incorporates the SONOS transistor into the modified

spiking analog circuit of Figure 5-5. The transistors are all organic TFTs, including the

SONOS transistor of Q11. The SONOS transistor provides a single synapse and

replaces the input current source of I1. Voltage source V3 controls the SONOS input

behavior and source V4 provides the learning signal. The circuit is otherwise the same

as in Figure 5-5. In a full device, numerous synapses will exist in parallel and will be

integrated by the membrane capacitance. A simulation of the membrane potential from

this circuit is shown in Figure 5-16. Q11 is driven by the voltage pulses of V3 and V4.

For the simulation shown, the input voltage pulse is an alternating square wave, of 1s

period, on from 0s to 0.5s, off from 0.5s to 1.0s. The synaptic current comes from the

SONOS organic TFT at Q11. Here we can see the spiking behavior as well as short

term adaptation as the response to the second input pulse at 1s is insufficient to reach

the threshold voltage.
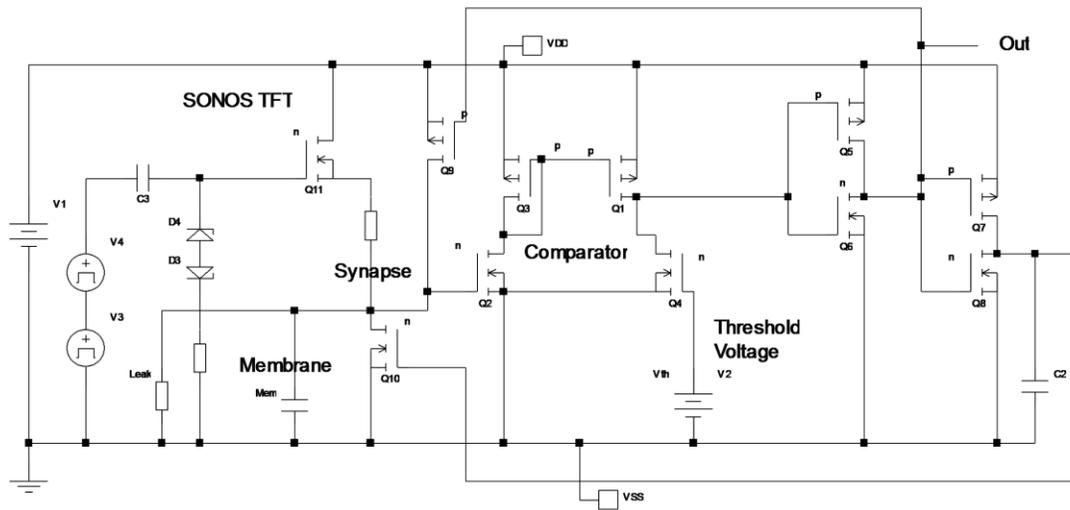
Figure 5-15.   Spiking Analog Neural Circuit with SONOS OTFT.
SONOS TFT is at Q11 and includes capacitor C3 and opposing diodes D3 and D4.
This circuit is a modification of the circuit in Figure 5-5 with the current source
I1 replace by a single SONOS transistor.
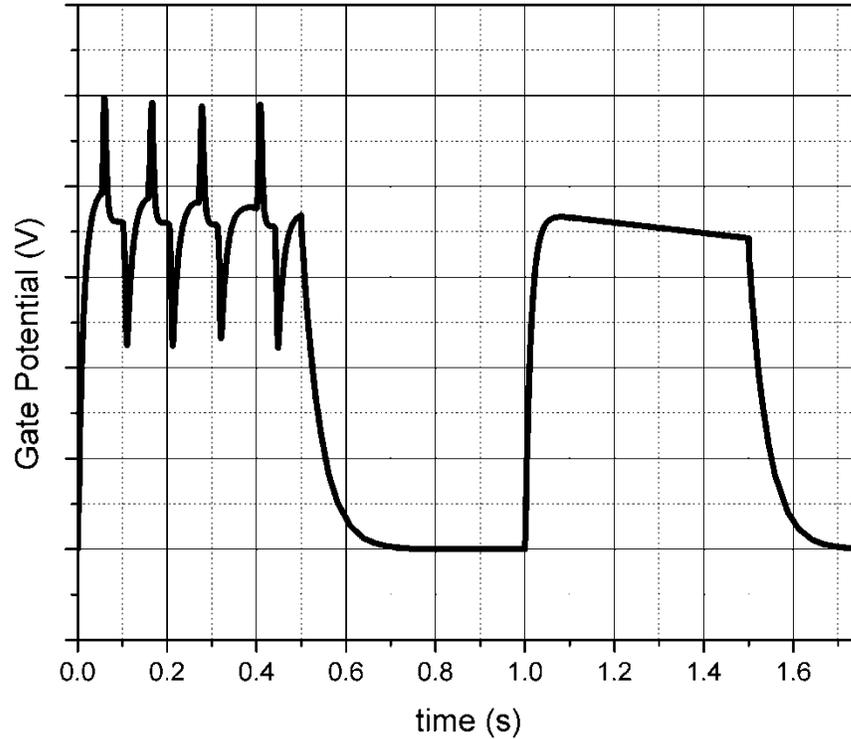
Figure 5-16.   Output Spiking Behaviour and Adaptation of the Basic Analog Spiking Neural Circuit.
Input voltage pulses controlled the SONOS synapse. The response to two input pulses (0s to 0.5 s, and 1 s to 1.5 s) are shown. The response of the circuit to the second pulse is insufficient to reach the threshold voltage and cause spiking.

This learning behavior of this circuit, as outlined in Figure 5-11, is simulated using the learning pulse from V4. This is shown by the output in Figure 5-17, as the synaptic current through Q11 is increased after a learning pulse from V4 at 0.7 s. The adaptation can be seen by the gradual decrease in the synaptic current.
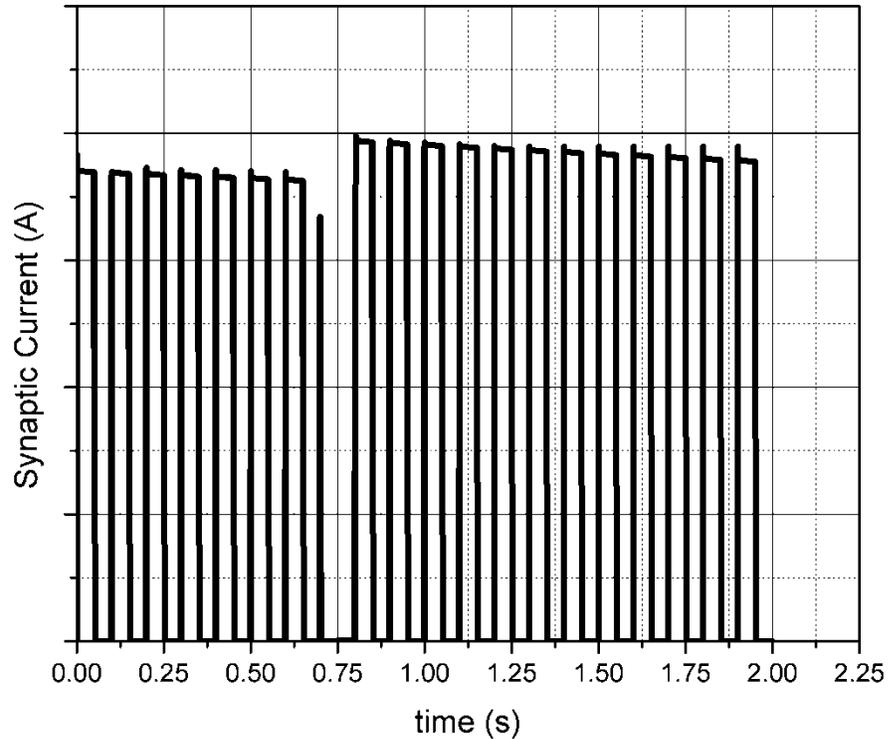
Figure 5-17. Synaptic Current Modification of the Organic SONOS TFT Incorporated into the Circuit in Figure 5-15.
A learning pulse is applied at t = 0.75 s to the SONOS TFT at Q11. The synaptic current increases from 1.8 uA to 2 uA after the learning pulse.

5.8   Chapter Summary

The modeling in this chapter covered the initial demonstration of; 1. The use of organic transistors in spiking analog neural circuits. 2. The model of an organic SONOS transistor. 3. A simple Hebbian learning circuit. 4. The organic SONOS transistor in a spiking analog neural circuit.

93

6 SUMMARY AND OUTLOOK

6.1 Summary

6.1.1 SONOS Capacitors

We have successfully demonstrated that SONOS capacitors can be fabricated using either an amorphous silicon or an organic semiconductor material (AlQ3) and compared these to control samples and crystalline silicon SONOS devices. The memory effect of charging in the SONOS capacitors is demonstrated through the hysteresis in the C-V plots. This hysteresis is shown to be a result of the SONOS structure rather than any interface effects. This is achieved by comparison to devices using crystalline silicon with and without the SONOS structure. These structures have been previously analyzed with the current results matching those of the previous works. No hysteresis was shown in devices without the SONOS structure.

The SONOS structure was also examined using TEM and EDS. This confirmed that the expected structures were present rather than some unknown structure (such as a mixed layer with various interface states).

Then with the demonstrated ability to reproduce the SONOS structures in crystalline silicon, structures were produced using amorphous silicon, AlQ3 and CuPc as the semiconductor material. These results demonstrated that the SONOS structures also resulted in a hysteresis effect in the devices. They also confirmed that the organic materials behaved as semiconductor materials in the CV analysis.

6.1.2   Field Effect Thin Film Transistors

The next stage of analysis involved the design, fabrication and characterization of amorphous transistors. The main objective was to determine if organic field effect transistors could be produced with SONOS gates and exhibit a memory effect. Functional organic transistors were produced, followed by the design, fabrication and characterization of SONOS TFTs using CuPc as the semiconductor material. These devices showed a memory effect in the induced shift in the transfer characteristics. SONOS capacitors, as opposed to complete transistors, could also be used as discrete elements in a more complicated spiking analog circuit.

Simple split gate CuPc FETFTs were also produced to demonstrate the feasibility of these devices in a spiking analog circuit.

6.1.3   Modeling of Analog Spiking Circuits with Embedded Memory

Using the results of the characterization of the organic TFTs, spiking analog circuits were modeled. First an existing spiking circuit using standard crystalline silicon FETs was analysed. This circuit was then re-developed to work with organic transistors. This is significant in that the amorphous nature of the organic transistor allows them to be produced in stacks as they do not require a crystalline substrate. This allows for the potential design and manufacture of three dimensional circuits with high interconnect density. These circuits were then modified to include the memory effect in the SONOS gate organic FET. This memory effect is similar to synaptic plasticity. A simple Hebbian learning circuit was also designed and shown to be capable of unsupervised learning. The ability to adjust the TFT characteristics of amorphous transistors

combined with the manufacture-ability of the devices makes these transistors aptly suitable for use in the design of complex analog neural networks with high connectivity and unsupervised learning capability. The embedded Hebbian learning circuits and the ability to stack amorphous organic cells in 3-dimensional circuits allows for the design and manufacture of high-density circuits.

6.2 Outlook

The main area for further research is in the design, fabrication and characterization of complete and advanced analog neural spiking circuits using the techniques outlined in this thesis. The recent advances and economic shifts in the semiconductor processing industry have opened the door to the development of specialty analog circuits. The reduction in cost, and the ease of manufacture of amorphous electronics including organic devices allows for the research and development of specialty circuits without the requirement of enormous research budgets. Up until now, the bulk of implementation and research has been in the areas of digital, serial neural circuits. These serial circuits are convenient implementations that leverage the existing design of FPGAs and basic digital circuitry. New areas of research will allow for the analysis of more advanced analog and mixed analog-digital circuits. This will likely reveal new device artifacts that will have potential in further iterations of circuits. It is also of particular interest that in biological neural systems, the dominant development process proceeds through evolution. Rapid semiconductor prototyping techniques will allow

for a measure of this same evolutionary process in artificial neural circuit development.

6.3   Concluding Remarks

This work is intended as a general overview of the use of Organic field effect thin film transistors with tunneling gates in spiking analog neural circuits. Organic electronics is a relatively new field of study and the interface effects, including tunneling from and to organic layers requires more study. The long term stability of organic SONOS devices is also required. There is significant potential for these, and similar, devices for use in neural circuits.

7 REFERENCES

1. Savran, Aydoğan and Ünsal, Serkan. *Hardware Implementation Of A Feedforward Neural Network Using Fpgas*. Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), v 4234 LNCS - III, p 1095-1104, 2006.

2. Ali, Haitham Kareem and Mohammed, Esraa Zeki. *Design Artificial Neural Network Using FPGA*. IJCSNS International Journal of Computer Science and Network Security, VOL.10 No.8, August 2010.

3. Sahoolizadeh, Hossein, Keshavarz, Ahmad, and Tadbir, Behin. *A FPGA Implementation of Neural/Wavelet Face Detection System* Australian Journal of Basic and Applied Sciences, 4(3): 379-388, 2010.

4. Maeda, Yutaka and Tada, Toshiki. *FPGA Implementation of a Pulse Density Neural Network With Learning Ability Using Simultaneous Perturbation*. IEEE Transactions On Neural Networks, Vol. 14, No. 3, May 2003.

5. Brassai, Sándor Tihamér, László, Dávid, and László, Bakó. *Hardware Implementation of CMAC-based Artificial Network with Process Control Application, Timişoara, Transaction on Electronics and Communication*. Scientific bulletin of the Politehnica University. pp. 209-213. 2004.

6. Jilani, Saudagar Abdul Khader, and Sattar, Syed Abdul. *JPEG Image Compression using FPGA with Artificial Neural Networks*. IACSIT International Journal of Engineering and Technology, Vol.2, No.3, June 2010.

7. Letendre, James and Zhou, Ziyan. *Artificial Neural Network*. DSD Project Final Report. 2010.

8. Eldredge, James G., Hutchings, Brad L. *RRANN: a hardware implementation of the backpropagation algorithm using reconfigurable FPGAs*. IEEE International Conference on Neural Networks - Conference Proceedings, v 4, p 2097-2102, 1994.

9.   Bellis, S. Razeeb, K.M.; Saha, C.; Delaney, K.; O'Mathuna, C.; Pounds-Cornish, A.; De Souza, G.; Colley, M.; Hagras, H.; Clarke, G.; Callaghan, V.; Argyropoulos, C.; Karistianos, C.; Nikiforidis, G. *FPGA implementation of spiking neural networks - An initial step towards building tangible collaborative autonomous agents.* Proceedings - 2004 IEEE International Conference on Field-Programmable Technology, FPT '04, p 449-452, 2004.

10.   Lee, Yongsoon. *A Neural Network Face Detector Design Using Bit-Width Reduced* Fpu *In Fpga.* Conference on Electrical and Computer Engineering, p 1914-1917, 2007.

11.   Raeisi, Reza, Kabir, Armin. *Implementation Of Artificial Neural Network On Fpga* American Society for Engineering Education March 31-April 1, 2006 – Indiana University Purdue University Fort Wayne (IPFW) 2006 Illinois-Indiana and North Central Joint Section Conference.

12.   Lina, Cheng-Jian, Tsaib, Hung-Ming. *FPGA implementation of a wavelet neural network with particle swarm optimization learning.* Mathematical and Computer Modeling 47 (2008) 982–996.

13.   Bringk, Stephen (School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, United States); Koziol, Scott; Ramakrishnan, Shuba; Hasler, Paul. *A biophysically based dendrite model using programmable floating-gate devices.* Proceedings - IEEE International Symposium on Circuits and Systems, p 432-435, 2008.

14.   Zhao, J. and Kim, Y-B. *Circuit Implementation of FitzHugh-Nagumo Neuron Model Using Field Programmable Analog Arrays.* Midwest Symposium on Circuits and Systems 50th Midwest Symposium on Circuits and Systems, MWSCAS - Conference Proceedings. p 772-775, 2007.

15.   Dayan, P. and Abott, L. F. *Theoretical Neuroscience: Computational and Mathematical Modeling of Neural Systems. 2001.* The MIT Press.

16.   Shepherd, G. M. *Neurobiology.* Oxford University Press. 1983.

17.   Koch, C. *Biophysics of Computation: Information Processing in Single Neurons.* Oxford University Press. 1999.

18.   Ioana, Domnica Marian. Master's Thesis. *A biologically inspired model of* motor *control of direction.* University College Dublin, Dublin, Ireland, October 2002.

19.   Indiveri, Giacomo. *Analog VLSI circuits for spiking neural networks*. ICANN 2009.

20.   van Schaik, A. *Building blocks for electronic spiking neural networks*. Neural Networks 14, 617-628. 2001.

21.   Ip, Henry M.D., Drakakis, Emmanuel M., Bharath, Anil A. *Towards Analog VLSI Arrays for Nonseparable 3D Spatiotemporal Filtering*. 2006 10th International Workshop on Cellular Neural Networks and Their Applications. 2006.

22.   Milev, Momchil, and Hristove, Marin. *Analog Implementation of ANN with Inherent Quadratic Nonlinearity of the Synapses*. IEEE Transactions on Neural Networks, Vol. 14 No. 5. September 2003.

23.   Kim, Hyunjung, Son, Hongrak, Lee, Jeonwon, Kim, In-cheol, and Kim, Hyingsuk. *An Analog Viterbi Decoder for PRML using Analog Parallel Processing Circuits of the CNN*. 2006 10th International Workshop on Cellular Networks and their Applications. August 2006.

24.   Andreou, Andreas G. *Analog VLSI neuromorphic systems.* Proceedings - IEEE International Symposium on Circuits and Systems, v 2, p 1471-1474, 1993.

25.   Pashaie, Ramin, and Farhat, Nabil H. *Optical realization of bioinspired spiking neurons in the electron trapping material thin film*. Applied Optics. 10 Vol. 46, No 35. December 2007.

26.   Keles, Fatih, Yildirim, Tulay. *Pattern Recognition Using N0 input Neuron Circuits Based on Floating Gate MOS Transistors*. IEEE EUROCON 2009, p 224-229, 2009.

27.   Brink, Stephen, Koziol, Scott, Ramakrishnan, Shubha, Hasler, Paul. A *Biophysically Based Dendrite Model Using Programmable Floating Gate Devices*. IEEE 2008.

28.   Fujita, Osamu and Amemiya, Yoshihito. *A Floating Gate Analog Memory Device for Neural Networks*. IEEE Transactions On Electron devices. Vol. 40. N0 11. November 1993.

29.   Hu, Jingzhen and Gordon, Christal. *A Wide Range Charge Balancing Circuit using Floating Gate Transistors*. Proceedings of the 29th Annual International Conference of the IEEE EMBS. August 2007.

30. Naess, Oivind, Aunet, Snorre, Berg, Yngvar. *Low Voltage Pseudo Floating Gate Reconfigurable Linear Threshold Elements*. Proceedings of International Joint Conference on Neural Networks. 2005.

31. De Lima, Jader A., and Cordeiro, Adriano S. *A Low Voltage Low Power Analog Memory Cell with Built in 4-Quadrant Multiplication*. IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing Vol. 50., No. 4. April 2003.

32. Li, Ming-*Ze*, Ping-Wang, Po, Tang, Kea-Tiong, and Fang, Wai-Chi. *Multi-Input Silicon Neuron with Weighting Adaptation.* 2009 IEEE/NIH Life Science Systems and Applications Workshop, LiSSA 2009, p 194-197, 2009.

33. Haas, Hugo L. and Gomes, Jose Gabriel R. C. *Analog inner product* operations *for image compression in 0.35 um CMOS*. Analog Integrated Circuit Signal Processing. 2008.

34. Kinoshita, Shigeo, Morie, Takashi, Nagata, Makoto, Iwata, Atsushi. *A PWM Analog Memory Programming Circuit for Floating Gate MOSFETs with 75-us Programming Time and 11-bit Updating Resolution*. IEEE Journal of Solid-State Circuits. Vol. 36. No 8. August 2001.

35. VogelStein, R. Jacob. Mallik, Udayan, Vogelstein, Joshua T. and Cauwenberghs, Gert. *Dynamically Reconfigurable Silicon Array of Spiking Neurons with Conductance Based Synapses*. IEEE Transactions on Neural Networks. Vol. 18. No 1. January 2007.

36. Fujii, R. H. Nemoto, R. Satou, N. *Spiking Analog Neuron Circuit Design, Analysis, and Simulation*. Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems. p 482-6 vol.1, 2001.

37. Wijekoon, Jayawan, Dudek, Piotr. *Spiking and Bursting Firing Patterns of a Compact VLSI Cortical Neuron Circuit*. Proceedings of International Joint Conference on Neural Networks, p 1331-6, 2007.

38. Mondragon-Torres, A.F., Schneider, M.C. and Sanchez-Sinencio, E. *Well-driven floating gate transistors*. Electronics Letters. Vol. 38. No 11. May 2002.

39. White, Marvin H. and Chen, Chun Yu. *Electrically Modifiable Non-volatile Synapses for Neural Networks*. Proceedings - IEEE International Symposium on Circuits and Systems, v 2, p 1213-1216, 1989.

40. Chun-Yu Malcolm Chen, Marvin H. White and Margaret French. *A Solid-state Electronic Linear Adaptive Neuron with Electrically Alterable Synapses*. 91 IEEE Int Jt Conf Neural Networks IJCNN 91, p 1801-1806, 1991.

41. Hanyu, Takahiro Kaeriyama, Shunichi; Kameyama, Michitaka. *Logic-in-memory VLSI circuit for fully parallel nearest pattern matching based on floating-gate-MOS pass-transistor logic.* Journal of Multiple-Valued Logic and Soft Computing, v 11, n 5-6, p 619-632, 2005.

42. Harrison, R.R., Bragg, J.A.; Hasler, P.; Minch, B.A.; Deweerth, A. *CMOS programmable analog memory-cell array using floating-gate circuits* S.P. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, v 48, n 1, p 4-11, January 2001.

43. Fujita, Osamu and Amemiya, Yoshihito. *A Floating Gate Analog Memory Device* for *Neural Networks*. IEEE Transactions on Electron Devices. Vol. 40. N0 11. November 1993.

44. Yang, Kewe and Andreou, Andreas G. *Multiple input floating gate MOS differential amplifier. An analog computational building block*. Proceedings - IEEE International Symposium on Circuits and Systems, v 5, p 37-40, 1994.

45. *Naess*, Oivind, Aunet, Snorre, Berg, Yngvar. *Low Voltage Pseudo Floating Gate Reconfigurable Linear Threshold Elements*. Proceedings of the International Joint Conference on Neural Networks 2005. p 675-80 vol. 2, 2005.

46. Kinoshita, Shigeo, Morie, Takashi, Nagata, Makoto, Iwata, Atsushi. *A PWM Analog Memory Programming Circuit for Floating Gate MOSFETs with 75-us Programming Time and 11-bit Updating Resolution*. IEEE Journal of Solid-State Circuits. Vol. 36. No 8. August 2001.

47. Mondragon-Torres, A.F., Schneider, M.C. and Sanchez-Sinencio, E. *Well-driven* floating *gate transistors*. Electronics Letters. Vol. 38. No 11. May 2002.

48. Sarah Paydavosi, Hassen Abdu, Geoffrey J. Supran, and Vladimir Bulovic. *Performance Comparison of Different Organic Molecular Floating-Gate Memories*. IEEE Transactions on Nanotechnology, Vol. 10, No. 3, May 2011.

49. Haykin, Simon. *Neural Networks and Learning Machines*. Pearson Education Inc. 2009.

50. Haykin, Simon. McMaster University ECE 775 Course Notes. 2010.

51. Goldberg, David and Andreou, Andreas G. *Spike communication of dynamic stimuli: Rate decoding versus temporal decoding.* Neurocomputing, v 58-60, p 101-107, June 2004.

52. P. Adibi, M. R. Meybodi, R. Safabakhsh. *Unsupervised Learning of Synaptic Delays Based on Learning Automata in an RBF-like Network of Spiking Neurons for Data Clustering.* Neurocomputing. Vol. 64. Pp. 335-357. 2005.

53. Zaghloul, K. A., Boahen, K., Demb, J. B.. *Contrast Adaptation in Subthreshold and Spiking Responses of Mammalian Y-Type Retinal Ganglion Cells.* The Journal of Neuroscience. January 26. Pp 860-868. 2001.

54. Capela, S. , Tomas, P., Souza, L.. *Stochastic Integrate and Fire Model for the Retina.* European Signal Processing Conference, p 2514-2518, 2007.

55. Bressloff, P. C., Coombes, S. *Dynamics of Strongly Coupled Spiking Neurons.* Neural Computation. 12, pp. 91 – 129. 2009.

56. Meister, M. and Berry, J. M. *The Neural Code of the Retina.* Neuron. Vol 22. Pp. 435 – 450. 1999.

57. Martins, S. F., Sousa, L. A., Martins, J. C. *Additive Logistic Regression Applied to Retina Modeling.* Proceedings - International Conference on Image Processing, ICIP, v 3, p III309-III312, 2006.

58. Tomas, P., Martins, J. , Sousa, L. *Towards a Unified Model for the Retina.* Biosignals 2008 - Proceedings of the 1st International Conference on Bio-inspired Systems and Signal Processing, v 2, p 528-533, 2008.

59. Choe, Y., Miikkulainen, R. *Self Organization and Segmentation in a Laterally* Connected *Orientation Map of Spiking Neurons.* Neurocomputing 21. Pp 139 – 157. 1998.

60. Pillow, J. W., Paninski, L., Uzzell, V. J., Simoncelli, E. P., Chichilnisky, E. J. *Prediction and Decoding of Retinal Ganglion Cell Responses with a Probabilistic Spiking Model.* The Journal of Neuroscience. Pp 11003-11013. November 23, 2005.

61. Patel, A., Kosko, B. *Stochastic Resonance in Noisy Spiking Retinal and Sensory Neuron Models.* Neural Networks. 18. Pp 467 – 478. 2005.

62. Izhikevich, Eugene M. *Simple Model of Spiking Neurons.* IEEE Transactions on Neural Networks 14:1569-1572. 2003.

63. Izhikevich, Eugene M., *Which Model to Use for Cortical Spiking Neurons* IEEE Transactions on Neural Networks. 15:1063-1070. 2004.

64. Izhikevich, Eugene M., Polychronization: *Computation With Spikes*. Neural Computation. 18:245-28. 2006.

65. Herz, Andreas V.M. et al. *Modeling Single-Neuron Dynamics and Computations: A Balance of Detail and Abstraction*. Science. 314:80. 2006.

66. Chen, C.Y. and White, M. H. *Electrically Modifiable Nonvolatile Synapses for Neural Networks*. Solid-State Electronics, 30, 307. 1987.

67. Lee, I-Che, Tsai, Chun-Chien, Kuo, Hsu-Hang, Yang, Po-Yu, Wang, Chao-Lung, Cheng, Huang-Chung. *A novel sonos memory with recessed-channel poly-si TFT via excimer laser crystallization*. IEEE Electron Device Letters, v 33, n 4, p 558-560, April 2012.

68. Zhou, Xianda, Ng, Jacky C. W., Sin, Johnny K. O. *UIS analysis and* characterization *of the SONOS gate power MOSFET*. IEEE Transactions on Electron Devices, v 59, n 2, p 408-413, February 2012.

69. Li, Hua-Min, Zhang, Gang, Yoo, Won Jong. *Estimation of trapped charge density in SONOS flash memory using a parallel capacitor model*. IEEE Transactions on Electron Devices, v 58, n 10, p 3254-3259, October 2011.

70. Jang-Gn Yun , Yoon Kim, Il Han Park, Jung Hoon Lee, Sangwoo Kang, Dong-Hua Lee, Seongjae Cho, Doo-Hyun Kim, Gil Sung Lee, Won-Bo Sim, Younghwan Son, Hyungcheol Shin,Jong Duk Lee, Byung-Gook Park. *Fabrication and characterization of fin SONOS flash memory with separated double-gate structure*. Solid-State Electronics 52, 1498–1504. 2008.

71. Arreghini, A., Akil, N., Driussi, F., Esseni, D., Selmi , L., van Duuren, Michiel. *Long term charge retention dynamics of SONOS cells*. Solid-State Electronics 52. 1460–1466. 2008.

72. Yong Kyu Lee, Suk Kang Sung, Jae Sung Sim, Ki Whan Song, Jong Duk Lee, Byung-Gook Park, Sung Taeg Kang, Chilhee Chung, Donggun Park, Kinam Kim. *Scalable 2-bit silicon–oxide–nitride–oxide–silicon (SONOS) memory with physically separated local nitrides under a merged gate.* Solid-State Electronics 48. 1771–1775. 2004.

73. Van Den Bosch, G., Kar, G.S., Arreghini, A. Cacciato, A.; Breuil, L.; De Keersgieter, A.; Paraschiv, V.; Vrancken, C.; Douhard, B.; Richard, O.; Van Aerde, S.; Debusschere, I.; Van Houdt, J. *Highly scaled vertical cylindrical SONOS cell with bilayer polysilicon channel for 3-D nand flash memory.* IEEE Electron Device Letters, v 32, n 11, p 1501-1503, November 2011.

74. Luo, Cheng-Wei , Lin, Horng-Chih; Lee, Ko-Hui; Chen, Wei-Chen; Hsu, Hsing-Hui; Huang, Tiao-Yuan. *Impacts of nanocrystal location on the operation of trap-layer-engineered poly-Si nanowired gate-all-around SONOS memory devices.* IEEE Transactions on Electron Devices, v 58, n 7, p 1879-1885, July 2011.

75. Lin, Horng-Chih, Lin, Zer-Ming; Chen, Wei-Chen; Huang, Tiao-Yuan. *Read characteristics of independent double-gate poly-Si nanowire SONOS devices.* IEEE Transactions on Electron Devices, v 58, n 11, p 3771-3777, November 2011.

76. Breuil, L. Van *Den* Bosch, G.; Cacciato, A.; Date, L.; Kar, G.S.; Tang, B.; Arreghini, A.; Debusschere, I.; Van Houdt, J. *Optimization of gate stack parameters towards 3D-SONOS application.* Microelectronic Engineering, v 88, n 7, p 1164-1167, July 2011.

77. Sun, Y. , Yu, H.Y.; Singh, N.; Leong, K.C.; Lo, G.Q.; Kwong, D.L. *Junctionless vertical-si-nanowire-channel-based SONOS memory with 2-bit storage per cell.* IEEE Electron Device Letters, v 32, n 6, p 725-727, June 2011.

78. Shih, Chun-Hsing, Chang, Wei; Luo, Yan-Xiang; Liang, Ji-Ting; Huang, Ming-Kun; Chien, Nguyen Dang; Shia, Ruei-Kai; Tsai, Jr-Jie; Wu, Wen-Fa; Lien, Chenhsin. *Schottky barrier silicon nanowire sonos memory with ultralow programming and erasing voltages.* IEEE Electron Device Letters, v 32, n 11, p 1477-1479, November 2011.

79. Lin, Chia-Sheng, Chen, Ying-Chung; Chang, Ting-Chang; Jian, Fu-Yen; Li, Hung-Wei; Chen, Shih-Ching; Chuang, Ying-Shao; Chen, Te-Chih; Tai, Ya-Hsiang; Lee, Ming-Hsien; Chen, Jim-Shone. *Charge-trapping-induced parasitic capacitance and resistance in SONOS TFTs under gate bias stress.* IEEE Electron Device Letters, v 32, n 3, p 321-323, March 2011.

80. van Schaijk, Rob,van Duuren, Michiel, Mei, Wan Yuet, Jeugd, Kees van der, Rothschild, Aude, and Demand, Marc. *Oxide–nitride–oxide layer optimisation for reliable embedded SONOS memories*. Microelectronic Engineering. Vol 72. 395-398. 2004.

81. Duuren, Michiel Van, Akil, Nader, Boutchich, Mohamed, Golubovic, Dusan S. New *Writing Mechanism for Reliable SONOS Embedded Memories with Thick Tunnel Oxide*. 2008 IEEE International Conference on IC Design and Technology & Tutorial (ICICDT), p 181-4, 2008.

82. Asha, Rani. *Simulation and Modeling of SONOS Non-Volatile Memory*. A Thesis Submitted to the Graduate Faculty of George Mason University in Partial Fulfillment of The Requirements for the Degree of Master of Science Electrical Engineering. 2010.

83. Myung Kwan Cho and Dae M. Kim. *High Performance SONOS Memory Cells Free of Drain Turn-On and Over-Erase: Compatibility Issue with* Current *Flash Technology*. IEEE Electron Device Letters, Vol. 21, NO. 8, August 2000.

84. Clement H.-J. Wann and Chenming Hu. *High Endurance Ultra-Thin Tunnel Oxide for* Dynamic *Memory Application*. IEEE Electron Device Letters, v 16, n 11, p 491-493, Nov 1995.

85. White, M. H., Yang, Y., Purwar, A. and French, M. L. *A low voltage SONOS nonvolatile* semiconductor *memory technology*. IEEE Trans. Comp., Packag., Manufact. Technol. A, vol. 20, pp. 190–195, June 1997.

86. Libsch, F. R., White, M. H. *Charge Transport and Storage of Low* Programming *Voltage SONOS/MONOS memory devices*. Solid State Electronics, VOL. 33, No. 1, pp. 105-26, 1990.

87. White, M. H., Yang, Y. , Purwar, A. and French, M. L. *A low voltage SONOS nonvolatile semiconductor memory technology*. IEEE Trans. Comp., Packag., Manufact. Technol. A, vol. 20, pp. 190–195, June 1997.

88. Lee, Wen-Chin. *Modeling CMOS tunneling Currents Through Ultrathin* Gate *Oxide Due to Conduction- and Valence-Band Electron and Hole Tunneling*. IEEE Transactions on Electron Devices, vol. 48, no. 7, July 2001.

89. Stegemann, Bert . *Ultra-thin silicon dioxide layers on silicon: interface optimisation and characterisation at the atomic level* Galvanotechnik, v 101, n 10, p 2376-2385, October 2010.

90. Momose, H. S., Ono, M., Yoshitomi, T., Ohguro, T., Nakamura, S.-I., Saito, M. and Iwai, H. *1.5 nm direct-tunneling gate oxide Si MOSFETs.* IEEE Trans. Electron Devices, vol. 43, no. 8, pp. 1233–1242, 1996.

91. Shi, Y., Ma, T. P., Prasad, S. and Dhanda, S. *Polarity-dependent tunneling current and oxide breakdown in dual-gate CMOSFETs.* IEEE Electron Device Lett., vol. 19, no. 10, pp. 391–393, 1998.

92. Shi, Y., Ma, T. P. and Prasad, S. *Polarity dependent gate tunneling currents in dual-gate CMOSFETs.* IEEE Trans. Electron Devices, vol. 45,no. 11, pp. 2355–2360, 1998.

93. Lee, W.-C., King, T.-J. and Hu, C. *Evidence of hole direct tunneling through ultrathin gate oxide using P poly-SiGe gate.* IEEE Electron Device Lett., vol. 20, no. 6, pp. 268–270, 1999.

94. Tarr, N. G., Pulfrey, D. L., and Camporese, D. S. *An Analytic Model for the MIS Tunnel Junction.* IEEE Trans. Electron Devices, vol. ED-30, pp. 1760–1770, 1983.

95. Rana, F., Tiwari, S. And Buchanan, D. A. *Self-consistent modeling of* accumulation *layers and tunneling currents through very thin oxides.* Appl. Phys. Lett., vol. 69, no. 8, p. 1104, 1996.

96. Depas, M. , Vermeire, B., Mertens, P. W., Van Meirhaeghe, R. L., and Yeyns, M. M. *Determination of tunneling parameters in ultra-thin oxide layer poly-Si=SiO =Si structures.* Solid State Electron. vol. 38, no. 8, pp. 1465–1471, 1995.

97. Maserjian, J. and Zamani, N. *Behavior of the Si=SiO interface observed by* Fowler-*Nordheim tunnelling.* J. Appl. Phys. vol. 53, no. 1, pp. 559–567, 1982.

98. Brar, B., Wilk, G. D.and Seabaugh, A. C. *Direct Extraction of the Electron Tunneling Effective Mass in Ultrathin SiO.* Appl. Phys. Lett. vol. 69, no. 18, pp. 2728–2730. 1990.

99. Hill, I. G., Rajagopal, A., Kahna, A., and Hu, Y. *Molecular level alignment at organic semiconductor-metal interfaces.* Applied Physics Letters Volume 73, Number 5 3 August 1998.

100. Yang, C., Kwack, Y., Kim, S.H., An, T.K., Hong, K., Nama, S., Park, M., Choi, W.S., Park, C.E., *Ambipolar thin-film transistors and an inverter based on pentacene/self-assembled monolayer modified ZnO hybrid structures for balanced hole and electron mobilities.* Organic Electronics 12, 411–418. 2011.

101. Kitamura, M., Imada, T., Arakawa, Y. *Organic Transistor Circuits for Application to Organic Light-Emitting-Diode Displays* Jpn. J. Appl. Phys. Vol. 42, pp. 2483–2487 Part 1, No. 4B, April 2003.

102. Sakanoue, T., Yahiro, M., Adachi, C., Takimiya, K., Toshimitsu, A. *Electrical characteristics of single-component ambipolar Organic field-effect transistors and effects of air exposure on them*. J. Appl. Phys. 103, 094509 2008.

103. Yang, Chanwoo, Kwack, Youngjin, Kim, Se Hyun, An, Tae Kyu, Hong, Kipyo , Nama, Sooji, Park, Mijeong, Choi, Woon-Seop, and Park, Chan Eon. *Ambipolar thin-film transistors and an inverter based on pentacene/self-assembled monolayer modified ZnO hybrid structures for balanced hole and electron mobilities*. Organic Electronics 12, 411–418. 2011.

104. Klauk, Hagen, Gundlach, David J., Nichols, Jonathan A. and Jackson, Thomas N. *Pentacene Organic Thin-Film Transistors for Circuit and Display Applications.* IEEE Transactions on Electron Devices, Vol. 46, No. 6, June 1999.

105. Burroughes, J. H. Jones, C. A. Friend, R. H. *New semiconductor device physics in polymer diodes and transistors*. Nature, v 335, n 6186, p 137-141, Sep 8 1988.

106. Lee, Josephine B. and Subramanian, Vivek. *Organic Transistors on Fiber: A first step towards electronic textiles*. Technical Digest - International Electron Devices Meeting, p 199-202, 2003.

107. Kymissis, Ioannis, Akinwande, Akintunde I. *Organic Filed Emission Device Integrated with Organic Transistor*. IEEE Transactions on Electron Devices, v 52, n 8, p 1907-1914, August 2005.

108. Kitamura, Masatoshi, Imada, Tadahiro and Arakawa, Yasuhiko. *Organic Transistor Circuits for Application to Organic Light-Emitting-Diode Displays* Jpn. J. Appl. Phys. Vol. 42 (2003) pp. 2483–2487 Part 1, No. 4B, April 2003.

109. Cerdeira, A. Estrada, M. Garcia, R. Ortiz-Conde, A. Garcia Sanches, F.J. *New Procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions*. Solid State Electronics 45, 1077-1080. 2001.

110. Wong, William S., Ready, Steven E., Lu, Jeng-Ping and Street, Robert A. *Hydrogenated Amorphous Silicon Thin-Film Transistor Arrays Fabricated by Digital Lithography* IEEE Electron Device Letters, Vol. 24, No. 9, September 2003.

111. Kunigunde, H., Cherenack, Alex Z., Kattamis, Hekmatshoar, Bahman, Sturm, James C. and Wagner, Sigurd. *Amorphous-Silicon Thin-Film Transistors*

Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic 1004 IEEE Electron Device Letters, Vol. 28, No. 11, November 2007.

112. Shlimak, I. Friedland, K.-J., Kravchenko, S.V., Ginodman, V., Butenko, A., Klapwijk, T.M. *Longitudinal resistivity in the quantum Hall effect regime in a split-gate Si MOSFET with variable electron density*. Physica Status Solidi (C) Current Topics in Solid State Physics, v 5, n 3, p 839-841, 2008.

113. Akiya, M. and Nakashima, S.. *Novel Split-Gate MOSFET*. IEEE Transactions On Electron Devices, Vol. Ed-32, No. 3, March 1985.

114. Kranti, A., Chung, T. M., Flandre, D. and Raskin, J. P. *Laterally asymmetric channel engineering in fully depleted double gate SOI MOSFETs for high performance analog applications*. Solid State Electron., vol 48, no. 6, pp.947-959, 2004.

115. Long, W., Ou, H., Kuo, J.-M. and Chin, K. K. *Dual-Material Gate (DMG) Field Effect Transistor*. IEEE Trans. Electron Devices, vol. 46, no. 5, pp. 865-870, 1999.

116. Baishay, S. , Mallik, A., and Sarkar, C. K. *A Pseudo Two-Dimensional Subthreshold Surface Potential Model for Dual-Material Gate MOSFET*. IEEE Trans. Electron Devices, vol. 54, no. 9, pp. 2520-2524, 2007.

117. Tsormpatzoglou, A, Dimitriadis, C. A., Clere, R., Rafhay, Q., Pananakakis, G. and Ghibaudo, G. *Semi-Analitical Modeling of Short-Channel Effects in Si and Ge Symetric Double-Gate MOSFETs*. IEEE Trans. Electron Devices, vol. 54, no. 8, pp. 1943-1951, 2007.

118. Hosseini, S . E., Tarbiat, Sabzevar. *Split gate SOI MOSFET with Drain Dependent Bias for Short Channel Effects Reduction*. 2009 International Conference on Signal Processing Systems. 978-0-7695-3654-5/09. 2009.

119. Wojcik, J., Roschuk, T., Zalloum, O.H.Y., Heng, C.L., lakie, D.E., Knights, A.P., Mascher, P. *Fabrication and characterization of silicon nanostructures for integration in photonics devices and circuits*. P.1. SVC 50th Annual Technical Conference Proceedings, 344-7, 2007.

8   APPENDIX A. DIGITAL NEURAL NETWORKS

This appendix contains a paper accepted for publication at the time of writing for the SPIE conference proceedings for Photonics North 2012. Significant background investigations of the implementation of digital neural networks were undertaken as part of this research. This paper covers some of this background work.

8.1   Digital Implementation of a Neural Network for Imaging

Digital Implementation of a Neural Network for Imaging

Richard Wood[1], Alex McGlashan[2], Jay Yatulis[2], Peter Mascher[1], and Ian Bruce [3]

[1] Department of Engineering Physics and the Centre for Emerging Device Technologies, McMaster University, Canada,
[2] Photonics Engineering Technology, Niagara College, Canada,
[3]Department of Electrical and Computer Engineering, McMaster University, Canada

This paper outlines the design and testing of a digital imaging system that utilizes an artificial neural network with unsupervised and supervised learning to convert streaming input (real time) image space into parameter space. The primary objective of this work is to investigate the effectiveness of using a neural network to significantly reduce the information density of streaming images so that objects can be readily identified by a limited set of primary parameters and act as an enhanced human machine interface (HMI). Many applications are envisioned including use in biomedical imaging, anomaly detection and as an assistive device for the visually impaired. A digital circuit was designed and tested using a Field Programmable Gate Array (FPGA) and an off the shelf digital camera. Our results indicate that the networks can be readily trained when subject to limited sets of objects such as the alphabet. We can also separate limited object sets with rotational and positional invariance. The results also show that limited visual fields form with only local connectivity.

Keywords: Neural Network, imaging, digital, FPGA, parameter space, human machine interface, HMI

Introduction

The field programmable gate array (FPGA) is a useful prototyping device in general for digital designs and is ideal for the development of a neural network device. Neural networks have been designed in FPGAs with many examples available [1-12]. These provide a reasonable starting point. The nature of the boards allows for the development of firing rate based neural networks or standard weight based matrices (a combination of the two is also possible).

The cited previous work [1-12] has been used as the initial template for the design of the present neural processing system and a brief overview of these systems is given. The overall system structure follows that proposed by Savran et al. [1], as shown in Figure 1. Here, a state machine controls the mode that the system is in (learning, operating, etc.). It also controls the timing between network units (between aspect and decision space for example). This timing control is critical due to the overall system architecture. That is, the system uses the advantages of the digital FPGA by converting a parallel neural network into a sequential system. Although a true parallel system could be designed, it would be cumbersome and difficult to implement as the nature of digital prototyping devices is inherently serial. In the system shown in Figure 2 [1], in normal operating mode, each input is sequentially modified by a given synaptic weight with the result added to an accumulator. The output of the accumulator is then filtered. All the data and the weights are digitized and will have a limited resolution based on this digitization (Typically 0-127 settings, although resolution higher than 8 bits is possible if required). Only when the entire layer is modified, can the system switch to the next layer, hence, the criticality of the aforementioned timing via the state machine. This conversion to a sequential mode is feasible due to the high clock speed of digital processors (GHz).
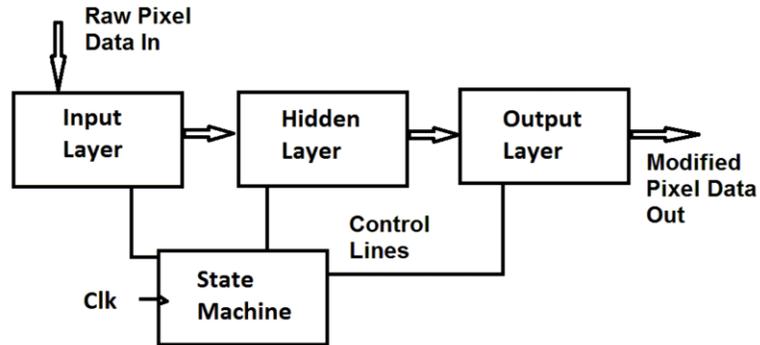
Figure 1. Digital Neural System Architecture. A state machine controls the sequencing between neural layers.
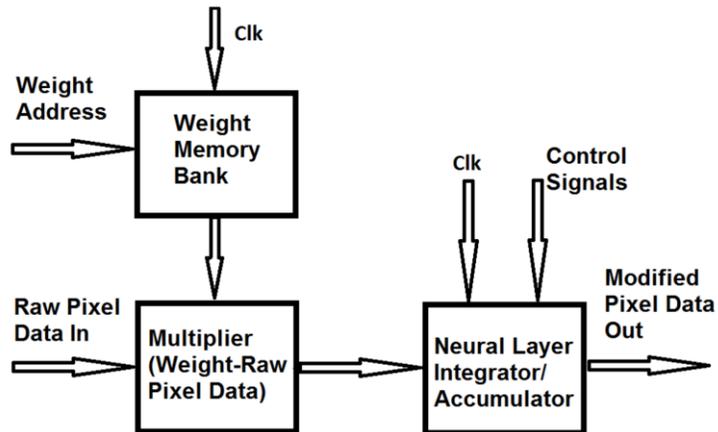
Figure 2. Single Neuron Schematic. Each pixel is modified by the weights and is integrated in an accumulator.

The basic learning configuration is shown in Figure 3 [2]. Here a separate module exists to modify the synaptic weights. This unit must also be controlled by the state machine, which can enable the learning cycle and back propagation. As shown in Figure 3, teaching signals can be taken from an external source. Unsupervised learning can also be used without the teaching signals. In this case an autocorrelation function of the output (and or input) signals can be generated in the learning unit.

Figure 1. Learning Configuration. Teaching data required for supervised learning.
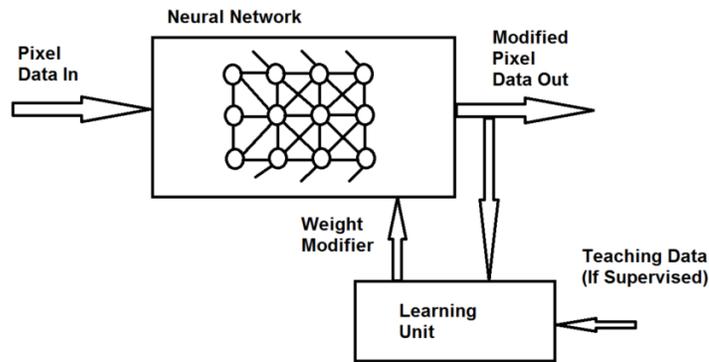
There are various aspects to neural learning. A brief description is included here to illustrate the relevant aspects of Hebbian learning. In the simplest form, Hebbian learning will occur when a neuron fires and in turn a connected neuron fires in sequence, then the synapse between these neurons is strengthened. In the matrix shown in Figure 4, the weights are modified by the relation $\tau_w\, dw/dt = vu$ where the rate of change of the weights depends on whether the output neuron fires in time with the given input u. The learning rate is also modified by the constant τ_w.

In a modified Hebbian system, synapses can also be weakened between neurons that do not fire. In a system of neurons, the synapses will require some form of normalization to prevent a synaptic overload. Unsupervised learning for self-organization is possible with this basic premise. This will require the system to operate under four simple rules, Figure 5 [13]. First, the system follows the basic Hebbian premise. Second, the system follows a winner take all scenario. Third, there is cooperative interaction between neurons. Lastly, structure information is required in the training process. This simple Hebbian
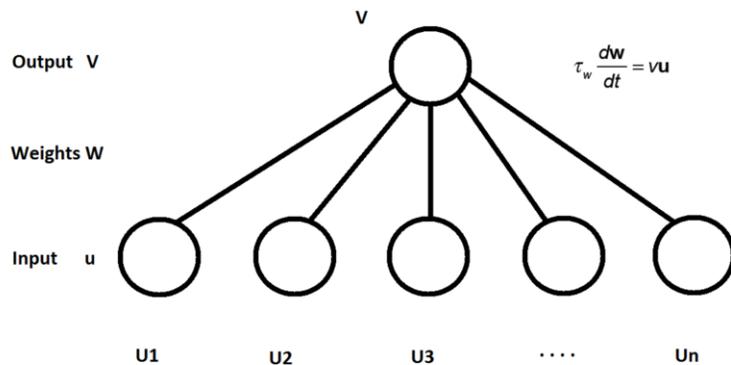

Figure 2. Simple neuron system with the Hebbian learning formula $\tau_w\, dw/dt = vu$. Shown is one output neuron and 5 input neurons, Un and 5 weights, W.
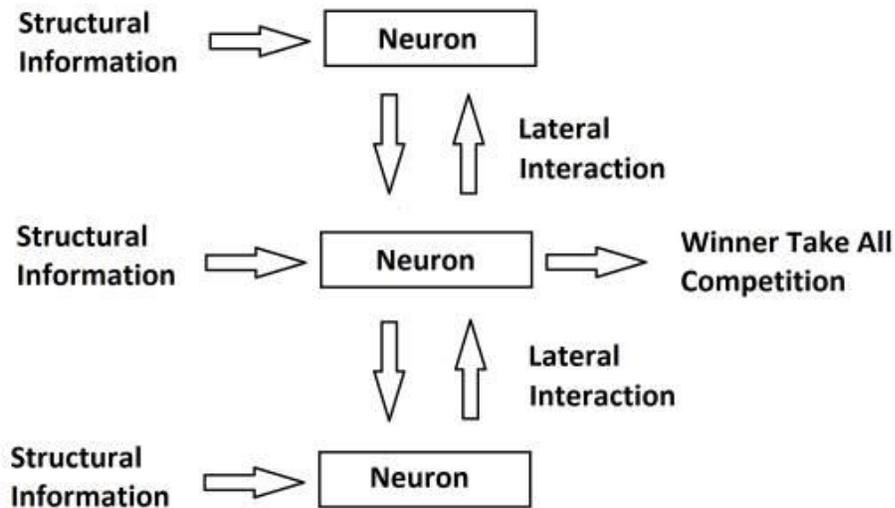
Figure 1. Self-Organization. Requires structural information, lateral interaction and a winner take all system with Hebbian learning.

Methodology

As part of the background examination of digital neural networks, several digital versions were generated for the current analysis. In particular, a simple visual neural field was created that was able to identify simple objects, such as letters and numbers, using the serial implementation of a weighted neural matrix. A 20 x 20 pixel imaging space was designed and implemented on an Altera DE2 prototyping FPGA board with a simple paired (both inhibitory and excitatory neurons) layer to convert streaming images into parameter space(s). Several parallel processing units were produced to examine the ability of the system to learn to identify various parameters such as texture, color, and edges. Each neural processing unit was compared in parallel to standard image processing routines for texture, color and edge detection. In addition, a character identification system was constructed to convert letter images into parameter space, Figure 6. In this case, the 26 letters of the Roman alphabet are converted into 10 parameters (Table 1). In this case the parameters are imposed but could also be self-assigned by the system.

The learning of the system was conducted by exposing the neural network to randomly selected images (from a limited set of rotated images of individual characters). Both supervised and unsupervised learning was examined.
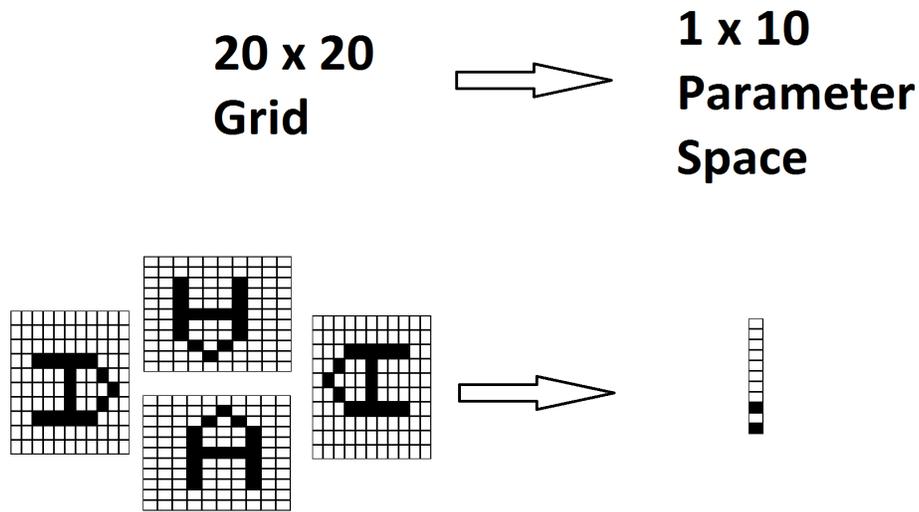
Figure 1. Character Space Conversion to Parameter Space.

Table 1. Parameters for Roman Characters

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
small curve	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0
2 vertical ends	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	0
cross	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	0
one diagonal line	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	1
2 horizontal line	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1
2 line segments	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0
large curve	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
external point	1	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1
horizontal ends	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1
intersection-3	1	1	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0	0	0	1	1	0

Results and Discussion

A representative plot of a single 20 x 20 neural mesh is shown in Figure 7. Shown is a mesh from a character space to a single parameter space routine (there are 10 sets of these in the case of the character space conversion). Our initial results indicate that the network can be used to identify characters through the conversion to parameters, which are predominantly orientationally invariant. The network was found to be generally comparable to human recognition of characters, limited by extremes of orientation.
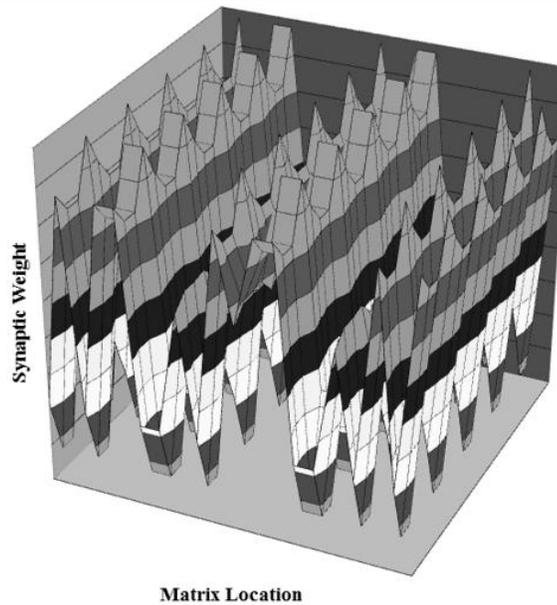
Figure 7. Representative Synaptic Weight Distribution

In Figure 8 a, b, c, an abdominal image is shown after conversion into various parameter spaces using neural processing subroutines. A representative image of a neural network edge detection routine is shown in Figure 8a. Here the image is differentiated into three parts; foreground, background and edges. This routine was trained to recognize vertical, horizontal, and diagonal edges. A black and white version of the edge detection routine, showing a converted angiogram, is shown in figure 8d. The texture analysis neural subroutine of the abdominal image is shown in figure 8b. Here the texture of the image has been converted into a greyscale representation of the 20 x 20 image area. The texture analysis routine was trained to distinguish repeating parallel lines by subjecting the imaging routine to randomly oriented lines with varying spatial frequencies. A representative image of the color conversion neural routine is shown in Figure 8c.

These reduced information spaces were examined for ease of recognition. As with the character to parameter conversion system, this network was found to be generally comparable to human recognition of objects, again limited by extremes of orientation.
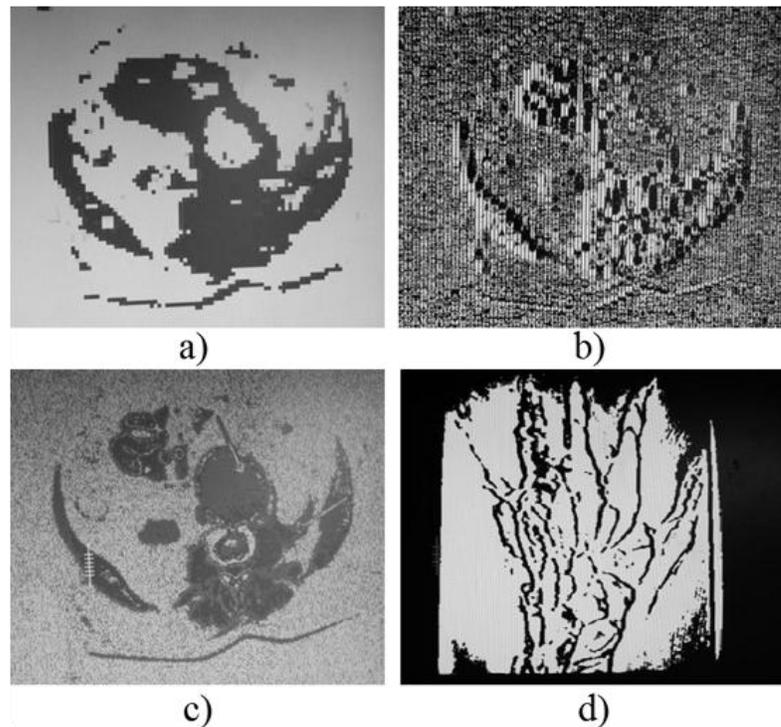
Figure 8. Image Conversion Results. a) Edge Detection. b) Texture c) Color Separation d) Angiogram Conversion.

Conclusions

Our initial results indicate that our digital Neural Network can be trained to convert streaming images to parameter space (corners, colors, texture) and has been found to be consistent with the limitations of human recognition of characters and objects. Our next steps are the quantitative evaluation of the network through comparison with a sample set of human subjects. Our main objective is the enhancement of human machine interfaces (HMI) by developing systems that parallel and enhance human visual recognition systems. These developed digital preprocessor routines can then be enhanced through the addition of additional recognition and action systems with enhanced memories.

Acknowledgments

References

[1] Savran, A. and Ünsal, S., "Hardware Implementation of a Feedforward Neural Network Using FPGAs," Lecture Notes in Computer Science v 4234 LNCS – III, 1095-1104 (2006)

[2] Maeda, Y. and Tada, T., "FPGA Implementation of a Pulse Density Neural Network With Learning Ability Using Simultaneous Perturbation," IEEE Transactions on Neural Networks VOL. 14, NO. 3, (2003)

[1] Ali, H. K. and Mohammed, E.Z., "Design Artificial Neural Network Using FPGA," IJCSNS International Journal of Computer Science and Network Security, VOL.10 No.8, (2010)

[2] Sahoolizadeh, H., Keshavarz, A., and Tadbir, B., "A FPGA Implementation of Neural/Wavelet Face Detection System," Australian Journal of Basic and Applied Sciences 4(3), 379-388 (2010).

[3] Brassai, S. T., László, D., and László, B., "Hardware Implementation of CMAC-based Artificial Network with Process Control Application," Scientific buletin of the Politehnica University of imisoara, 209-213 (2004).

[4] Jilani, S., Abdul K., and Sattar, S. A., "JPEG Image Compression using FPGA with Artificial Neural Networks," IACSIT International Journal of Engineering and Technology, Vol.2, No.3, (June 2010)

[5] Letendre, J. and Zhou, Z., "Artificial Neural Network," DSD Project Final Report. (2010)

[6] Silva, M. L., Ferreira, J. C., Run-time generation of partial FPGA configurations for subword operations," Microprocessors and Microsystems, v 36, n 5, 365-374 (2012)

[7] Bellis, S., Razeeb, K. M., Saha, C., Delaney, K., O'Mathuna, C., Pounds-Cornish, A., de Souza, G., Colley, M., Hagras, H., Clarke, G., Callaghan, V., Argyropoulos, C., Karistianos, C., and Nikiforidis, G., "FPGA Implementation of Spiking Neural Networks - an Initial Step towards Building Tangible Collaborative Autonomous Agents." Proceedings - 2004 IEEE International Conference on Field-Programmable Technology, FPT '04, 449-452 (2004)

[8] Lee, Y., and Ko, S. B., "FPGA implementation of a face detector using neural networks," Canadian Conference on Electrical and Computer Engineering, 1914-1917 (2007)

[9] Raeisi, R., Kabir, A., "Implementation of Artificial Neural Network on FPGA," American Society for Engineering Education March 31-April 1, (2006).

[10] Lina, C. J., and Tsaib, H. M., "FPGA implementation of a wavelet neural network with particle swarm optimization learning," Mathematical and Computer Modeling 47, 982–996 (2008)

[11] Haykin, Simon, [Neural Networks and Learning Machines]. Pearson Education Inc. 2009.