ELECTRICAL TRANSPORT PROPERTIES OF MIS AND SIS STRUCTURES

ELECTRICAL TRANSPORT PROPERTIES OF METAL-INSULATOR-SEMICONDUCTOR (MIS) AND SEMICONDUCTOR-INSULATOR-SEMICONDUCTOR (SIS) STRUCTURES

By

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SCOPE AND CONTENTS: The major purpose of the work presented in this thesis has been to consider some important electrical transport properties of Metal-Insulator-Semiconductor (MIS or MOS) and Semiconductor-Insulator-Semiconductor (SIS) diodes.

In particular the d.c. tunnel current-voltage characteristics of the MIS diode are studied and shown to divide naturally into two categories corresponding to the state of equilibrium of the semiconductor of a diode. In "equilibrium" diodes the carrier distributions in the semiconductor are effectively maintained in thermal equilibrium despite the presence of d.c. current flow. I-V characteristics of a range of this type of diode are presented and analyzed. Tunnel induced non-equilibrium conditions in the semiconductor are also investigated and shown to have visible effects on the I-V characteristics of the MIS tunnel diode.

These effects are seen to be functions of oxide thickness, minority carrier supply rate and doping density.

The tunnel currents of both "equilibrium" and "non-equilibrium" diodes are analyzed by comparison with a comprehensive finite temperature tunnel theory. Employment of numerical techniques permits the inclusion in these calculations of the effects of a two band model of the insulator, image force potentials in the barrier and space charge tunneling.

A practical application of the properties of the "non-equilibrium" diode in the form of a new type of active device, the Surface Oxide Transistor (SOT), is demonstrated. The characteristics of such structures are investigated and models of their operation proposed.

The final work presented in this thesis deals with a new type of barrier dominated semiconductor structure, the SIS diode. The capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics of thick oxide diodes of this type are presented and compared with theory. A wide range of interesting characteristics are observed. The d.c. current-voltage behaviour of the SIS tunnel diode, while not studied experimentally, is compared qualitatively with that of the MIS tunnel diode.

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CHAPTER 1

INTRODUCTION

The electrical transport mechanism of principal interest in this thesis is that of tunneling in solids. The theory of tunneling predicts that charge carriers in an allowed state in one material have a finite probability of making the transition through an intervening classically forbidden region to an allowed state in a second, possibly dissimilar, material. Interest in tunneling phenomena has existed since the initial application by Oppenheimer in 1928 of quantum-mechanical tunnel theories to describe the autoionization of the excited states of atomic hydrogen in a strong electric field [1]. Only within the last fifteen years, though, with the discovery of the p-n tunnel diode [2], has research on tunneling received the necessary impetus from private enterprise to make this field realize its potential as one of the most important in solid state physics [3].

A great deal of basic research is possible by means of what has come to be known as tunneling "spectroscopy". This new form of spectroscopy employs the tunneling charge carrier from a metal, for instance, to scan in energy the band structure of a second electrode. Any interactions that occur within the intervening insulator or in the second electrode will generally have a noticeable effect on the

current-voltage (I-V) or conductance-voltage (G-V) characteristics of the diode. Employing a metal-insulator-metal (MIM) structure with one superconducting metal electrode, I. Giaever [4] was able to observe directly for the first time, the superconducting energy gap of lead by means of tunneling spectroscopy.

A natural outcome of this interest in tunneling spectroscopy has been research into metal-insulator-semiconductor (MIS) tunneling. This work divides naturally into two categories: studies of the tunnel current interactions with phonons and impurities in the semiconductor or insulator [5], and studies of the basic tunnel currents themselves and their interaction with the semiconductor energy gap [6-9]. A major part of this thesis is devoted to a presentation of research of the latter type with the intention of providing a more thorough understanding of MIS tunnel currents than has been obtained to date.

The most widely applied theory for calculating tunnel currents in barrier dominated structures, such as the MIS diode, is the independent particle model of Harrison [10]. Such an approach is also adopted in this thesis. In the past, numerous approximations have been made concerning the barrier and semiconductor in order to reduce the general tunnel current expressions of this model to an analytic form suitable for calculations. Use of numerical techniques in

performing the necessary integrations, allows many of these approximations to be eliminated in this work. The remaining approximations are examined in Chapter 2 for their effects on the I-V characteristics of a typical MIS tunnel diode. Also included in this chapter is a discussion of the theoretical effects of surface states on these current-voltage characteristics.

In Chapter 3 the experimentally observed I-V characteristics of a number of "equilibrium" diodes are compared with theory. The use of the term "equilibrium" in this sense is meant to signify that, despite the presence of current flow in the diode, a single Fermi level is sufficient to characterize the charge densities in the semiconductor. In devices where current flow results in a split of the Fermi energy into two "quasi" Fermi levels the term "non-equilibrium" diode will be employed [11]. The I-V characteristics of such "non-equilibrium" devices are presented in Chapter 4. The effects of the injection of excess minority carriers on both "equilibrium" and "non-equilibrium" diode characteristics are also considered.

One of the distinguishing features of the "non-equilibrium" diode employing a non-degenerate semiconductor is a saturating I-V characteristic whose current magnitude is controlled by the minority carrier supply rate in the semiconductor. Such control offers the possibility that

transistor action might be obtained with such diodes [12]. In Chapter 5 the properties of a three terminal transistor structure based on the "non-equilibrium" diode are investigated.

Another insulator-dominated structure for which interesting I-V characteristics have been theorized [13-15] is the semiconductor-insulator-semiconductor (SIS) diode. While attempts made to fabricate these thin oxide devices have as yet not been successful, thick oxide SIS diodes were constructed and studied [16-18]. The a.c. transport properties of these structures are presented in Chapter 6. The expected d.c. characteristics of the SIS tunnel diode are also discussed and examples of theoretical I-V characteristics given.

CHAPTER 2

THEORETICAL CONSIDERATIONS CONCERNING MIS TUNNEL CURRENTS

2.1 Introduction

A common approach to tunneling phenomena, due to Harrison[10], has been to view these effects in terms of the transition of electrons across the barrier. This is as opposed to the earlier (essentially equivalent) view of electron flows in terms of the transmission of electron waves through the barrier. To promote electronic transitions, it is necessary to introduce a tunneling term in the Hamiltonian of the system. Where such a term is lacking (e.g., in MIS systems with thick insulators) the total Hamiltonian contains only the two terms - H_1 and H_2, describing materials 1 (the metal) and 2 (the semiconductor). Associated with these terms are the eigenstates ψ_1 and ψ_2. For insulators in which tunneling is appreciable, ψ_1 and ψ_2 will have a considerable overlap. A new solution of Schrodinger's equation for the system is necessary, involving linear combinations of ψ_1 and ψ_2. The complete one-electron Hamiltonian is then written as

$$H = H_1 + H_2 + H_T$$

where H_T is defined by its matrix element $M_{k_1k_2}$ and k_1k_2 are the labels of the eigenstates. In this situation, the Hamiltonian H_T is treated as a perturbation permitting the probability of a transition, P_{12}, to be calculated with perturbation theory. The details of such a calculation are reviewed in Appendix A. It is seen in this appendix that the transition probability P_{12} can be defined in terms of a transmission coefficient, D(E), times the frequency with which the electron in state k_1 or k_2 strikes the oxide barrier. The current expression for J_T, the total tunnel current, is then shown to be

$$J_T = \frac{4\pi qm}{h^3} \iint [f_2 - f_1] D(E - E_T) dE dE_T \qquad 2.1$$

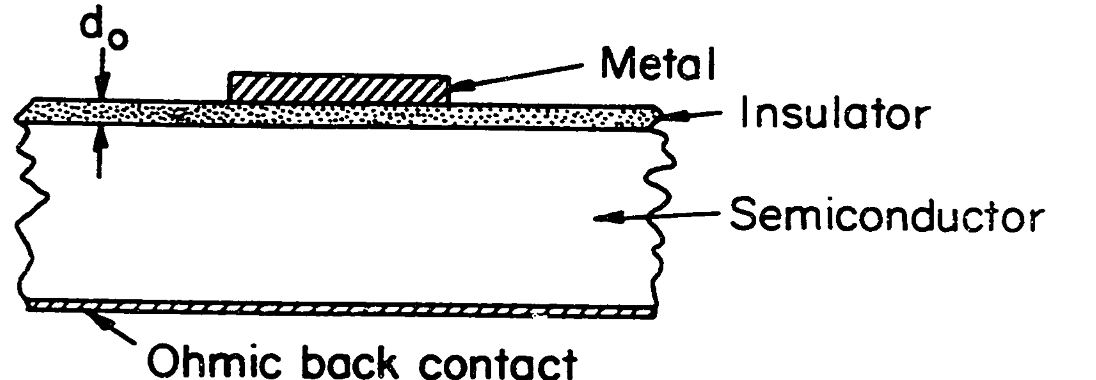
where m and q are the mass and charge of an electron, h is Planck's constant, and f_1, f_2 are the probability of occupation of states 1 and 2 respectively. The energies E and E_T are the total and transverse energies respectively. The latter quantity is the energy associated with motion parallel to the insulator.

It has been noted by Duke [3b] that an evaluation of most proposed "experimental tests" of the validity of equations such as 2.1 is difficult. This difficulty has been due in part to the fact that "experimental results are seldom compared directly with the consequences" of equations such as 2.1. Rather, an approximate evaluation of the

equation is attempted and these results compared to the data. We have tried to avoid this difficulty by making as few approximations in the evaluation of Eq. 2.1 as possible. This was accomplished by performing many of the integrations associated with this equation by numerical techniques. The remaining assumptions are necessary to rework Eq. 2.1 into a form suitable for the application of numerical techniques. In Sec. 2.2 the assumptions inherent in the WKB and WFM (wave function matching) approaches to the calculation of D(E) are discussed and the differences between both methods as seen in the I-V characteristics of typical diodes, examined. In Sec. 2.3 the model of the insulator employed is presented and the effects on diode characteristics of insulator band structure, insulator thickness and image forces considered. The assumptions associated with our model of the semiconductor are discussed in Sec. 2.4. The problems arising from the effects of semiconductor band structure and band tailing in degenerate semiconductors are considered, as well as the effects of field penetration of metal and semiconductor electrodes. Finally the model employed in the calculation of surface state tunnel currents is discussed in Sec. 2.5 and examples given of the various effects of surface states on the total observed tunnel current.

Before proceeding with the actual calculation of the I-V characteristics of a diode, it seems wise to describe the MIS system under consideration and to define the numerous, different tunnel currents that can flow in this system. A cross-sectional view of a typical MIS structure is shown in Fig. 2.1a along with the corresponding energy band picture of the structure (Fig. 2.1b). The type of MIS diode considered experimentally for this thesis consisted of various metals brought into intimate contact with thin insulators of SiO_2 thermally grown on polished silicon surfaces. The tunnel currents J_{mc}, J_{mv}, etc., which can pass through the insulator, are defined .. Fig. 2.1b by horizontal arrows (indicating equi-energy processes). The subscripts of these currents, m, c, v and s, refer to the metal, semiconductor conduction band, semiconductor valence band and surface states respectively. The direction of the arrows and order of the subscripts indicate the direction of electron flow. Thus a current designated 'J_{mc}' would imply a flow of electrons from the metal to the semiconductor conduction band. Hole currents are assumed for convenience to be electron flows in the opposite direction.

In an MIS diode with an ideal, defect free, insulator, the total current will be the sum, J_T, of all band currents, where



a

b

Fig. 2.1a Cross-sectional view of typical MIS diode

b Energy band diagram of MIS diode defining various tunnel current components

$$J_T = J_{mc} + J_{mv} + J_{cm} + J_{vm} \quad . \qquad 2.2$$

In experimental diodes, states exist at the I-S interface with energies in the semiconductor forbidden energy gap. The introduction of these surface states permits two more tunnel currents, J_{ms} and J_{sm} to flow. The necessary coupling between these states and the semiconductor conduction and valence bands is provided by the classical recombination-generation currents J_{cs}, J_{sc} and J_{vs}, J_{sv}. The total surface state current can, therefore, be defined as

$$J_{ss} = (J_{ms} + J_{sc} + J_{sv}) + (J_{sv} + J_{sc} + J_{sm}) \quad . \qquad 2.3$$

Each of these component tunnel currents can be evaluated, in principle, by an application of Eq. 2.1.

We will now proceed with our discussion of the approximations employed in the evaluation of MIS tunnel currents from Eq. 2.1. A detailed comparison of the resulting I-V characteristics with experimental data will be left until the next chapter.

2.2 The WKB and WFM Approximation

A number of different approaches have been employed to calculate the transmission coefficient D(E). Most are discussed by Duke in his book [3] and will, therefore, not be reviewed here. Elaborate formalisms and sophisticated barrier Hamiltonians have been proposed to handle the complications arising from electron-electron or electron-phonon interactions. Yet despite the sophistication of these approaches the functional form of the resulting current equation is basically quite similar to the historically first and definitely simplest approach, the WKB method. For this reason we have chosen to use a simple generalized WKB method, comparing it only with the WFM (wave function matching) approach.

In making the WKB approximation, it is assumed that the junction potential changes slowly over distances of the order of the electron's wavelength. This is as opposed to the assumption of an abrupt junction for the WFM calculation, where potential changes occur over distances small in comparison with the electron's wavelength. For silicon, with its indirect band gap, the wavelength of the conduction band electrons (at the band minimum) is typically 6 Å. This is also the wavelength of electrons near the Fermi-surface of

aluminum, a commonly employed metal electrode in this work. The wavelengths of valence band electrons at the band maximum ($k_{2V} = 0$) are considerably longer. In either case, the junction potential at the interface can be expected to change rapidly over distances of the order of these wavelengths. A WFM treatment should, therefore, be more accurate, particularly for the valence band carriers.

The expression for the tunnel probability D(E), obtained by the WFM procedure (Appendix A) is

$$D(E) = 4\pi^2 |M_{12}|^2 \rho_1 \rho_2$$

$$= \frac{16\left[\frac{m_1}{k_1} \frac{m_2}{k_2} \left(\frac{m_b}{k_b}\right)^2\right]}{\left[\left(\frac{m_1}{k_1}\right)^2 + \left(\frac{m_b}{k_b}\right)^2\right]\left[\left(\frac{m_b}{k_b}\right)^2 + \left(\frac{m_2}{k_2}\right)^2\right]}$$

$$\times \exp\left[-2 \int_{x_1}^{x_2} \eta_b \, dx\right] \quad . \qquad 2.4$$

Employing the WKB approximation (Appendix A), D(E) becomes

$$D(E) = 4\pi^2 |M_{12}|^2 \rho_1 \rho_2 = \exp\left[-2 \int_{x_1}^{x_2} \eta_b \, dx\right] \quad . \qquad 2.5$$

In Eqs. 2.4 and 2.5, k_1 and k_2 are the momentum vectors of the charge carrier in the metal and semiconductor with m_1 and m_2, the corresponding masses. η_b is the attenuation constant in the insulator. These quantities along with the average mass m_b and average k vector k_b for the barrier are defined in Appendix A. Figure 2.2 is used to define the various energies and potentials involved in these definitions.

The theoretical I-V characteristics for an MIS diode with an n-type semiconductor (silicon) of doping density $N_D = 10^{21}/m^3$ (an N_{21} diode) and a P_{26} diode are presented in Fig. 2.3. The details of the calculational method are given in Appendix B. In each case two current-voltage characteristics are shown, one calculated with the WKB tunnel probability (solid lines) and one with the WFM tunnel probability (dashed lines). In presenting these characteristics we have chosen to normalize all currents to the current magnitude at -1.5 V. Magnitude differences between the various I-V characteristics are, therefore, ignored and only relative curve shapes compared. This is done because of the uncertainties involved in determining for experimental diodes, the values of d_T, the oxide tunnel thickness, and A, the effective diode area. Such uncertainties make absolute magnitude comparisons quite difficult.

The WKB and WFM approaches both give essentially identical curve shapes for the I-V characteristics of the N_{21} diode (curve a). The scale factors for determining the

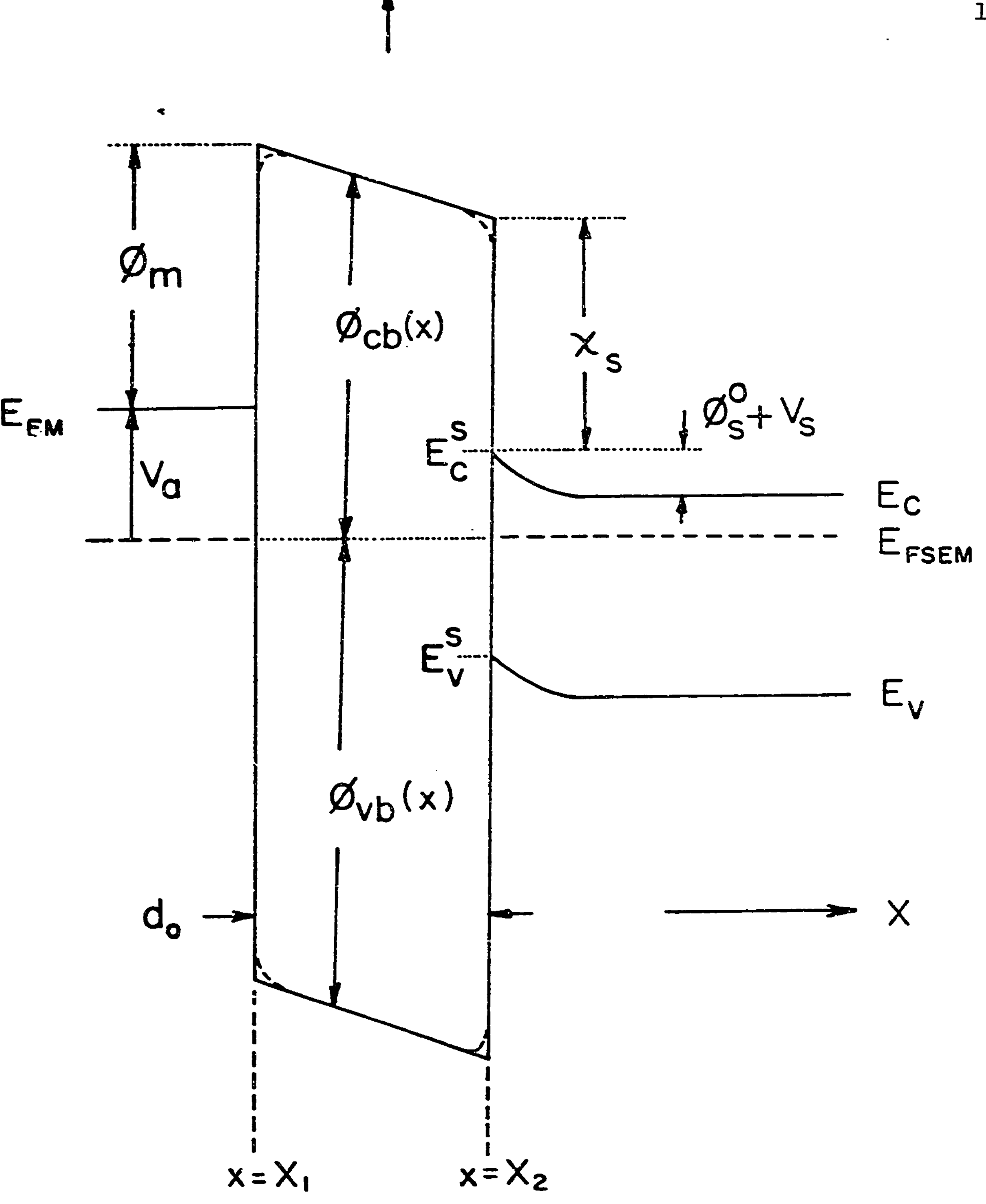


Fig. 2.2 Energy band diagram defining physical parameters associated with the MIS diode

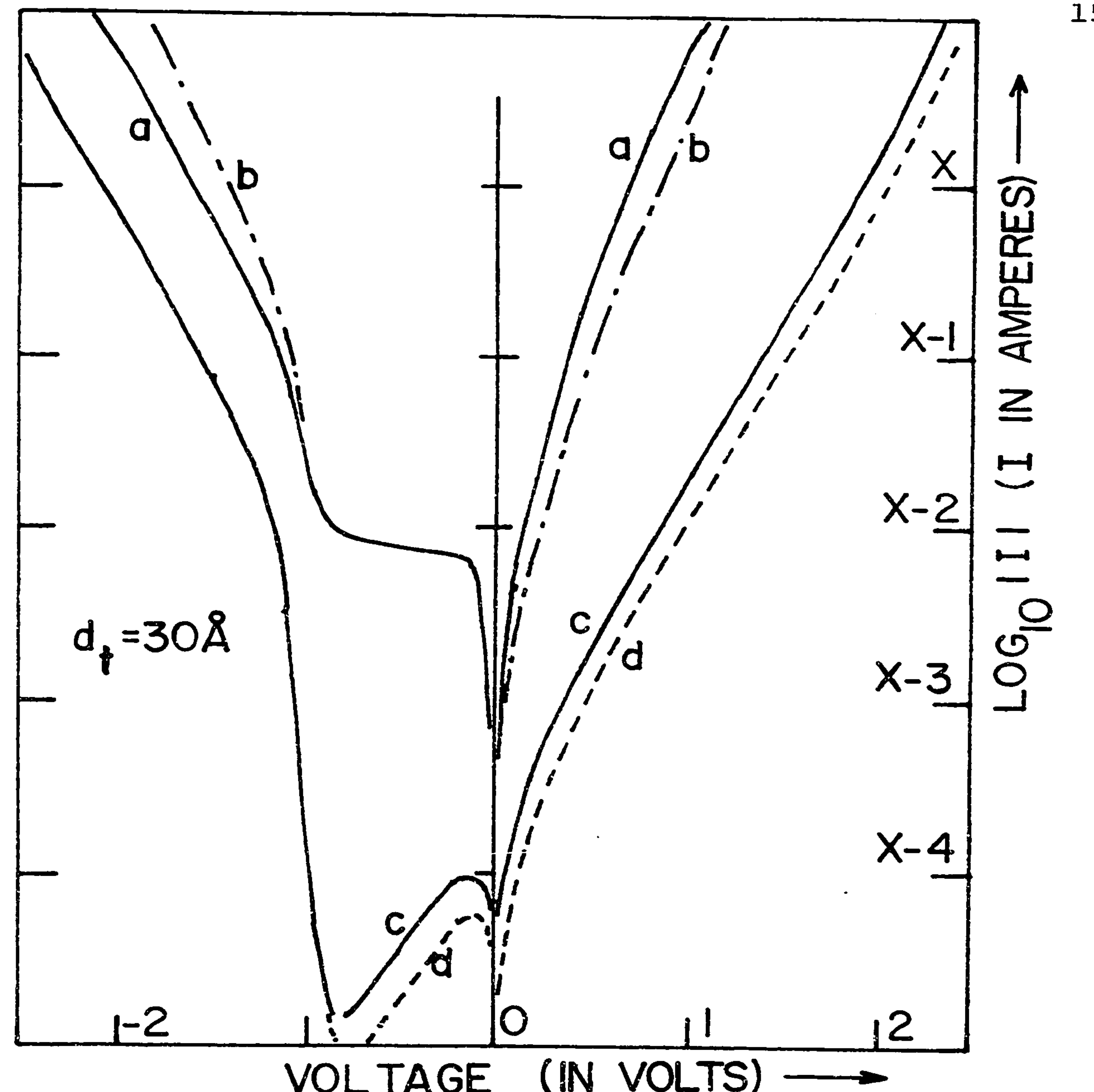


Fig. 2.3 Normalized log I-V characteristics of an N_{21} (curves 'a' and 'b') and P_{26} (curves 'c' and 'd') diode with d_T = 30 Å. For normal silicon diodes, curves 'a' and 'c' (curves 'a' and 'd') calculated with WKB (WFM) tunnel probability. The corresponding scale factors for the N_{21} diode are X = -9 (WKB) and X = -10 (WFM) and for the P_{26} diode are X = -8 (WKB) and X = -9 (WFM). Curve 'b' is calculated for a hypothetical direct band gap silicon N_{21} diode (i.e., k_0 = 0 in Eq. A.32)

absolute magnitude of these currents are given by X = -9 and X = -10 respectively. For the P_{26} diode, the WKB method gives curve c and the WFM method gives curve d. It will be seen later, that in the voltage regions where c and d differ, the currents J_{mv} or J_{vm} dominate. It is the small values of momentum vector the carriers of these currents have in the semiconductor, that result in the observed differences between curves c and d in Fig. 2.3. Currents comprised of carriers with larger k vectors in the semiconductor (i.e., J_{cm} and J_{mc} in the N_{21} diode) show little dependence of curve shape on the coefficient of the exponential in Eq. 2.4. It is interesting to note that even where differences in curve shape do appear they are quite small and really only detectable by comparing the relative magnitudes of the positive and negative bias branches of the curve. Such comparisons are made in a later chapter when fitting experimental data with theory and tend to favour the WFM approach as the better approximation.

To illustrate this point further, the I-V characteristics were calculated for an N_{21} diode of identical physical specifications but with a direct band gap semiconductor (i.e., $k_0 = 0$ in Eq. A.32). The results obtained by the WFM approach are shown in Fig. 2.3 as well (i.e., curve b). The WKB curves were identical, of course, to those obtained for the first N_{21} diode (curve a). It can

be seen that for a direct band gap N_{21} diode, the current-voltage curves also show differences in relative curve shape induced by the coefficient of the exponential term in the WFM current expression (Eq. 2.4). These differences are comparable to those seen with the P_{26} diode.

2.3 The Model of the Insulator

2.3.1 The Effects of Insulator Band Structure

In calculating the I-V characteristics shown in Fig. 2.3 a one band model of the insulator was assumed. In this model the insulator conduction band (assumed to be parabolic in k) is extended into complex k space [19-20]. The linear relation resulting between E and k_b^2 is then assumed to hold for all energies of interest. Such a one band model for experimental diodes is somewhat suspect in view of the theoretical findings of Schnupp [21]. Employing a Kronig-Penney model of the insulator, Schnupp determined the $E(k^2)$ dependence in an insulator of an MIM system with an arbitrary number of crystal planes in the insulator's width. For more than 10 planes he found that a two band model of the insulator was appropriate with a different mass associated with each band edge. More importantly, for any more than a single plane, pronounced deviations from linearity in the derived $E(k^2)$ curve were present. Thus for devices with all but the very thinnest of insulators, two band effects will probably be present in the I-V characteristics. This conclusion was also reached by Sarnot and Dubey [22] from their analysis of two band effects in the insulators of MIM diodes.

In performing calculations assuming a two-band model of the insulator, the barrier potential as a function of x is defined in Fig. 2.2 by $\phi_{cb}(x)$ and $\phi_{vb}(x)$ for the conduction and valence bands, respectively, of the insulator. An average of wavevectors associated with each band is calculated in Ref. 19 and is given by

$$\eta_b^{-2} = \eta_{cb}^{-2} + \eta_{vb}^{-2} \qquad 2.6$$

where

$$\eta_{cb}^2 = \frac{2m_{cb}^*}{\hbar^2} (\phi_{cb}(x) - E + E_T) \qquad 2.7a$$

$$\eta_{vb}^2 = \frac{2m_{vb}^*}{\hbar^2} (E + E_T - \phi_{vb}(x)) \qquad 2.7b$$

the quantities m_{cb}^* and m_{vb}^* are independently variable band masses for the conduction and valence bands of the insulator. Provision was made for the inclusion in $\phi_{cb}(x)$ and $\phi_{vb}(x)$, of the effects of image force, applied bias, and space charge in the insulator.

The effect of various combinations of insulator masses m_{cb} and m_{vb}, on the I-V characteristics of an N_{21} diode, are shown in Fig. 2.4. Here also, the current magnitude differences have been ignored and characteristics superimposed on each other by normalizing to the current

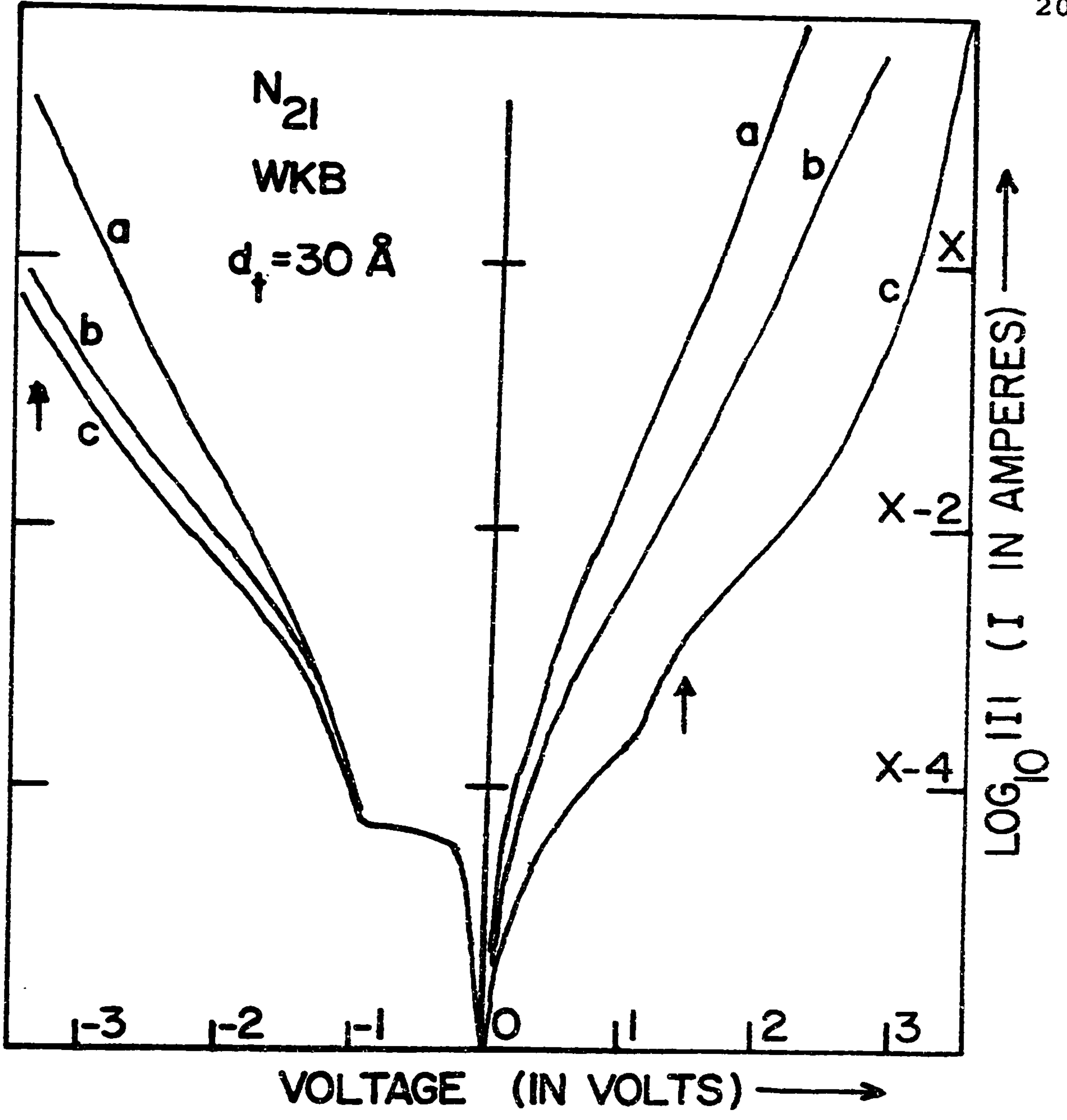


Fig. 2.4 Normalized log I-V characteristics of N_{21} diode calculated with WKB tunnel probability and d_T = 30 Å as a function of two-band insulator masses, m^*_{cb} and m^*_{vb}.

Curve 'a' calculated assuming $m^*_{cb} = 1$, $m^*_{vb} = \infty$ (X =-6.3),
curve 'b' assuming $m^*_{cb} = 1$, $m^*_{vb} = 2$ (X =-3.6),
curve 'c' assuming $m^*_{cb} = 2$, $m^*_{vb} = 1$ (X = -6)

level at -1 V. Three mass combinations were considered, $m_{cb}/m_{vb} = 1/\infty$ (curve a), 1/2 (curve b), 2/1 (curve c). Curve 'a' is simply the I-V characteristic seen in Fig. 2.3 for an N_{21} diode calculated with the WKB tunnel probability and a (effectively) one band insulator. Decreasing the hole mass, introduces an increasing amount of hole-like nature to all carriers (the charge of these carriers, of course, remains negative). The result is a decrease in logarithmic slope of the I-V characteristics of J_{cm} and J_{vm}. At the same time, the hole currents J_{vm} and J_{mv} are enhanced. In curve 'c' it can be seen that the latter currents are enhanced to the point where their presence has visible effects on the log I-V characteristic (i.e., at $V_a = +1.5$ V and $V_a < -2.0$ V). The presence or lack of any such hole current induced features in actual experimental current-voltage curves is used in the next chapter to place bounds on the possible values of hole band mass m_{vb} in the insulator.

Corresponding to the three insulator mass combinations employed for the curves of Fig. 2.4 are three different effective barrier profiles. These profiles (of $\eta_b^2(x)$ vs. x) along with the corresponding plots of E vs. k_b^2 for energies in the insulator energy gap, are shown in Fig. 2.5. The explanation of the relative increase in hole currents becomes obvious from considering the barrier height seen by the minority carriers. This barrier height has been

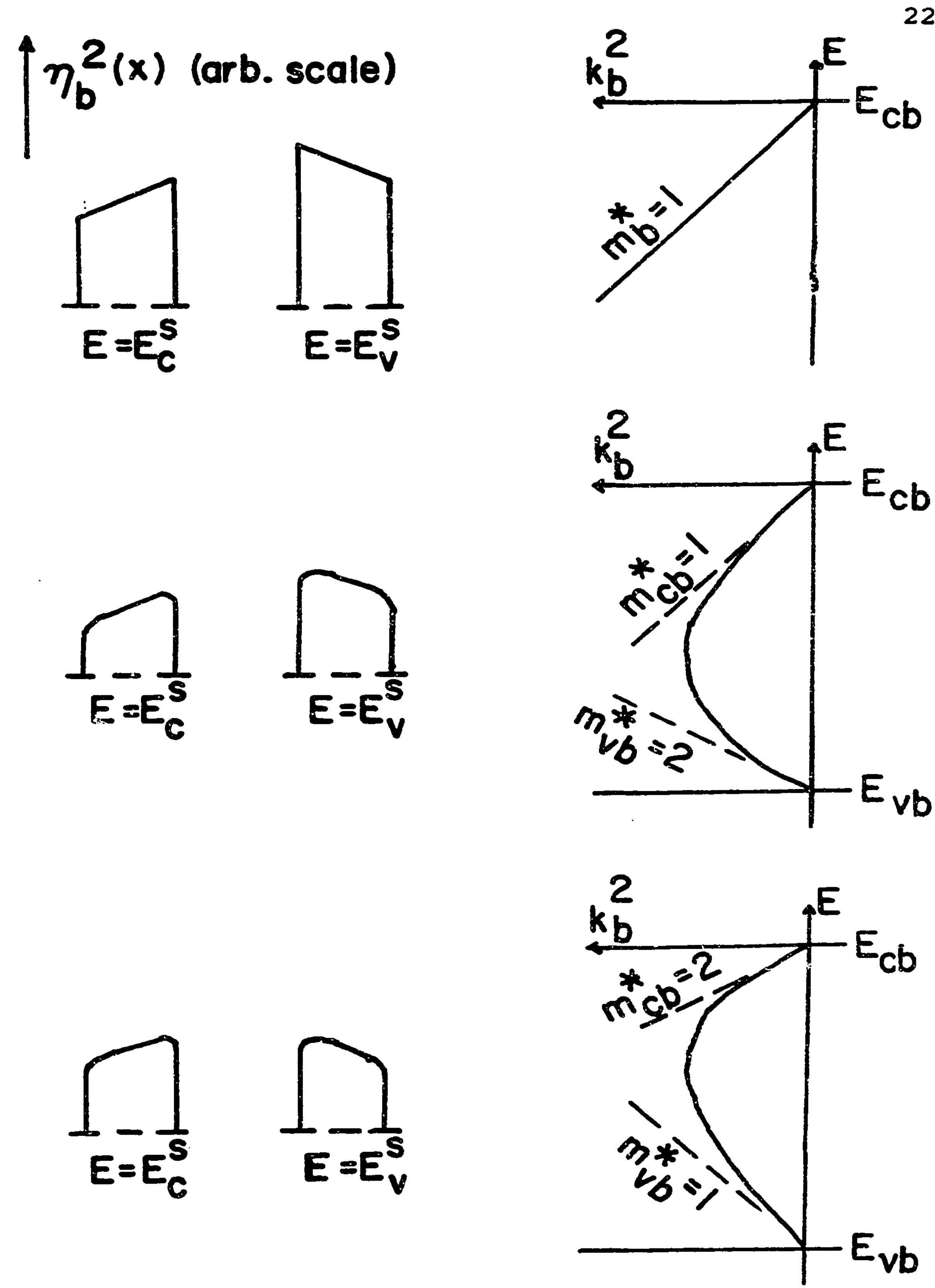


Fig. 2.5 Qualitative potential barrier shape given by $\eta_b^2(x)$ vs x is shown for carriers at two energies, $E = E_c^s$ and $E = E_v^s$. Also shown is the corresponding E vs k_b^2 relationship in the insulator energy gap. All are shown for (a) $m_{cb}^* = 1$, $m_{vb}^* = \infty$; (b) $m_{cb}^* = 1$, $m_{vb}^* = 2$; (c) $m_{cb}^* = 2$, $m_{vb}^* = 1$

significantly reduced for a hole facing the valence band barrier, also for an electron (from the semiconductor valence band) facing the oxide conduction band barrier. From the $E(k^2)$ plots b and c, it can be seen, as pointed out by Esaki [7], that a one band model of the insulator (linear $E(k^2)$) can be assumed only for energies near one of the band edges. In Si-SiO_2 diodes, the band-gap of SiO_2 is reported to be ~8 ev [23]. With the semiconductor band edges typically situated at 3.2 and 4.3 ev below the oxide conduction band, carriers are definitely well into the two band region of the insulator.

2.3.2 The Effects of Insulator Thickness

From its position in the exponent of the exponential tunnel probability (Eq. 2.4), it can be surmised that the insulator thickness, d_T (= x_2 - x_1) will also have pronounced effects on current-voltage curve shape. These effects are demonstrated in Fig. 2.6 for an N_{21} diode with an insulator effective mass combination of m_{cb}/m_{vb} = 2/1. The WKB tunnel probability was employed. A similarity can be seen between the effect of increasing the ratio of oxide masses m_{cb}/m_{vb} (Fig. 2.4) and that of decreasing the insulator thickness (Fig. 2.6). This similarity extends only to the changes in logarithimic slope of the I-V characteristics. The relative

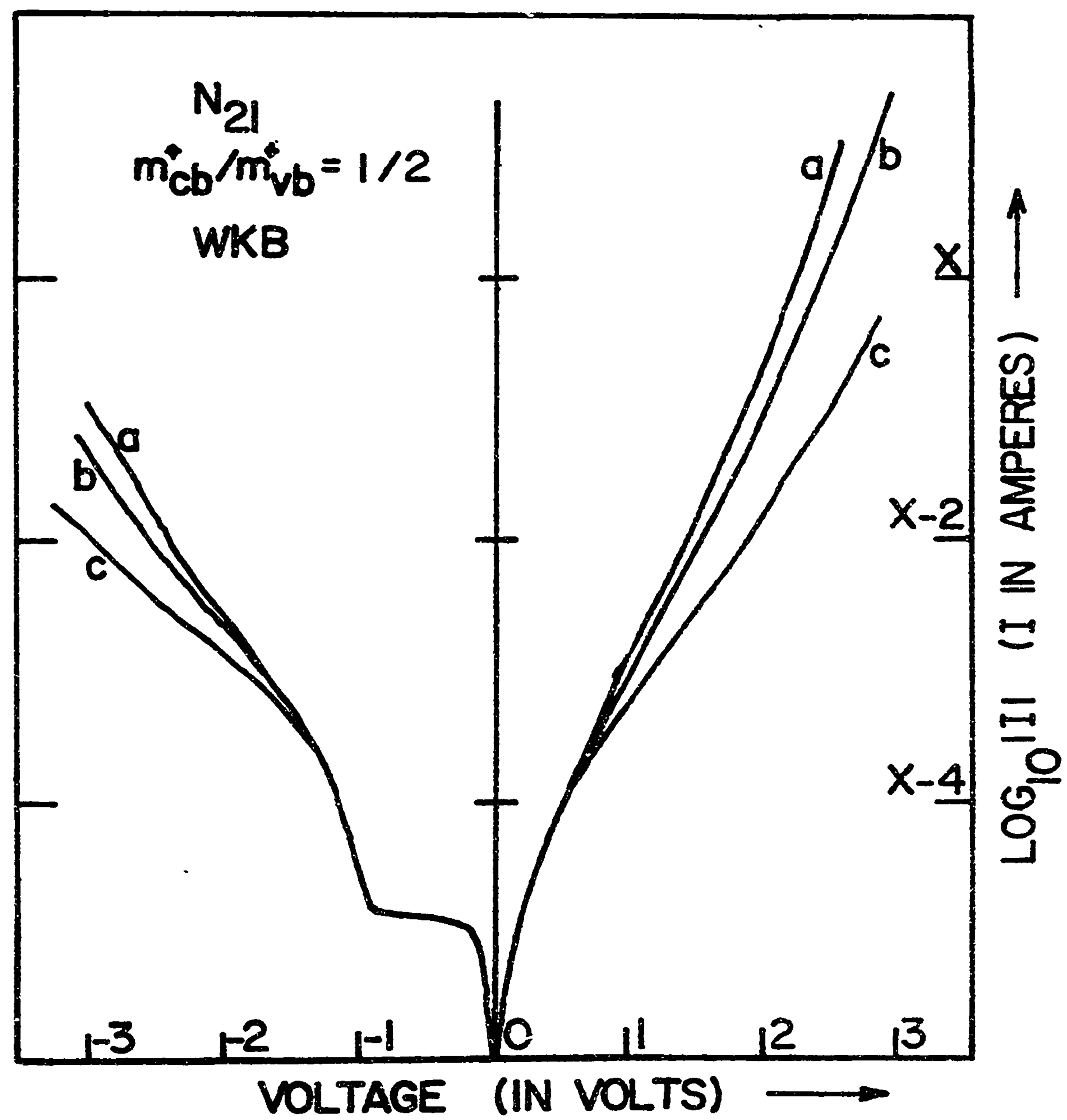


Fig. 2.6 Normalized log I-V characteristics of N_{21} diode, calculated with WKB tunnel probability, barrier masses of $m^*_{cb} = 1$ and $m^*_{vb} = 2$ and (a) $d_T = 20$ Å (X = +4); (b) $d_T = 30$ Å (X = -3); (c) $d_T = 35$ Å (X = -6)

magnitudes of J_{mv} and J_{vm} to J_{mc} and J_{cm} respectively stay roughly constant. However, the existence of such a similarity results in an unfortunate ambiguity which inhibits an accurate determination of the barrier effective masses in experimental diodes. An accurate determination of d_T is required first. A partial test of the model can at least be made by comparing the log I-V curve shapes obtained with diodes of differing insulator thicknesses. The results of such a test are discussed in the next chapter.

2.3.3 The Effects of Image Forces

Incorporated in the calculated curves presented in Figs. 2.4 and 2.6 were the effects of a variable image potential. This potential was of the form

$$V_i = \frac{8}{4\pi\varepsilon_i}\left(\frac{1}{x} + \frac{R}{d_T - x}\right) \qquad 2.8$$

where $R = R(Q_s)$

$$= \frac{\varepsilon_s - \varepsilon_i}{\varepsilon_s + \varepsilon_i} + \frac{1}{1 + Q_s'/Q_s}\left(1 - \frac{\varepsilon_s - \varepsilon_i}{\varepsilon_s + \varepsilon_i}\right) \qquad 2.9$$

and $\lambda = 1.15\ \pi\ \ell n\ 2$ and $Q_s = Q_s(V_a)$ is the mobile charge density at the semiconductor surface, Q_s' is an arbitrary constant charge density to be determined from experiment and

ε_s is the dielectric constant of the semiconductor. The first term in brackets in Eq. 2.8 represents the image force at the M-I interface, while the second term gives the image force at the I-S interface. For $Q_s >> Q_s'$ the large charge density at the semiconductor surface allows this electrode to behave like a metal (R = 1). Equation 2.8 at this voltage reduces to Simmon's image force potential [24] for an MIM system. If at other applied biases $Q_s << Q_s'$ the second term represents the image force found at a dielectric-dielectric interface [25] (with $R = (\varepsilon_s - \varepsilon_i)/(\varepsilon_s + \varepsilon_i) = 0.51$ at an SiO_2-Si interface). The relative effects of three different assumptions for Q_s' on the I-V characteristic of an N_{21} diode are compared in Fig. 2.7. Included are curves calculated with R = 1 at all voltages ($Q_s' = 10^{-40}/m^2$, curve a), R = 0.51 at all voltages ($Q_s' = 10^{+40}/m^2$, curve b), and $0.51 < R < 1$ ($Q_s' = 10^{23}/m^2$, curve c). The only region appreciably affected by the different types of image potential is the depletion region between 0 and -1 V. For the variable image force (curve b), the current levels in this region are depressed slightly from those obtained assuming a constant image potential of the MIM type (curve a). This reduction in current magnitude occurs when the charge at the semiconductor surfaces makes the transition from $Q_s >> Q_s'$ (i.e., for $V_a \lesssim -1.5$ V) to $Q_s << Q_s'$ (i.e., for $0\ V > V_a > -1.0$ V). Current levels in this latter region match those obtained

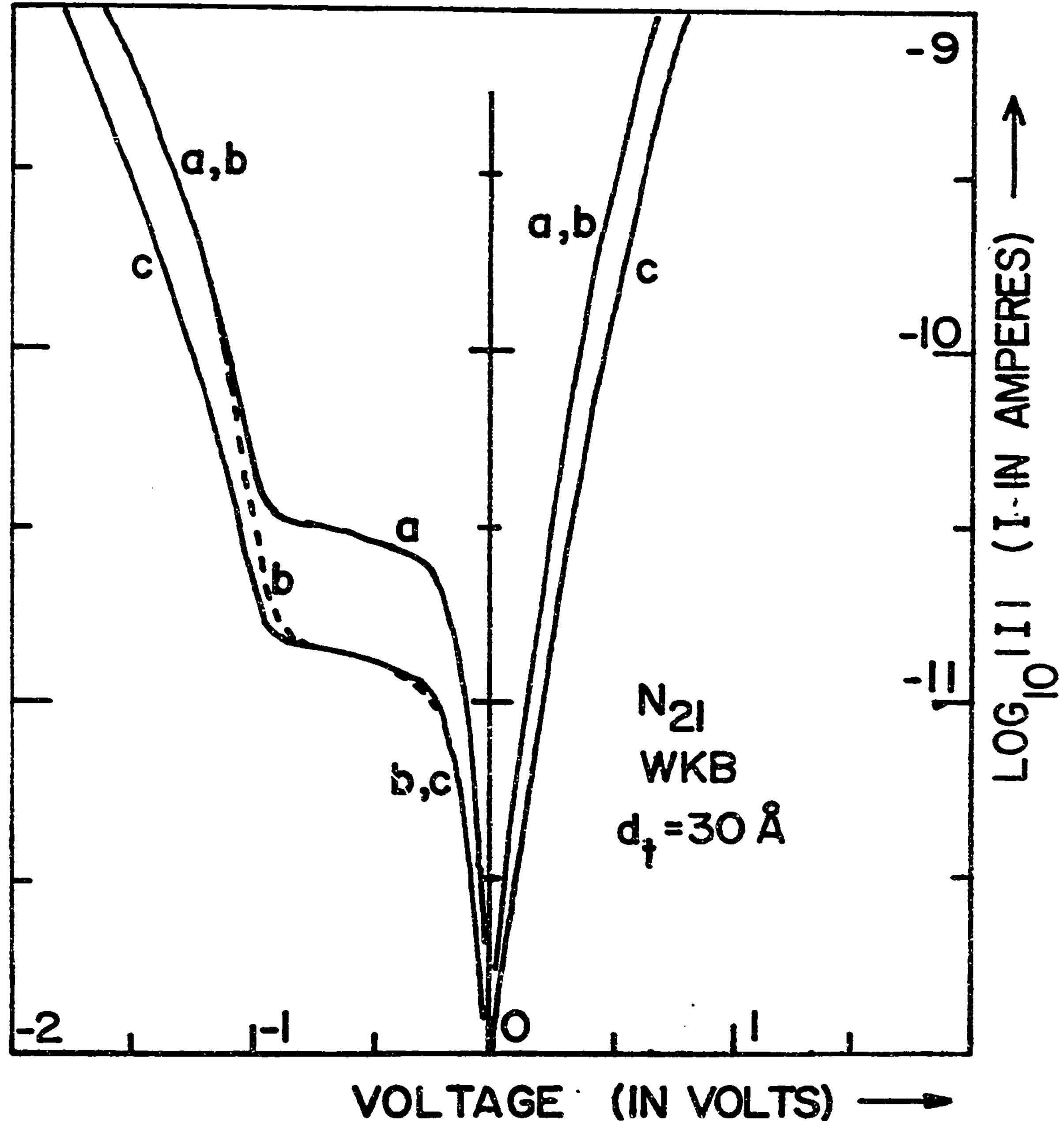


Fig. 2.7 Log I-V characteristics of N_{21} diode, calculated with WKB tunnel probability, d_T = 30 Å, and various types of image force resulting from the assumption in Eq. 2.8 that a) R = 1; b) 0.51 < R < 1 ($Q_S' = 10^{23}/m^3$); c) R = 0.51

assuming the semiconductor always behaves as a dielectric (curve c).

From considerations of the model of the insulator we now move to considerations of the model of the semiconductor and the assumptions concerning the calculation of the voltage distribution in this semiconductor.

2.4 The Model of the Semiconductor

2.4.1 The Semiconductor Band Structure

In considering the effects of the semiconductor on band-to-band tunnel currents it is necessary to adopt a model for the energy band structure of this material. It is well known [26] that the conduction band energy surfaces of silicon form six ellipsoids in k-space, each centered at a point $k_0 = \frac{2\pi}{a}(0.85, 0, 0)$ along the <100> axes. The incorporation of the full band structure into the calculations of MIS tunnel currents has never been carried out. Generally two simplifying assumptions are made. The first is that the integrand of Eq. 2.1 is sharply peaked at $E_T = 0$. The implications of this assumption are discussed in Appendix A. By eliminating the detailed calculation over all E_T the problem is reduced essentially to a one dimensional problem. The second assumption is that a parabolic $E(k)$ relationship holds for all energies in the conduction band. This last approximation is obviously inappropriate for energies much above the conduction band minimum but the lack of dependence of tunnel currents on k_2, as seen in Sec. 2.2, indicates there is little loss of accuracy in making this approximation.

In our calculations, both of the above approximations are made. Included though, were the effects of the offset of the conduction band minimum from k=0 as discussed in Sec. 2.2. In considering indirect band gap materials, such as silicon, an important question can be raised concerning the validity of the assumption that transverse momentum must be conserved. It has been pointed out by Busch and Fischer [27] that a consequence of this assumption in silicon is that for current flow perpendicular to the (111) face there can be no tunneling transitions with $k_T = 0$. The reason for this can be seen from Fig. 2.8 where the projection (or "shadow") [10] of the metal Fermi sphere on this face as well as on the (100) face is shown. Shown also is the corresponding shadow of the semiconductor conduction band energy surfaces. The regions of overlap (cross hatched areas) indicate states in both materials between which equi-energy tunnel transitions can occur with k_T being conserved. For the (111) face no overlap exists at $k_T = 0$. A minimum k_T and therefore, a minimum energy E_T associated with this momentum, is required by a carrier before a tunnel transition can occur. A sharp reduction in current to the (111) face for a given d_T should, therefore, be noted compared to the current to the (100) face. Such effects, likened to the results of an enhanced work function difference for the (111) face, have never been observed experimentally. Busch and Fischer in their studies of field

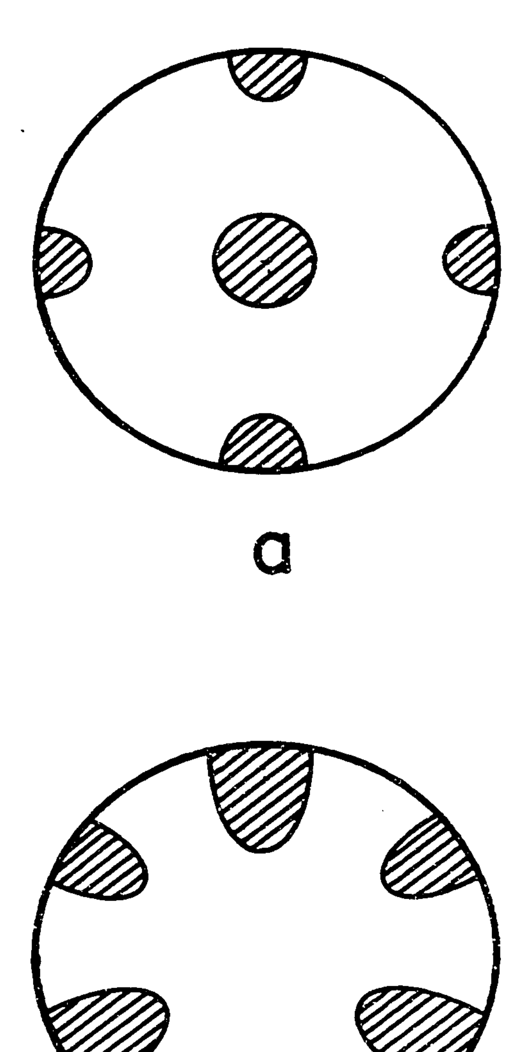


Fig. 2.8 Qualitative projection or shadow [10] of metal and semiconductor Fermi surface on plane of the I-S interface for (a) (100) silicon face; (b) (111) silicon face. Regions of overlap are cross-hatched. Only regions within the shadow of the metal Fermi surface are considered

emission from silicon points attributed this lack of orientation dependence in their results to non-conservation of k_T for tunneling electrons (i.e., diffuse transmission). Stratton [28] disagreed with this conclusion in view of the predictions of his model for the effect of diffuse boundary conditions on tunneling. The question has yet to be resolved. Experimentally the MIS diode might be expected to be a good system for observing such orientation effects but changes in the work function differences have effects essentially indistinguishable from the effects of oxide charge and voltage dependent image forces on the I-V characteristics of the diode.

Where non-conservation effects exist in MIS diodes their probable bias dependence should make them detectable. For example, under positive bias, electrons will accumulate near the conduction band minimum of the N_{21} diode and then tunnel to the metal. The overlapping shadow region will be correspondingly small. Under negative bias for electron flows from metal to semiconductor, the metal Fermi level can reach energies 1-2 ev above the conduction band minimum. Large energy surface overlap regions must, therefore, be considered and non-conservation effects limited to these regions [28] would be correspondingly larger. This argument will be discussed further in connection with a disagreement between the simple theory and experiment in negative voltage regions.

2.4.2 The D.C. Voltage Distribution

A problem which is of considerable importance to the I-V characteristics of the MIS diode is that of field penetration of the electrodes. Potential drops of up to 1 V can be supported across the semiconductor of an "equilibrium" diode, and as will be seen later, much more in a "non-equilibrium" diode. This drop reduces the effect of bias on tunnel currents in certain bias regions. The potential energy distribution in the semiconductor employed in the calculations of tunnel current in this thesis was obtained by the method of Temple and Shewchun [29,30] (cf. Appendix B). This method has a number of advantages, the first being the ability to dictate a prescribed accuracy. Secondly, it uses Fermi integrals over bands with arbitrary densities of states and can, therefore, be confidently applied at bias voltages where the Fermi level extends into the conduction or valence band. This is particularly important for considering current flows in degenerate silicon diodes. It is also important in calculating currents in any MIS device at large positive or negative biases. Other features of the method include the consideration of band tailing effects (following the equations and procedures outlined in Ref. 31) and applicability at any temperature for which the appropriate energy band parameters are available. Non-equilibrium effects such as that caused by

illumination of the semiconductor can be simulated by constant quasi-fermi level separations. The effects of any distribution of surface states capable of being described by discrete states spread over 120 energy intervals in the band gap, can also be included.

With a knowledge of the potential distributions as a function of x into the semiconductor, the field at the surface can be accurately determined for a given surface potential. From Gauss' Law, including the effects of surface state and oxide charge at the I-S interface, the voltage V_{ox} across the oxide can easily be calculated. Provision was made for including fixed charges at positions in the insulator other than at the I-S interface but little change in the calculated characteristics was observed.

Not as prominent, but considered in any case, is field penetration of the metal electrode. The voltage drop, V_m, due to this cause is given by Ref. 32 as

$$V_m = \frac{\varepsilon_i}{\varepsilon_m} FL \qquad 2.10$$

where $F = V_a/d_T$

$$L = \left(\frac{\varepsilon_m E_{FM}}{2\eta_0 q^2}\right)^{1/2}$$, a characteristic length of the

metal and η_0 is the free electron density in the metal, ε_m and ε_i the dielectric constants of metal and insulator, and

E_{FM} is the Fermi energy of the metal. Values of V_m were typically less than 0.1 V for all but the highest fields and thinnest oxides.

2.4.3 The Degenerate Semiconductor Model

Employing the pure WKB model, the only semiconductor band parameters entering the band-to-band current equation (Eq. 2.1) are the limits of integration. In the non-degenerate semiconductor these limits are well defined. However, in the degenerate case the "electron band" - "impurity center" interaction leads to considerable band tailing effects. For a high enough impurity density the "impurity center" - "impurity center" interaction leads to a broadening of the impurity band. These problems have been treated by Kleppinger and Lindholm [31]. Their expression for the resultant effective band edge was adopted by Temple [30,33] and provides an extra tunneling parameter to be checked phenomenologically.

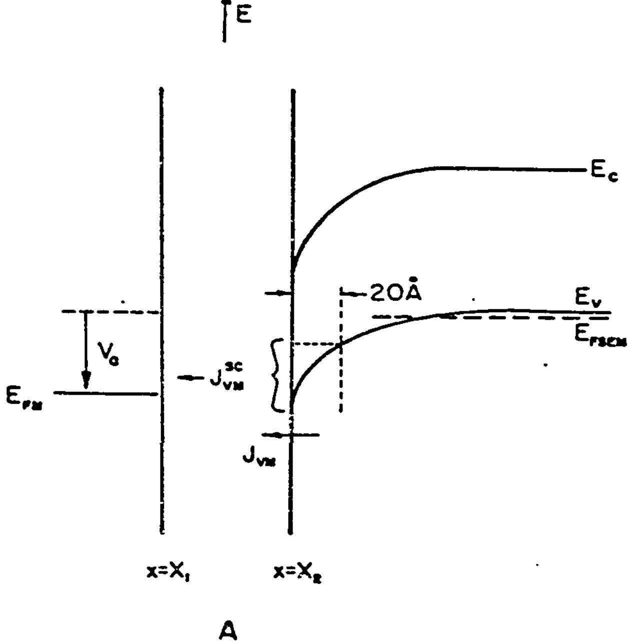
For a degenerate n-silicon diode for instance, this parameter would be the energy of the 'tailed' conduction band edge above which tunneling transitions can occur. In the work of Kleppinger et al. [31], a Gaussian distribution was assumed for the impurity band broadening. Within this distribution are $2N_{imp}$ non-localized states which are

presumably capable of taking part in the tunneling process. Unfortunately the Gaussian does not represent a practical distribution from a tunneling point of view as it has no sharp edge at which the density of states goes to zero. The choice of lower limit for tunneling then is more or less arbitrary. In the theory of SIS tunneling by Temple [30,33] a choice of $E = E_D - 2\sigma$ was made where σ is the variance of the Gaussian. Unfortunately as seen later this choice does not appear to predict tunnel I-V characteristics for a degenerate n-silicon diode which fit experimental data. This lower limit is, therefore, treated as an arbitrary parameter.

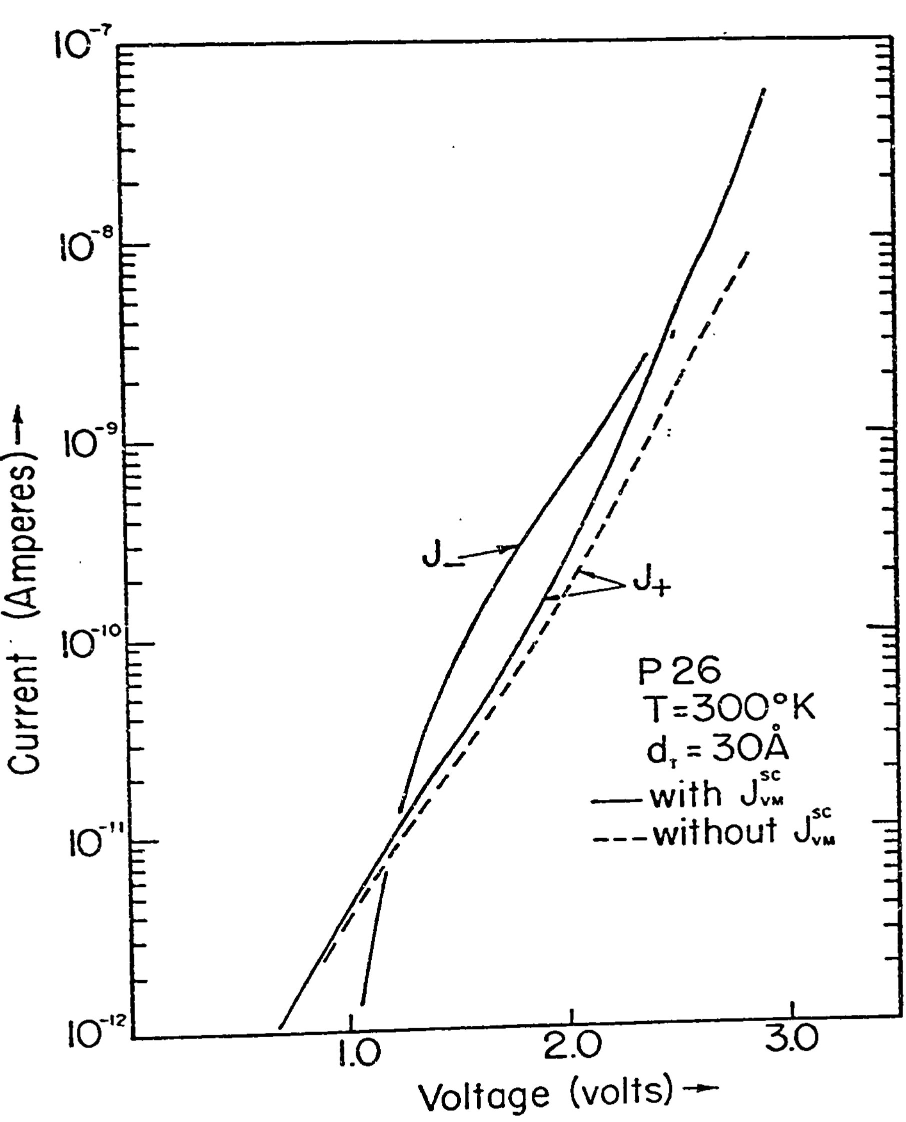
A second problem associated with degenerate MIS diodes is that of space charge tunneling. Extremely high fields are often encountered at the surface of biased degenerate devices. Under these conditions a thin space charge barrier can be created which in the case of a P_{26} diode for instance can be $\lesssim 100$ Å. Additional tunneling channels can, therefore, be expected through the combined insulator and space charge barrier at energies in the semiconductor band gap. Such channels are indicated for a P_{26} diode under positive bias in Fig. 2.9. The additional current flow in this case is designated J^{sc}_{vm}. Other space charge tunnel currents are correspondingly designated J^{sc}_{mv}, J^{sc}_{mc} and J^{sc}_{cm}.

Fig. 2.9a Energy band diagram of degenerate p-type diode defining additional tunnel current J_{vm}^{sc}

b Theoretically calculated log I-V characteristics of P_{26} diode showing total tunnel current with (solid curve) and without (dashed curve) space charge tunneling



A



B

Figure 2·9

From a knowledge of the semiconductor band bending as a function of x it is possible to obtain the tunnel probability for the carriers in these extra currents. This is accomplished by including an additional integration over x (from X_2 to d_{sc} where d_{sc} is an appropriate distance into the semiconductor) into the exponent in Eqs. 2.4 and 2.5. The resulting I-V characteristics including and excluding the space charge tunnel currents are shown for a P_{26} diode in Fig. 2.9b. A value of d_{sc} = 20 Å was employed. Also, a WKB tunnel probability and one band model of the insulator were assumed. As can be expected in a P_{26} diode much of the additional flow occurs at large positive voltages where fields in the semiconductor are high.

In the next section the effects of another type of tunneling that occurs at energies in the semiconductor energy gap is considered, i.e., surface state tunneling. Expressions for these currents are presented and the assumptions involved in their derivation are discussed. As with space charge tunneling, additional current flows are possible. It will be seen that just as important as the additional current is the effect of surface state charge on the band-to-band current in certain bias regions.

2.5 The Surface State Tunneling Model

2.5.1 The Current Expression

The total surface state tunnel current was defined in Eq. 2.3 and shown schematically in Fig. 2.1. Expressions for the tunneling components of these currents, J_{ms} and J_{sm}, can be derived along similar lines to those shown in Appendix A for the band-to-band currents. Adopting the approach of Freeman and Dahlke [34], the following WKB expression for surface state tunnel current can be derived (Appendix C)

$$J_{si} = J_{sm} - J_{ms}$$

$$= \frac{4q}{\pi h} \left. \frac{\sigma_{Ti} N_i (f_1 - f_i) \eta_b(x_2) \eta_{ss}(x_2) \exp(-2\int \eta_b dx)}{\int \frac{d\eta_b}{dE_T} dx} \right|_{E_T=0} \qquad 2.11$$

where f_i , N_i and σ_{Ti} are, respectively, the probability of occupation, the density and the effective tunnel capture cross-section of the surface state at the ith energy level. $\eta_{ss}(x_2)$ is an average of the semiconductor and insulator attenuation constants at the I-S interface ($x = x_2$). The tunnel current expression assuming a WFM tunnel probability is

$$J_{si} = \frac{32q}{\pi h} \frac{\sigma_{Ti} N_i (f_1 - f_i) \eta_b (x_2) \{\frac{m_1}{k_1} \frac{m_{ss}}{\eta_{ss}(x_2)} (\frac{m_b}{k_b})^2\} \exp(-2\int \eta_b dx)}{\{(\frac{m_1}{k_1})^2 + (\frac{m_b}{k_b})^2\}\{(\frac{m_b}{k_b})^2 + (\frac{m_{ss}}{\eta_{ss}(x_2)})^2\} \int \frac{d\eta_b}{dE_T} dx} \qquad 2.12$$

where m_{ss} is an average semiconductor mass defined in Appendix C.

The assumption implicit in the use of Eqs. 2.11 and 2.12 is that the recombination processes filling or emptying the states are as fast as required. In other words, the occupation of these states is controlled by the bulk semiconductor Fermi level. In actual practice, of course, a quasi-fermi level for these states should be defined. An iterative procedure could be used to determine state occupancy (and, therefore, the quasi-fermi level energy) in the presence of tunnel current flow. This procedure fortunately is necessary only in certain cases. A convenient simplification of the problem has been made by Freeman[33]. By defining a so-called effective "tunnel time constant", τ_{Ti}, given by

$$\tau_{Ti} = \frac{q N_i (f_1 - f_i)}{J_{si}} \qquad 2.13$$

a comparison can be made with the usual S.R.H. recombination time constant τ_{Ri}[35]. For $\tau_{Ti} >> \tau_{Ri}$ the implicit assumption of Eqs. 2.11 and 2.12 is justified. Only for thin insulators

($d_T \approx 10$ Å) and low temperatures was it found that $\tau_{Ri} \gtrsim \tau_{Ti}$. In these regions the approximation could be questioned.

Examples of the surface state tunnel current-voltage characteristics are shown in Fig. 2.10. In calculating the currents shown in Fig. 2.10a, an N_{21} diode with $d_T = 30$ Å, a WKB tunnel probability and an MIM form of image potential were assumed, in addition to a one band model of the insulator. The curves of Fig. 2.10b were calculated with a two band model of the insulator and several combinations of electron and hole masses in the barrier. The surface state distribution SS2 was used in the latter calculations. All surface state distributions employed are shown in Fig. 2.11.

The current-voltage curve shapes seen in Fig. 2.10a are similar for all surface state distributions. The one curve which shows any differences (curve c) was calculated with SS2 but assuming a variable image force (i.e., in Eq. 2.9, $Q_s' = 10^{23}/m^2$). In Fig. 2.7 the effects of image force on the band-to-band currents were seen to result in changes which would be difficult to differentiate from surface state or oxide charge effects. Such is not the case in curve c of Fig. 2.10a. Distinctive structure in the surface state log I-V characteristics result from the use of the variable image force. Observation of such structure in an experimental device would require the dominance of surface

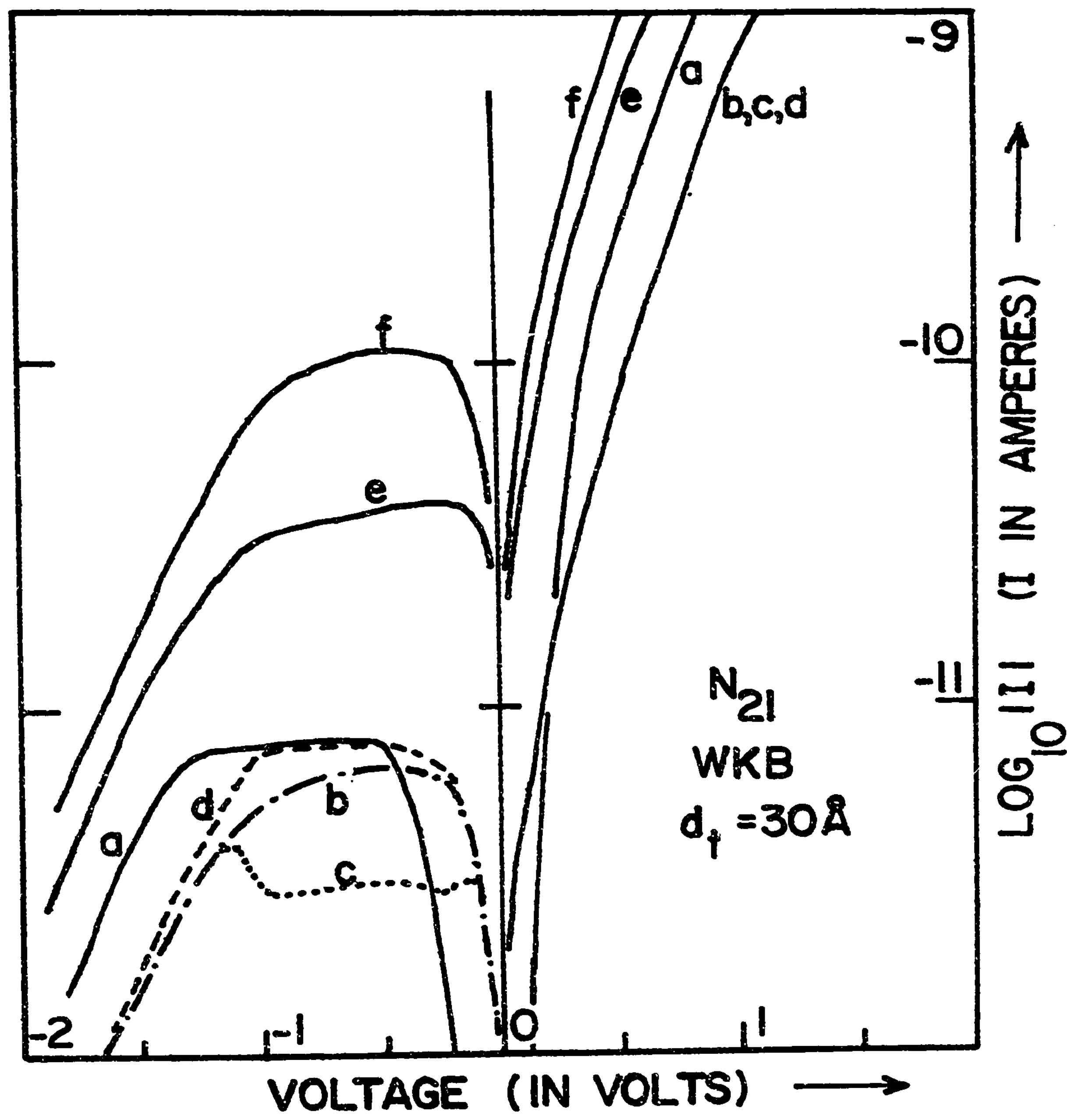


Fig. 2.10a Log I-V characteristics of surface state tunnel currents calculated for an N_{21} diode with WKB tunnel probability, and d_T = 30 Å, with the following surface state distributions. For curve 'a' - SS1, 'b' - SS2, 'c' - SS2 and variable image force, 'd' - SS3, 'e' - SS4, 'f' - SS5. Where not mentioned, the image force was of the MIM type.

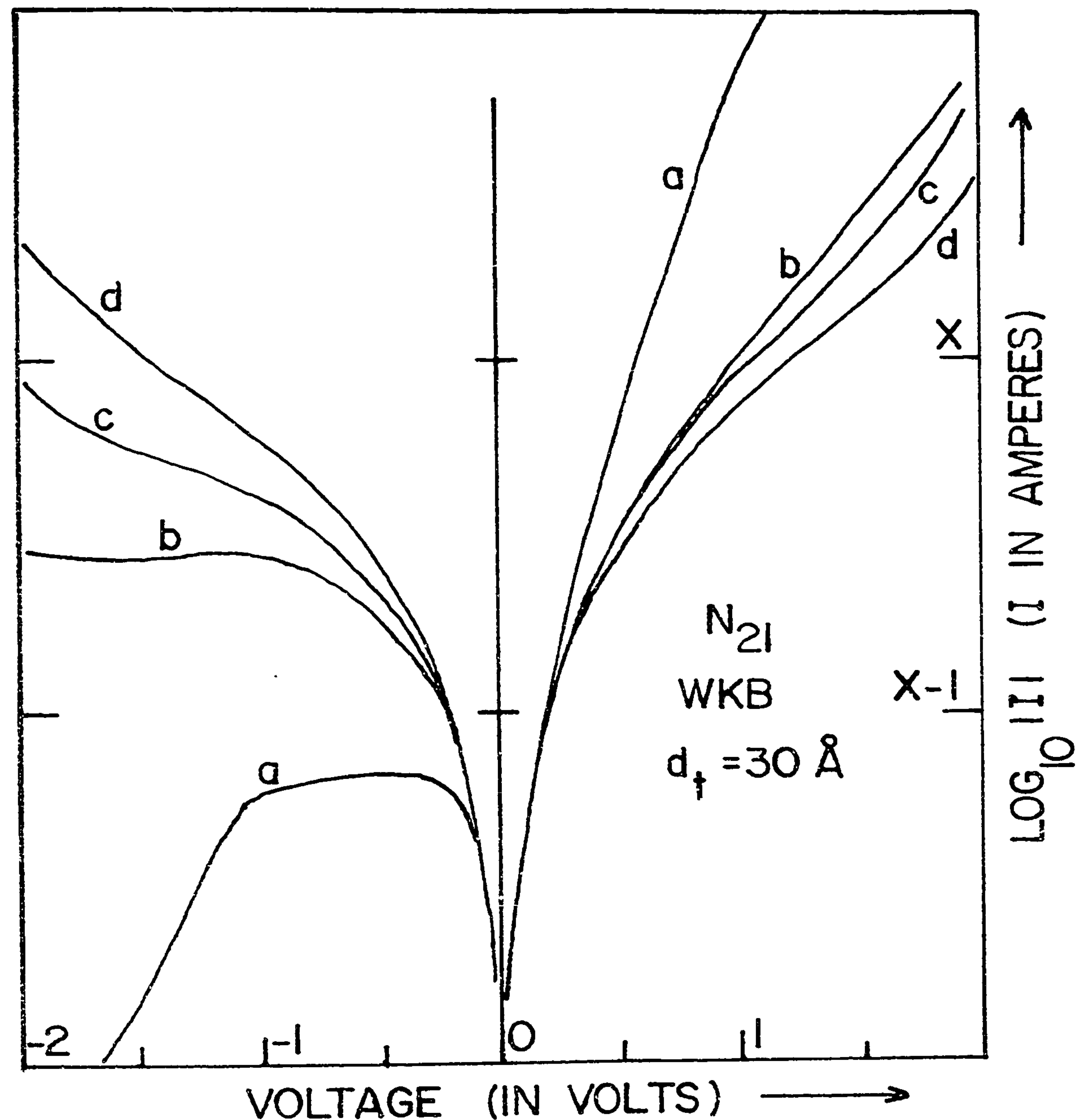


Fig. 2.10b Normalized log I-V characteristics of the surface state (SS2) currents in an N_{21} diode calculated with WKB tunnel probability, d_T = 30 Å, and insulator masses of m^*_{cb} = 1, m^*_{vb} = ∞ in curve 'a'; m^*_{cb} = 1, m^*_{vb} = 1 in curve 'b'; m^*_{cb} = 1.5, m^*_{vb} = 1 in curve 'c'; m^*_{cb} = 2, m^*_{vb} = 1 in curve 'd'.

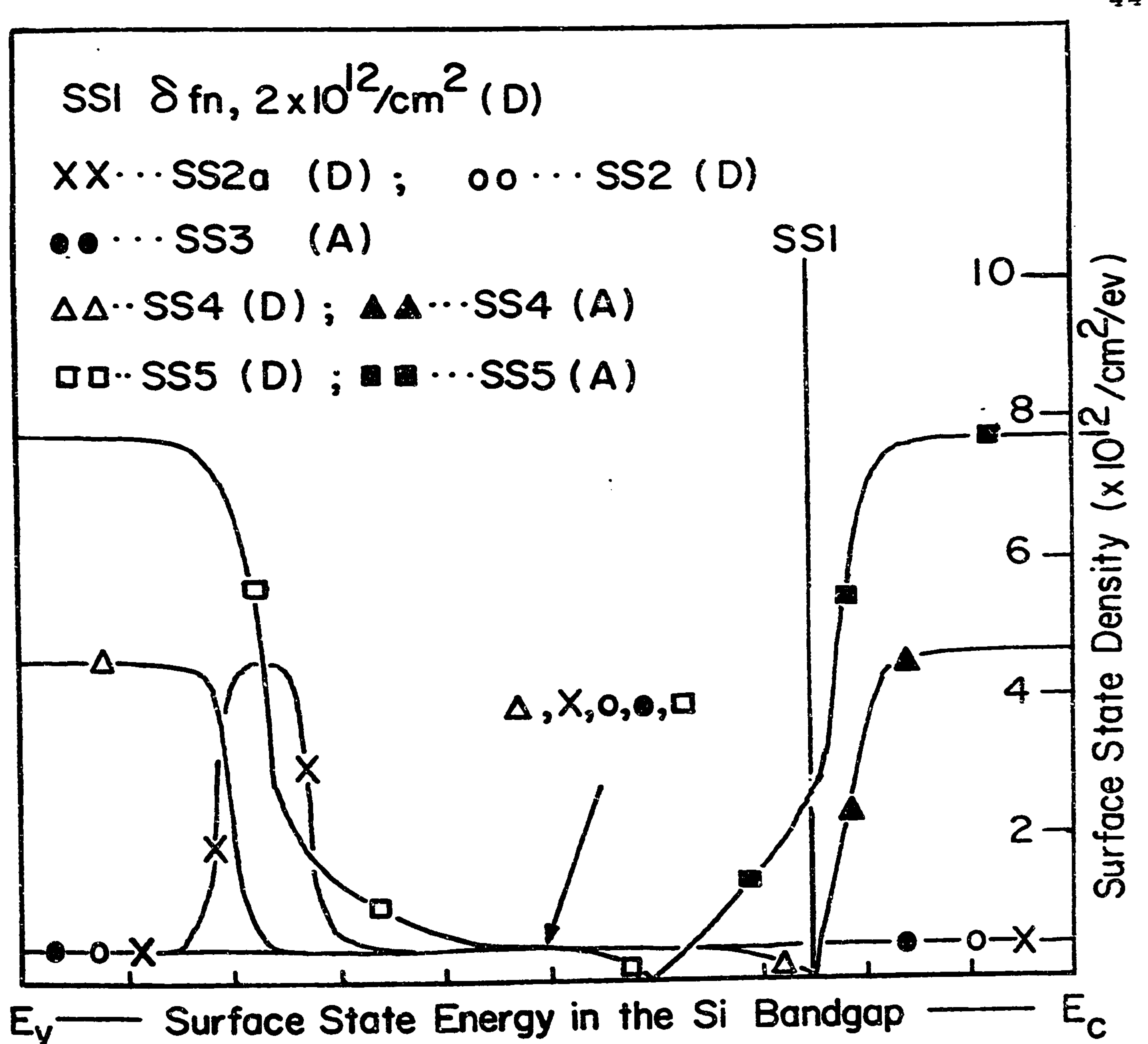


Fig. 2.11 Surface state distributions assumed for various calculations shown in Figs. 2.10a and 2.10b.

state currents over the band-to-band currents and would provide an excellent verification of the variable image force model. The characteristics of a diode in which it is possible such conditions are met, are presented in a later chapter. The variable image force model will be seen to provide one possible explanation of the observed results.

In Fig. 2.10a the actual magnitude of all currents is shown (the currents of Fig. 2.10b are normalized to the current at -0.5 V). The expected correspondence between current magnitude and surface state density is apparent. One exception to note is curve a. Despite the large density of states associated with SS1 (cf. Fig. 2.11) relatively little current is passed. This is due to the position of the energy level of these states in the semiconductor band gap. As a one band model of the insulator was employed in calculating these currents, the tunnel probability of such states is lower than for corresponding states near the conduction band edge.

The assumption of a two band insulator model can be seen in Fig. 2.10b to have a significant effect on surface state current-voltage curve shapes, particularly in the negative bias region. In these calculations the distribution SS2 was employed and, therefore, curve 'a' of Fig. 2.10b corresponds to curve b of Fig. 2.10a. A negative resistance region observed for currents calculated with a one band

model is seen to be a function of the two-band hole mass The existance of the negative resistance region is due to the fixed energy levels in the semiconductor energy gap at which surface state currents must tunnel. For increasing negative biases the tunnel probability decreases considerably for charge carriers at these energies due to the increasing barrier height of the insulator conduction band barrier. In a two-band model, where the hole and electron masses in the insulator are comparable, an increasing conduction band barrier height implies a decreasing valence band barrier height. The result of this on the I-V characteristics is an elimination of the negative resistance region under negative biases. The curve shape in this region would, therefore, provide a fairly accurate determination of the effective barrier masses. To do this though, a means would have to be found experimentally to isolate the surface state currents from the band currents, a rather difficult problem.

2.5.2 Surface State Effects on the Total Tunnel Current

The results of the addition of surface state currents to the band currents are shown in Fig. 2.12. The surface state distribution SS2 (cf. Fig. 2.11) was employed but with 5 different tunnel cross-sections from 0.1 σ_{Ti} (curve a) to 10^3 σ_{Ti} (curve d) where $\sigma_{Ti} = 10^{-18}$ m^2. A one band

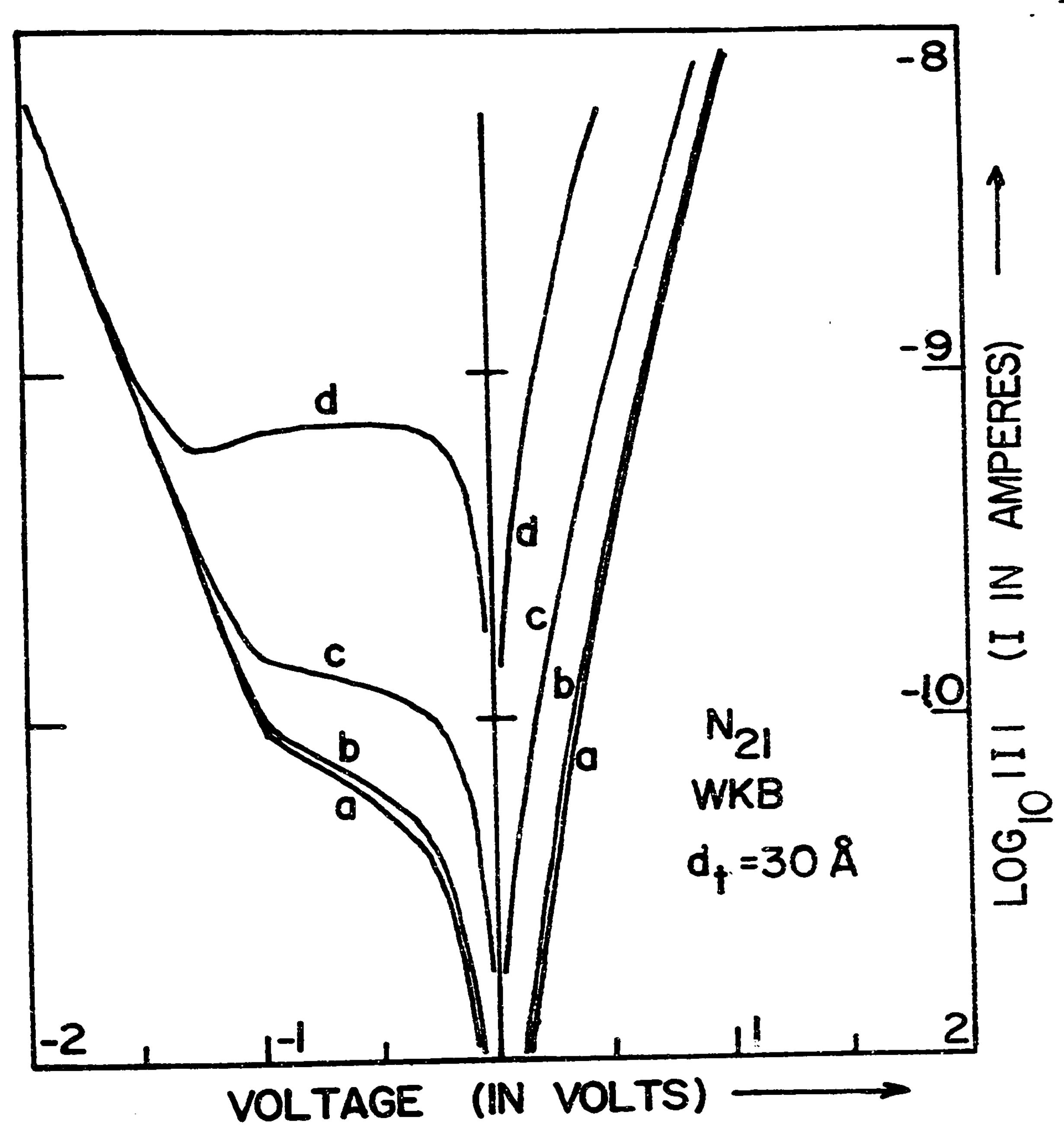


Fig. 2.12 Log I-V characteristics of tunnel current in N_{21} diode including surface state tunnel currents, the latter calculated with tunnel capture cross-sections of 0.1 and 1 × σ_T (curve 'a'), 10 σ_T (curve 'b'), 10^2 σ_T (curve 'c') and 10^3 σ_T (curve 'd') where $\sigma_T = 10^{-18}$ m^2. A WKB tunnel probability and d_T = 30 Å were assumed.

insulator model was also assumed. The largest contributions come, of course, with the assumption of the largest cross-sections (e.g., 10^{-15} m^2 for curve d). In this case the presence of a negative resistance region in the total current-voltage characteristic is seen. This is due to the negative resistance region of the surface state currents just seen in Fig. 2.10a. The addition of surface state current is not detectable for cross-sections $\leq 10^{-18}$ m^2 (with this particular surface state distribution). A.C. techniques were used by Kar and Dahlke [35] to determine the density and cross-section of surface states in p-silicon MIS tunnel diodes. Their measurements indicated that cross-sections of states, in their diodes, could be as large as 10^{-11} m^2 (when diode was annealed) and as small as 10^{-22} m^2. The theoretical values we have assumed were intermediate to these extremes.

A second important way in which surface states affect the total current is by their influence on the voltage distribution. The results of this influence are demonstrated in Fig. 2.13 for an N_{21} diode. The curve labelled 'i' in the figure represents the ideal log I-V characteristics of an N_{21} diode assuming no surface states and an MIM form of image potential. The currents have not been normalized in order that the relative magnitudes of the effects can be studied.

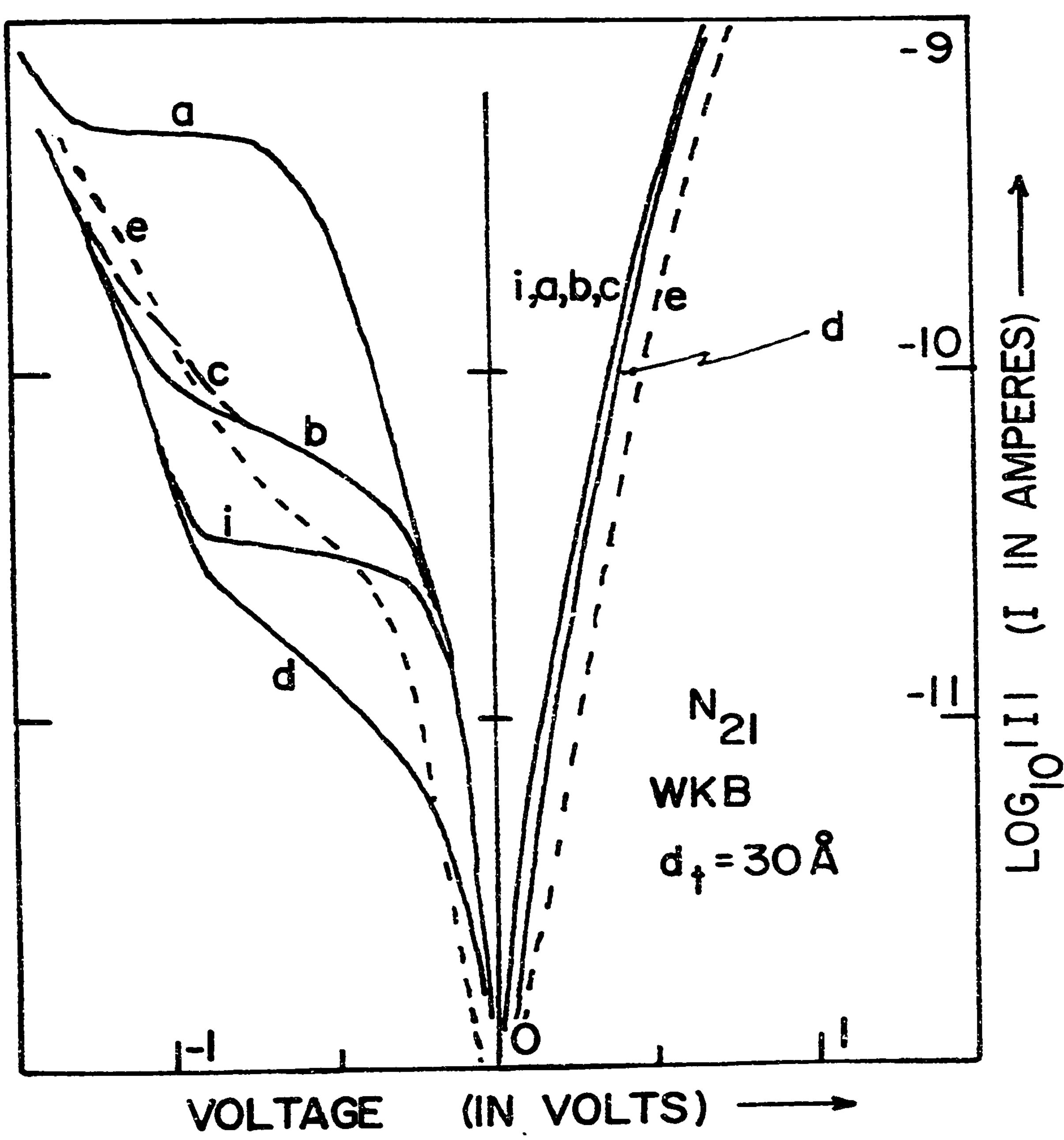


Fig. 2.13 Log I-V characteristics of N_{21} diode showing the effect on the band tunnel currents of surface state distributions (cf. Fig. 2.11) SS1 (curve 'a'), SS2 (curve 'b'), SS2a (curve 'c'), SS3 (curve 'd'), SS5 (curve 'e'). The ideal curve with no surface state is given by curve 'i'.

The most effect is seen for negative biases ($0 > V_a > -1.0$ V). The greater the net amount of positive charge, and this is true of fixed oxide charge as well as surface states, the larger the current magnitude in this bias region. It is important to differentiate net charge here from total charge since curve 'f' was calculated with SS5 which contains the largest total charge but essentially zero net charge.

Whereas current magnitude is controlled by net charge in this region of bias, current-voltage curve shape is controlled by surface state density. Thus for distribution with the highest surface state densities, a large increase in slope of the I-V characteristic is obtained (e.g., curve f). For curve 'a', a very large net charge was assumed but the location of this charge at a single discrete energy level implies a very low charge density at other energies in the band gap. The voltage at which such discrete levels affect the I-V characteristic depends, of course, on its energy. For curve 'a', the discrete level was located in the conduction band half of the semiconductor band gap. In curve 'c', the distribution SS2 was employed but a discrete state was located at $E_i - E_V = 0.25$ ev. Its effect is felt only as the semiconductor Fermi level sweeps through the state's energy level.

To aid in differentiating among the effects of different surface state distributions, the current-voltage curves are plotted in latter chapters against absolute voltage. In this way a new parameter can be defined by which these effects can be classified. This parameter is the voltage at which J_+ and J_- are found to have identical magnitudes and will be designated the first cross-over voltage. (Cross-overs which sometimes occur at very low biases are ignored.) As a general rule it can be shown that a large cross-over voltage implies a large net positive charge at the I-S interface. In contrast to this, if surface state currents dominate, the cross-over voltage is roughly independent of both charge sign and density in energy.

Summarizing then, the effects of surface states can be divided into two categories: the effect on total tunnel current due to the addition of surface state tunnel currents and the effects on total tunnel current due to the d.c. charge in these states. In the former case large capture cross-sections ($>10^{-18}$ m^2) or large surface state densities are required to make these currents dominate the band-to-band tunnel currents. In the latter case significant effects on cross-over voltage and I-V curve shape are seen for relatively small surface densities.

CHAPTER 3

EXPERIMENTALLY OBSERVED MIS TUNNEL DIODE CHARACTERISTICS

3.1 Introduction

The tunnel current-voltage characteristics of silicon MIS diodes were first studied by Grey [6]. This work was limited to the conductance characteristics of p-doped devices with average oxide thicknesses estimated to be 40 to 70 Å. Later studies by Shewchun et al. [7] and Dahlke and Sze [8] extended this work. In the former case the effects of surface states and doping on the a.c. conductance "well" of the MIS tunnel diode were studied. In the latter case interest also centered on the a.c. conductance due to surface states, in particular the effects of sample annealing on this conductance. In addition Dahlke and Sze considered the d.c. characteristics of several types of MIS diode. Their analysis of these characteristics was not particularly extensive.

Predating slightly the work of Shewchun et al. and Dahlke and Sze was a series of interesting experiments by Esaki et al. [7] on a different type of MIS system. Employing the evaporated degenerate p-type semiconductors SnTe and GeTe, the tunnel I-V characteristics of $A\ell$-$A\ell_2O_3$-SnTe and

$Al-Al_2O_3$-GeTe diodes were investigated. Theoretical predictions of the I-V characteristics of these devices, employing a single band model of the insulator and a WKB tunnel probability (neglecting image force effects and band binding), proved to be in good qualitative agreement with experiment.

Apart from the calculations of Esaki and co-workers and to a lesser extent Dahlke and Sze, little effort has gone into analysing the d.c. currents in the equilibrium MIS tunnel diode. This is particularly true for diodes employing non-degenerate semiconductors. An extensive theoretical model of tunneling into surface states in MIS diodes has been developed by Freeman and Dahlke [33]. The a.c. aspects of this model have been applied to experiment by Kar and Dahlke [35] but again little consideration was given to the d.c. currents flowing through these states and the effects of both current and charge on the basic band currents.

In this chapter we discuss the d.c. tunnel currents observed in silicon MIS diodes of varying doping density and doping type. By comparison with the theory developed in the previous chapter, a determination of the dominant band or surface state current in a given bias region can be made. From the consistency between theory and experiment the validity of the models employed can be checked.

The techniques used in the fabrication of the MIS diodes discussed in this thesis are described in Sec. 3.2.

In Sec. 3.3 experimental results obtained with diodes employing non-degenerate semiconductors are considered, while in Sec. 3.4 the log I-V characteristics of degenerate silicon MIS diodes are presented. The dominance of tunneling currents in the latter diodes is confirmed by the superconducting electrode test.[3] Qualitative agreement between theory and experiment is obtained in all cases.

In non-degenerate silicon devices it is necessary to consider carefully the effects of current flow on the thermal equilibrium in the diode. It has been found that the I-V characteristics of non-degenerate silicon diodes can be placed into two categories, "equilibrium" and "non-equilibrium" characteristics. The distinction between these two categories was discussed in Chapter 1. Only current-voltage data of the former type are presented in this chapter. A presentation of results in the latter category is left to Chapter 4.

3.2 Experimental Procedure

The MIS tunnel diodes studied in this thesis were generally fabricated from polished Monsanto wafers of (111)- or (100)-oriented p or n-type silicon. Each wafer was first chemically prepared [37], and then thermally oxidized in a wet oxygen or steam atmosphere at 800-900°C. Metal contacts were applied to the oxide by evaporation of the metal of interest (typically aluminum) through masks, the masks serving to define the contact geometry (typically 15 mil diameter dots). Large area ohmic back contacts were formed by similar means on the stripped unpolished back side of each wafer. Evaporations were carried out in an NRC vacuum evaporator with a liquid nitrogen-trapped oil diffusion pump of base pressure $\sim 5 \times 10^{-7}$ torr.

A completed wafer, with its array of MIS diodes, was then transferred to an enclosed probe table where contact could be made to individual members of the diode array by means of micromanipulated tungsten wires. Electrical properties investigated included the C-V, G-V and I-V characteristics of a diode. The C-V and G-V measurement apparatus employed has been described adequately elsewhere [38]. I-V measurements were conducted either point by point with a Kiethley picoampmeter or by means of a continuously reading log I-V system manufactured in house. The sensitivity of the former instrument was $\sim 10^{-13}$ amps, while of the latter, $\sim 10^{-11}$ amps.

Temperature dependences of the diode characteristics could be checked by introducing liquid nitrogen into the measurement chamber to cool the copper pedestal on which the wafer rested. This permitted the effect of temperature variations between 77°K and 300°K to be studied. For low temperature studies (i.e., 4.2°K) individual diodes were scribed from the wafer and mounted by means of conducting silver epoxy on TO-5 headers. Connections between the metal electrodes of the diode and the through-pins of the header were made by means of indium wire. A cold welding technique [39] was found to be an excellent means of providing a good bond between the freshly cleaved indium wire and the metal electrode. To complete the connection, the other end of the indium wire was then soldered to the header lead. The main advantage of this bonding technique over ultrasonic bonding techniques, for example, is the lack of mechanical damage incurred by the sample.

Determination of the insulator thickness was accomplished by one of two means, ellipsometry [40] or comparison of experimental C-V results with theory. A description of the former technique is given in Ref. 40 and will not be elaborated upon. In the latter case the usual approach taken is to obtain the diode capacitance magnitude in extreme accumulation where $C \rightarrow C_o$. In these thin oxide structures, however, a limit is placed on the voltage that

can be applied to the diode by the maximum dielectric strength of the insulator (i.e., for $SiO_2 \sim 10^7$ V/cm) [23]. As a result, only a rather crude extrapolated value of C_o can be obtained by this method. This problem can be circumvented by a comparison of theoretical C-V curve shape and magnitude with experimental data at biases in the light accumulation region. This method is quite accurate but rather tedious. A much faster method, with sufficient accuracy for our purposes, was the use of the approximation that the diode capacitance at a given bias was generally a known fraction of C_o. This approximation was found to give fairly accurate values of C_o over the limited range of thicknesses studied. For example, at +1 volt in n-silicon diodes, the capacitance was found to be equal to $\sim 0.93\ C_o$ for our devices (and processing procedure).

The overall accuracy of both the ellipsometry and capacitance method is limited mainly by any inaccuracy in ε_i, the relative dielectric constant of the insulator. In the former method the optical value of ε_i for SiO_2 was employed (given by $\varepsilon_i = 2.13$) [41]. In the latter, the static value for SiO_2 of $\varepsilon_i = 3.8$ was assumed [23]. For comparison, the values of d_0 found by each method for several diodes are plotted in Fig. 3.1 versus oxidation time, t_{ox}, of each silicon wafer. The ellipsometry measurements were made on each wafer prior to the evaporation of the metal field

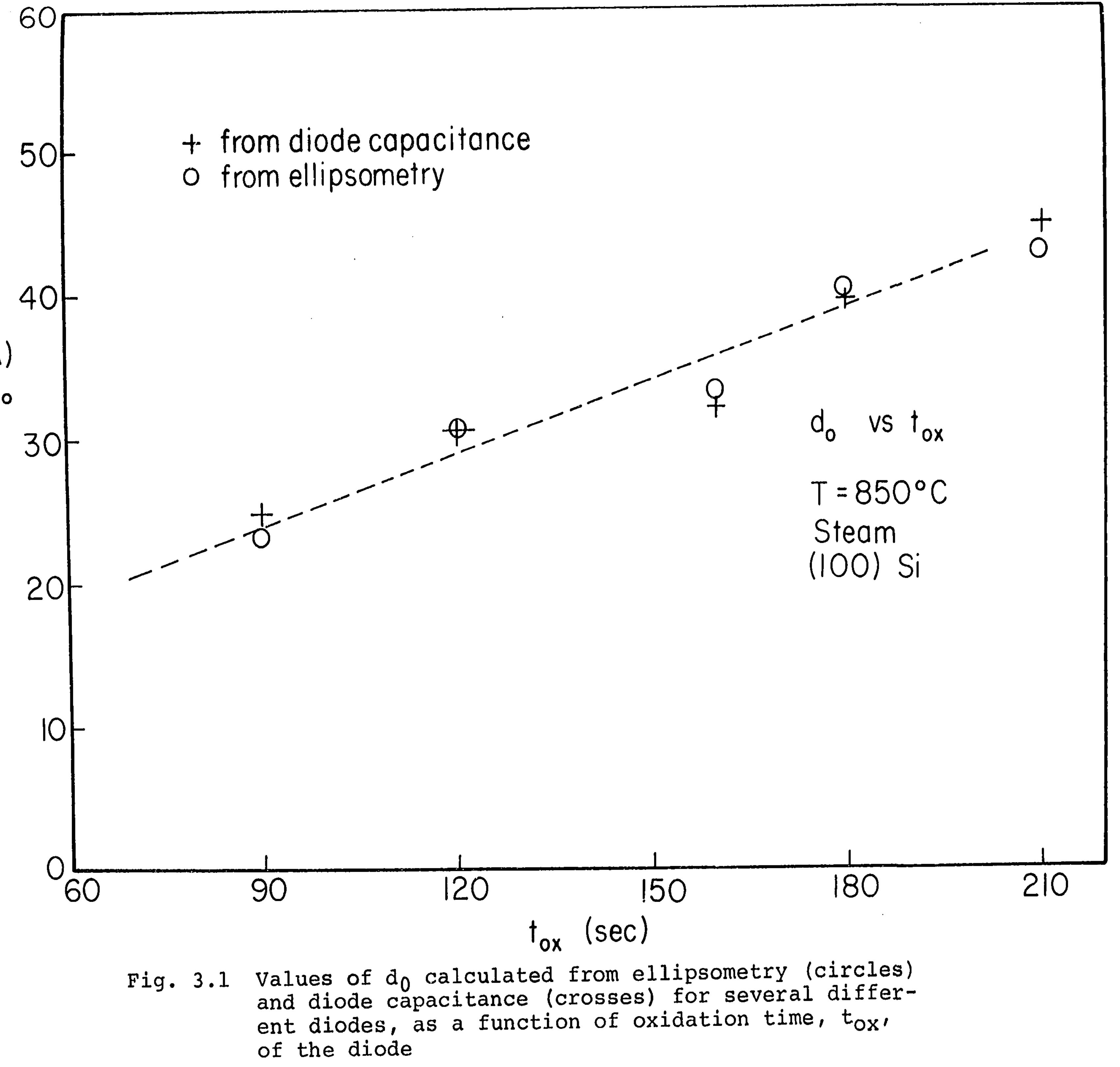


Fig. 3.1 Values of d_0 calculated from ellipsometry (circles) and diode capacitance (crosses) for several different diodes, as a function of oxidation time, t_{ox}, of the diode

plates employed for the capacitance measurements. Agreement in the predicted values of d_0 was typically within 10%.

It should be noted that both of the above approaches provide only a measure of the average oxide thickness, d_0. Several authors have observed [42-44] that $d_0 > d_T$, the tunnel oxide thickness. Since it is this latter thickness which we are interested in, the values of d_0 found can merely be used to classify a particular diode or set an upper bound on the value of d_T.

It is possible to obtain an estimate of d_T, experimentally, from measurements of J_T in a series of diodes of different d_0. A plot of J_T^{-1} (at +1 V) vs d_0 can then be obtained as shown in Fig. 3.2. To understand the significance of such a plot, consider the theoretical expression for the tunnel probability given by Eq. 2.5. Assuming, merely to illustrate the point, that the barrier has a constant rectangular barrier potential, then an analytic expression for the tunnel probability can be written as

$$J_T \propto e^{-Kd_T} \quad . \qquad 3.1$$

This equation can be rewritten in the form

$$J_T \propto e^{-K'd_0} \qquad 3.2$$

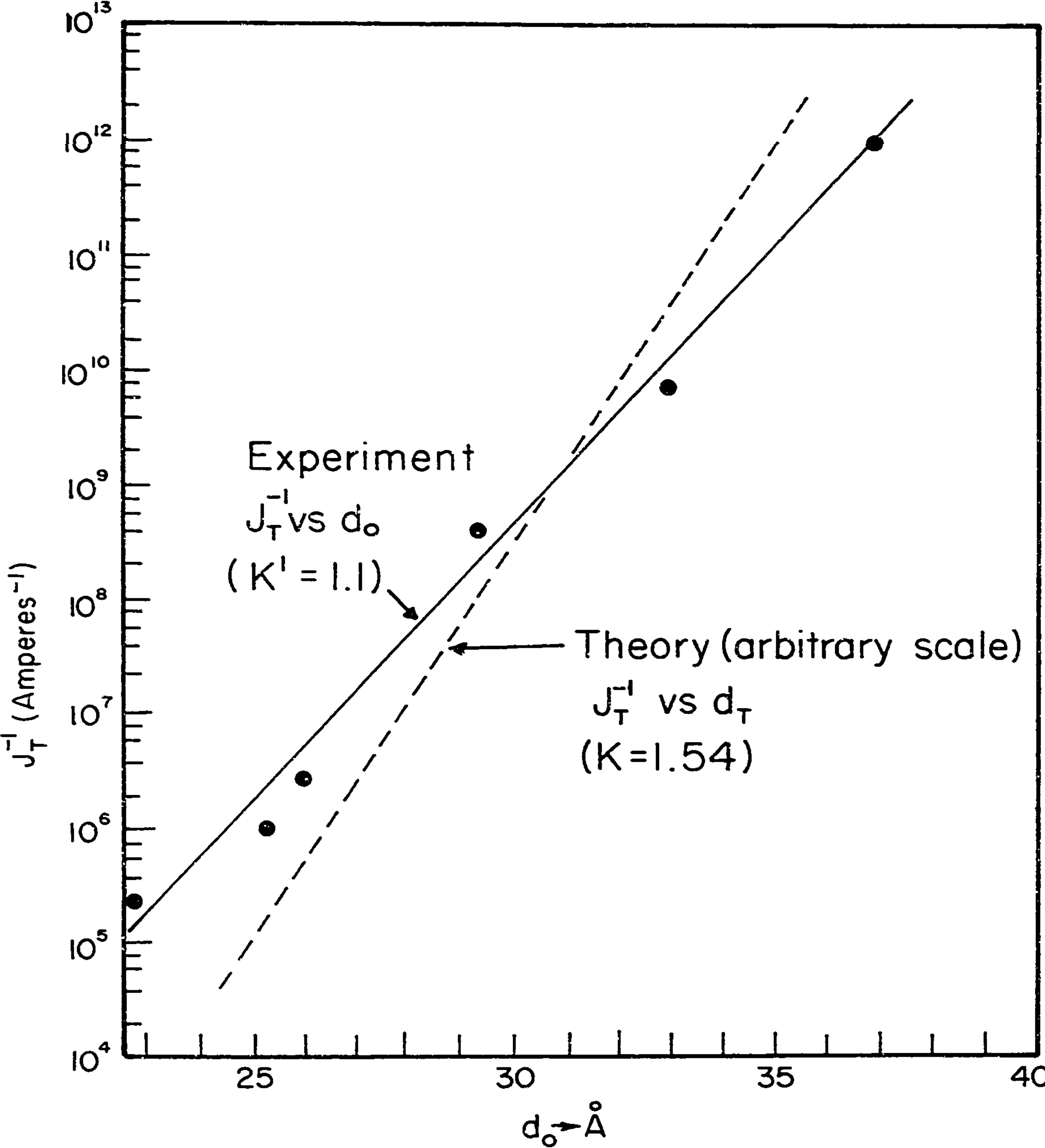


Fig. 3.2 Experimentally determined values of J_T^{-1} (dots) plotted versus d_0 give straight line of slope K' = 1.1. Theoretically determined plot of J_T^{-1} versus d_T (dashed curve) gives K = 1.54.

where

$$K' = Kd_T/d_0 \quad . \qquad 3.3$$

Thus by comparing the theoretically determined value of K with the experimentally determined value of K', the ratio of d_T/d_0 can be obtained. Assuming this ratio to be constant for the range of d_0 considered, d_T can be estimated for any given diode, from a determination of d_0. In Fig. 3.2 a value of K' = 1.1 was obtained (where thicknesses were measured in Angstroms). Making no assumptions concerning the shape of the barrier, a theoretical plot of J_T^{-1} vs d_T was obtained that is shown in Fig. 3.2 (the dashed curve). The slope of this latter curve is K = 1.54.

Thus

$$\frac{d_T}{d_0} = \frac{K'}{K} \equiv n$$

$$= 0.7 \quad .$$

This value of n is within the range of values determined by Pollack and Morris [43] for MIM diodes and indicates that the tunnel oxide thickness, d_T, can vary considerably from the average oxide thickness, d_0. An accurate determination of d_T for a given diode is obviously quite difficult.

As a final note, all diodes may be assumed, unless otherwise stated, to be Aℓ-SiO_2-Si devices with steam grown insulators on (100)-oriented silicon. No major differences were apparent when using wet oxygen instead of steam. However, quite noticeable differences were observed with diodes fabricated from (111)-oriented silicon as opposed to (100)-oriented material. These differences will be discussed in later sections.

3.3 Non-Degenerate Silicon MIS Tunnel Diodes

Before proceeding to a presentation of data concerning the d.c. transport in our non-degenerate silicon diodes, consider first the C-V characteristics of two typical diodes shown in Fig. 3.3. These diodes were fabricated with 10 Ω-cm n-type and 1 Ω-cm p-type material respectively. In the nomenclature of Chapter 2 they are, therefore, designated ${}_4N_{20}$ and P_{22} diodes.

The C-V data in Fig. 3.3 is presented here for two reasons. First it establishes the identity of the structures being considered as MIS diodes, and second, it confirms that equilibrium conditions prevail in the semiconductor despite the presence of d.c. current flow. The distinctive voltage variable capacitance behaviour of the MIS diode has been the subject of much research and many articles. The reader is directed to Grove's "Physics and Technology of Semiconductor Devices" [23] for a review of the a.c. properties of these devices.

The C-V feature of particular interest, which establishes a particular diode as an MIS diode, is the saturation of the C-V characteristic at biases corresponding to the "accumulation" of the semiconductor surface. Such a property is shown by both the C-V curves of Fig. 3.3.

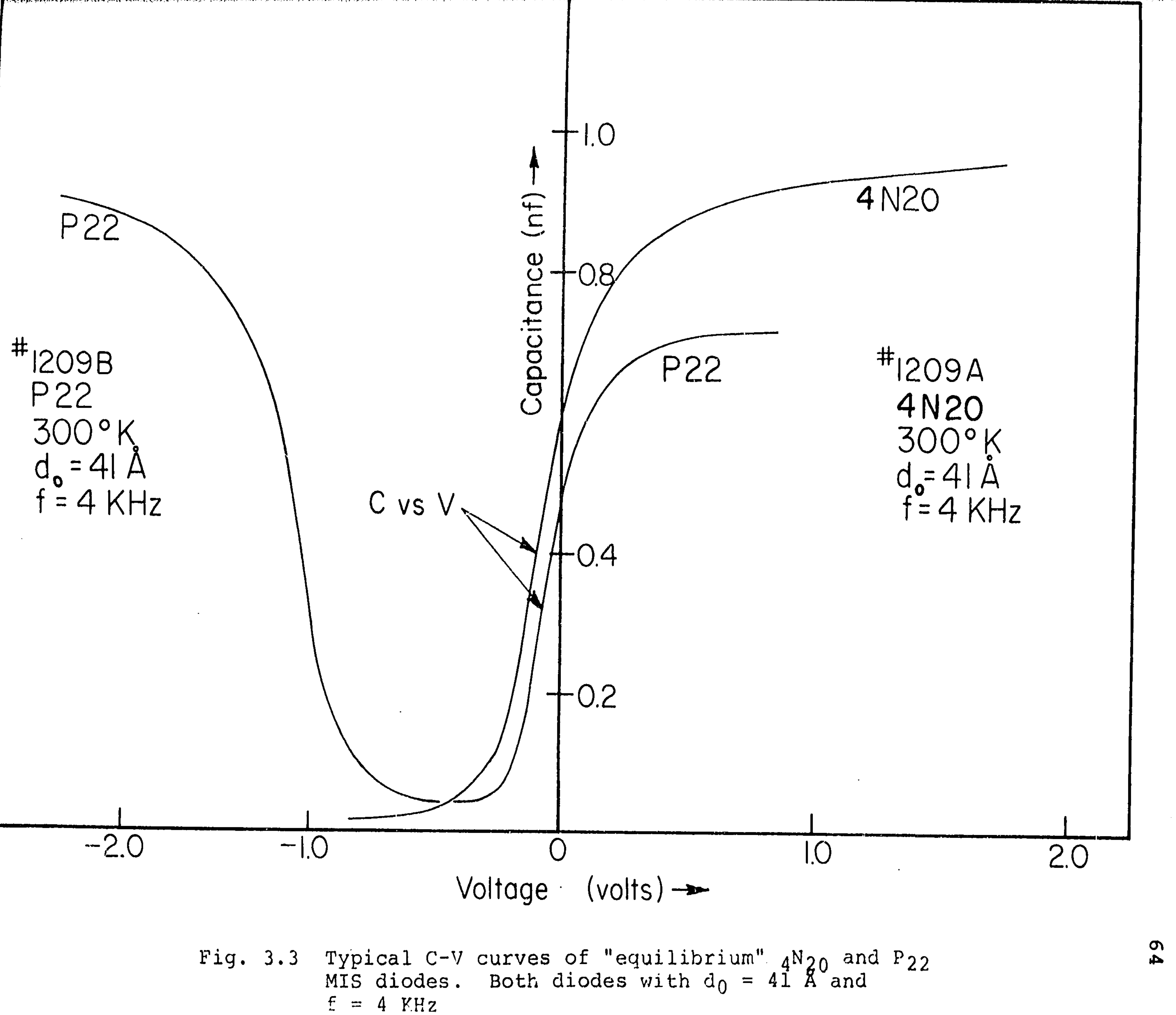


Fig. 3.3 Typical C-V curves of "equilibrium" $_4N_{20}$ and P_{22} MIS diodes. Both diodes with d_0 = 41 Å and f = 4 KHz

This saturation essentially implies that the majority carrier distributions are thermal equilibrium distributions. The carrier supply from the back ohmic contact in a biased diode is sufficient to maintain thermal equilibrium under any conditions of moderate current flow. In diodes where a saturating accumulation capacitance is in evidence, therefore, it will be assumed ϕ_n (for n-silicon) and ϕ_p (for p-silicon) $\sim E_{FSEM}$. The situation for minority carriers is considerably different, sufficiently so that a separate chapter will be devoted to the effects on the MIS diode transport properties of non-equilibrium conditions for minority carriers. Suffice it to say here that a saturating inversion capacitance is indicative (in the absence of external stimuli such as light) of a thermal equilibrium distribution of minority carriers throughout the semiconductor, with ϕ_p (for n-silicon) and ϕ_n (for p-silicon) $\sim E_{FSEM}$.

After establishing that the structures being studied are "equilibrium" MIS diodes, the d.c. transport properties of these structures are now considered. Typical log I-V characteristics of n and p-type MIS diodes are presented in Figs. 3.4a and 3.4b. These I-V characteristics are shown at both 300°K (solid lines) and 100°K (dashed lines). Of the seven basic conduction processes in insulators [46] (these include Schottky emission, Frenkel-Poole emission, ionic conduction, ohmic conduction, space charge limited

Fig. 3.4 Log I-V characteristics of ${}_4N_{20}$ (#1209 A) and P_{22} (#1209 B) diodes at 300°K (solid curve) and 100°K (dashed curve). Both diodes have d_0 = 41 Å. Theory for "equilibrium" diodes at 300°K (100°K) given by triangles (circles). Parameters for theory listed in Table 3.1

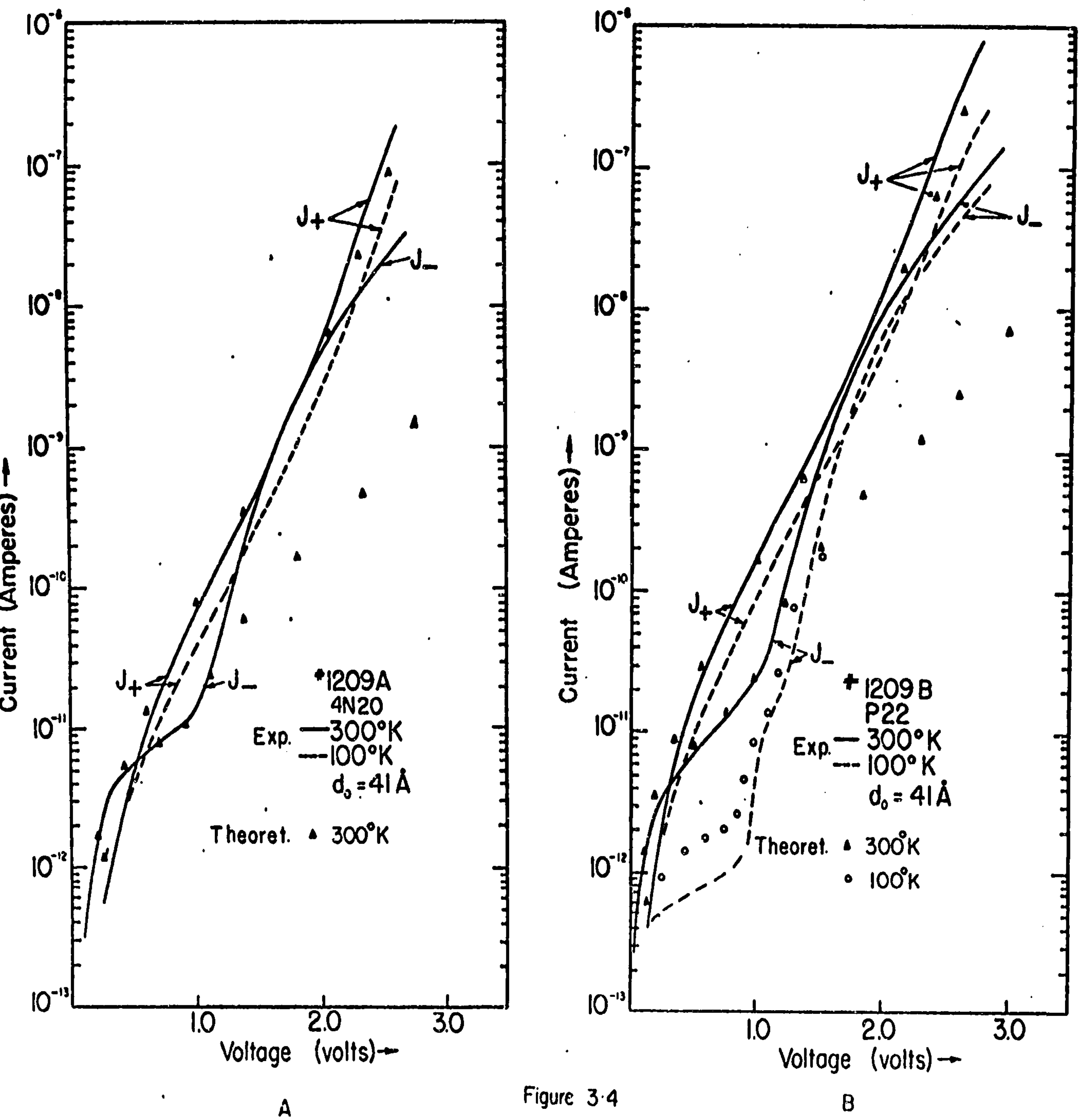


Figure 3·4

conduction, field emission into the insulator conduction band and tunneling), only tunneling can adequately explain the temperature independent current-voltage curves seen in Figs. 3.4a and 3.4b. This assumption can be confirmed experimentally, in degenerate silicon diodes, by applying the superconducting electrode test [3]. The results of such tests are discussed in the next section. Unfortunately non-degenerate semiconductor devices are not suited for this test due to the low temperatures required (i.e., $\lesssim 7°K$ for diodes with Pb electrodes). Such temperatures freeze out a large percentage of the majority carriers making the semiconductor into a virtual insulator. However, since the fabrication procedures are identical for both degenerate and non-degenerate diodes it seems reasonable to conclude that tunneling is also the dominant conduction process through insulators of the non-degenerate diodes as well.

It can be seen in Figs. 3.4a and 3.4b that the choice of dopant species in these non-degenerate diodes makes little difference to the log I-V characteristics. Virtually identical current-voltage curves are obtained for both p and n-type diodes. As will be seen in the theoretical analysis, this is due to the fact that identical tunnel current components are responsible for I-V characteristics of both diodes.

Under positive biases in these diodes, a more or less exponential increase in current magnitude with bias is

obtained. Under negative bias the current initially saturates then, as $V_a < -1$ V, rises sharply with bias. Thus it can be seen that, as in the C-V data of the n-silicon diode, there are three basic bias regions to be considered, corresponding to accumulation, depletion and inversion respectively. In the p-silicon diode it is interesting to note that the converse is true and that these same regions correspond to inversion, depletion and accumulation respectively.

Before proceeding with a theoretical analysis of these currents we present here the results of one other experiment which will aid in the determination of the physical parameters associated with the MIS system. In Fig. 3.5 the positive bias log I-V characteristics of two diodes of differing insulator thickness are presented. Both diodes are (111)-oriented silicon N_{21} diodes, one with $d_0 \sim 34$ Å and one with $d_0 \sim 41$ Å. The current scales of these two current-voltage curves have been adjusted to place the curves side by side in order that the logarithmic slopes can be compared. Virtually no difference in slope between the two curves can be seen despite the approximately three orders of magnitude difference in current level.

In analysing the observed currents in the non-degenerate MIS diodes, we first present typical theoretical log I-V characteristics as a function of temperature. The various tunnel current components are shown in order that

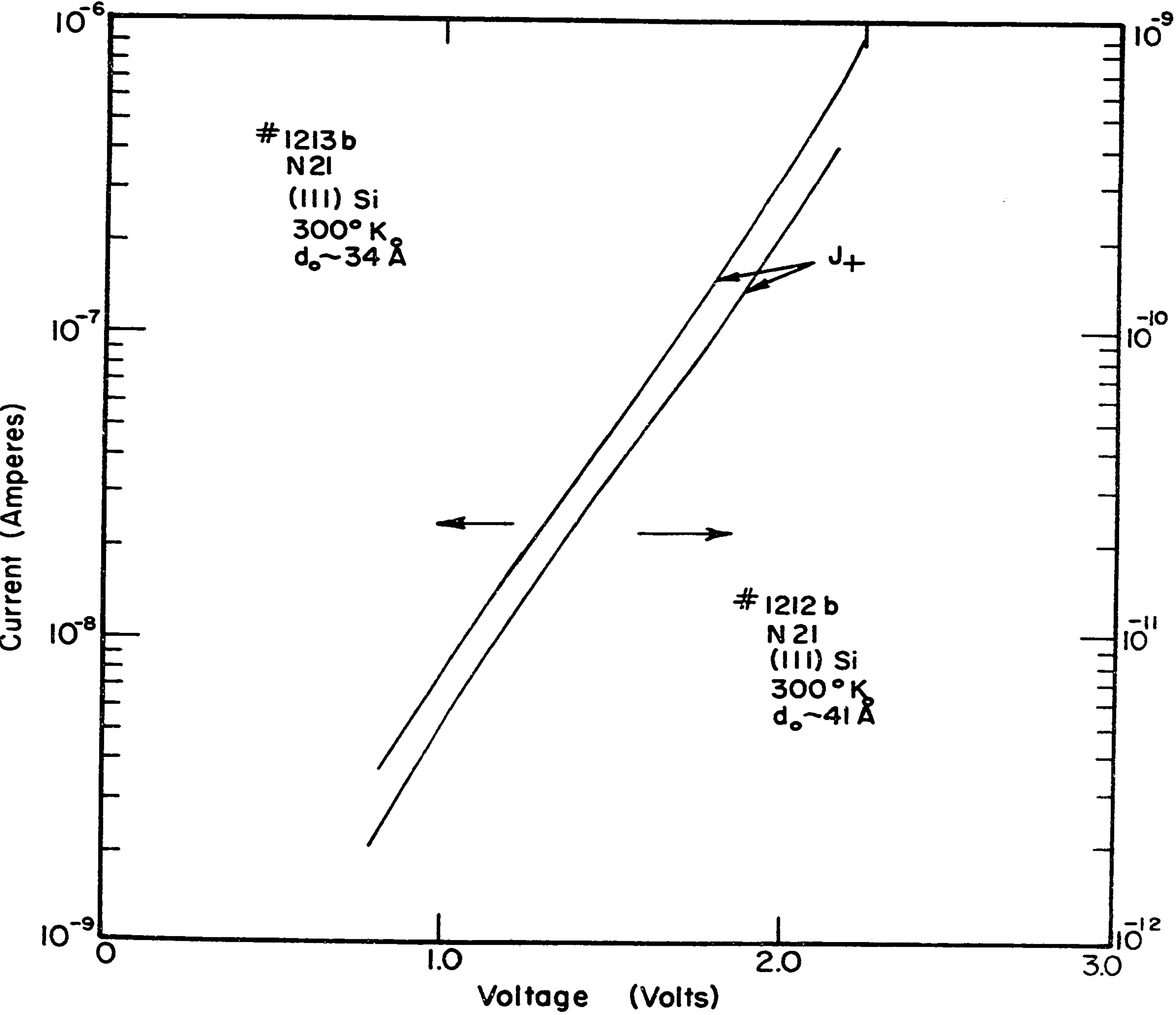


Fig. 3.5 Log I-V characteristics (+ve bias) of two N_{21} diodes, #1213b with $d_0 \sim 34$ Å and #1212b with $d_0 \sim 41$ Å. Both diodes fabricated with (111)-Si

their relative magnitudes can be compared. Following this, a detailed comparison of theory and experiment is made and the problems associated with obtaining a fit of theoretical and experimental I-V curves in each bias region are discussed.

The theoretical I-V characteristics of a P_{22} diode are shown in Fig. 3.6, calculated for the temperatures 300°K (solid lines) and 100°K (dashed lines). Other physical parameters assumed are listed in Table 3.1. Although the device was taken to be a p-silicon diode, the I-V curves of Fig. 3.6 could equally well have been applied to an n-silicon device. For this reason only one set of current-voltage characteristics is presented. Essentially all of the features of the experimental log I-V characteristics of both p and n-type diodes (cf. Fig. 3.4) are qualitatively reproduced in the theoretical log I-V curves of Fig. 3.6. This similarity extends to the variations with temperature as well. It can be seen that the major influence of a temperature decrease to 100°K is felt in the bias region $0 > V_a > -1$ V, in both theory and experiment. This region is the depletion region of both these diodes and reflects the temperature dependence of the quantity $f_2 - f_1$ as in Eq. 2.1. It should be noted that no experimental curve for the n-silicon diode at 100°K (cf. Fig. 3.4a) is presented. The reasons for this will become apparent in the next chapter and are related to a non-equilibrium condition for minority carriers in the semiconductor at these temperatures.

At large negative and positive biases the theory predicts essentially no influence of temperature on current

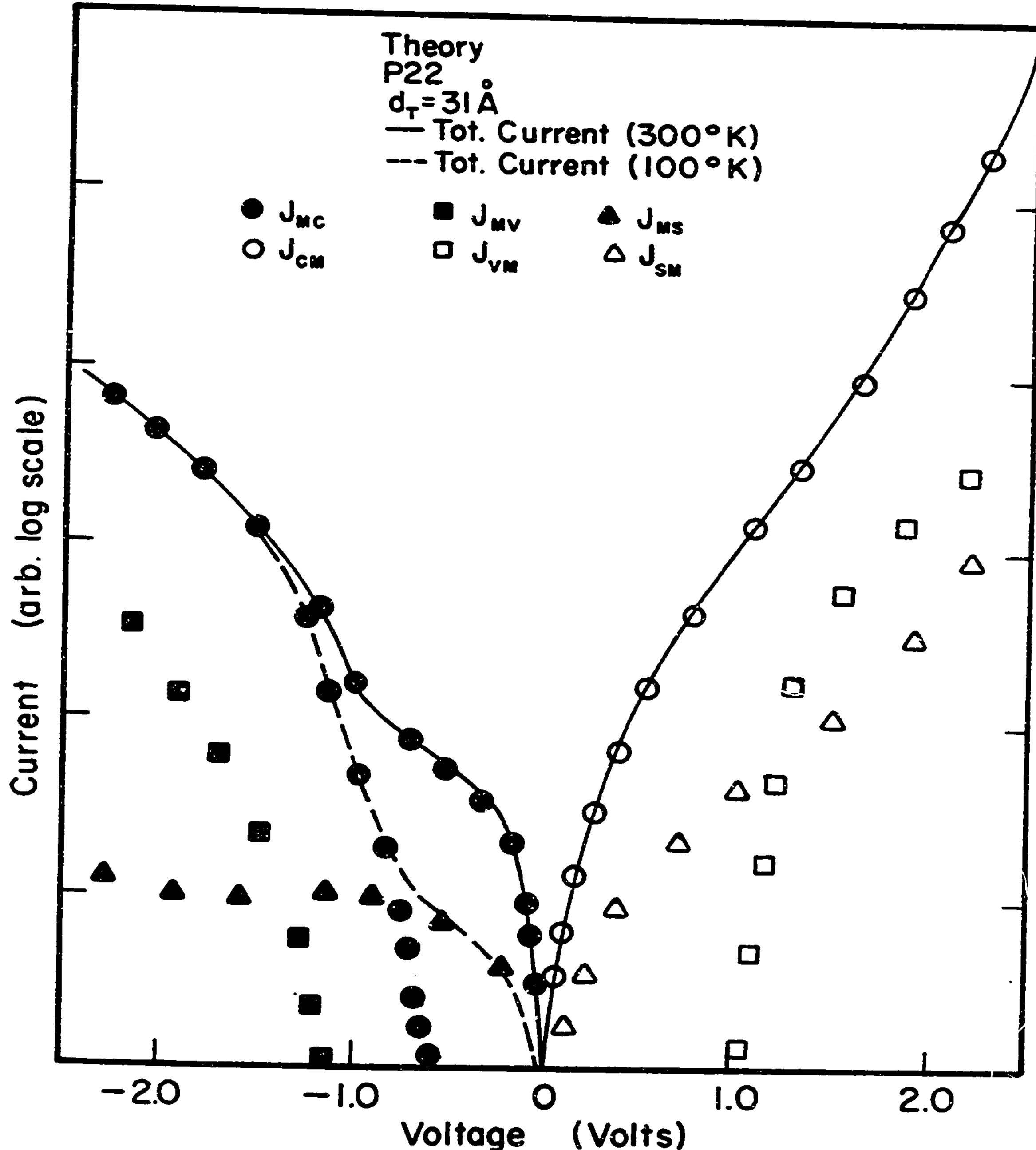


Fig. 3.6 Theoretical log I-V curves of P_{22} diode with d_T = 31 Å. Total current at 300°K (100°K) given by solid (dashed) curves. Components of the total tunnel current are as listed in the figure with only J_{mc} (dots) being temperature dependent. The total tunnel current is replotted in Fig. 3.4b. Parameters assumed are listed in Table 3.1.

Table 3.1

Parameters assumed for the theoretical calculations shown in Figs. 3.4a, 3.4b and 3.6

Data for theory of	Fig. 3.4a	Fig. 3.4b
Semiconductor	N-Si	P-Si
Doping Density	$4\times10^{20}/m^3$	$10^{22}/m^3$
Temperature	300°K	300°K/100°K
Tunnel Probability	WKB	WKB
Image Force Potential	MIM	MIM
m^*_{cb}	1	1
m^*_{vb}	1	1
d_T	32 Å	31 Å
E_{gox}	8 eV	8 eV
X	3.2 eV	3.2 eV
ϕ_m	3.2 eV	3.2 eV
N_{ox}	$4\times10^{16}/m^2$	$3\times10^{16}/m^2$
Surface State Distribution (cf. Fig. 2.11)	SS3 (+ $6\times10^{16}/m^2/eV$ peak near valence edge)	SS3

magnitude. This is not the case experimentally, although the influence is relatively small. A possible explanation for the weak temperature dependence of the experimentally observed currents has been noted by Keyes [47]. He has suggested that, at least in tunnel diodes, such temperature effects could be due to thermal ionization of carriers over locally low barriers. These lowerings of barrier height, he attributes to charge fluctuations in the space-charge barrier. The presence of charge in the insulator of MIS diodes could also create local variations in barrier height. However, the large magnitude of the original barrier of these diodes (i.e., ∿3.2 eV) should make thermally ionized currents improbable if the variations are minor.

In the theoretical I-V curves of Fig. 3.6 the dominant currents at all biases are predicted to be electron flows (i.e., J_{cm} and J_{mc}). This fact is perhaps surprising only in the p-silicon case and indicates that the probability of carriers tunneling to or from the semiconductor valence band is considerably lower than the probability of carriers tunneling to or from the semiconductor conduction band (for the particular barrier masses assumed for these calculations).

Under negative bias, the electron current, J_{mc}, can be seen in Fig. 3.6 to dominate the total current. The saturation of this current in the bias region $0 > V_a > -1$ V is due to the influence of the semiconductor band bending on the tunnel currents. Shewchun et al. [8] have shown that in

this bias region, V_{ox}, is essentially constant. Increases in applied bias appear predominantly across the semiconductor. The metal Fermi level, therefore, becomes pinned with respect to the semiconductor conduction band edge, E_c^s. This condition persists, in an "equilibrium" diode, only until sufficient bias is applied to invert the surface. Thus for $V_a < -1$ V, J_{mc} rises sharply. This bias also corresponds to the voltage at which J_{mv} becomes appreciable. However, as in the positive bias case (e.g., with J_{vm}), the valence band current remains relatively small with respect to the conduction band current.

Concerning this latter point, it should be noted that while the valence band current is relatively small, it is not entirely negligible. This fact will be important in the analysis of a transistor structure, employing MIS tunnel diodes, that is discussed in a subsequent chapter.

Employing the surface state distribution SS3 (cf. Fig. 2.11) with a tunnel capture cross-section of 10^{-18} m^2, the I-V curves given by the triangles in Fig. 3.6 were obtained. As shown here, little direct contribution to the total tunnel current is provided by these surface state currents (for T = 300°K). This is not the case at lower temperatures, as seen by the dashed curve in Fig. 3.6. It is apparent that, while the band currents in the depletion region are quite temperature dependent, the surface state

currents are not. Thus at 100°K, the dominant current for $0 > V_a > -1$ V is the latter current. A similar drop in the current magnitude of the saturation current can be seen in the experimental data of Fig. 3.4b. The resulting current level must, therefore, be a direct measure of the magnitude of the surface state currents in these p-silicon diodes. As this magnitude is small compared to the room temperature current levels, it can be concluded that surface state currents are indeed negligible in our (100)-oriented silicon, non-degenerate diodes.

The total theoretical tunnel current in Fig. 3.6 has also been plotted in Fig. 3.4b for direct comparison with experiment. The theory calculated at T = 300°K is given by the solid triangles, while the theory for T = 100°K is given by the open circles. In two of the three basic bias regions considered (i.e., $V_a > 0$ and $0 > V_a > -1$ V), an excellent qualitative fit to experiment is obtained. Only in the third region (i.e., $V_a < -1$ V) are discrepancies apparent.

The problem in matching theory and experiment is principally the choice of physical parameters for the barrier, in particular, the insulator masses, m^*_{cb} and m^*_{vb}. Several sources of information concerning these masses are available. The first is the experimental log I-V curve shape itself. The overall curve shape is consistent with the view that the dominant current components are tunneling via the insulator

conduction band. This is made apparent by the lack of current flow from the semiconductor valence band to any great degree. It was pointed out in Chapter 2 that, were this not the case, distinctive features in the I-V curves would become obvious (cf. Fig. 2.4, curve 'c'). From this, it can be concluded that a lower limit on m^*_{vb} can be assumed, given by $m^*_{vb} > m^*_{cb}$.

A second source of information is the data of Fig. 3.5. In Chapter 2 it was seen that both the insulator masses and thickness, d_T, influence the slope of the log I-V characteristics of these diodes. While the insulator masses cannot be readily controlled, the value of d_T can. In Fig. 3.5 it is seen that despite a large change in d_0 and apparently d_T (as indicated by current magnitude) virtually no change in slope was found. This result, although somewhat puzzling, can be explained qualitatively from the theoretical findings of Schnupp [21]. His model of the insulator predicted, in effect, that $m^*_{vb} \to \infty$ as $d_T \to 0$. The effects of increasing d_T would, therefore, be cancelled by the effects of decreasing m^*_{vb}.

One final source of information discussed here, concerning the tunnel carrier masses in the insulator, is the ratio of J_+ to J_- e.g. at $|V_a| = 2$ V. Although not shown, this ratio becomes quite large with a one band model of the insulator. To reduce this ratio to the value seen in the

theoretical curves presented in Fig. 3.4b, it was necessary to assume a value, $m^*_{vb} = 1$. Even at this value, the ratio does not agree with that found experimentally, as also seen in Fig. 3.4b. Further reduction in m^*_{vb} cannot be permitted without enhancing the currents, J_{vm} and J_{mv}. Also, a reduction in both masses simultaneously (i.e., $m^*_{vb} = m^*_{cb} = 0.5$) is not possible since values of $d_T \gtrsim d_0$ are then necessary to obtain a slope of the log I-V characteristics which matches experiment.

Part of the problem with the latter approach is that independent of the masses, barrier height or tunnel thickness assumed, the theory appears unable to predict the appropriate negative bias I-V curve, at least in a fashion which is consistent with the remaining portions of the I-V curve. One possible reason for this inadequacy is, of course, the voltage distribution assumed. But, considering the fairly sophisticated methods employed for the calculation of the voltage distribution, it does not seem likely that this is the source of the problem. More likely it is an experimental condition not considered by the theory. One such condition is diffuse scattering of tunnel carriers [28] at the M-I and I-S interfaces. In asymmetric structures, such as the MIS diode particularly, this condition could influence the currents of one bias polarity more than the other. In any case, until the inconsistency is resolved, the value of m^*_{vb} cannot be estimated with any degree of accuracy by the latter means.

From the foregoing, it must be concluded that in non-degenerate diodes, there is no direct method of distinguishing the effects of mass variations (for $m_{vb} \gtrsim m_{cb}$) from thickness, or for that matter, barrier height variations. As a result, the phenomenological approach will be adopted and the best fit possible obtained with whatever masses are necessary. The test of the model will be the consistency with which the I-V characteristics of other types of MIS diodes can be predicted.

The effects of the barrier parameters on I-V curve shape apply, for the most part, to bias regions with $|V_a| > 1$ V. For biases $|V_a| < 1$ V, particularly in the depletion region, the effects of surface state and oxide charge as well as image forces predominate. With sufficient amounts of computer time, excellent fits of theoretical and experimental I-V curves are obtained in this region. In Fig. 3.4b, a fit was obtained employing the distribtuion SS3, an oxide charge density of $N_{ox} = 3 \times 10^{15}/m^2$ and an MIM type of image force. The voltage variable image force could have been used with the addition of $N_{ox} \sim 5 \times 10^{15}/m^2$. A good fit to the n-type diode's I-V characteristics (cf. Fig. 3.4a) was also obtained, but with $N_{ox} = 4 \times 10^{15}/m^2$ and with an addition to SS3 of a large density of acceptor like states (i.e., $N_{ss} \sim 6 \times 10^{16}/m^2/eV$) located in energy near the conduction band edge. The existence of such a peak at the I-S interface of thick oxide n-Si MIS diodes was first noted by Grey and Brown [36] employing an entirely different approach.

Summarizing the results of this section then, it has been seen that I-V characteristics of non-degenerate p and n-type MIS tunnel diodes are essentially identical. It was shown by means of theoretical calculations that this reflected the fact that identical tunnel current components (i.e., J_{mc} and J_{cm}) were dominant in each diode. A good qualitative fit of theoretical and experimental I-V curves of both types of diodes was found in most bias regions. To obtain this fit, insulator carrier masses, $m^*_{cb} = m^*_{vb} = 1$ were assumed.

3.4 Degenerate Silicon MIS Tunnel Diodes

Typical log I-V and G-V characteristics for a $_5N_{25}$ diode with $d_0 \sim 34$ Å (and lead electrode) are presented in Fig. 3.7. Similar data are presented in Fig. 3.8 for two P_{26} diodes, one (# 1219B in Fig. 3.8a) with $d_0 \sim 39$ Å and an aluminum electrode and the second (# 1220 in Fig. 3.8b) with $d_0 \sim 27$ Å and a lead electrode. The G-V data in Figs. 3.8c and 3.8d are of the latter diode. In both Figs. 3.7 and 3.8, solid curves depict data taken at 300°K while dashed curves, data taken at 4.2°K. For the G-V curves of the $_5N_{25}$ diode, the a.c. signal frequency was 1.5KHz while for the P_{26} diode, 5 kHz.

Just as with non-degenerate diodes, the majority carriers in the semiconductor of these devices will be assumed to have thermal equilibrium distributions. As for the minority carriers, it will be seen in the next chapter that the presence of a non-equilibrium distribution of these carriers has no discernable effect on the I-V characteristics of a degenerate silicon diode. We proceed, therefore, to the question of transport mechanisms in these diodes.

The zero bias regions of the G-V curves seen in Figs. 3.7b and 3.8c have been expanded and are shown in Figs. 3.7c and 3.8d respectively. In both cases, Pb

Fig. 3.7a Log I-V characteristics of ${}_5N_{25}$ diode (#1222) at 300°K (solid curve) and 4.2°K (dashed curve). This diode has a Pb contact, $d_0 \sim 34$ Å, and is fabricated from (111)-oriented silicon. Theory (at 300°K) given by solid triangles. Parameters for theory are listed in Table 3.2

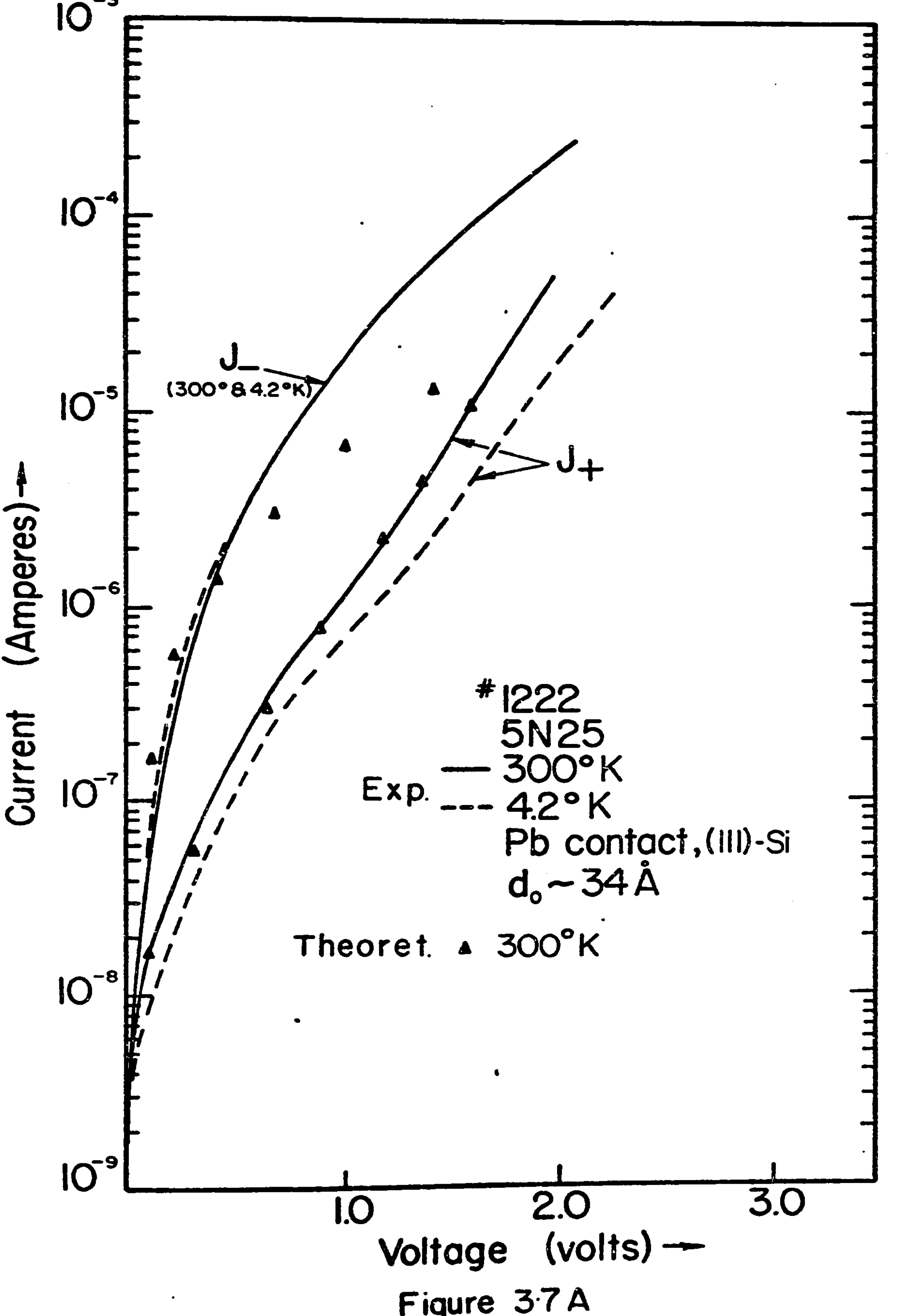


Figure 3·7 A

Fig. 3.7b G-V data for diode #1222 in Fig. 3.7a. Data taken at 300°K (solid curve) and 4.2°K (dashed curve). Signal frequency is f = 1.5 KHz

c Expanded view of zero bias region of data in Fig. 3.7b. Data taken at 300°K (solid curve) and 4.2°K (dashed curve). Signal frequency is f = 1.5 KHz (signal size is 750 μV, peak to peak)

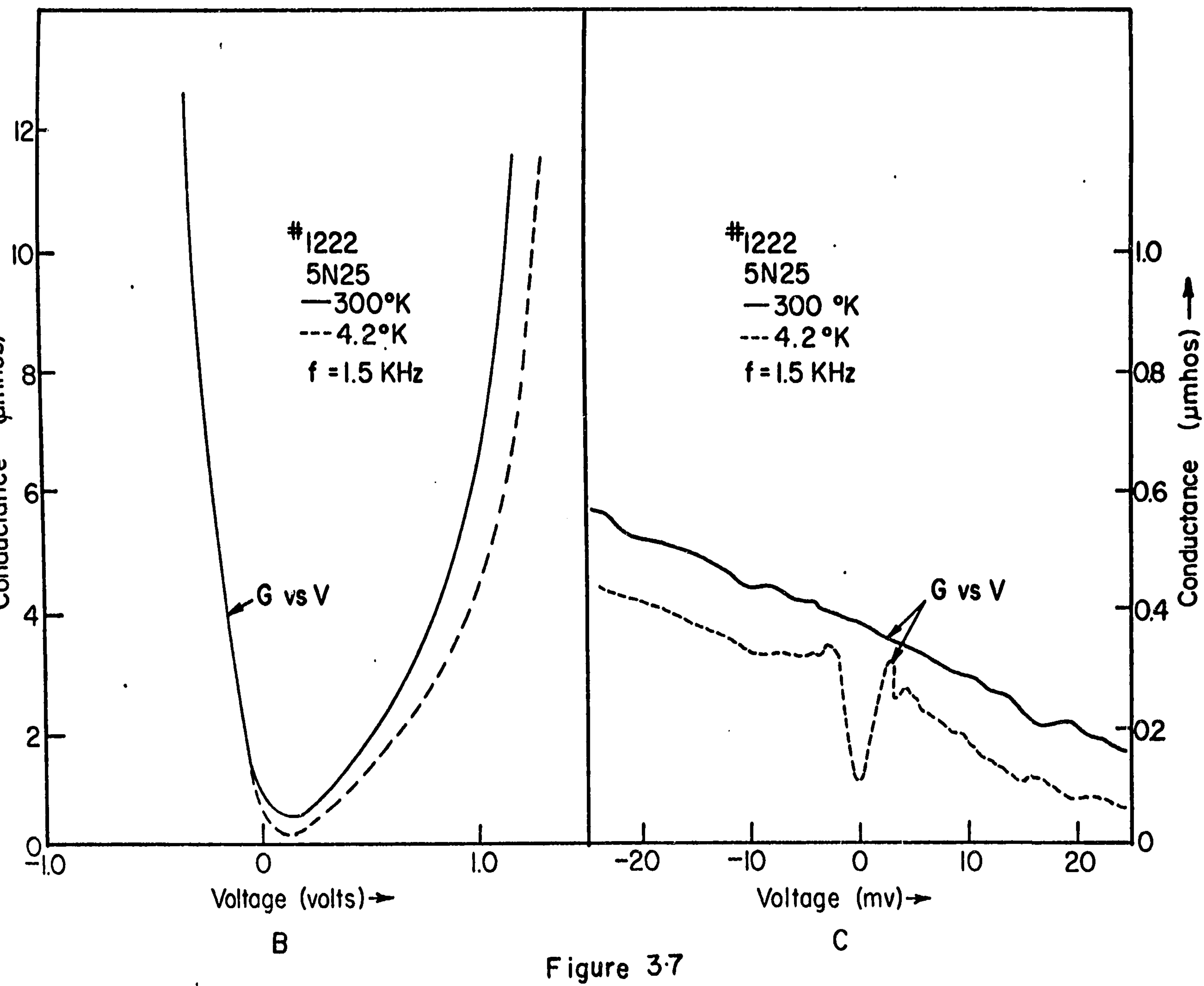


Figure 3·7

Fig. 3.8a Log I-V characteristics of P_{26} diode (#1219 B) at 300°K (solid curve). This diode has an Aℓ contact, $d_0 \sim 34$ Å and is fabricated with (111)-oriented silicon. Theory (at 300°K) given by solid triangles. Parameters for theory are listed in Table 3.2

b Log I-V characteristics of P_{26} diode (#1220) at 300°K (solid curve) and 4.2°K (dashed curve). This diode has a Pb contact, $d_0 \sim 27$ Å and is fabricated with (111)-oriented silicon.

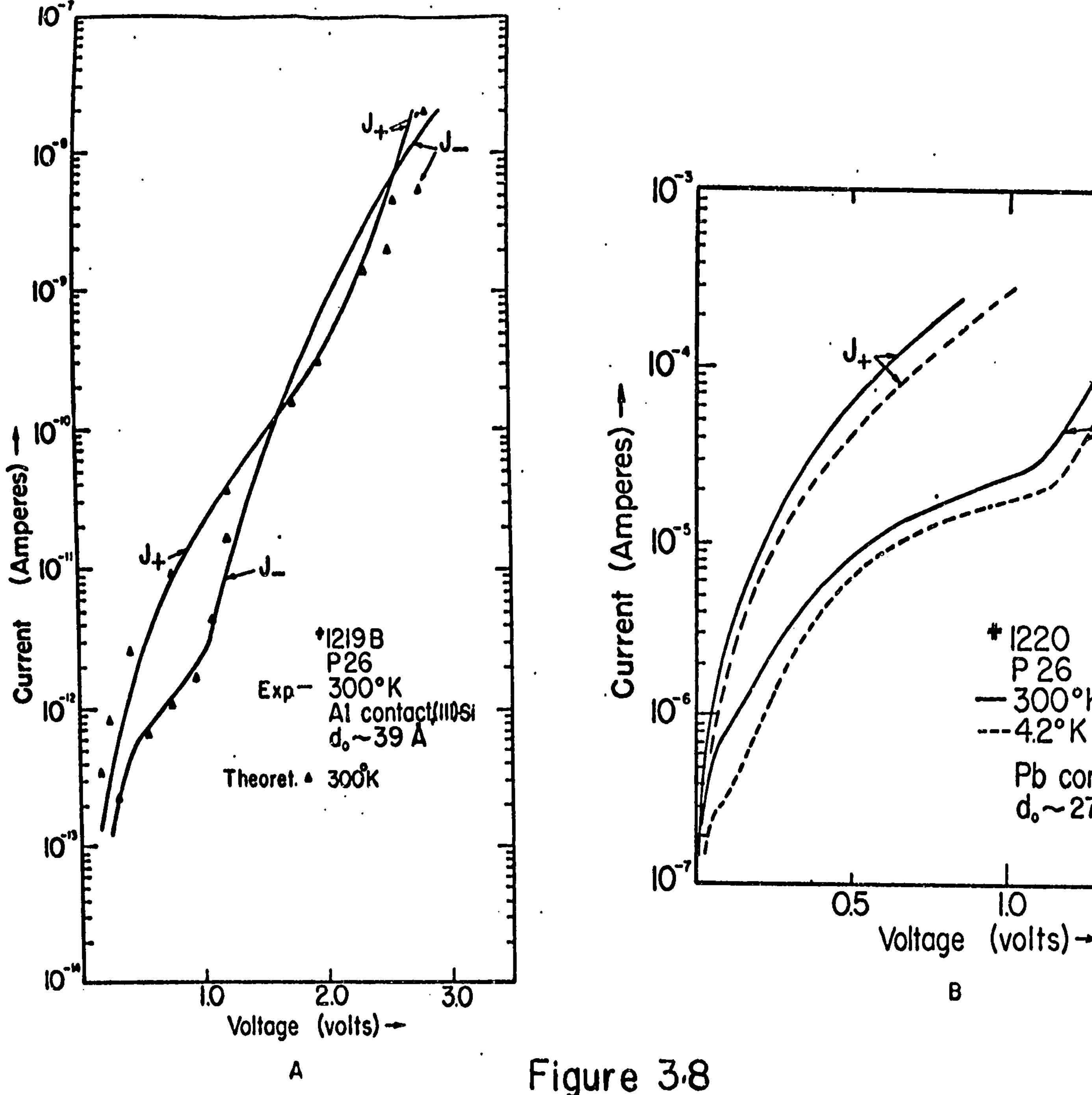


Figure 3.8

Fig. 3.8c G-V data for diode #1220 in Fig. 3.8b. Data taken at 300°K (solid curve) and 4.2°K (dashed curve). Signal frequency is f = 5 KHz

d Expanded view of zero bias region of data in Fig. 3.8c. Data taken at 300°K (solid curve) and 4.2°K (dashed curve). Signal frequency is f = 1.5 KHz (signal size is 750 μV, peak to peak)

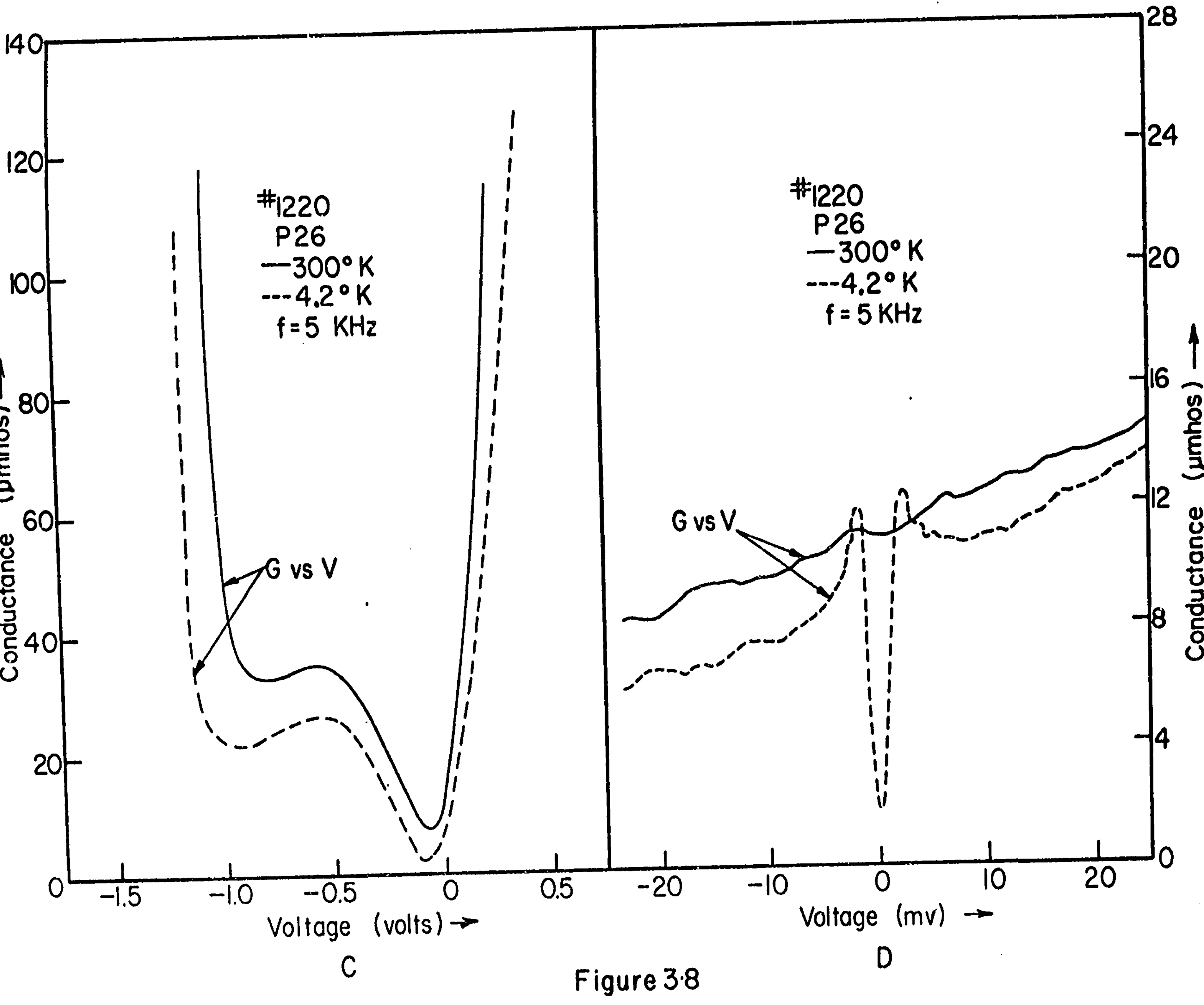


Figure 3·8

electrodes have been employed for which the superconducting transition temperature is known to be $T_c = 7.175°K$ [41]. Hence, structure appearing in the conductance-voltage characteristics near zero bias at $T = 4.2°K$ can be attributed to the superconducting properties of these electrodes.

For a metal in the superconducting state, an energy gap is created due to electron-phonon interactions [36]. As a result, the metal takes a form rather analogous to an intrinsic semiconductor with band gap $E_g = 2\Delta$ and chemical potential $E_F = \Delta$. The parameter Δ is associated with the binding energy of the "condensed" electron-pair states in a superconductor, and is of the order 1 meV. Thus it can be seen that for applied voltages of less than 1 mV, there are few electrons with sufficient energy in the semiconductor (at 4.2°K, 1 kT is only 0.3 meV) to tunnel to the unoccupied states above the superconducting energy gap. The conductance, therefore, shows a marked drop at voltages $-1 < V_a < 1$ mV.

The important point to be noted concerning the zero bias structure in the G-V results, is the fact that it can only be obtained if the currents involved are tunnel currents. Such structure thus provides excellent verification of the tunneling mechanisms in our degenerate MIS diodes. Two qualifications must be made to this statement. First, this test confirms tunneling only for $V_a \rightarrow 0$. At larger applied voltages, other mechanisms could conceivably come into play.

The general temperature independence of the I-V characteristics of the diode and the consistency of these characteristics with tunnel theories remain the only verification of tunneling at these larger voltages. Second, the superconducting electrode test was limited in application to diodes with relatively thin oxides (i.e., $d_0 \lesssim 35$ Å). This was due to the sensitivity of the available measuring apparatus. As a rule of thumb, it was found that zero bias conductances would be too low with which to obtain positive results, if current levels at $\sim$0.5 V were $<10^{-7}$ amps. Thus for the thicker oxide structures (i.e., $d_0 \gtrsim 35$ Å), no direct confirmation of tunneling mechanisms was obtained.

Consider now the log I-V characteristics of these diodes. In Fig. 3.7a, it can be seen that the negative bias current is now greater than the positive bias current for $V_a > 2.5$ V. In other words, the first cross-over point has increased from $V_a \sim 0.5$ V in Fig. 3.4a for the non-degenerate n-type diode to $V_a > 2.5$ V in the degenerate n-type diode. Corresponding to this increase is a lack of the saturation region exhibited by the I-V curves of the non-degenerate devices. As a result, the curves are rather featureless with both positive and negative bias currents increasing more or less exponentially with bias.

This is not the case with the I-V curves of the degenerate p-type diodes. In Fig. 3.8a it can be seen that

the overall I-V curve shape is somewhat similar to that obtained with non-degenerate diodes. There are several differences to be noted, however. There is a much larger first cross-over voltage as in the case of the $_5N_{25}$ diode. Also, the positive bias current initially has a rather small log slope which, for $V_a > 2.0$ V, increases rapidly with bias. Another observation is the existence of a second cross-over point. In the non-degenerate diodes for $|V_a| > 1$ V, it can be seen (cf. Fig. 3.4), that the positive bias current is generally larger than the negative bias current.

In giving a theoretical analysis of these I-V characteristics, the format of the previous section will be adopted. Thus, the various tunnel currents predicted for these diodes will first be presented and discussed, then a comparison with experiment made.

The theoretical log I-V curves for a $_5N_{25}$ diode are shown in Fig. 3.9 and for a P_{26} diode in Fig. 3.10. The physical parameters assumed for each set of calculations are given in Table 3.2. Dealing first with the I-V curves of the $_5N_{25}$ diode, it can be seen that the conduction band currents (i.e., J_{mc} and J_{cm}) dominate in this structure as they did in the non-degenerate silicon devices. But, with little band bending in the semiconductor, the saturation of J_{mc} for $0 > V_a > -1$ V seen in Fig. 3.6, is no longer in evidence.

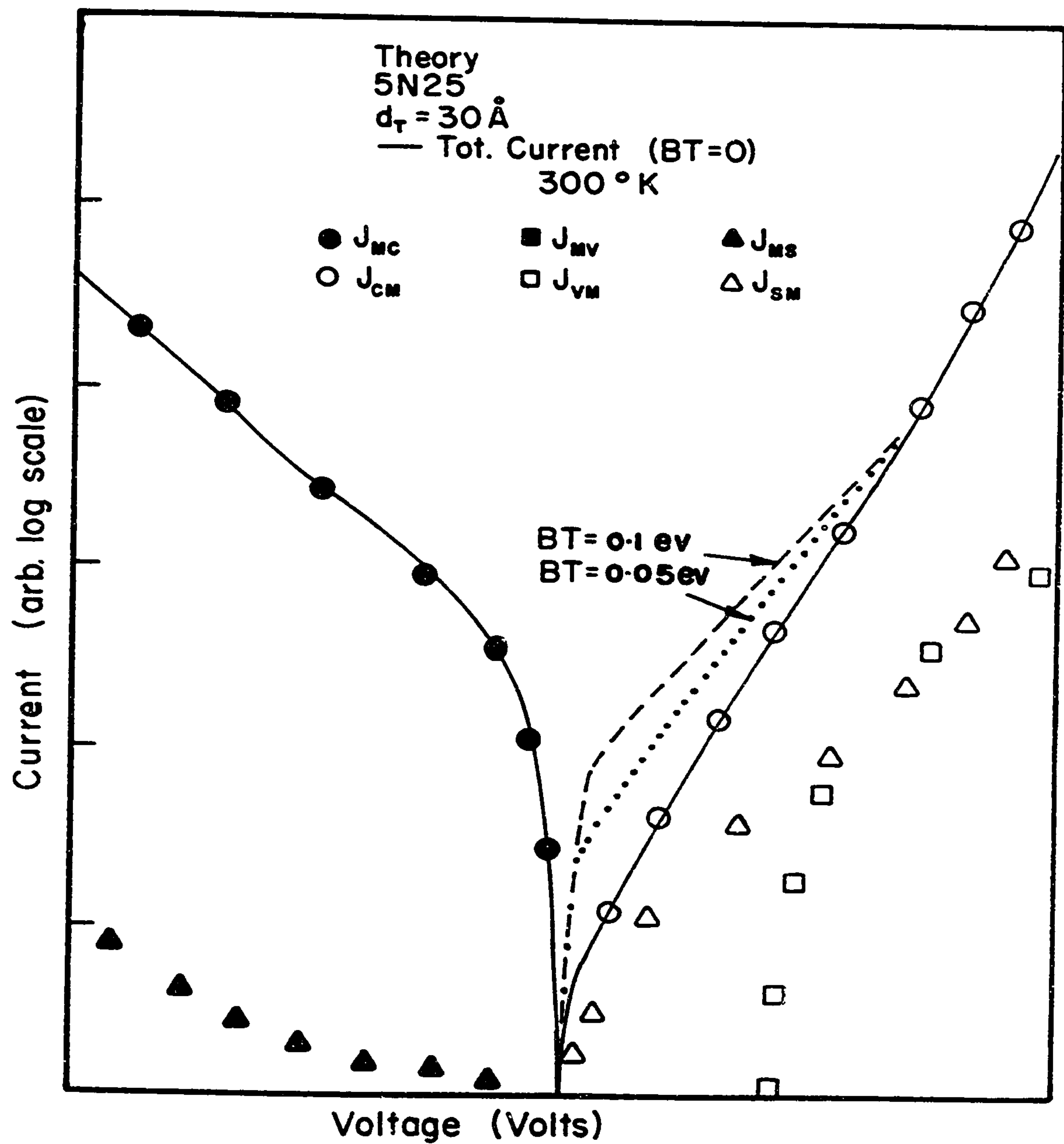


Fig. 3.9 Theoretical log I-V curves of $_5N_{25}$ diode with d_T = 30 Å. Total current at 300°K given by solid curve. Components of total current are as listed in the figure. Band tailing assumed was BT = 0 (solid curve), BT = 0.05 eV (dotted curve) and BT = 0.1 eV (dashed curve). Other parameters assumed are listed in Table 3.2. This theory is replotted in Fig. 3.7a (solid triangles)

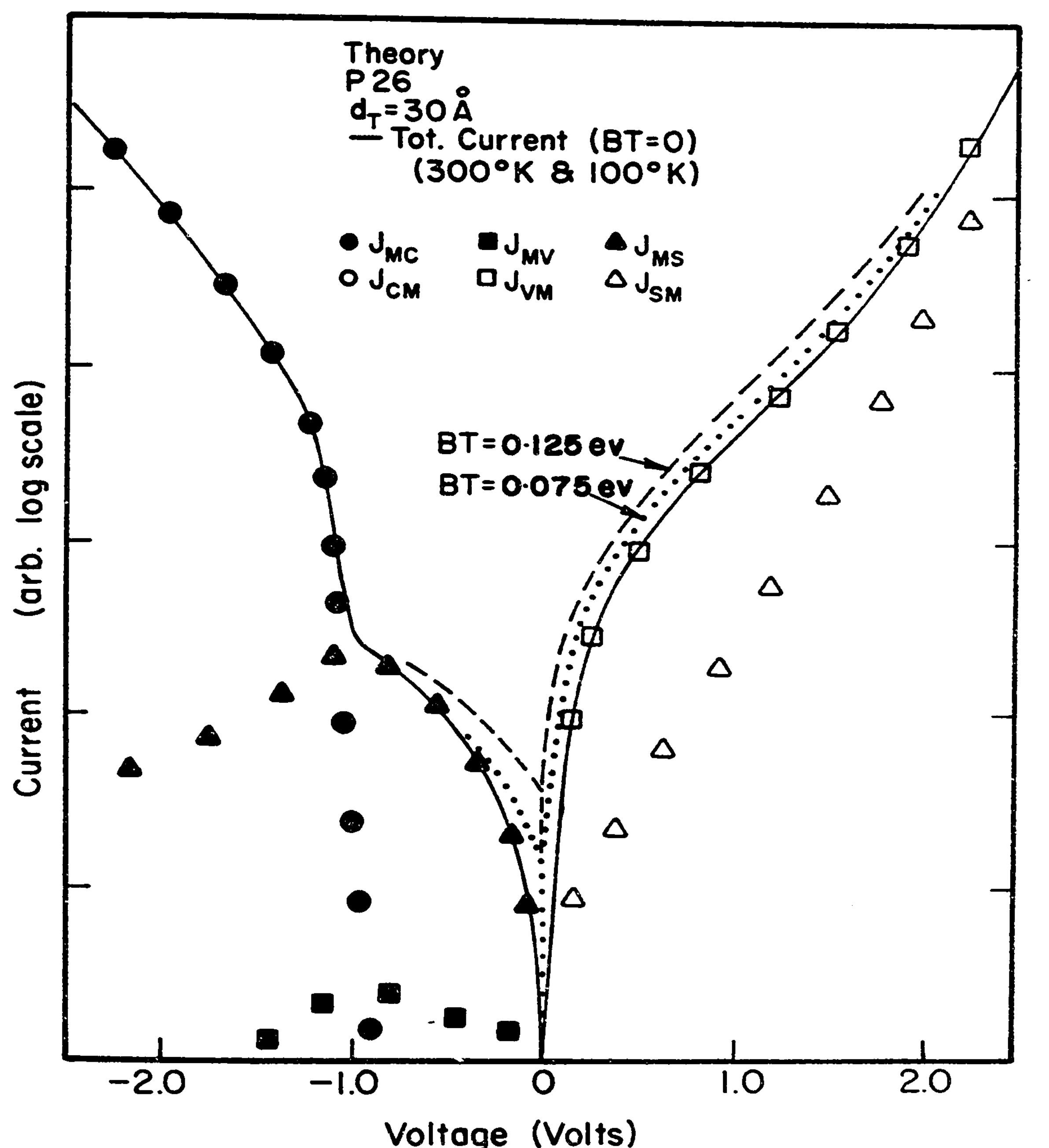


Fig. 3.10 Theoretical log I-V curves of P_{26} diode with d_T = 30 Å. Total current at 300°K given by solid curve. Components of total current are as listed in figure. Band tailing assumed was BT = 0 (solid curve), BT = 0.075 eV (dotted curve) and BT = 1.25 eV (dashed curve). Other parameters assumed are listed in Table 3.2. This theory is replotted in Fig. 3.8a (solid triangles)

Table 3.2

Parameters assumed for the theoretical calculations shown in Figs. 3.7a, 3.8a, 3.9 and 3.10

Semiconductor	N-Si	P-Si
Doping Density	$5\times10^{25}/m^3$	$10^{26}/m^3$
Temperature	300°K	300°K
Tunnel Probability	WKB	WFM
Image Force Potential	MIM	MIM
m^*_{cb}	1	1
m^*_{vb}	1	2.5
d_T	30 Å	30 Å
E_{gox}	8 eV	8 eV
X	3.2 eV	3.2 eV
ϕ_m	3.2 eV	3.2 eV
N_{ox}	0	0
Surface State Distribution (cf. Fig. 2.11)	SS3	SS3

Other differences predicted for the degenerate n-type diode are as follows. J_{mv} is greatly reduced (not visible on scale in Fig. 3.9). Surface state currents, J_{ms} and J_{sm}, are more asymmetric with bias, maximum contribution to the total current coming for small positive biases. Surface state charge effects are negligible for all but the largest surface state densities. Temperature effects on the I-V curve shape are small in all bias regions, with actual increases in current magnitude at 100°K predicted (although not shown in Fig. 3.9) for positive and small negative biases.

In Fig. 3.10 the I-V characteristics of the P_{26} diode can be seen to have a curve shape rather similar to that of the non-degenerate devices. This similarity extends to the shape only, as can be seen from a consideration of the individual tunnel components comprising the total tunnel current. Under positive bias, a valence band current, J_{vm}, is dominant, instead of J_{cm}, as in the other types of diode. For large negative biases, the current J_{mc} dominates. But, as predicted by Dahlke and Sze [9], the surface state current, J_{ms}, apparently dominates for $0 > V_a > -1$ V.

A feature of semiconductors, which becomes prominent as doping densities increase, is band edge tailing of the majority carrier band. This situation was discussed in Sec. 2.4.3 where it was concluded that for tunneling currents

no sharply defined band edge E_C^S or E_V^S was predicted by the theory [31]. We have chosen, therefore, to treat band tailing with still another adjustable parameter. A quantity BT is defined to be the difference, in electron-volts, between the original band edge and the band-tailed edge. Thus tunnel currents are calculated as if they had access to states BT eV below the original band edge. In Figs. 3.9 and 3.10, the solid curves were calculated with BT = 0, i.e., the majority carrier band was untailed. The dotted and dashed curves of Fig. 3.9 were calculated with BT = 0.05 eV and 0.1 eV respectively. For Fig. 3.10 the corresponding curves were calculated with BT = 0.075 and 0.125 eV respectively.

In both types of diode it can be seen that the positive bias currents are increased as BT increases. In the P_{26} diode (cf. Fig. 3.10) the negative bias surface state currents are also affected. Only comparison with experiment can provide any justification for the choice of a particular value of BT. In metal-semiconductor tunnel diodes (with $N_A = 10^{26}/m^3$), Mahon and Conley [47b] found from tunnel current conductance measurements that a valence band-edge tail of $\sim$0.1 eV existed in GaAs.

Let us turn now to a comparison of the theoretical I-V curves of Figs. 3.9 and 3.10 and the corresponding experimental data in Figs. 3.7a and 3.8a respectively. The theory in these two latter figures is given by the triangles.

For both the ${}_5N_{25}$ and P_{26} diodes the qualitative fit between theory and experiment at positive biases is seen generally to be good. But, as with non-degenerate diodes, discrepancies in the fit are apparent for large negative biases. For the P_{26} diode this problem is not as great, but this is partly due to the fact that the valence band mass was assumed to be $m^*_{vb} = 2.5$ rather than $m^*_{vb} = 1$. Thus a better fit is obtained only at the expense of consistency with the other three types of diodes considered. It should be noted that were a mass of $m^*_{vb} = 1$ to be assumed, the current J_- would have dropped below J_+ and no cross-over would have been obtained. With the current J_- thus low in all four cases the problem appears definitely to be associated with J_{mc}, the dominant tunnel component under large negative bias. Whether this problem is inherent in our calculation or due to a lack of consideration of some experimental situation is yet to be determined.

Within the limitations imposed by the above problem, it is still possible to deduce a range of possible masses, m^*_{vb}. The fit of theory and experiment for the P_{26} diode suggests $m^*_{vb} \lesssim 2.5$. A comparison of the experimentally observed absolute current magnitudes of the degenerate p and n-type diodes can also be used to predict the value of m^*_{vb} (employing diodes with similar d_0). Still another method is discussed in the next chapter. These latter two methods

both suggest $1 < m^*_{vb} < 2.5$. Considering the possible dependence of m^*_{vb} on d_0, it is difficult to determine m^*_{vb} to any greater accuracy at present.

From the comparison of theory and experiment in Figs. 3.7a and 3.8a, it is also possible to infer a value of BT. For both the P_{26} and $_5N_{25}$ diodes, the better fit was obtained with BT = 0. In other words, in the degenerate semiconductors employed in our MIS tunnel structures, either band tailing of the semiconductor band edges is not as severe as was the case in GaAs (BT = 0.1 eV) [47b], or these states do not provide a significant tunnel current.

The final point to be discussed concerning these degenerate MIS diodes is the effect of surface states. In the $_5N_{25}$ diode, despite the fact that (111)-oriented silicon was employed, both surface state charge and current contributions to the total tunnel current are apparently negligible. This is not the case in the P_{26} diode where the addition of surface state current to the total tunnel current is necessary to obtain the required I-V curve shape for $0 > V_a > -1$ V. While such surface state currents were felt by Dahlke and Sze to mask a negative resistance region, it is interesting to note in Fig. 3.10 that such a region would not necessarily have been observed. The two band model of the insulator results in a prediction of a more or less saturating region of total band tunnel current until

$V_a < -1$ V. The actual observation of negative resistance region by Esaki [7] in $A\ell$-$A\ell_2O_3$-SnTe diodes indicates two features of his diodes. The surface state tunnel currents are strangely absent and the insulator mass m^*_{vb} effectively $\rightarrow \infty$. This latter fact could be due either to the thickness of the insulator or to the position in energy of the SnTe energy gap in relation to the $A\ell_2O_3$ energy gap.

In summary then we have presented the I-V characteristics of both p and n degenerate silicon MIS diodes. The transport mechanism in the barrier of these diodes was confirmed to be tunneling, by means of the superconducting electrode test. Analysis of the currents in the various bias regions of the degenerate n-type diode indicated the dominance of J_{mc} and J_{cm}, as was the case in the non-degenerate MIS diode. In the degenerate p-type diode on the other hand, the valence band current, J_{vm}, was seen to dominate under positive bias, and a surface state current, J_{ms}, under small negative biases. For large negative biases the current J_{mc} was dominant.

Confirmation of the above analysis was obtained from the good qualitative fit of theory and experiment in most bias regions. Some discrepancies in this fit at large negative biases appeared to be common to all the diode I-V characteristics studied. Within the limitations imposed by the nature of these discrepancies, a value of barrier mass

$1 < m^*_{vb} < 2.5$ was indicated, definitely confirming the need for a two band model of the insulator.

CHAPTER 4

NON-EQUILIBRIUM EFFECTS ON MIS TUNNEL CURRENTS

4.1 Introduction

In this chapter we investigate the types of non-equilibrium conditions in the semiconductor, described in Chapter 1, and their effects on the I-V characteristics of MIS tunnel diodes. These non-equilibrium conditions are as follows: first, a tunnel-induced minority carrier deficiency at the semiconductor surface; second, a minority carrier excess in the semiconductor bulk; and third, a combination of the first two conditions occuring simultaneously. The first type of condition will be seen to be an intrinsic property of the diode and not due to any external influences. Hence, the term " 'non-equilibrium' diode" will be reserved for use only with such devices. The second and third non-equilibrium conditions represent the effects of excess minority carriers on "equilibrium" and "non-equilibrium" diodes respectively.

In silicon MIS diodes with thermally grown oxides, the insulator thicknesses for which minority carrier deficiencies are obtained, are shown later to be typically $\lesssim 30$ Å. The effect of this type of non-equilibrium

condition is generally detectable in the I-V characteristics of a tunnel diode only in cases where the semiconductor doping density $\lesssim 10^{19}/cm^3$. Typically, there is a current saturation in certain bias regions of non-degenerate diodes. This saturation occurs at biases where, in equilibrium devices, the current levels are increasing rapidly with bias.

Recognition of the possible existence of saturation phenomena in the current curves of MIS tunnel diodes, was first reported by Dahlke and Sze [9]. At that time though, they presented little experimental or theoretical verification of the transport mechanisms involved in such diodes. One of the first publications devoted to this type of diode was presented by Clarke and Shewchun [11]. Independently, similar findings were presented by Card and Rhoderick [48].

Similarities are immediately obvious between the saturating I-V characteristics of the 'non-equilibrium' MIS diode and the Schottky barrier diode [9,11,36]. However, several important differences have also been noted [11]. These differences were investigated and the results are discussed in subsequent sections.

In studying the properties of diodes with tunnel-induced minority carrier deficiencies, it is natural to consider the effects on these properties of minority carrier injection into the bulk semiconductor. These effects are discussed for non-degenerate n-silicon diodes ("equilibrium"

and "non-equilibrium") in the next section and for other types of MIS diode in Sec. 4.3. The influence of excess minority carriers on the admittance properties of thick oxide MIS diodes have been studied previously both theoretically and experimentally [29,49-50]. Such influences are well understood. Little work though has been published on the corresponding influences of minority carrier injection on the d.c. currents of the MIS tunnel diode [11].

Fabrication and testing of all diodes discussed in this chapter was similar to that for diodes presented earlier. No further comments need be made here on the subject. Similarly the theoretical approach will be that previously employed with the addition of several further assumptions. In treating the diodes exhibiting the effects of minority carrier deficiencies, the population of these carriers will be assumed to saturate at the same bias values as the corresponding currents. The effects of minority carrier injection will be assumed to alter this saturated population at the surface in addition to creating a constant quasi-fermi level separation in the bulk semiconductor [29,50].

With these assumptions, we will proceed in the next section with a discussion of non-equilibrium effects on non-degenerate n-silicon MIS tunnel diodes.

4.2 The Non-Degenerate N-Silicon MIS Diode

4.2.1 Effects of Minority Carrier Deficiencies

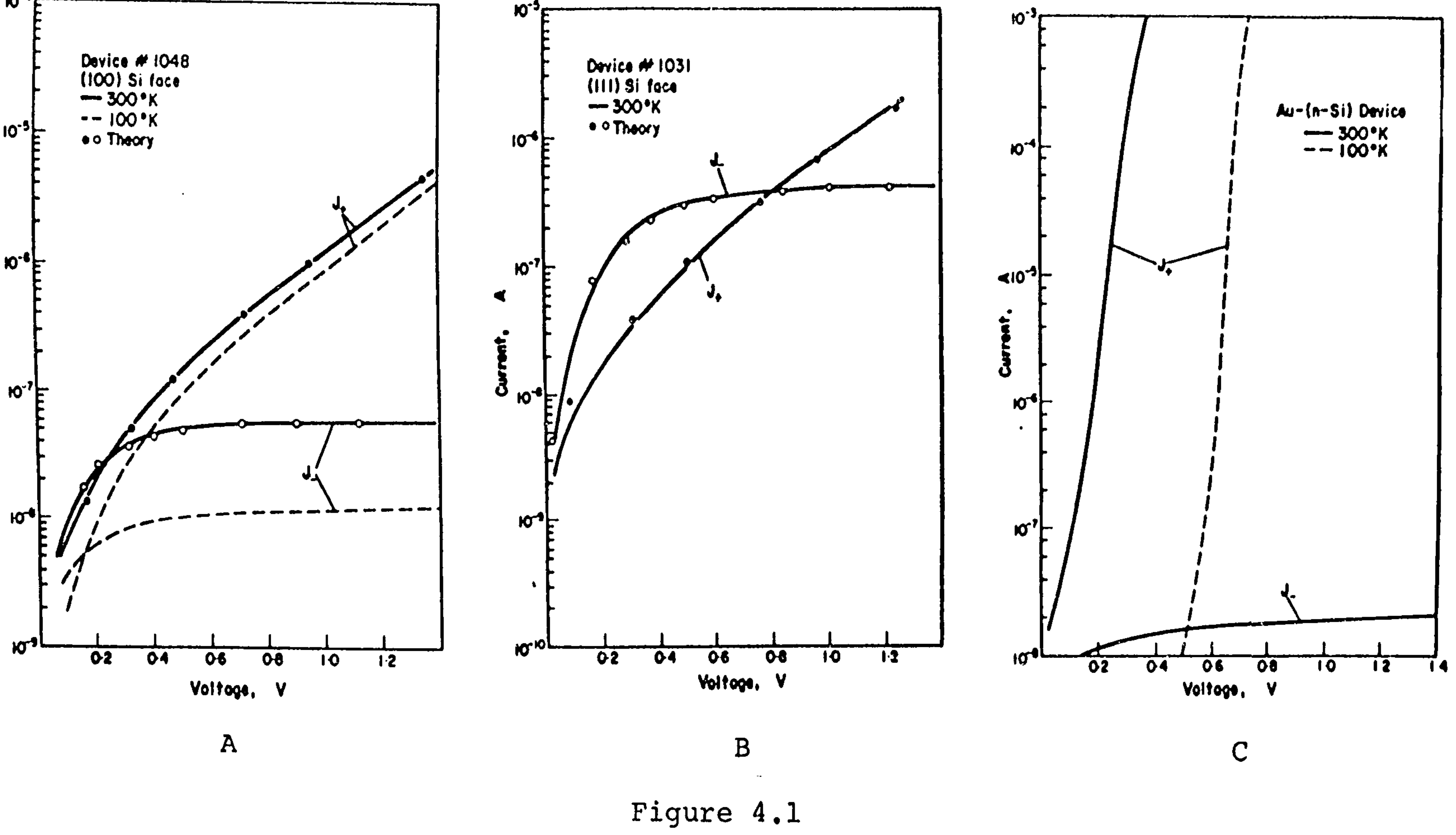
Typical I-V characteristics of lightly doped n-silicon diodes with oxide thickness less than 30 Å are presented in Fig. 4.1a, b. The (100)-oriented silicon diode has d_0 = 26 Å while for the (111)-oriented device, d_0 = 28 Å. It can be seen that in both cases a current saturation exists under negative bias. The saturation is similar in some respects to the saturation obtained with n-type Schottky barrier diodes as seen in Fig. 4.1c. This Au-(n-Si) diode was fabricated by the evaporation of gold directly onto a chemically cleaned silicon surface. Any oxide present at the Au-Si interface would be of thickness $d_0 \lesssim$ 15 Å (due to natural oxidation processes) with a tunnel thickness presumably of $d_T \sim 0$). Because of the similarities between the I-V curve shapes, the MIS currents will be designated "forward" (for metal dot positive - J_+) and "reverse" (for metal dot negative - J_-) in analogous fashion to that of the Schottky barrier diode currents.

Despite these similarities, it is evident from the temperature dependence exhibited by these currents that

Fig. 4.1a Log I-V characteristics of MIS tunnel diode (#1048, a $_4N_{20}$ diode) with d_0 = 26 Å and (100)-oriented silicon under "non-equilibrium" conditions. Solid (dashed) curves indicate data from diode at 300°K (100°K). Theory given by ● (+ve bias) and O (-ve bias) calculated with d_T = 13 Å

b Same as above with (#1031, a $_4N_{20}$ diode) with d_0 = 28 Å and (111)-oriented silicon

c Log I-V characteristics of Au-(n-Si) Schottky barrier diode at T = 300°K (solid curve) and 100°K (dashed curve)



A

B

C

Figure 4.1

entirely different mechanisms are responsible for the flow of these currents. Schottky barrier diodes have been extensively studied (cf Ref. 51). It is well known that current flows in such diodes are due to thermal ionization processes. In Fig. 4.1c this is reflected in the fact that at 100°K the forward current has decreased by over 5 orders of magnitude. The reverse saturation current, representing the direct collection of minority carriers from the bulk semiconductor, has become negligible at these low temperatures. In contrast to this, the currents of the MIS diode were relatively unchanged at 100°K (Fig. 4.1a), an attribute consistent with currents produced by tunneling mechanisms. In testing for tunneling in these diodes it is impractical to apply the more conclusive superconducting electrode test employed earlier on degenerate silicon devices. This is due to the freeze-out of majority carriers at the low temperatures employed in this test. Still, the consistency of the diode's I-V characteristics with theory (as will be shown), the temperature independence of the currents and the thickness of the insulator were taken to be convincing evidence that tunneling is the dominant mechanism of charge transfer across the barrier in these "non-equilibrium" diodes.

In the Schottky diode, as with a p-n junction, the reverse bias current is forced to saturate because of the limitations on minority carrier production in the bulk

semiconductor. It would seem likely that such limitations would be responsible for current saturation in MIS diodes as well. Evidence for this can be seen in the C-V curves shown in Fig. 4.2 for typical "non-equilibrium" diodes. Curve 1 in this figure is for the (100)-oriented silicon diode of Fig. 4.1a while curve 2 is for the (111)-oriented device of Fig. 4.1b. The negative bias region of curve 1 has been expanded and is shown in the inset. There, it is compared with two theoretical C-V curves. The dash-dot curve indicates the high frequency (HF) capacitance characteristics of an "equilibrium" diode with physical specifications similar to those of the experimental device. The dashed C-V curve was calculated assuming a deep depletion model in which the density of minority carriers at the surface is assumed to be $p_{nsc} \ll p_{ns}$, the equilibrium surface density. Good agreement between the depletion C-V curve and experiment indicates that the minority carriers are not in thermal equilibrium (at least between the valence and conduction bands) at the semiconductor surface.

More direct experimental evidence of deep depletion effects on the tunneling currents themselves can be obtained by studying the effect of oxide thickness variations on the "non-equilibrium" diode characteristics. Shown in Fig. 4.3 are the log I-V characteristics of two diodes with oxide thicknesses varying by only several angstroms. With

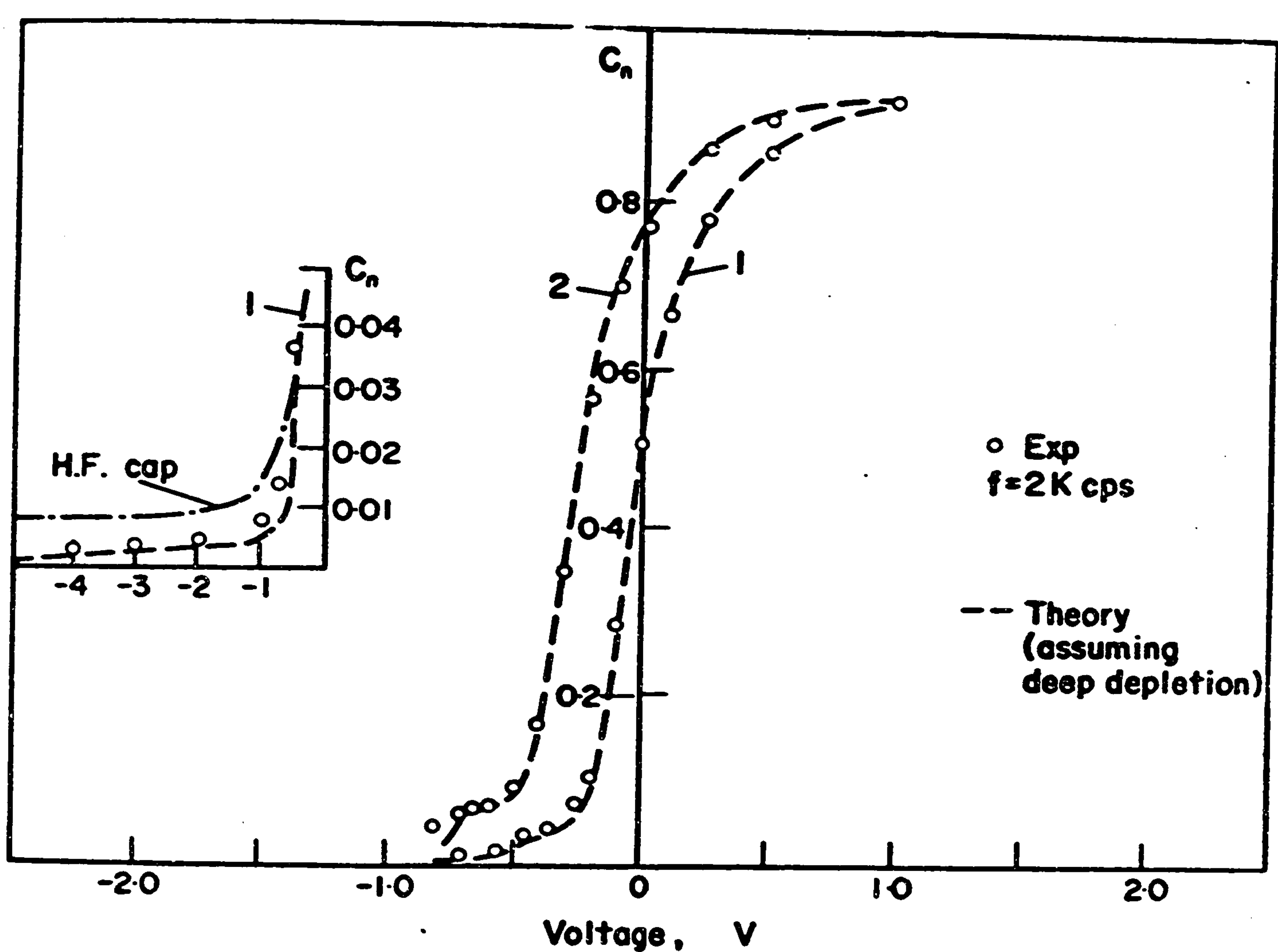


Fig. 4.2 C-V data of device #1048 (curve 1) and #1031 (curve 2). Both diodes are $_4N_{20}$ devices. Normalized experimental (theoretical) data given by circles (dashed curves). Theory calculated with depletion model assuming parameters listed in Table 4.1

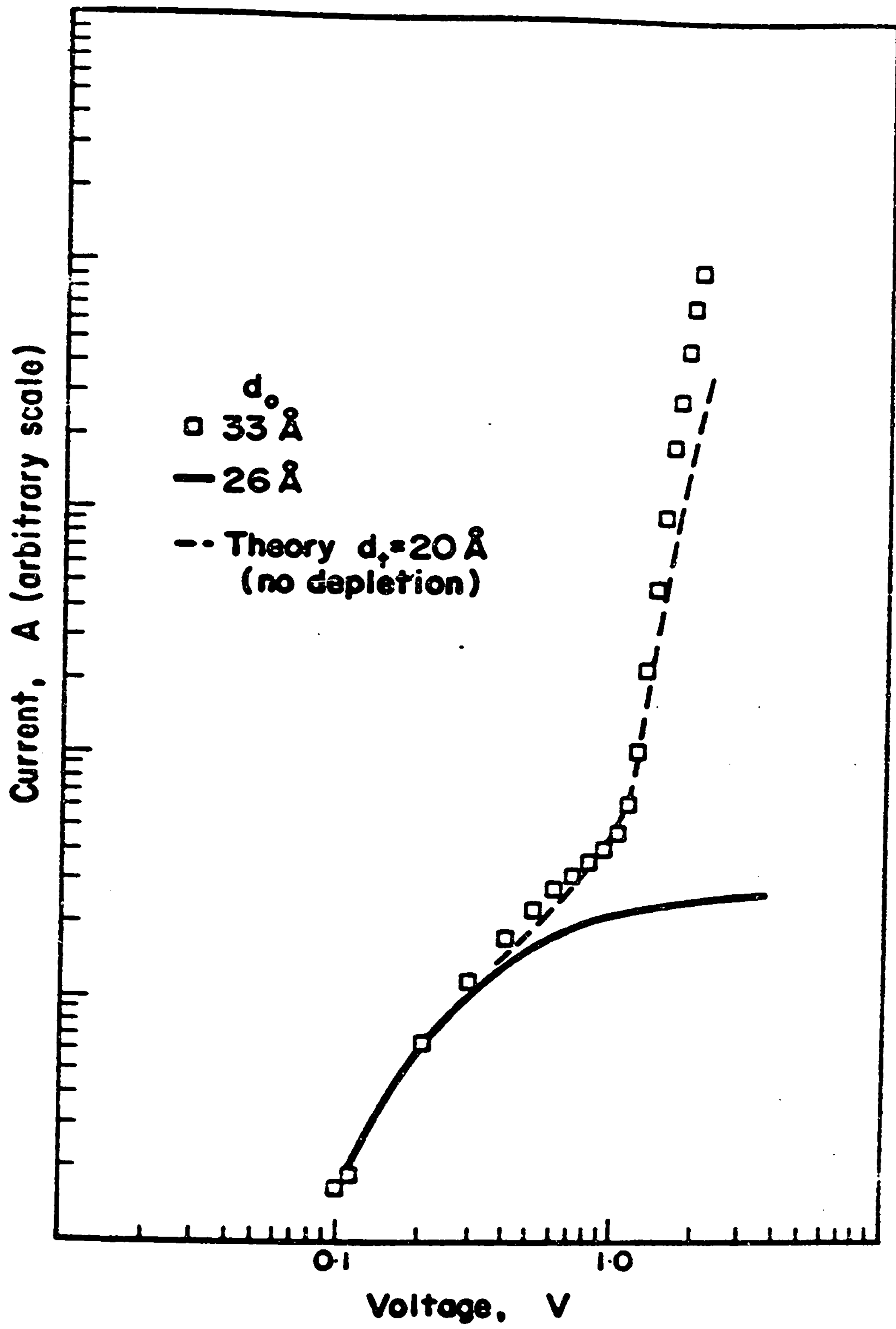


Fig. 4.3 Log of observed reverse current magnitude is plotted against log of voltage for two $_4N_{20}$ devices of different d_0 (current-voltage curves have been arbitrarily superimposed on the same current scale). Dashed curves show typical theoretical reverse characteristic of "equilibrium" tunnel diode (d_T = 20 Å)

$d_0 = 33\ \text{Å}$ the saturating current has been eliminated and is replaced by the usual "equilibrium" current. This characteristic is compared with the theoretical "equilibrium" I-V curve of an N_{21} diode with tunnel oxide thickness $d_T = 20\ \text{Å}$ (a WKB approximation and one band model of the insulator were assumed). In order to compare the I-V curve shapes, the currents have all been superimposed on an arbitrary current scale.

It would appear from Fig. 4.3 that there is a critical value of insulator thickness beyond which the semiconductor of the diode can be maintained essentially in equilibrium. In practice this critical value of thickness is actually a function of processing and might better be described as a critical "region" of thickness. In this critical region, which can extend from as low as 30 Å to as high as 40 Å, complicated time and voltage dependent effects on the reverse biased currents can be observed. Such effects reflect the attempt of the diode, after each increase in reverse bias, to reach an equilibrium or quasi-equilibrium condition. For instance, moderately fast sweep speeds can result in a current saturation beyond a particular voltage, say -2.0 V. If the bias is then fixed at -2.5 V the current will gradually increase in time, in some cases returning to its "equilibrium" value.

The C-V results of the diode tested under these conditions show corresponding effects. For rapid increases in negative bias beyond -2.0 V, a deep depletion C-V behaviour can be noted. Upon return of the diode to equilibrium, the capacitance again returns to its normal high frequency values. In thick oxide MIS diodes, without the complications of minority carrier loss through tunneling, such transient response C-V characteristics have been found useful in determining minority carrier lifetimes in the bulk semiconductor [52].

At room temperature the time constants for charging effects in the MIS tunnel diode were typically of the order of 10's of seconds. These times were found to increase considerably at low temperatures. This made it quite difficult to measure reliably the reverse-biased equilibrium I-V characteristic of such diodes at 100°K. On the other hand, charging time constants decreased noticeably under the effects of diode illumination. This is obviously due to the resulting increase in minority carrier supply rate to the surface. The effects of such increases are investigated in more detail in the next sub-section.

4.2.2 Effects of Variations in Minority Carrier Supply Rate

Two methods were investigated as a means of enhancing the minority carrier populations in the bulk semiconductor. The first method was simply to illuminate the semiconductor with light of energy $E_\nu > E_g$. A second, and more interesting method from a device point of view, is the use of the minority carrier injecting properties of MIS tunnel diodes themselves. By placing a ring shaped metal electrode concentrically around the original circular contact and forward biasing this ring, significant amounts of minority carriers can be made available to the semiconductor.

The effects of these externally induced minority carrier population increases on the reverse saturation current of a "non-equilibrium" diode (the one discussed in the previous chapter) are shown in Fig. 4.4a. Both methods of minority carrier injection can be seen to result in increased minority carrier saturation current but in qualitatively different fashions (cf. Fig. 4.4a curves 2 and 3). These differences in I-V curve shape are probably due to the different spatial distributions of excess minority carriers created in the bulk semiconductor by the two different methods. In the first method, light creates the more even distribution of excess carriers and results in a saturation current of slightly increased (curve 2), but still

Fig. 4.4a Reverse I-V curves (J_-) of diode #1048 ($_4N_{20}$) with

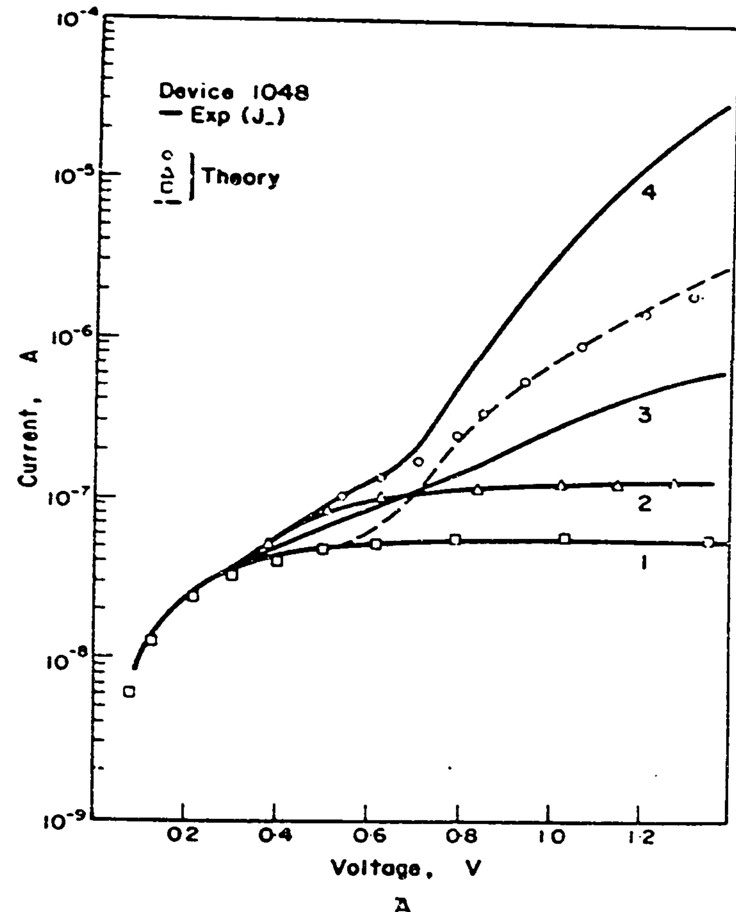
(1) no illumination (Theory (□) calculated with $p_{nsc} = 10^{11}/m^3$)

(2) illumination with light of $\lambda = 1.03\ \mu$ (Theory (Δ) calculated with $p_{nsc} = 2\times10^{18}/m^3$ and $\phi_p - E_v = 0.4$ eV)

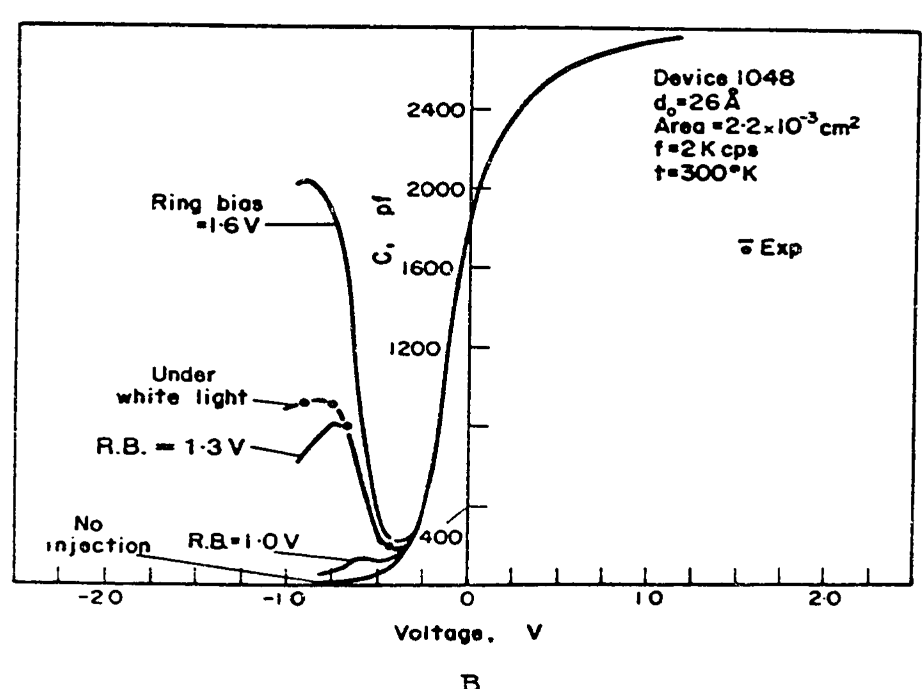
(3) injection from ring biased at 1.3 V

(4) illumination by high intensity white light (Theory (O) calculated with $\phi_p - E_v = 0.4$ eV but no critical hole density)

b C-V curves for diode #1048 ($_4N_{20}$) with injection by illumination (dotted line) and ring bias



A



B

Figure 4.4

voltage independent, current magnitude. In the second method, minority carriers from the ring electrode must diffuse across the intervening space to the first contact. Such carriers are, therefore, more susceptible to field assistance from the depletion fields of the collector. As a result, saturation is not complete (curve 3).

For an entirely different reason the collector current under high level injection by light or ring can also be seen not to saturate (curve 4). By comparison, similar levels of illumination on the Schottky diode resulted in a saturating current of $\lesssim 10^{-6}$ amps. The figure of 10^{-6} amps ($\sim 5 \times 10^{-4}$ A/cm^2) for a Schottky barrier device represents the maximum light induced minority carrier flow under these levels of illumination. From Fig. 4.4a (curve 4) the reverse current of the MIS diode can be seen to exceed this value by over an order of magnitude without saturating. The magnitude of the hole current (J_{mv}) would be insufficient, therefore, to explain this behaviour. It is obvious that the dominant current flow in the reverse biased Schottky barrier diode is not identical to that of the MIS diode. This, therefore, represents another important difference between the Schottky barrier and MIS diodes.

From Fig. 4.4b it can be seen that both methods of hole injection also produced significant effects on the C-V characteristics of the "non-equilibrium" diode. The reverse

bias capacitance curve of this diode was seen in Fig. 4.2 (curve 1) to exhibit a deep depletion behaviour. Upon hole injection, whether from the forward biased ring or from the effects of light, a relatively high frequency inversion capacitance response is obtained. In addition the capacitance 'well' at $V_a \sim -0.5$ V is narrower and the capacitance minimum greater than that obtained for an equilibrium diode. Such characteristics have been noted in the C-V data of thick oxide MIS diodes under conditions of illumination [49] and are known to be due to the creation of excess minority carriers in the semiconductor.

Periodically, while studying the effects of illumination on "non-equilibrium" (111)-oriented silicon devices, an interesting negative resistance feature was obtained in the I-V characteristics. While such behaviour was by no means typical, its interesting nature has led us to present an example here, in Fig. 4.5, for consideration. The usual saturating reverse bias characteristic is obtained with no illumination of the diode. In comparison with either of the I-V curves in Fig. 4.1a or b it can be seen that the first cross-over voltage is considerably larger. As mentioned in Chapter 2 such large cross-over points were typical of large surface state or oxide charge densities. Under illumination the reverse characteristic of this diode increases until at $V_a \sim 2.0$ V a sharp peak occurs with a

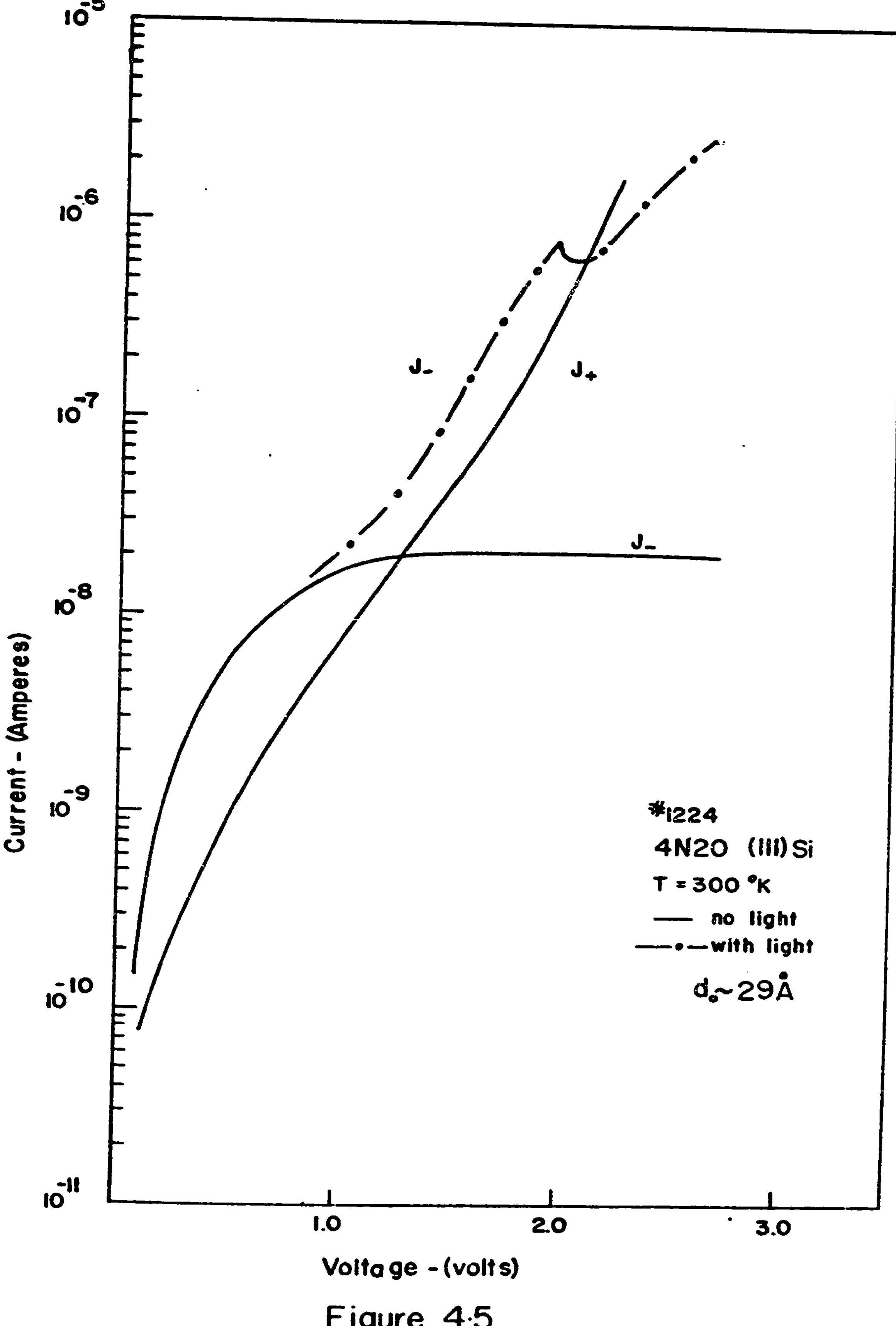


Figure 4.5

Fig. 4.5 Log I-V characteristics of an atypical $_4N_{20}$ device without (solid curve) and with (dash-dot curve) illumination. Device fabricated with (111) Si and $d_0 \sim 29$ Å

negative resistance region following. This characteristic was quite repeatable and stable from voltage sweep to sweep and, therefore, probably not produced by any oxide breakdown or forming effects. Several explanations are possible, and these will be discussed in the next sub-section.

In considering the influence of minority carrier injection on the current-voltage curves of the MIS diode it is informative to study the effects of light on the "equilibrium" diode as well as on the "non-equilibrium" diode. An example, employing light as the means of injection, is shown in Fig. 4.6. As in the "non-equilibrium" diodes the effects of light are limited to the bias region with $V_a < -1$ V. Under high level illumination of the non-equilibrium diode it can be seen, by comparing the results of Figs. 4.4a and 4.6, that similar I-V characteristics are obtained. This would suggest both currents are dominated by the same current component. In Chapter 3 it was found that in the equilibrium diode this current was J_{mc}. The dominance of this current in reverse biased "non-equilibrium" diodes would explain many of the observed features of these devices. For confirmation of this fact we must turn to a theoretical analysis of the problem. Such an analysis is presented in the next section.

Fig. 4.6 Log I-V characteristics of "equilibrium" $_4N_{20}$ diode showing effects of illumination on J_-, both experimentally (dash-dot curve) and theoretically (open triangles). Solid curves (solid triangles) represent experimental (theoretical) data for unilluminated diode. For this device d_0 = 41 Å. Parameters for theory listed in Table 3.1

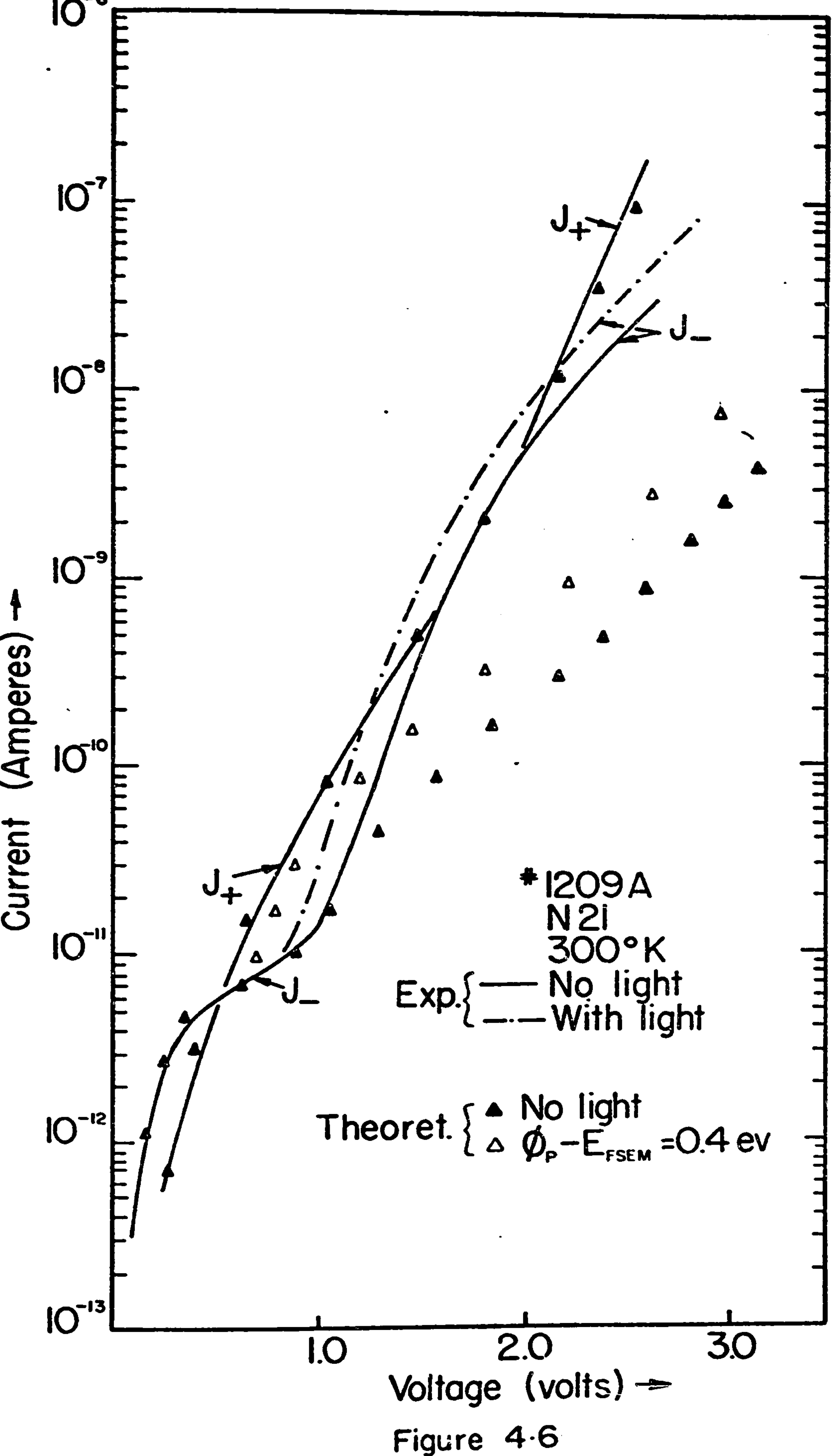


Figure 4·6

4.2.3 Discussion of Results and Comparison with Theory

In Chapter 3 it can be observed that a characteristic of barrier dominated current flows in MIS diodes is a roughly exponential increase in current magnitude with voltage except in certain limited bias regions. For non-degenerate semiconductor devices the effects of the semiconductor depletion region on the I-V characteristics of the diode were seen to result in a current saturation for the biases $0 > V_a > -1$ V. The observation of current saturation for $V_a < -1.0$ V, therefore, suggests that the effects of the semiconductor depletion layer are being felt over a much wider range of biases. In other words the MIS tunnel diode I-V characteristics have become semiconductor dominated in the negative bias region as opposed to being barrier dominated.

To simulate this type of deep depletion behaviour in both the tunneling and capacitance results, it is necessary to prevent the build-up of an inversion layer at the semiconductor surface. It is this inversion layer which screens the semiconductor depletion layer and gives rise to the usual exponential increase in current with bias for large negative biases. Such a build-up can be prevented in a theoretical approach simply by assuming that the minority carrier charge density, p_{ns}, never reaches a value $>p_{nsc}$,

a preset critical density. The justification for such an assumption comes quite readily from a consideration of the effects of a large hole tunnel current. With increasing negative bias, the hole tunnel current (J_{mv}) will also increase to a point at which any additional holes arriving at the surface will tunnel away as fast as they arrive and no further build-up will be possible. At this point the minority carrier tunnel flow will exactly equal the minority carrier supply rate to the surface. This supply rate is characteristic of the bulk material, and in the absence of external stimuli and large recombination-generation currents, is a fixed quantity for any given temperature. Further increases in bias will have no effect on this current magnitude. Since other tunnel currents, such as J_{mc}, would alter if further changes in the oxide voltage occured, all bias increases must appear across the semiconductor after saturation is reached. It is the decreasing depletion layer capacitance which causes the deep depletion capacitance behaviour seen in Fig. 4.2.

Theoretical log I-V curves are shown in Fig. 4.1a and b, calculated assuming a value of $p_{nsc} = 10^{11}/m^3$. This value was chosen to insure that $p_{nsc} << N_D$ where N_D is the semiconductor doping density ($= 5 \times 10^{20}/m^3$). A WKB approximation and a one band model of the insulator were employed in these calculations. Image forces were of the MIM type. The surface state and oxide charge densities

employed to obtain a fit between theory and experiment are listed in Table 4.1. Corresponding calculations were made of the C-V characteristics with the appropriate parameters also listed in Table 4.1.

In all cases excellent agreement of theory and experiment is obtained. By maintaining the theoretical hole density $p_{ns} \leq p_{nsc}$, the current is made to saturate completely for $V_a \lesssim -1.9$ V in correspondence with the observed I-V characteristics. In actual practice small variations in p_{nsc} might occur due to recombination-generation processes in the space charge region. Such processes are voltage dependent and might, therefore, be expected to affect the saturation current. To a good approximation such variations can be ignored. This is due to the insensitivity theoretically of the saturating current magnitude to small changes in the value of p_{nsc} (as long as $p_{nsc} << N_D$).

From the voltage distribution employed in the calculation of this theory, it is possible to determine the relative position at various voltages of the metal Fermi level with respect to the semiconductor band edges. The energy band picture for the "non-equilibrium" diode is shown in Fig. 4.7. The band bending in these figures has been drawn roughly to scale in terms of an insulator thickness, d_T = 13 Å. On this distance scale, bands appear flat in all but the positive bias (accumulation) case. To

$\phi_m = 3.2$ (eV) $\chi = 3.2$	I–V		C–V	
	Q_{ox} /cm^2	S.S. dist.	Q_{ox} /cm^2	S.S. dist.
1031 (111) Si	5.6×10^{12}	Tot.= 2.5×10^{12}/cm^2; # per cm^2 /eV$\times 10^{13}$ (axis 1, 2, 3; E_v to E_c; +, −)	1.4×10^{12}	Tot.= 1.4×10^{11} /cm^2; # per cm^2 /eV$\times 10^{13}$ (axis 0.5, 1.0; E_v to E_c; +, −)
1048 (100) Si	1.0×10^{12}	Tot.= 7.5×10^{11}/cm; # per cm^2 /eV$\times 10^{13}$ (axis 0.5, 1.0; E_v to E_c; +, −)	-2.0×10^{11}	Tot.= 1.1×10^{11} /cm^2; # per cm^2 /eV$\times 10^{13}$ (axis 0.5, 1.0; E_v to E_c; +, −)

Table 4.1

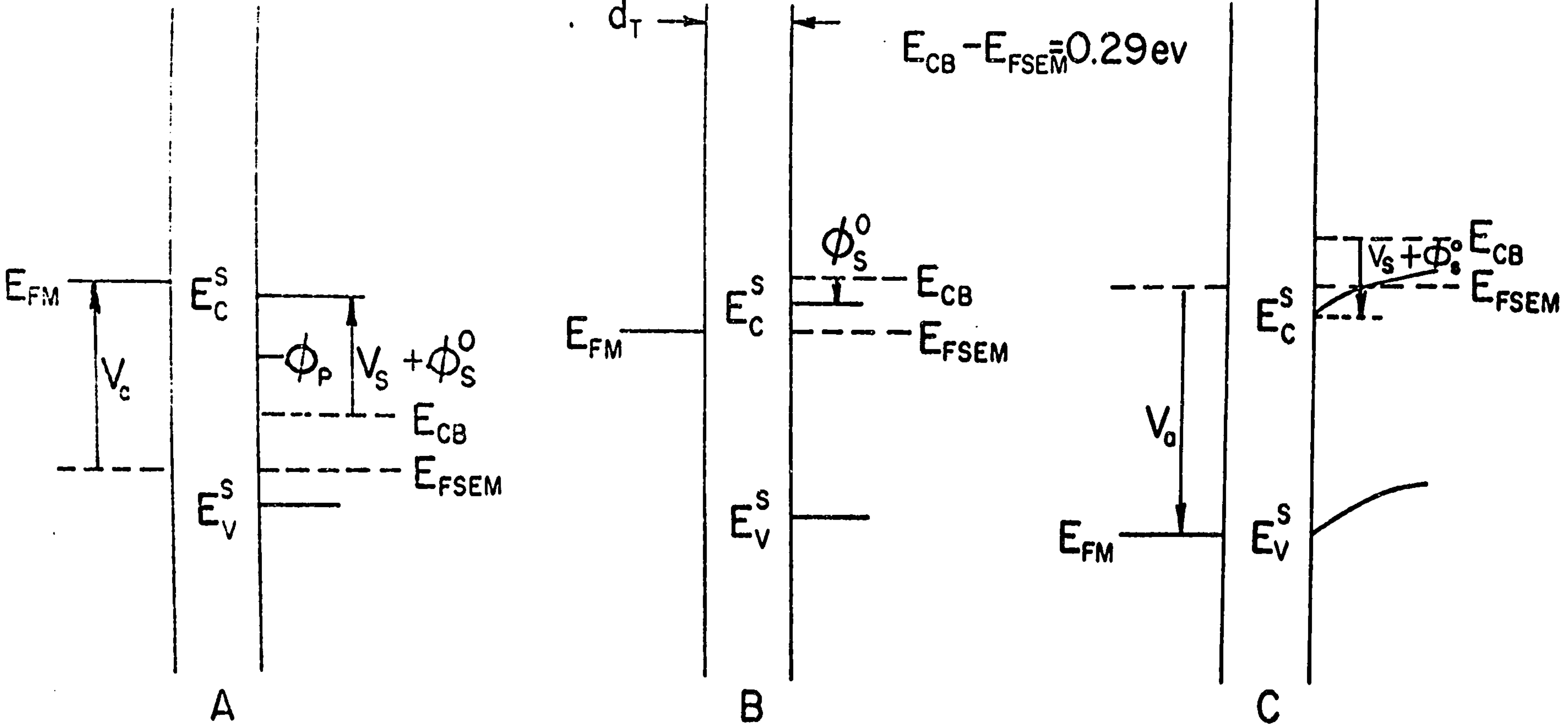


Fig. 4.7 Energy band diagram of "non-equilibrium" MIS diode under differing bias conditions with (a) $V_a = -1.0$ V; (b) $V_a = 0$; (c) $V_a = 1.3$ V

indicate the amount of band bending, therefore, the bulk conduction, valence and Fermi energies are given by dashed lines. The energies of the band edges at the surface are given by E_c^S and E_v^S. The total surface potential is defined as $V_S + \phi_S^0$, the sum of the applied voltage in the semiconductor and initial band bending due to work function differences and insulator charge.

Under positive and zero bias (Figs. 4.6c and d), the carriers in the diode are in thermal equilibrium and negligible quasi-fermi level separation occurs (i.e. $\phi_p = \phi_n = E_{FSEM}$). Under negative bias (Fig. 4.7a), the valence band energy E_v^S is seen to be approaching the bulk Fermi energy. In equilibrium, a large minority carrier charge density would be present at this bias. The assumption that such a build-up is prohibited by the loss of charge through tunneling forces a large quasi-fermi level separation at the surface.

As a result of this separation the metal Fermi level becomes pinned with respect to the semiconductor conduction band energy. It is the position of this metal Fermi level that is of importance in determining the relative magnitudes of the various components of the saturating current. From Fig. 4.6a it can be seen that E_{FM} has become pinned at an energy above the conduction band edge at the semiconductor surface. It is this fact which explains the dominance of

J_{mc} in the saturating current. While this dominance in diodes such as #1048 (Fig. 4.1a) may be slight (e.g. compare the saturation current magnitudes in Figs. 4.1a and 4.1c), it is nevertheless important. It is because of this dominance that illumination can eliminate current saturation.

The position of the pinned metal Fermi level is also influenced by such factors as the initial band bending ϕ_S^0 in the semiconductor. Such band bending is due to a combination of work function differences and surface state and oxide charge. The differences in saturation current magnitude in Figs. 4.1a and b are essentially due to the latter cause. Surface state densities are known to be strongly dependent on silicon orientation [53]. Also, oxide charge densities are suspected to be related to the surface state charge density [54]. The net result is an increased value of ϕ_S^0 for the (111)-oriented n-silicon surface over that found with the (100)-oriented silicon surface. The metal Fermi level becomes pinned opposite energies that are higher in the semiconductor conduction band for larger ϕ_S^0. A larger current flow J_{mc} results.

In addition to being sensitive to initial band bending ϕ_S^0, the reverse saturation current was seen in Fig. 4.4 to be sensitive to the presence of excess minority carriers in the bulk semiconductor. Such behaviour is also consistent with our deep depletion model of tunneling in

this type of "non-equilibrium" diode. If a steady state condition of excess minority carriers can be established, the minority carrier supply rate to a sink at the surface will be significantly increased. The hole current flow J_{mv} equated with this supply rate will also increase. However, this in itself would be insufficient to explain curve 4 of Fig. 4.4a as has already been mentioned.

More important in determining the reverse biased tunnel current magnitude is the corresponding increase in p_{nsc} that can be assumed. The assumption of $p_{nsc} = 2 \times 10^{18}/m^3$ and $\phi_p - E_v^S = 0.4$ eV at the surface results in an increased but still saturating current in good agreement with experiment as seen in Fig. 4.4a, curve 2. The critical density, p_{nsc}, is still low and for this reason J_{mc} still saturates. As expected, the saturation effect can be eliminated entirely for sufficiently large values of p_{nsc}. The theoretical curves representing the upper limit with $p_{nsc} \to \infty$ are given in Fig. 4.4a by circles (or the dashed line which was calculated for an identical device without the peak of surface states near the valence band edge). The discrepancies seen in Fig. 4.4a between the non-saturating reverse bias current curve (curve 4) and theory (circles) are similar to that seen in Chapter 3 for equilibrium diodes. It is presumably due to similar origins in both "equilibrium" and "non-equilibrium" diodes.

The rather unique behaviour shown in Fig. 4.5 for an illuminated "non-equilibrium" diode has several possible explanations. For instance, traps could be filling or emptying at the particular bias where the negative resistance feature is observed. The voltage distribution might change sufficiently to result in a negative resistance. This explanation appears unlikely due to the lack of any appreciable hysteresis in the I-V curve which such a mechanism is likely to cause.

An interesting possible explanation is the effect of image forces on the surface state tunnel currents (cf. Fig. 2.10a). Certainly the large cross-over voltage seen in Fig. 4.5 suggests very large surface state or oxide charge densities. The large slope of the I-V characteristic for $0 > V_a > -1$ V suggest the former. It is, therefore, quite possible that surface state tunnel currents are of the same order, if not greater, than the band-to-band currents in the diode at these biases. Any abrupt structure in the I-V characteristics of these devices might be explained by the image force effects seen in Fig. 2.7 (curve c). This connection is too tenuous as yet to reach definite conclusions but does suggest a method of proceeding in the investigation of image force effects in MIS tunnel diodes.

The effects of light on "equilibrium" diodes helps to confirm the model of the "non-equilibrium" diode. This

can be seen by comparing the results shown in Fig. 4.6 and Fig. 4.4. In both cases the influence of light affects only the currents in the bias region $V_a < -1$ V. The similarity between the negative bias I-V curves of both types of device when under illumination is marked. Theoretical calculations are also shown in Fig. 4.6 made with $E_{FSEM} - \phi_p = 0.1$ eV (dots) and $E_{FSEM} - \phi_p = 0.2$ eV (circles). Although the relative shape of the theoretical reverse current does not fit experiment exactly, the effects of theoretical quasi-fermi level shifts in the bulk semiconductor can be seen to predict changes in this reverse current which do agree qualitatively with experiment.

Briefly summarizing, the influence of non-equilibrium conditions in the semiconductor of n-silicon MIS diodes on the I-V characteristics of these diodes have been considered. For non-degenerate silicon devices a negative bias current saturation was observed if the device insulator thickness was $\lesssim 30$ Å. Such saturation was found to be due to minority carrier deficiencies at the semiconductor surface. Similarities in curve shape were noted between MIS "non-equilibrium" diode and Schottky diode I-V characteristics. Nevertheless, analysis of the currents and their transport mechanisms across the barrier region of both devices indicated several major differences existed. It was concluded that the dominant current in the "non-equilibrium" n-type

MIS tunnel diode (under negative bias) was J_{mc}. The influence of thickness and illumination of the diode on the observed current saturation was consistent with a deep depletion model of tunneling. In this model it is proposed that a majority (normally non-saturating) carrier flow is forced to saturate due to two influences, first the depletion of the inversion layer of the MIS tunnel diode by tunnel currents and second the inability of the bulk semiconductor to supply minority carriers at a rate sufficient to maintain this inversion layer. The similarities of current-voltage curve shape between illuminated "equilibrium" and "non-equilibrium" diodes tends to confirm this analysis of the current components.

In the next section, discussion of non-equilibrium effects will be extended to diodes fabricated with both p and n type semiconductors of a variety of doping densities.

4.3 Other Types of MIS Diode

4.3.1 The Non-Degenerate P-Silicon Diode

The current-voltage characteristics of a 1Ω-cm p-silicon diode with $d_0 = 30$ Å are shown in Fig. 4.8. The saturating current in this type of "non-equilibrium" diode can be seen to be J_+ as opposed to J_- for the n-silicon diodes. In addition to the difference in voltage polarity, several other features can be noted that differentiate the saturation currents of p and n-type devices. The magnitude of the saturation current in the former case is typically 10^{-10} amps (for a 15 mil diameter contact) while from Fig. 4.1 the magnitude of J_- is seen to be several orders greater than this. It can also be seen, by comparison of the saturation current magnitudes at 100°K and 300°K, that the temperature dependence of these currents differs. In Fig. 4.8a J_+ at 100°K is not shown but is $<10^{-12}$ amps, a drop of over two orders of magnitude, whereas in Fig. 4.1a J_- was seen to drop by less than an order of magnitude between room temperature and 100°K.

The C-V results for the p-silicon diode are shown in Fig. 4.8b. Confirmation of a deep depletion state at the surface is obtained from the C-V curve for voltages $V_a > 0.5$ V. A plot of $1/C^2$ vs. V in this region gives a

Fig. 4.8a Log I-V characteristics of "non-equilibrium" P_{22} diode (#1229) with no light at 300°K (solid curve) and at 100°K (dashed curve) as well as with illumination at 300°K (dashed-dot curve). Oxide thickness is d_0 = 30 Å.

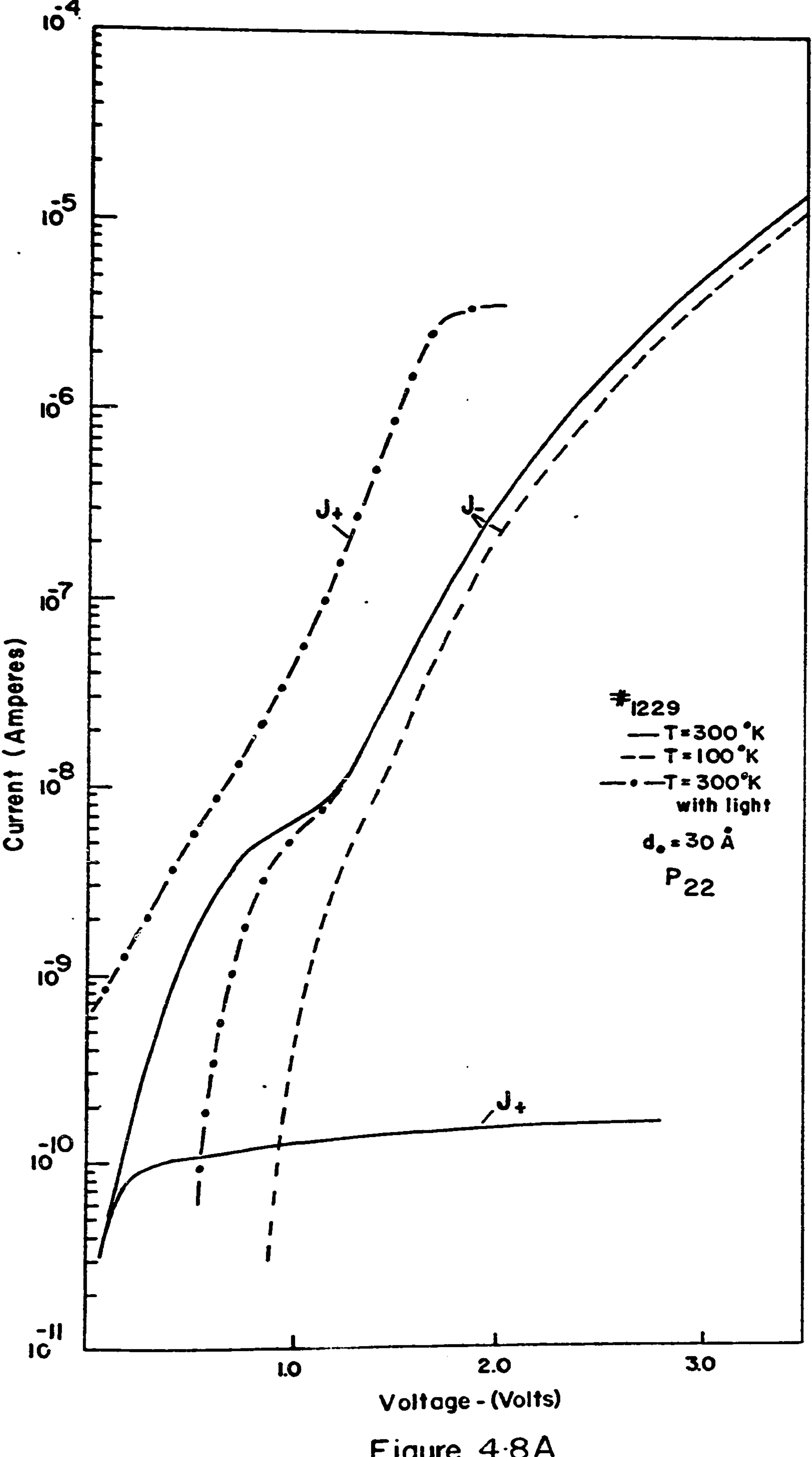


Figure 4·8A

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Fig. 4.8b C-V curves of "non-equilibrium" P_{22} diode (#1229) at 300°K (solid curve). Oxide thickness is d $d_0 = 30$ Å and measurement frequency f = 2 KHz. Also shown is theoretical ideal P_{22} C-V data (dashed curve) assuming no surface states or oxide charge. Inset on left shows plot of $1/C^2$ vs V

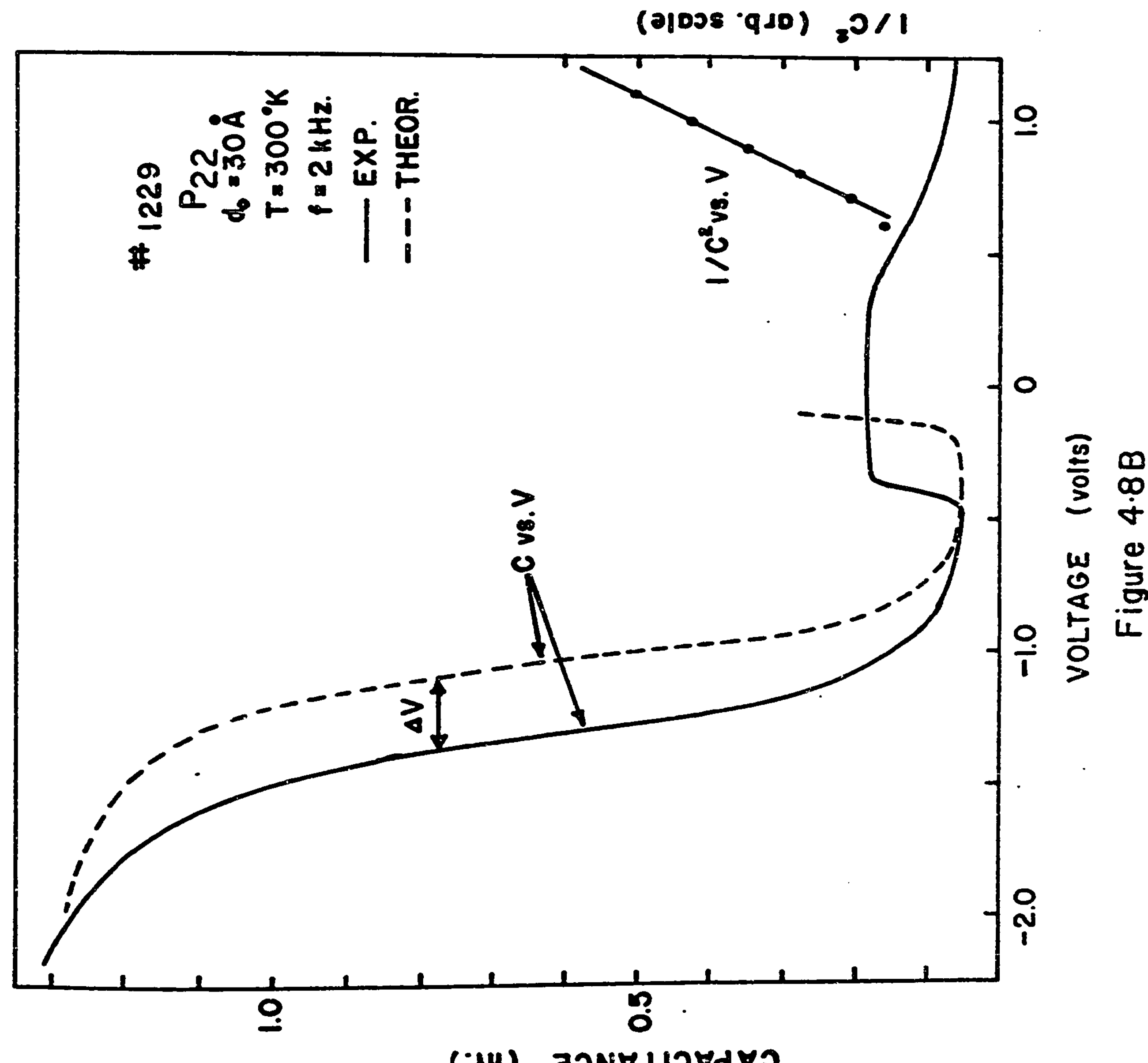


Figure 4·8B

straight line as can be seen also in Fig. 4.8b. This linear dependence of $1/C^2$ on voltage is typical of deep depletion capacitance behaviour. The C-V results for an ideal P_{22} diode with $d_0 = 31$ Å are also given in Fig. 4.8b. By comparison of experimental and theoretical curves it can be seen that the former curve has been shifted to more negative voltages by $\Delta V \sim 0.25$ V. Such shifts indicate the presence of a net positive charge density in the insulator of $Q_{ox} = 2 \times 10^{12}/cm^2$ for a diode of area equal to 1.1×10^{-3} cm^2.

The effect of thickness on the non-equilibrium results of the p-type diode is somewhat similar to that seen with n-type devices. That is, as seen in Fig. 3.3, equilibrium characteristics can be obtained for diodes with thicker insulators. The difference in p-diodes, though, is an absence of the charging effects discussed in Sec. 4.2. Positive bias currents respond quite quickly to increases in voltage. Another difference noted was a certain unpredictability in the thickness at which "equilibrium" characteristics were obtained. Diodes with insulator thicknesses great enough to provide equilibrium characteristics in n-silicon devices would show current saturation, sometimes at quite large voltages. An example of such characteristics is shown in Fig. 4.9. Both the C-V and I-V data show the onset of non-equilibrium effects at $V_a \sim 2.5$ V.

Fig. 4.9a C-V curve of P_{22} diode (#1101) with $d_0 \sim 40$ Å measured at T = 300°K with f = 4 KHz. Onset of non-equilibrium conditions occurs at arrow

b Log I-V curve of P_{22} diode (#1101) with $d_0 \sim 40$ Å measured at T = 300°K. Onset of non-equilibrium conditions occurs at $V_a = -2.5$ V

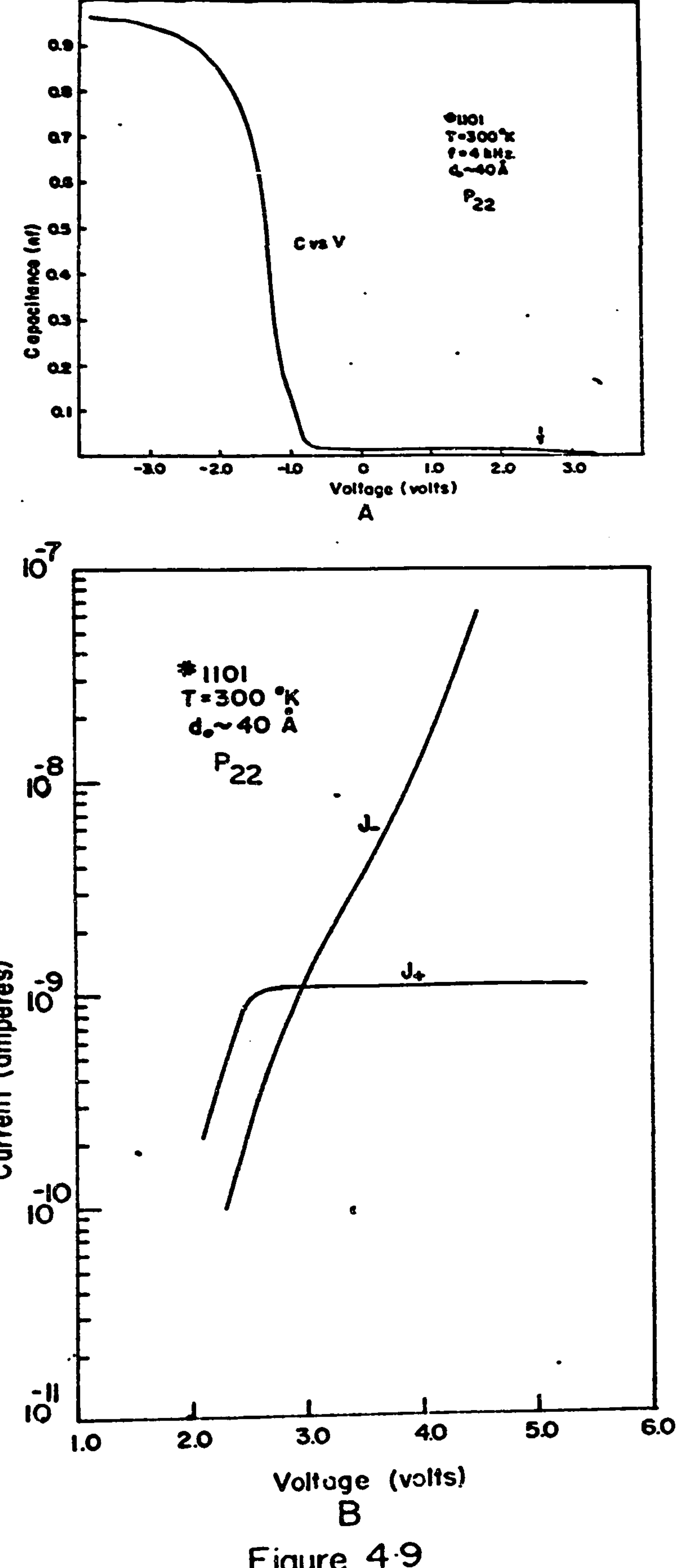


Figure 4·9

In the former case the capacitance begins to drop quadratically with voltage and in the latter case the current saturates.

The explanation of all these results is based on the identity of the dominant current flow in the p-type diode. In Chapter 3 it was seen that J_{cm} and J_{mc} were the dominating currents in all non-degenerate MIS tunnel diodes. The difference is that these currents are majority carrier flows in the n-silicon devices and minority carrier flows in p-silicon devices. Both magnitude and temperature dependence of the saturation current in Fig. 4.8a would tend to confirm the supposition that a minority carrier flow is dominant in the positive bias current of "non-equilibrium" p-type diodes as well.

The magnitude of such a current will generally be low, as it represents a direct measure of the bulk supply rate of minority carriers. Similarly, the temperature dependence of these currents reflects the thermal processes involved in their generation. The effects of thickness are harder to understand. The current saturation observed at thicker oxides in Fig. 4.9 is actually what one would expect for minority carrier currents. In terms of this model, what is unexpected is the fact that an "equilibrium" I-V characteristic, such as seen in Fig. 3.3, was obtained at all. Only if all positive bias currents are less than the minority

carrier supply rate should a non-saturating characteristic be obtained.

The most likely explanation for this behaviour is the increased minority carrier supply rate often found in thermally oxidized p-silicon MIS diodes. Such increases are due to the presence in the insulator of a net positive charge which is spread more or less uniformly across the wafer. The density of such charge was seen in Fig. 4.8b to be $\sim 2 \times 10^{12}/cm^2$ (as determined by the voltage shift of the diode's C-V curve). The resulting depletion-inversion layer at the semiconductor surface provides a relatively easy path for the lateral flow of minority carriers. The effects of this lateral communication have been studied in thick insulator MIS systems by Nicollian and Geotzberger [55] and in thin insulator MIS tunnel diodes by Waxman and Shewchun [8]. In both cases interest was centered on the more prominant effects of this lateral response on the a.c. properties of these diodes.

An example of the effects of such lateral flows on the a.c. response in our diodes can be seen in Fig. 4.8b. At voltages where the deep depletion effects had not yet set in, a large inversion capacitance response was obtained at the relatively high measurement frequency of 2 KHz. In the thicker oxide devices, where equilibrium characteristics can be obtained if supply rates are large enough, a

correlation can be found between large a.c. response and large d.c. current flow (as seen for example in Fig. 3.3a). In Fig. 4.9 for a diode with $d_0 = 40$ Å, no inversion response was seen at 4 kHz and the current saturated at 10^{-9} amps. On the other hand in Fig. 3.3c the diode ($d_0 \sim 41$ Å) exhibits a very large inversion response at 4 kHz corresponding to its large current flows ($J_- > 10^{-6}$ amps with no saturation).

It should be noted that these large currents do not necessarily signify minority carrier excesses in the bulk semiconductor. That is to say, the lateral response mechanisms still represent "equilibrium" processes and the use of the term "equilibrium diode" is still legitimate. The effect can be considered analogous to enlarging the apparent area of the metal contact seen by minority carriers.

The much different effects of actual minority carrier injection corroborate this analysis. In Fig. 4.8a the dashed-dot curve illustrates the effect of illumination on a non-equilibrium diode's I-V characteristics. Corresponding effects can be noted in Fig. 4.10 where the I-V characteristics of an "equilibrium" diode under illumination are presented. Theoretical curves in the latter figure are also presented for which it was assumed a quasi-fermi level separation of $\phi_n - \phi_p = 0.1$ and 0.2 eV respectively.

Fig. 4.10 Log I-V characteristics of "equilibrium" P_{22} diode showing effects of illumination on J_+ both experimentally (dash-dot curve) and theoretically (open triangles). Solid curves (solid triangles) represent experimental (theoretical) data for unilluminated diode. For this device $d_0 = 41$ Å. Parameters for theory listed in Table 3.1

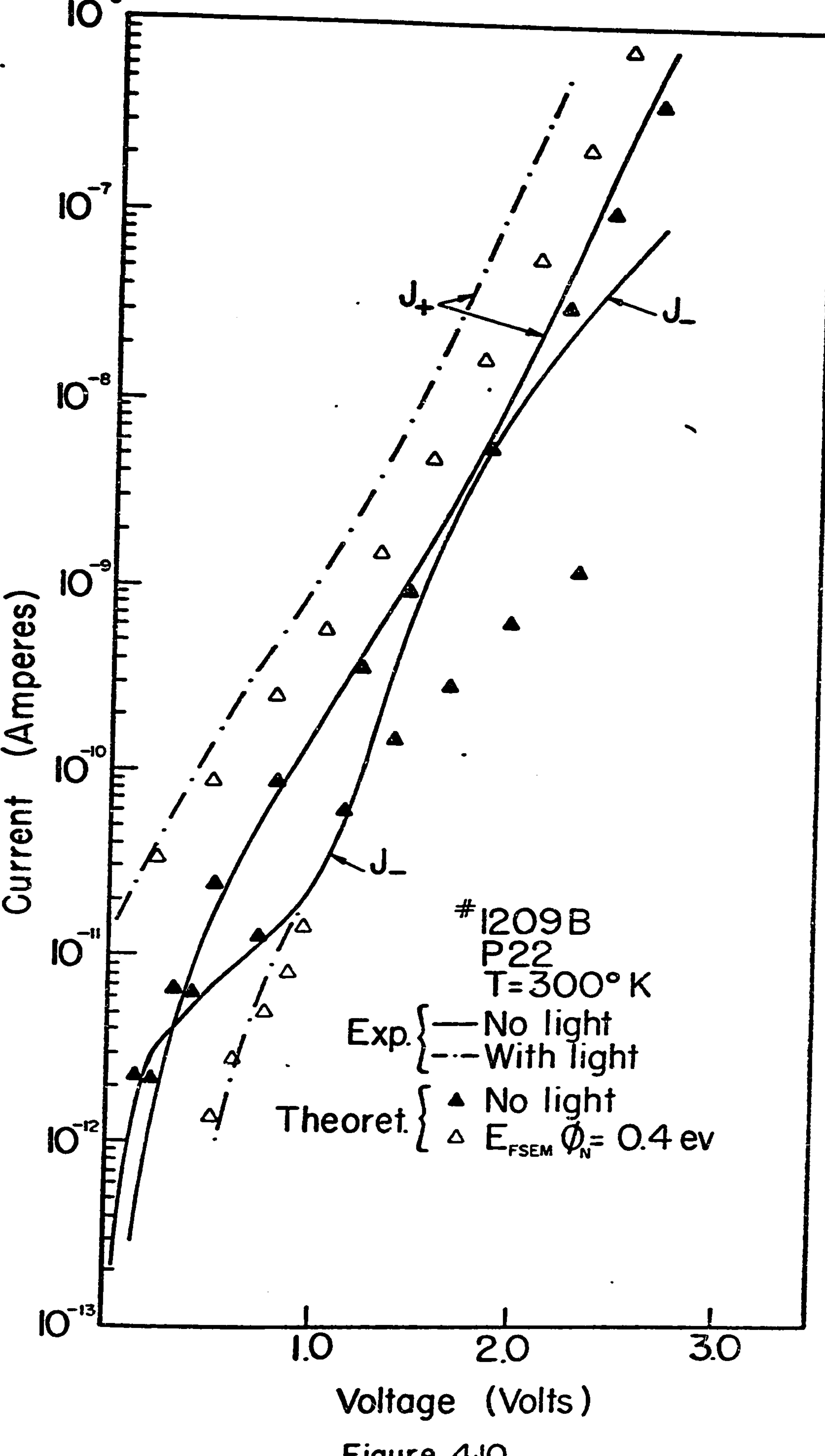


Figure 4·10

As expected, minority carrier injection can be seen to affect mainly the positive bias current, J_{cm}, in a p-type diode. In addition the negative bias current for $V_a > -1$ V has been considerably reduced. It can be shown that at zero bias there is a positive current flowing, a condition common to other diodes with intrinsic depletion layers at zero bias, such as Schottky barrier and p-n junction diodes.

No theoretical I-V curves are presented for the "non-equilibrium" p-silicon diode. This is due to a calculational rather than conceptual problem. It has been seen that large charge densities cannot be permitted at the surface of the semiconductor if a saturating I-V characteristic is desired. In p-silicon diodes at zero bias and small negative biases, a very large density of electrons is built up due to work function differences and oxide charge effects. This electron density is maintained by supply from the metal under negative and zero bias and is essentially an "equilibrium" density. Under positive bias the electrons must be supplied by the semiconductor and the supply, as already seen, is quite limited. The large zero bias electron density can not be maintained and must decrease as positive bias is increased. It will decrease until the voltage is reached at which the electron tunnel current J_{cm} equals the minority carrier supply rate. The calculational problem occured in the handling of the decreasing charge density and was insoluable

with the present method of determining the voltage distribution. It is not a simple problem to solve and requires a self consistent iterative approach to the solution of charge density and quasi-Fermi levels in the semiconductor.

4.3.2 The Effects of Doping Density

The log I - log V characteristics of three n-type diodes, with $d_0 < 30$ Å, and doping densities of $4 \times 10^{20}/m^3$, $10^{23}/m^3$ and $4 \times 10^{25}/m^3$ respectively are presented in Fig. 4.11. The current saturation that is characteristic of non-degenerate devices, can be seen to be a function of doping density. For the most heavily doped semiconductor ($N_D = 4 \times 10^{25}/m^3$) no indication can be seen of any saturation.

Similar behaviour is predicted by the "non-equilibrium" theory. Calculations of the I-V characteristics for diodes with a range of doping densities are shown in Fig. 4.12. Both "equilibrium" (curves a, b, c and d) and "non-equilibrium" (curves a', b', c' and d) characteristics are presented for each diode. For the diode with $N_D = 5 \times 10^{25}/m^3$ (curve d) the assumption of a minority carrier deficiency at the semiconductor surface has no effect at all on the predicted current-voltage curves. As expected, the maximum difference between "equilibrium" and "non-equilibrium" results occurs for the diode with the lowest value of doping density (curve a, $N_D = 10^{21}/m^3$).

These effects suggest that it is the total charge at the surface of the semiconductor (whether it is mobile or fixed charge) which controls the degree of current saturation. In semiconductors of low doping density, only

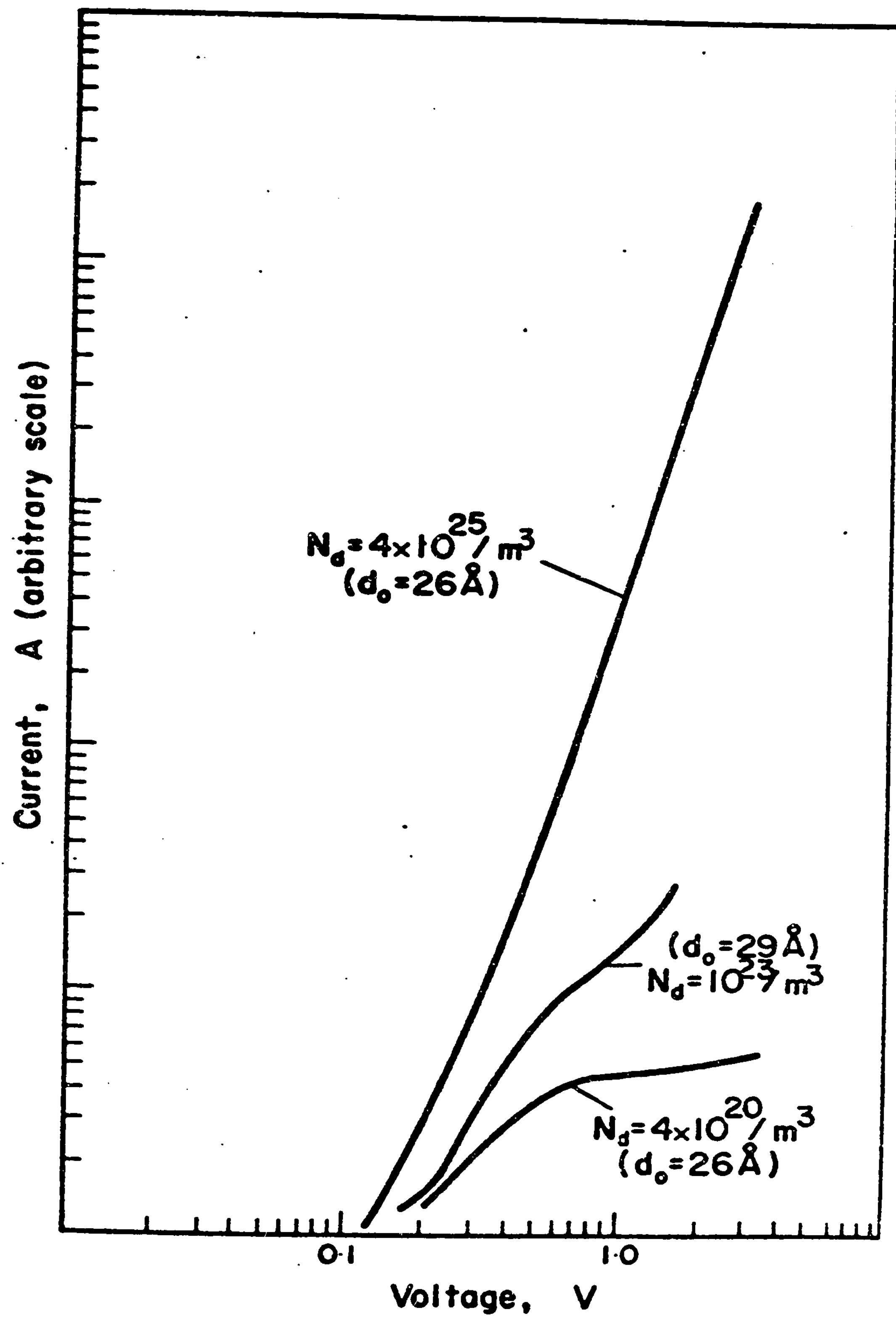


Fig. 4.11 Reverse (-ve) bias log I - log V curves (arbitrarily superimposed on same current scale) for "non-equilibrium" diodes of varying semiconductor doping densities

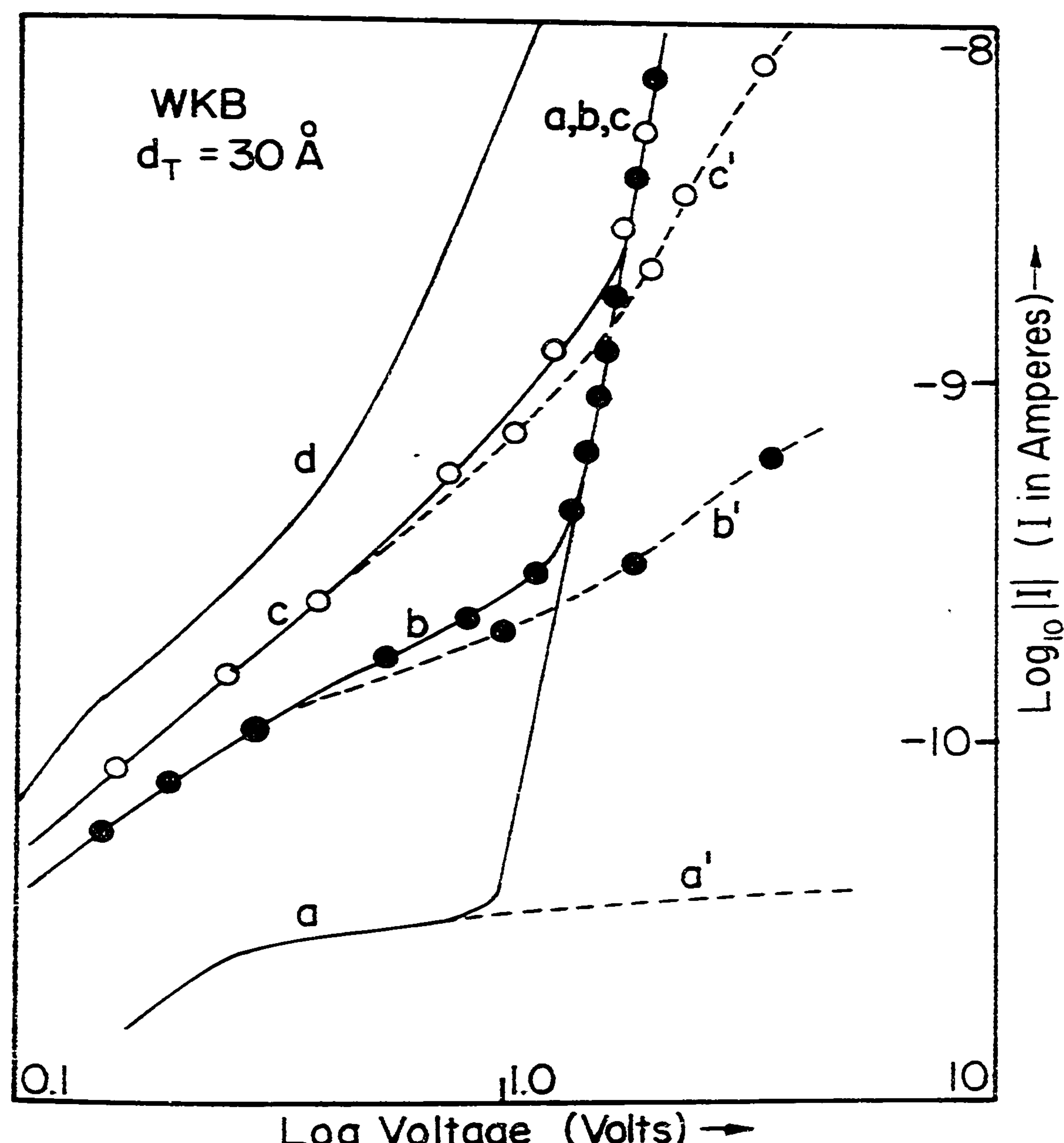


Fig. 4.12 Theoretical reverse (-ve) bias log I - log V curves of "non-equilibrium" (a', b', c',d) and "equilibrium" (a, b, c, d) diodes of differing doping densities given by

(a,a') $N_D = 5 \times 10^{20}/m^3$

(b,b') $N_D = 10^{23}/m^3$

(c,c') $N_D = 10^{24}/m^3$

(d) $N_D = 5 \times 10^{25}/m^3$

mobile charge densities can reach the required density (apparently $\sim 10^{26}/m^3$). If tunneling prevents a build-up of this mobile charge (i.e., of minority carriers under reverse bias) a saturation of the current-voltage characteristic occurs. In the more highly doped semiconductors, the presence of mobile charge is unnecessary. As tunneling cannot affect the static charge, no current saturation occurs.

To illustrate this point further, consider the field at the semiconductor surface. It is this field which, through Gauss' Law, controls the voltage drop across the oxide which, in turn, controls the tunnel current magnitude. An expression for the oxide voltage drop, V_{ox}, can be written as (neglecting oxide charge)

$$V_{ox} = (\varepsilon_s/\varepsilon_i)F_s \cdot d_T \qquad 4.1$$

where F_s is the semiconductor field at the surface. For current saturation, V_{ox} must remain constant with increasing bias. However, even in deep depletion, it can be shown that F_s is a continually varying function of bias. Consider some values for the quantities in Eq. 4.1. In non-degenerate materials F_s is typically 10^{+6} V/m. For a 20 Å oxide, therefore, $V_{ox} \sim 6$ mV. Obviously moderate changes in F_s will produce little discernable change in the currents controlled by V_{ox}.

For the much larger fields found at the surface of degenerate semiconductors (i.e., $\gtrsim 10^7$ V/m), this is no longer true.

The experimentally observed log I-V characteristics of p-silicon devices with doping density $N_A = 10^{25}/m^3$ are shown in Fig. 4.13. The device labelled #1226 was fabricated with an oxide thickness, $d_0 \sim 48$ Å. This diode could, therefore, be expected to be an "equilibrium" diode. On the other hand, the characteristics of the device #1227 with oxide thickness $d_0 \sim 31$ Å should be those of a "non-equilibrium" diode. A comparison of the I-V curves for each diode indicates that $J_+ > J_-$ for the "equilibrium" diode while $J_+ < J_-$ for the "non-equilibrium" device.

In addition to the effects of thickness on the current-voltage curves of a P_{25} diode, the influence of diode illumination is also shown (dashed curve) in Fig. 4.13. This can be compared with the results seen in Fig. 4.8 for a non-degenerate diode. In the latter case, the entire positive bias current-voltage curve was affected, while in the former case, only that portion of the curve with $V_a < 1.5$ V is seen to be affected. Although not demonstrated, the current J_+ of a degenerate p-type diode (i.e., $N_A > 10^{26}/m^3$) is unaffected by light.

The various results seen in Fig. 4.13 can be understood with a knowledge of the relative magnitudes of the component currents in a P_{25} diode. Consider first the

Fig. 4.13 Log I-V characteristics of "equilibrium" (#1226, $d_0 \sim 48$ Å) and "non-equilibrium" (#1227, $d_0 \sim 31$ Å) P_{25} diode. Solid curves indicate data taken at 300°K with no illumination. Effect of light on diode #1227 shown by dashed curve

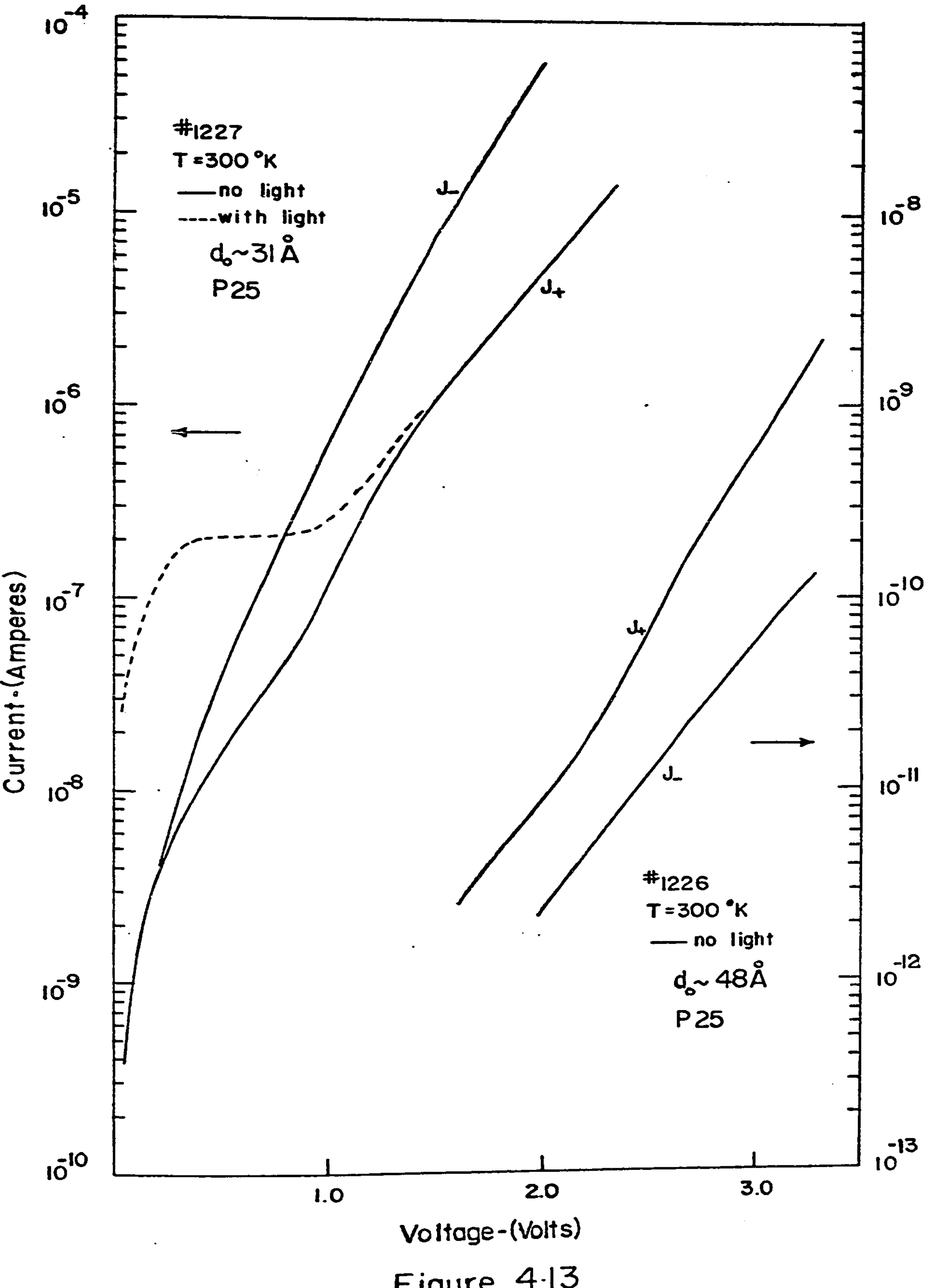


Figure 4.13

effect of thickness. In Fig. 4.12 it was seen that non-equilibrium conditions could still influence the currents of diodes with silicon doping densities as high as $10^{25}/m^3$. The change in the ratio of J_+ to J_- with thickness, could possibly be explained simply on this basis. However, the current flow in a P_{25} diode is, in theory, predominantly an electron flow under positive bias. This current will saturate regardless of doping density. The arguments, presented above for n-silicon diodes, apply to the effects of doping density on the saturation of majority carrier currents. The fact that J_+ does not saturate, but is merely reduced with respect to J_-, suggests that another current component has become dominant in the I-V characteristics of the "non-equilibrium" diode.

Such a view is consistent with the effects of light seen in Fig. 4.13. The light induced minority carrier current (dashed curve) can be seen to saturate at $\sim 2 \times 10^{-7}$ amps, a magnitude representing the maximum possible minority carrier flow. J_+ not only exceeds this value but is independent of illumination effects for $V_a > 1.5$ V. In diode #1227, therefore, J_+ must be considered a majority carrier flow whereas in "equilibrium" diodes (i.e., #1226) with $J_+ > J_-$, J_+ is predominantly a minority carrier current.

One interesting aspect of the behaviour of the P_{25} diode is the fact that a direct measurement of the insulator mass ratio of m^*_{cb}/m^*_{vb} can conceivably be made. Theoretically,

J_{vm} is greater than J_{cm} in a P_{25} diode by a factor which is a function of the insulator masses. Thus at $V_a = +1.5$ V, for instance, $J_{cm} \sim J_{vm}$ if $m^*_{cb} = m^*_{vb} = 1$, while $J_{cm} \sim 2 \times 10^3 \times J_{vm}$ for $m^*_{cb} = 1$ and $m^*_{vb} = \infty$. In Fig. 4.13 it can be seen that, relative to J_-, the saturation of J_{cm} in diode #1227 has reduced the current magnitude of J_+ by $\sim 50\times$. In other words, assuming the barrier masses to be independent of insulator thickness (contrary to what was concluded in Chapter 3), the magnitude of J_{cm} can be seen to be $\sim 50 \times J_{vm}$. This corresponds to $m^*_{cb} \sim 1$, $m^*_{vb} \sim 2$ theoretically. Because of the probable dependence of band masses on insulator thickness, this method cannot be taken as a definitive measure of these masses. However, these observations do tend to confirm the necessity of a two band model of the insulator.

4.3.3 Summary

In summary it has been shown that "non-equilibrium" effects can be observed for lightly doped p-silicon diodes in the form of a saturating current under positive bias. The magnitude and temperature dependence of this saturation current are indicative of the dominance of minority carrier flows. This was further confirmed by the effects of illumination on the diode. With this interpretation it was pointed out that all non-degenerate p-silicon diodes should

exhibit a positive bias current saturation at current levels dictated by minority carrier supply rates. It was, therefore, concluded that the observation of "equilibrium" diode characteristics was made possible only by the presence of extremely large lateral minority carrier flows. Such flows were attributed to the presence of an inversion layer at the semiconductor surface across the entire wafer, thereby considerably enlarging the effective area of the diode for minority carriers.

The influence of non-equilibrium conditions was seen to lessen for diodes with increasing doping density. No effects on current-voltage curves were discernable either experimentally or theoretically for diodes with N_D or $N_A \gtrsim 10^{26}/m^3$. Such behaviour was explained in terms of the effect of the charge density (whether mobile or static) at the semiconductor surface, on the voltage dependence of V_{ox}.

In p-silicon diodes of moderately high doping density (i.e., $N_A \sim 10^{25}/m^3$) non-equilibrium effects resulted in a change in the dominating current component of J_+. From the effects of illumination on this current, it was concluded that J_{cm} dominated in an "equilibrium" diode but that J_{vm} dominated in a "non-equilibrium" diode. A confirmation of the two band model of the insulator was indicated by these results.

CHAPTER 5

THE SURFACE OXIDE TRANSISTOR (SOT)

5.1 Introduction

The observation of non-equilibrium tunnel current-voltage (I-V) characteristics in metal-insulator-semiconductor (MIS) structures employing thin oxides of average oxide thickness $d_0 < 30$ Å and non-degenerate n-type semiconductors was discussed in Chapter 4. In particular, the effect of controlling the minority carrier density at the oxide-semiconductor (O-S) interface of these diodes was examined. It was shown that an increase in the minority carrier population in the bulk semiconductor (e.g., that due to minority carrier injection from a second MIS contact) resulted in a corresponding increase in the magnitude of the reverse-biased diode saturation current. However, the magnitude of the observed changes in diode current could not be explained solely in terms of an increased minority carrier current. It was concluded that this reverse saturation current was, in fact, comprised principally of majority carriers. This was confirmed by theoretical calculations which indicated that under non-equilibrium conditions the metal Fermi level could be pinned opposite the semiconductor conduction band, allowing a large but voltage-independent

majority carrier current flow to occur. These experiments suggest the feasibility of a three-terminal structure capable of transistor action. Such a device would employ a reverse biased MIS contact, of the type discussed above, as a collector and a second MIS contact, forward biased, as an emitter of the necessary minority carriers. The purpose of this chapter is to investigate the transistor behaviour obtained with thin oxide MIS structures of this nature.

Since the current flow mechanisms for the diodes and the corresponding current gains in the transistor structure are shown to be dependent on the presence of a thin oxide between the metal and the semiconductor, this device will be referred to as a Surface-Oxide-Transistor or SOT. The SOT differs from previous surface barrier transistors [56,57] due to the introduction of this thin oxide layer. In general, the principal advantages of such structures are the simplified fabrication techniques required (no semiconductor etching [57] or diffusions) and a planar configuration compatible with integrated circuit technology.

The transistor behaviour and diode characteristics of this structure were studied as a function of oxide thickness and contact separation distance. For diodes with all but the thinnest insulators ($d_0 \lesssim 25$ Å) it was beneficial to form the oxide by means of voltage stresses. The temperature dependence of this new type of MIS diode was investigated to

determine if any new transport mechanisms were involved in current flow. With such information, two models for the two distinct types of transistor action observed are proposed: one based on currents due to the tunneling of carriers through the oxide and a second based on the properties of small area Schottky barrier-like diodes.

5.2 Device Preparation

The devices, whose cross-sectional view may be seen in Fig. 5.1a, were fabricated from (100)-oriented 10 Ω-cm n-type silicon wafers. Initially, a thick oxide of ∿5000 Å was grown in steam on each wafer and, from this, oxide pads were delineated for bonding purposes using photo-lithographic (photoresist) techniques (Figs. 5.1a, 5.1b). The remaining silicon surface was recleaned and reoxidized to a thickness of 20–100 Å. Aluminum collector and emitter contacts were created on the top side of the wafer, also employing photoresist techniques. A third "base" contact was made to the back side of each wafer. For a typical contact geometry, seen in Fig. 5.1b, the width of a collector arm is typically 0.2 mil and the length of the emitter finger ∿0.5 mil. Contact spacing between collector and emitter could be varied between 0.15 and 0.8 mil.

Initially after processing, good transistor action is not observed. The reason for this is due to the fact that the reverse current in the collector diode either does not saturate under conditions of minority carrier injection [11] or is of negligible magnitude, oxide thickness controlling which particular behaviour is observed. To improve diode and, therefore, transistor behaviour and extend this behaviour to

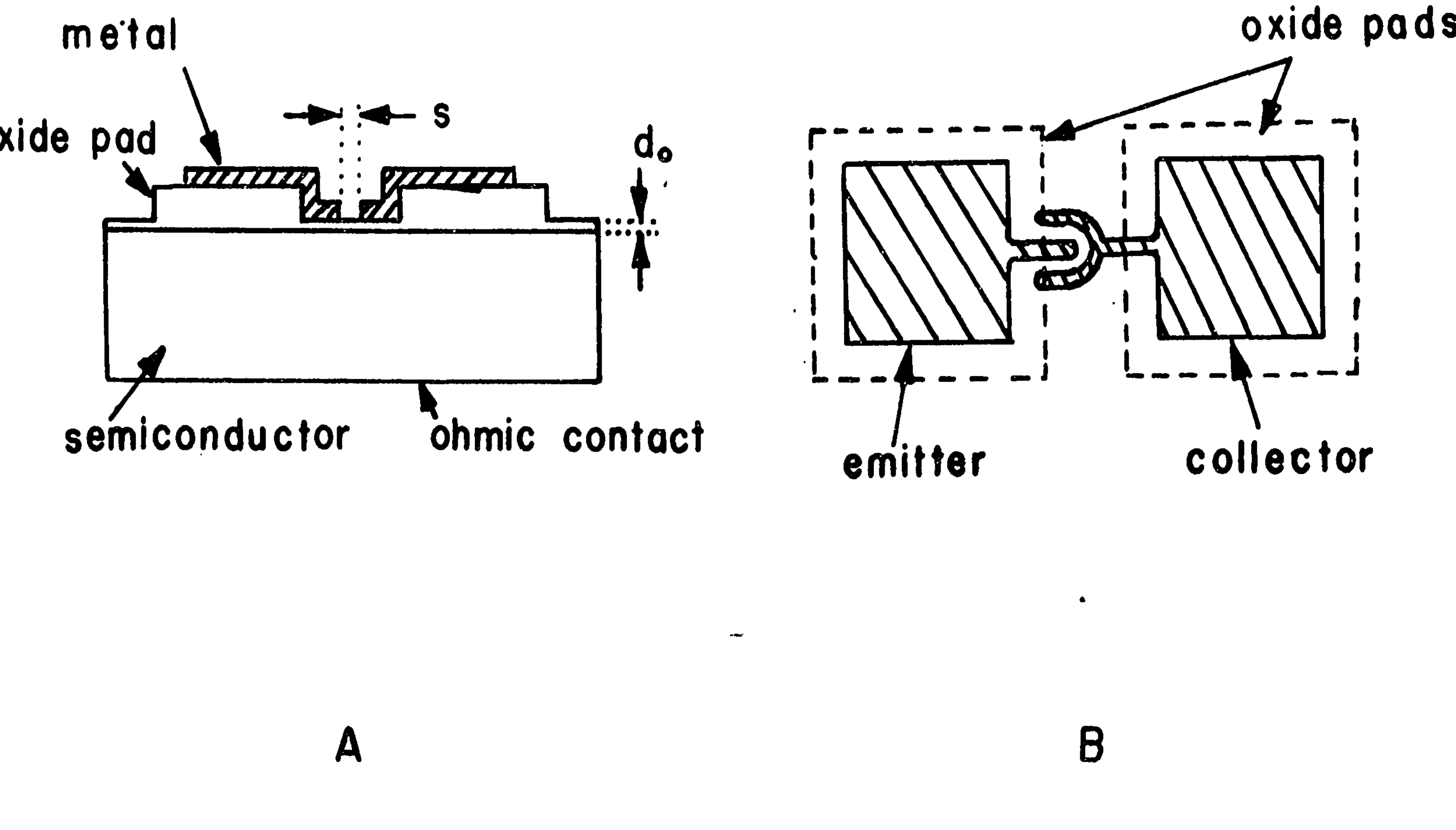


Fig. 5.1a A cross-sectional view of the Surface-Oxide-Transistor with average oxide thickness d_0, and contact separation S

b Top view of typical contact geometry

devices with oxide thickness $d_0 > 40$ Å, (the thickness beyond which diode currents are normally insignificant) a forming procedure was employed in which sufficient voltage was applied to each MIS contact to create a permanent change in the conductivity of the insulator. Whether oxide forming or oxide breakdown is the result of the applied voltage stress is difficult to ascertain. A detailed review of forming and breakdown effects has been carried out by Dearnaley et al. [58] and is not discussed here. It will only be noted that there is some evidence which suggests the forming does not simply occur at pinholes in the insulator. This point will be discussed later.

5.3 Device Characteristics

5.3.1 The Transistor

The two circuit configurations in which transistors are generally characterized are the common-base (C-B) and common-emitter (C-E) configurations. A Tektronix 575 curve tracer was employed to test devices for the current gains associated with these two operating modes, h_{FB} and h_{FE} respectively. These quantities are defined by $h_{FB} = \Delta I_C/\Delta I_E$ and $h_{FE} = \Delta I_C/\Delta I_B$ where ΔI_C, ΔI_E, ΔI_B are incremental increases in collector, emitter and base currents respectively. The observed transistor properties generally fell into two distinct classes characterized by (a) devices with $h_{FB} > 1$, and (b) devices with $h_{FB} \lesssim 1$. Transistors in these two groups shall be referred to as type 1 and type 2 devices respectively. It will be seen later that entirely different mechanisms are responsible for the behaviour of these two classes of device.

Examples of the characteristics of these two types of transistor are shown in Fig. 5.2. The characteristics of a device with an unformed collector contact ($d_0 \sim 20$ Å) are shown in Fig. 5.2a and demonstrate the effect of minority carrier injection on the reverse saturation current of thin oxide MIS diodes of the type seen in the previous chapter. A forward-biased emitter current level of $I_E = 2$ μa was

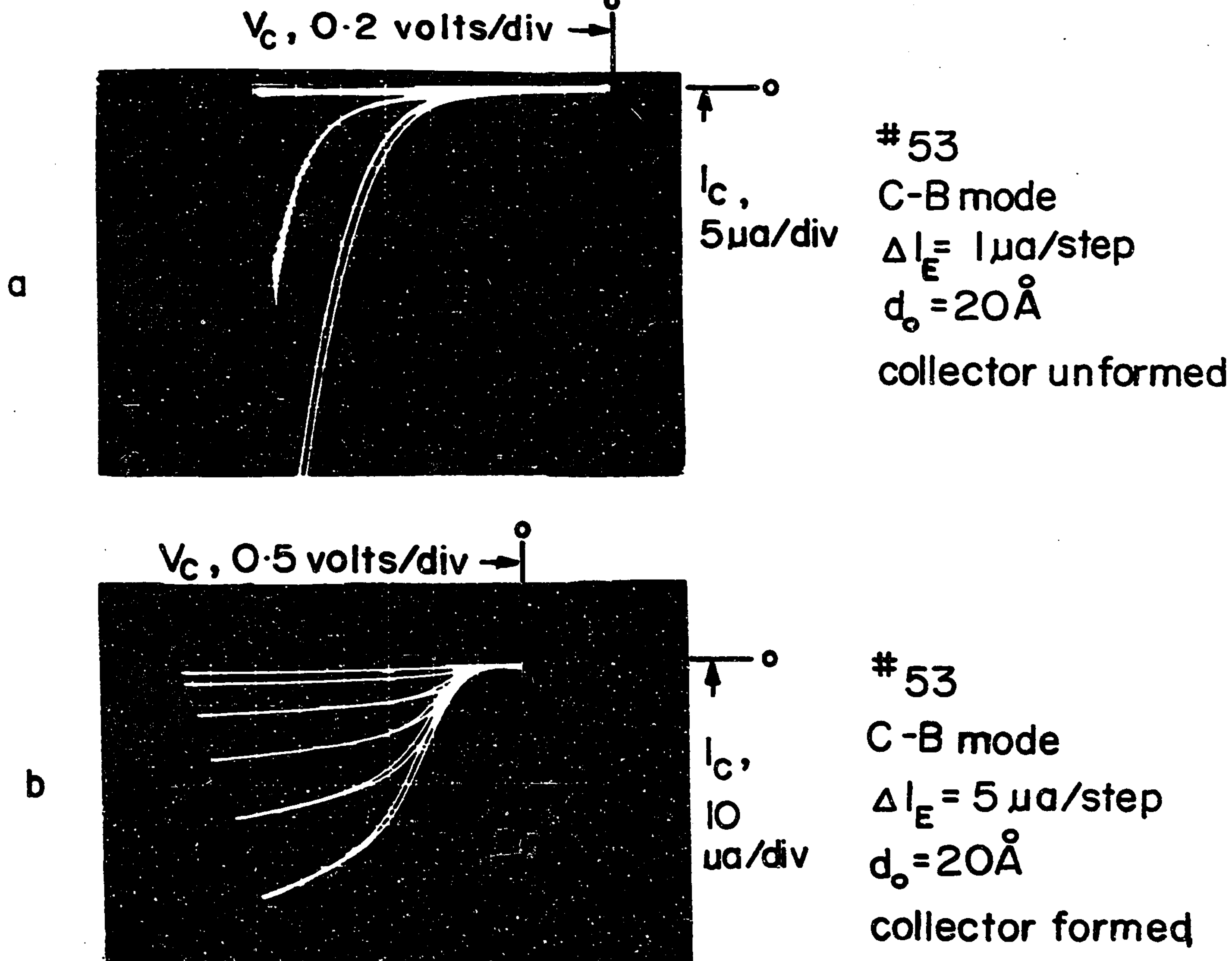


Fig. 5.2 Examples of the different types of transistor characteristics of $A\ell$-SiO_2-(n-Si) devices in

a C-B mode of device #53 with collector unformed, d_0 = 20 Å, and current steps of ΔI_E = 1 μa

b C-B mode of device #53 (type 1) after forming with d_0 = 20 Å and current steps of ΔI_E = 5 μa

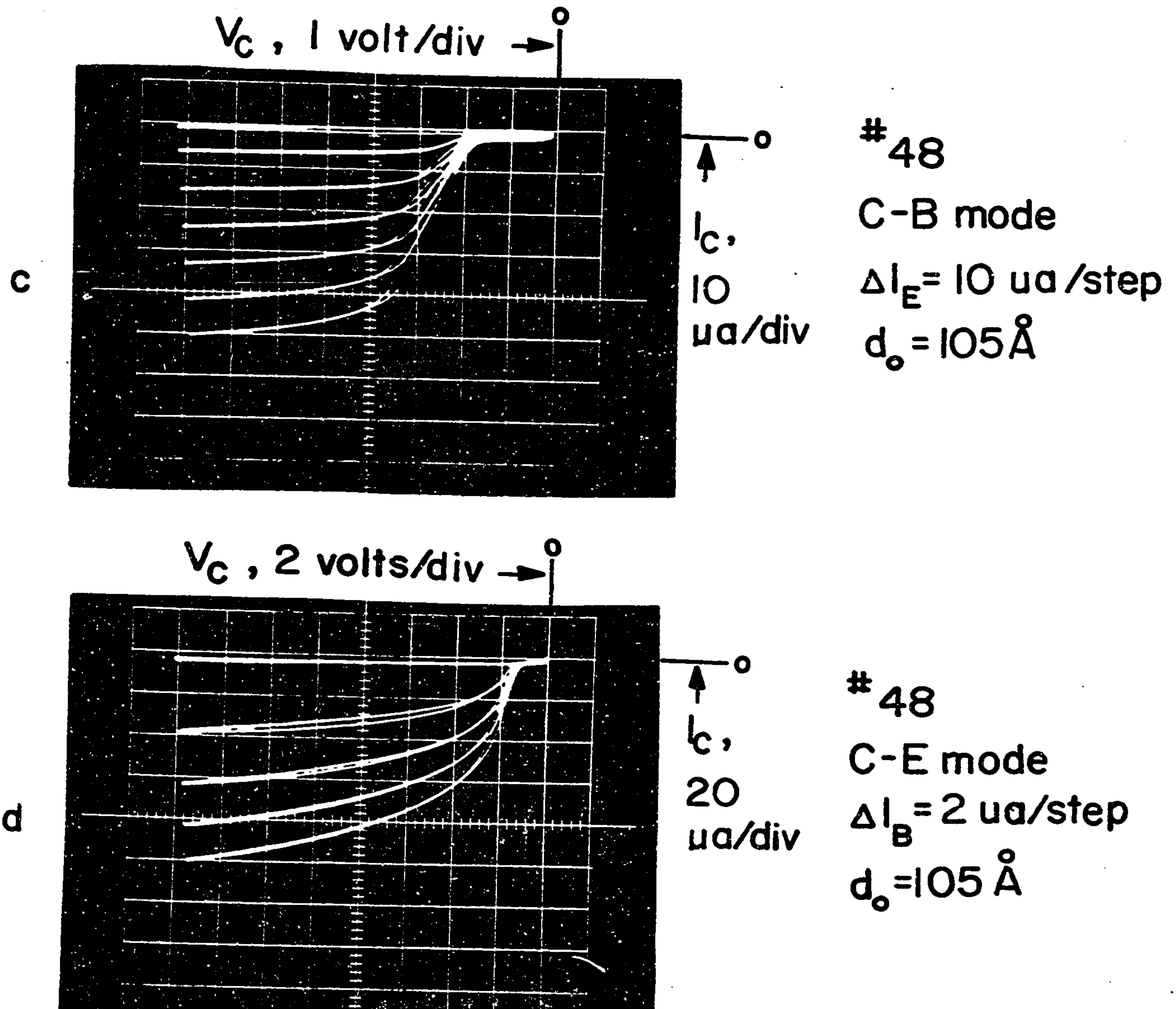


Fig. 5.2 Examples of the different types of transistor characteristics of Aℓ-SiO_2-(n-Si) devices in

c C-B mode of device #48 (type 2) after forming, with d_0 = 105 Å and current steps of ΔI_E = 10 μa

d C-E mode of device #48 (type 2) after collector forming with d_0 = 105 Å and current step ΔI_B = 2 μa

sufficient to result in a non-saturating reverse current in such a collector. Upon lightly forming the collector contact, a type 1 transistor (Fig. 5.2b) was obtained. A current gain of $h_{FB} \sim 4$ is seen for this particular device at emitter current levels of $I_E = 25$ μa. The type 2 transistor ($d_0 \approx 105$ Å), whose properties are shown in Figs. 5.2c and 5.2d, demonstrates a typical value of C-B current gain, $h_{FB} \sim 0.9$-0.95, as well as a C-E gain of $10 \lesssim h_{FE} \lesssim 20$. The variations observed in these quantities were functions of the emitter current level and collector voltage.

Typical values of current gain for a number of devices with varying oxide thickness are seen in Table 5.1. In most cases in this table two values of both h_{FB} and h_{FE} are given for a device. These values were measured at reverse collector biases of -10 and -25 volts respectively. It is apparent that there is a correlation between the type of transistor behaviour observed and the thickness of the insulator. A transition from type 1 ($h_{FB} > 1$) to type 2 ($h_{FB} \lesssim 1$) behaviour takes place at approximately $d_0 = 31$ Å. It should be noted that this correlation did not exist in devices with poorer quality insulators containing defects such as pinholes (as indicated by the insulator forming voltage [59]). In such devices it was generally possible to obtain only $h_{FB} << 1$ at all oxide thicknesses.

TABLE 5.1

Experimentally observed values of h_{FB} (for given emitter current step ΔI_E) and h_{FE} (for given base current step ΔI_B) at various oxide thicknesses, d_0. Devices #53 and #14 were not operable in common emitter mode. Where two values of gain are noted collector voltages of -10 and -25 V respectively were used.

Device #	d_0	$h_{FB}/\Delta I_E$	$h_{FE}/\Delta I_B$
53	∿20 Å	5/2 μa	not operable
14	30 Å	3/5 μa	not operable
17	32 Å	0.83/10 μa	5/2 μa
		0.91/10 μa	11/2 μa
41	42 Å	0.80/10 μa	5/2 μa
		0.92/10 μa	10/2 μa
19	64 Å	0.85/10 μa	4/5 μa
		0.95/10 μa	-
47	89 Å	0.9 /10 μa	-
		0.95/10 μa	22/2 μa
48	105 Å	0.9 /10 μa	12/2 μa
		-	-

A practical upper limit to the oxide thickness employable in a SOT was found to be ∿150 Å. At the opposite extreme, $d_0 \lesssim 15$ Å, the device becomes a simple Schottky barrier latteral transistor, which, although still capable of transistor action, has current gains of greatly reduced magnitude (never greater than one in either the C-B or C-E modes). For comparison, several Schottky barrier devices were constructed employing the same contact geometries seen in Fig. 5.1b. Any insulator present between the metal and semiconductor was of a thickness of $d_0 \lesssim 15$ Å (the natural oxide thickness). The characteristics of this type of transistor structure are shown in Figs. 5.3a and 5.3b. The Aℓ-(n-Si) Schottky barrier device (Fig. 5.3a), fabricated by a sintering process discussed in Ref. 60, shows a value of $h_{FB} \sim 0.04$ at $I_E = 2$ ma. The Au-(n-Si) device in Fig. 5.3b (given no special treatment) has an $h_{FB} \sim 0.03$ at similar emitter current levels, as well as a poor reverse saturation impedance.

Another important physical parameter in these structures is the collector to emitter contact separation as demonstrated (for a type 2 device) in Table 2. As expected, current gains drop as contact separation increases. For a 0.2 mil separation, the values $h_{FB} = 0.95$ and $h_{FE} = 22$ were obtained while with a 0.8 mil separation gains of $h_{FB} = 0.58$ and $h_{FE} = 2.5$ were measured. Type 1 devices did not show

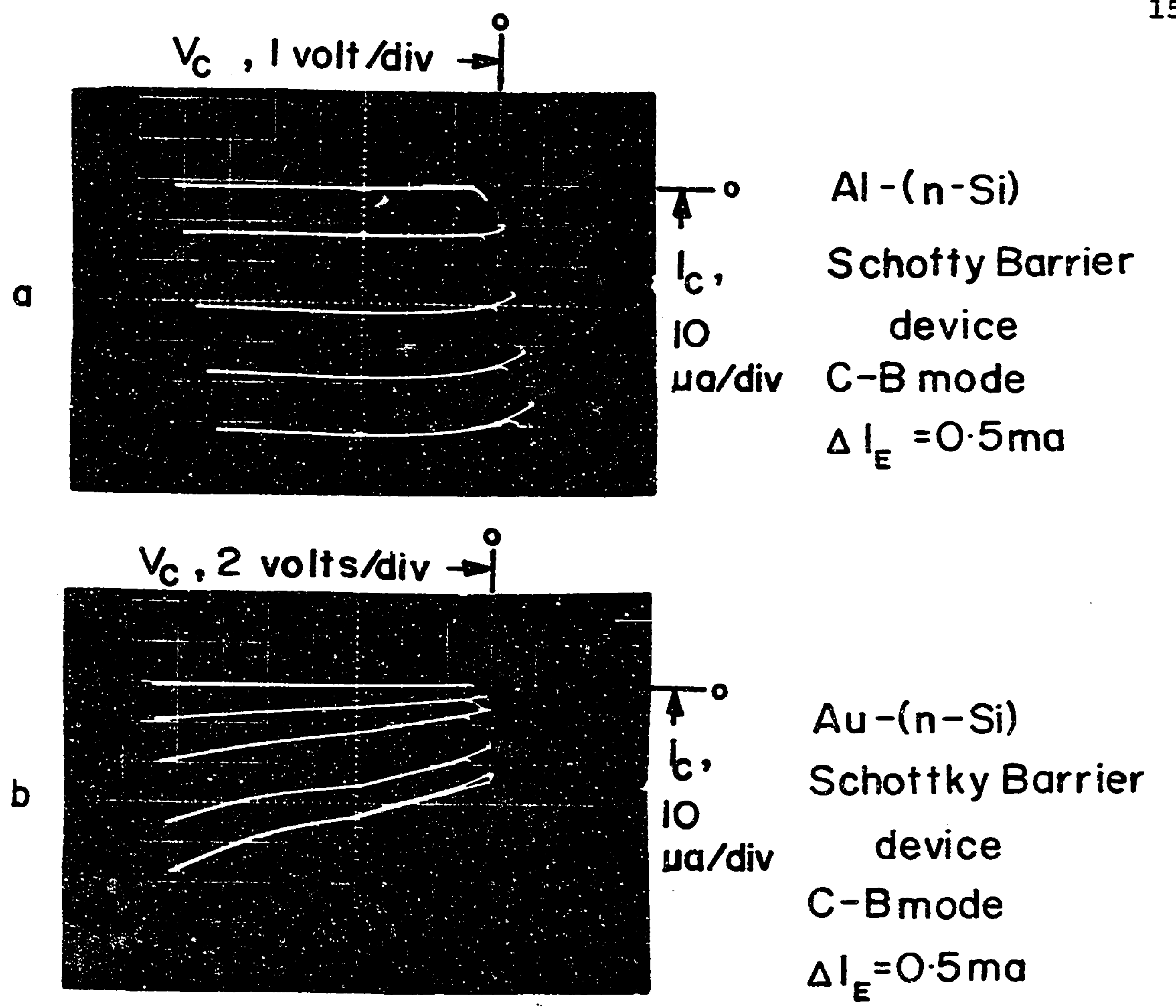


Fig. 5.3 Transistor characteristics of two Schottky barrier devices a) Aℓ-(n-Si); b) Au-(n-Si) fabricated with a contact geometry identical to devices used for Fig. 5.2. A C-B configuration with current steps ΔI_E = 0.5 ma was employed

TABLE 5.2

Experimentally observed values of h_{FB} (for given emitter current step ΔI_E) and h_{FE} (for given base current step ΔI_B) at various emitter to collector contact separations, S, and collector voltage of -25 V.

Contact Separation, S (mil)	$h_{FB}/\Delta I_E$	$h_{FE}/\Delta I_B$
0.2	0.95/10 μa	22/2 μa
0.45	0.8 /10 μa	5/2 μa
0.8	0.58/10 μa	2.5/2 μa

the marked contact separation dependence of type 2 devices over the same range of separations.

As a general rule the transistor action of the Aℓ-SiO_2-(n-Si) devices was quite reproducible. Attempts to construct complimentary devices employing p-silicon, though, met with only partial success. The forming process did not appear to yield diodes with the necessary stability and reproducibility for SOT devices. Reverse breakdown voltage and reverse impedance were often lower than for the corresponding n-Si devices. Gains were also generally lower.

5.3.2 The MIS Diode

The basis of the oxide barrier transistor demonstrated in the last section is the formed MIS diode. Figure 5.4, shows the log I-V characteristics (as a function of temperature) of the collector-base diode of the transistors whose characteristics have been seen in Fig. 5.2. Figure 5.4a shows the pre-formed log I-V behaviour and Fig. 5.4b the post-formed behaviour of a diode of a type 1 device. The post-forming characteristics of a diode of a type 2 transistor are shown in Fig. 5.4c. The observed currents in the latter

device #53
collector tobase diode
before forming
— 293°K
- - - 77°K

I_+

I_-

10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}

I - (Amperes)

0 0·2 0·4 0·6 0·8 1·0 1·2

|V|, volts →

Fig. 5.4a Log I-V characteristics as a function of temperature for collector-base diode of device #53, before forming. The solid (dashed) curves indicate data taken at 293°K (77°K). The designations I_+ and I_- indicate currents observed with positive and negative bias respectively on the metal

device #53
collector to base diode
after forming
— 293 °K
- - - 77 °K

I_+

I_-

10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}

I - (Amperes)

0 0·2 0·4 0·6 0·8 1·0 1·2

|V| , volts →

Fig. 5.4b Log I-V characteristics as a function of temperature for same diode as in Fig. 5.4a measured after forming. The solid (dashed) curves indicate data taken at 293°K (77°K). The designations I_+ and I_- indicate currents observed with positive and negative bias respectively on the metal

device # 48
collector to base diode
after forming
—— 293°K
---- 77°K

I_+

I - (Amperes)

10^{-5}, 10^{-6}, 10^{-7}, 10^{-8}, 10^{-9}

0 0·2 0·4 0·6 0·8 1·0 1·2

|V| , volts →

Fig. 5.4c Log I-V characteristics as a function of temperature for collector-base diode of device #48. The solid (dashed) curves indicate data taken at 293°K (77°K). The designations I_+ and I_- indicate currents observed with positive and negative bias respectively on the metal

diode, negligible before forming, were still $< 10^{-11}$ amps under reverse bias even after forming. The dashed curves in these figures represent the diode currents at 77°K.

A possible indication of the physical effects of forming, as determined by a scanning electron microscope (SEM), can be seen in the micrographs shown in Fig. 5.5. The device seen in this figure, at a magnification of 200x in the standard SEM mode, was similar in all respects to other devices discussed in this thesis except for contact geometry. The fingers of this geometry were 10 mils by 1 mil and, therefore, much larger in area than the contacts shown in Fig. 1. (The white bar running diagonally across the pictures in Fig. 5.5 is a bonding lead.) The micrographs shown in Figs. 5.5b and 5.5c were taken with the microscope in the Charge Collection Mode (CCM). In this mode, dark areas on the micrographs indicate regions of large, beam-induced, current flow. In Fig. 5.5b the emitter contact was unformed and shows no such dark areas while Fig. 5.5c was taken after emitter forming. It is evident that current flow in the contacts of a SOT can be through small localized areas in the insulator.

Fig. 5.5a Scanning electron micrograph (at 200×) of collector and emitter contacts of a SOT

b Charge Collection Mode (CCM) micrograph of device in Fig. 5.5a showing effects of collector forming

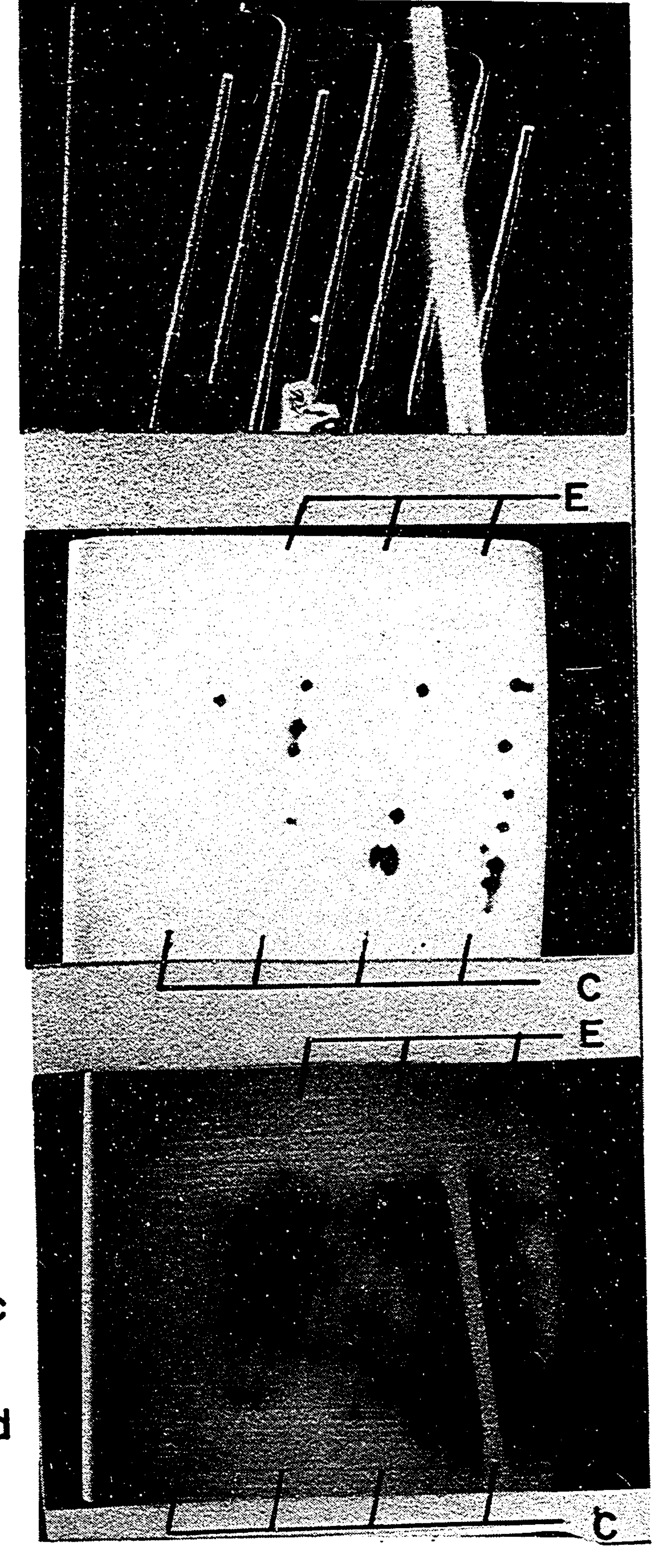
c Charge Collection Mode (CCM) micrograph of device in Fig. 5.5a after emitter forming as well

Scanning Electron

Micrograph

(200x)

a



b

E unformed

C.C.M. Micrographs

c

E formed

5.4 Discussion of Results

The explanation of the behaviour of both classes of surface oxide transistor presented in Sec. 5.3 can be found in the I-V characteristics of the diodes of these transistors. Turning first to the diodes of type 1 devices, it can be seen in Fig. 5.4b that the currents in these diodes are relatively independent of temperature variations. In fact, from a comparison of Figs. 5.4a and 5.4b, little difference can be noted between the I-V characteristics of pre-formed and post-formed diodes with insulators as thin as that of diode #53. Only under positive bias, $V_a > 0.4$ V, can any differences be observed, indicating that the basic tunnel barrier thickness of the diode, d_T, has remained unchanged during forming. This type of formed diode can, therefore, still be classified as a "non-equilibrium" MIS tunnel diode.

The rapid increase in current magnitude with bias for $V_a > 0.4$ V, suggests a new current component has been introduced into the system. The most likely source of such a component is an oxide trap caused by forming. In addition to causing an additional current component to be added to J_+, the presence of such a trap can also explain the alteration in the effects of minority carrier injection on the reverse saturation current, J_-, of the diode (cf. Figs. 5.2a and 5.2b). In Chapter 4 it was seen that the magnitude of the

saturation current in a "non-equilibrium" diode depended on the density of minority carriers that was allowed to build up at the semiconductor surface. For sufficiently large densities corresponding to large minority carrier supply rates, saturation was eliminated in a fashion similar to that seen in Fig. 5.2a. Forming would appear to prevent these build-ups from occuring by lowering the tunnel probability for minority carrier currents (J_{vm}). This would be possible if the energy level of the proposed oxide trap were situated opposite the valence band of the semiconductor.

In any case,the "non-equilibrium" theory of Chapter 4 predicts the necessary current multiplication to explain the observation of transistors with $h_{FB} > 1$. Despite the reduction in effective current "gain" produced by forming, current multiplication α_{IC} is still possible when the diode is employed as a collector in a transistor structure. The reduction of current gain is offset by the increased reversed bias impedance of the diode,as saturation can still be maintained.

The fact that type 1 transistors are not operable in the C-E mode is explicable in terms of the "non-equilibrium" model of the collector diode. That is, the application of bias between the collector and emitter results in an injection current of minority carriers that is dependent on the collector bias. A necessary condition for saturation of the

"non-equilibrium" diode is a fixed minority carrier supply rate. Thus when the supply rate becomes dependent on collector bias, saturation can no longer be maintained.

The temperature dependence of the diode currents in type 2 devices indicates that entirely different current flow mechanisms are involved in the operation of these transistors. The assumption was made that a thermionic emission current mechanism was dominant. A typical expression for such currents is given by [61]

$$J \propto T^2 \exp[-q(\phi_B - V_a)/kT] \qquad 5.1$$

where T is the temperature in °K, k is Boltzman's constant, q the charge on an electron, ϕ_B the effective barrier height, and V_a the applied voltage. Activation energy plots of log I/T^2 versus 1/T for diodes of several type 2 devices are shown in Fig. 6. For the diode with d_0 = 105 Å, a value of $\phi_B \simeq 1.0$ eV was obtained while for the diode with d_0 = 37 Å it was determined that $\phi_B \simeq 0.8$ eV. These values of ϕ_B are greater than that measured by Yu et al. [60] for the barrier height of their near-ideal Aℓ-(n-Si) Schottky barriers ($\phi_B = 0.69 \pm .01$ eV). It would appear, therefore, that in Aℓ-SiO_2-(n-Si) type 2 devices described in this thesis, a Schottky barrier-like diode is produced by the forming process, with a barrier height that is a function of the

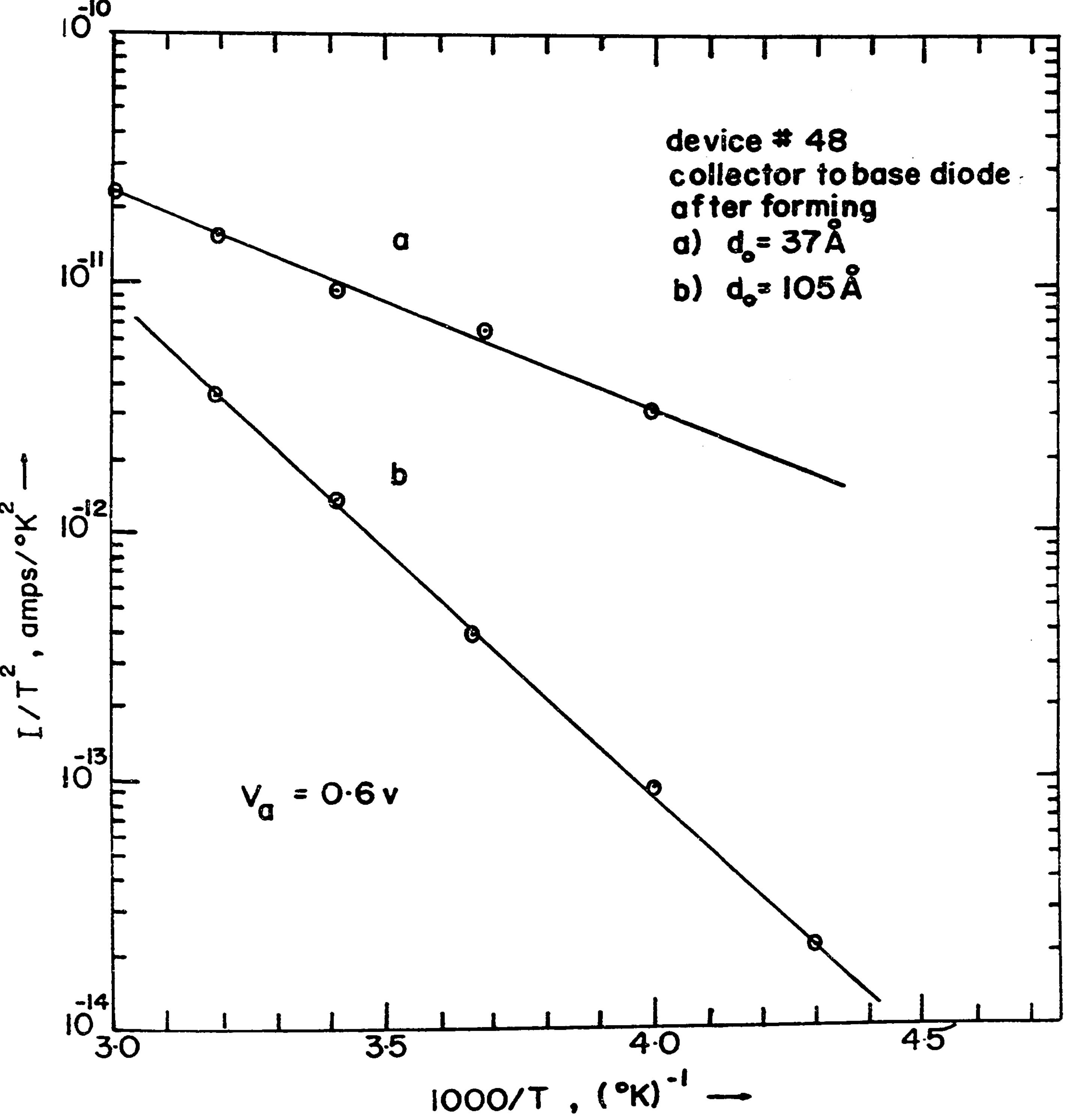


Fig. 5.6 Activation energy plot of forward currents in collector-base diode of devices with
a) d_o = 37A and
b) d_o = 107A (both at V_a = 0.6 V)

original insulator thickness, approaching the "ideal" value of barrier height as $d \rightarrow 0$.

As stated earlier, type 2 transistors did not display values of $h_{FB} > 1$. This behaviour is consistent with the fact that a Schottky barrier-like collector is created after forming. It can be expected that no current multiplication ($\alpha_{IC} = 1$) will occur in such a contact. The current flowing in the collector junction will, therefore, be principally a minority carrier current. As the minority carriers are almost entirely supplied by the emitter, the magnitude of the collector current will be controlled by two factors [62]: the injection efficiency (γ_E) of the emitter and the collection efficiency (β_F) of the collector ($h_{FB} = \gamma_E \cdot \beta_F \cdot \alpha_{IC}$). The latter quantity, β_F, should be a function of contact separation distance. This was confirmed by measurements of h_{FB} and h_{FE} for devices with different contact separations. The results are shown in Table 5.2. The voltage dependence of h_{FB} and h_{FE} seen in Table 5.1 can then be interpreted as a decrease in the "effective" separation between contacts as the collector contact depletion layer grows with increasing reverse bias (the variations in α_{IC} from transistor to transistor in type 1 devices, make it difficult to observe a similar large dependence of current gain on contact separations of this order). In general, methods for aiding collection efficiency developed for the lateral diffused

transistor [63,64] are applicable with a SOT. These include "drift-aid" in which ohmic contacts of an appropriate geometry are biased to provide field assistance to the diffusing carriers [63] and the use of heavily doped layers immediately below the junction to reduce loss of injected minority carriers to the bulk material [64]. Even without these aids it can be seen from Table 5.2 that β_F must already approach unity for 0.2 mil contact separation, S, and large collector voltages. Further enhancement of β_F is also possible simply by decreasing S.

With $\alpha_{IC} = 1$ and $\beta_F \sim 1$ it is apparent that γ_E will be an important parameter in determining the transistor gain of type 2 devices. Two major factors affecting γ_E are barrier height and contact area. The activation energy plots shown for type 2 diodes in Fig. 6 indicate that forming results in a relatively large effective barrier height ($0.8 < \phi_B < 1.0$ eV). Large barrier heights are known [65] to enhance γ_E in planar Schottky barriers. That contact area is also an important parameter can be seen from recent theoretical calculations [65-67] of γ_E for both Schottky barriers and point contact diodes. Entirely different values of γ_E and its variations with emitter current are predicted, depending on whether a planar or point contact geometry is assumed. In the latter case, $\gamma_E \sim 1$ for small values of current. Calculations have been made with a general Schottky barrier model [68] which confirm

that a definite increase in γ_E is observed with decreasing area. As seen in Fig. 5, current flow in type 2 diodes is apparently through regions of the insulator of very small area. The small area of these regions might be interpreted to indicate the presence of pinholes in the insulator originally but this is not necessarily the case. It was shown in Ref. 11 that non-uniformities in oxide thickness (but not pinholes) appeared to exist in the unformed insulator of MIS diodes. It can be expected, therefore, that forming would occur where the oxide is thinnest and fields highest. That such regions were small in area was indicated by comparison of the average oxide thickness, d_0, calculated from the oxide capacitance, and the oxide thickness calculated from tunnel current measurements [11]. Further confirmation is obtained from the fact that little change was observed, due to forming, in the capacitance-voltage (C-V) behaviour of a diode (typical values of oxide capacitance were $\sim$2 pf for $d_0 \simeq 100$ Å).

It is not known at present what the effect is, on the transistor action of the device, of the large areas under the unchanged portion of the contact subject to the normal electrostatic fields of an MIS diode. It is probable that β_F is enhanced by the extension of the reversed biased collector contact depletion layer under these areas. It is also felt that punch-through from collector to emitter is

retarded by the presence of an accumulation layer under the unformed portion of the forward biased emitter.

Such punch-through is responsible for the relatively poor transistor behaviour of the p-silicon SOT. Oxide charge, as discussed in previous chapters, results in the formation of a depletion-inversion layer at the surface of a p-silicon wafer, whether that surface is beneath a metal contact or not. Such a layer provides a low resistance path between collector and emitter. The collector bias by means of this path can then influence the emitter bias, thereby controlling the minority carrier injection from this latter contact. As seen with n-silicon type 1 devices, operated in the C-E mode, a saturating collector current can not be maintained under these conditions. This behaviour is unfortunate since the p-silicon MIS diode has an advantage which normally would make it attractive, at least as an emitter. From the analysis of the third chapter it can be seen that the predominant current flow in p-type MIS diodes is a minority carrier flow. Thus, values of $\gamma_E \rightarrow 1$ can be more readily attained with these diodes than with n-silicon diodes.

5.5 Summary

A new type of surface barrier transistor has been described, the Surface-Oxide-Transistor or SOT. Employing the properties of formed $A\ell$-SiO_2-(n-Si) contacts with average insulator thicknesses of $20\ \mathring{A} < d_0 < 150\ \mathring{A}$, two types of transistor action were observed, each based on different mechanisms of charge transport through the oxide. A model based on tunneling was proposed for type 1 devices with $h_{FB} > 1$ ($20\ \mathring{A} < d_0 < 30\ \mathring{A}$) because of the temperature independence of the diode currents in these structures. The non-equilibrium theory discussed in Chapter 4 which predicts values of collector current multiplication $\alpha_{IC} > 1$ proved adequate to explain the observed current gains. A second model was proposed to explain transistor action in type 2 devices with $h_{FB} \lesssim 1$ ($d_0 > 30\ \mathring{A}$). This model was based on the formation of small area Schottky barrier-like diodes in certain regions of the contact. An effective barrier height $0.8\ \text{eV} \leq \phi_B \leq 1.0\ \text{eV}$ was calculated for these devices from activation energy plots of $\log I/T^2$ versus $1/T$. The presence of the oxide is thought to result in an increased minority carrier injection ratio associated with the emitter. This increase was attributed mainly to the large effective barrier height and small effective area of the formed contact.

Minority carriers injected from the emitter would diffuse to and be collected by a Schottky barrier-like ($\alpha_{IC} = 1$) collector. The observed effect of contact separation on current gains obtained with type 2 devices was consistent with this model.

CHAPTER 6

ELECTRICAL TRANSPORT PROPERTIES OF THE SIS DIODE

6.1 Introduction

Although metal-insulator-semiconductor (MIS or MOS) diodes have been studied intensively in recent years, the semiconductor-insulator-semiconductor (SIS) diode has received little attention, the published work to date being mainly theoretical [14-16,69]. In the first part of this chapter a technique for manufacturing SIS devices is described and the experimentally observed admittance characteristics of these structures are presented and compared with the corresponding theory. In the second part the theoretically expected I-V characteristics of an SIS tunnel diode are discussed.

The structure of the SIS device, compared to the MIS diode, is more complicated in that two semiconductors (not necessarily the same) are utilized and the properties of these two materials can be made to differ widely by changes in conductivity-type and impurity concentration. Electrical properties of the structure are similarly more complex since they represent the combined effects of both semiconductors. A prime requisite for obtaining the combined effects is the ability of voltage applied to one semiconductor to create fields that penetrate into the second semiconductor. For this reason two MIS diodes connected in anti-series, for

example, will not have the same electrical properties as the SIS diode (unless a third terminal to bias the common field plates appropriately is introduced [70]). A somewhat analogous situation is the inability of two separate p-n junctions connected in anti-series to show the transistor action of a p-n-p junction transistor.

A typical SIS device is referred to henceforth as a p(Si)-i-n(Si) device, or, more specifically, a p(10)-i-n(10) device where n and p refer to the silicon doping type and the bracketed numbers refer to the semiconductor resistivity in ohm-cm.

6.2 Theoretical Considerations of the Admittance Properties of SIS Diodes

For an SIS device as shown in Fig. 6.1a, the application of a voltage across the device establishes accumulation or depletion-inversion space charge regions at the interior surfaces of both semiconductors. This is demonstrated for an n(Si)-i-n(Si) device in the energy band pictures in Fig. 6.1b. Because of the capacitance associated with each depletion space-charge region, two separate capacitance minima can generally be obtained in the capacitance-voltage (C-V) characteristics.

To demonstrate the features of the ideal SIS device, capacitance data for four different structures are shown in Fig. 6.2. A more comprehensive theoretical treatment of SIS devices including their corresponding conductance-voltage (G-V) characteristics is given in Ref. 18. This reference also describes the computational methods employed.

In Fig. 6.2a C-V curves for a symmetric n(5)-i-n(5) device demonstrate clearly the double minimum mentioned above. In addition, a relatively frequency independent capacitance peak centered at zero bias is obtained. For small voltages around zero bias, this frequency independence

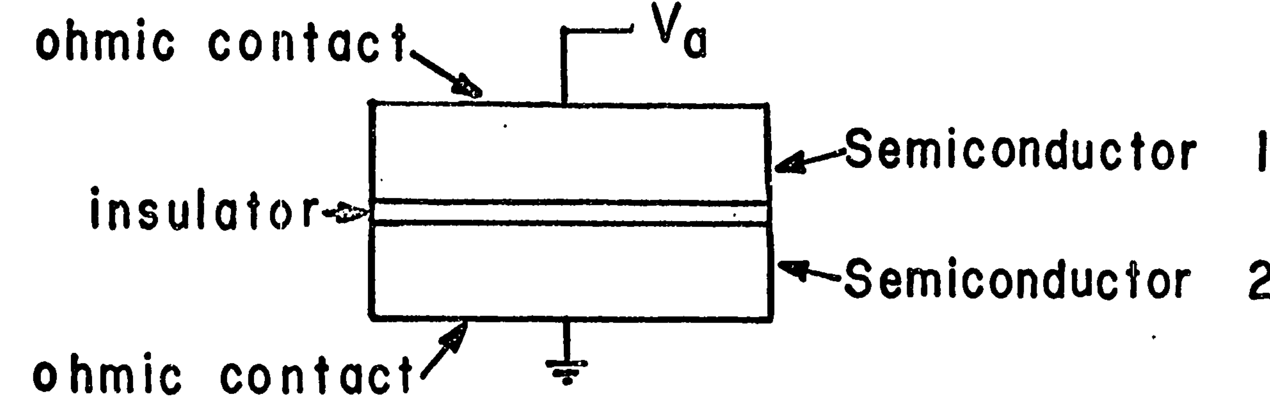


Fig. 6.1a Cross-sectional diagram of the SIS structure. In a circuit, the convention of referring to the material to which the voltage V_a is applied as semiconductor 1 is adopted

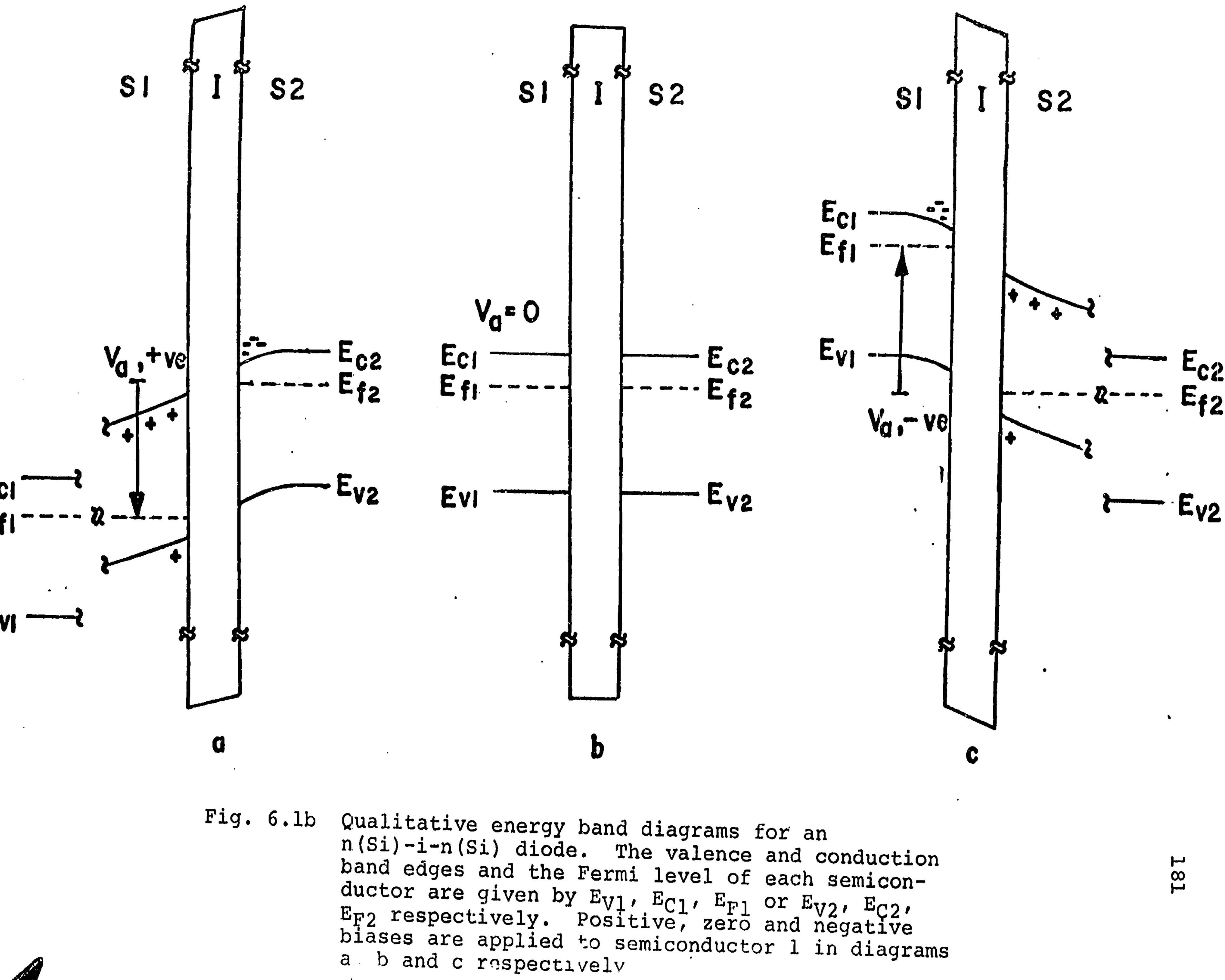


Fig. 6.1b Qualitative energy band diagrams for an n(Si)-i-n(Si) diode. The valence and conduction band edges and the Fermi level of each semiconductor are given by E_{V1}, E_{C1}, E_{F1} or E_{V2}, E_{C2}, E_{F2} respectively. Positive, zero and negative biases are applied to semiconductor 1 in diagrams a b and c respectively

Fig. 6.2 Theoretical ideal SIS C-V curves are shown as a function of frequency for four silicon devices a) n(5)-i-n(5), b) n(5)-i-n(500), c) n(5)-i-p(15) [identical doping densities of 10^{21} cu.m.] and d) n(500)-i-p(15). The oxide thickness is d_0 = 1000 Å and the corresponding value of the oxide capacitance is $C_{ox} = 3.45\times10^{-4}$ f/sq.m. The point labelled F.B. designates the voltage at which the flat band condition is reached simultaneously in both semiconductors

$C_{ox} = 3{\cdot}45 \times 10^{-4}$ f/sq.m.

n(5)-i-n(5)

ω =
0-0·1
1·0
10
≥100

1·0x C_{ox}

S2 inversion

F.B.

S1 inversion

-3 0 3

A

Voltage, Volts

n(5)-i-n(500)

ω =
0-1·0
10
100
≥1000

1·0x C_{ox}

0·5

0-0·1
1·0
10
≥100

S2 inversion

S1 inversion

F.B.

-3 0 3

B

Voltage, Volts

Figure 6.2

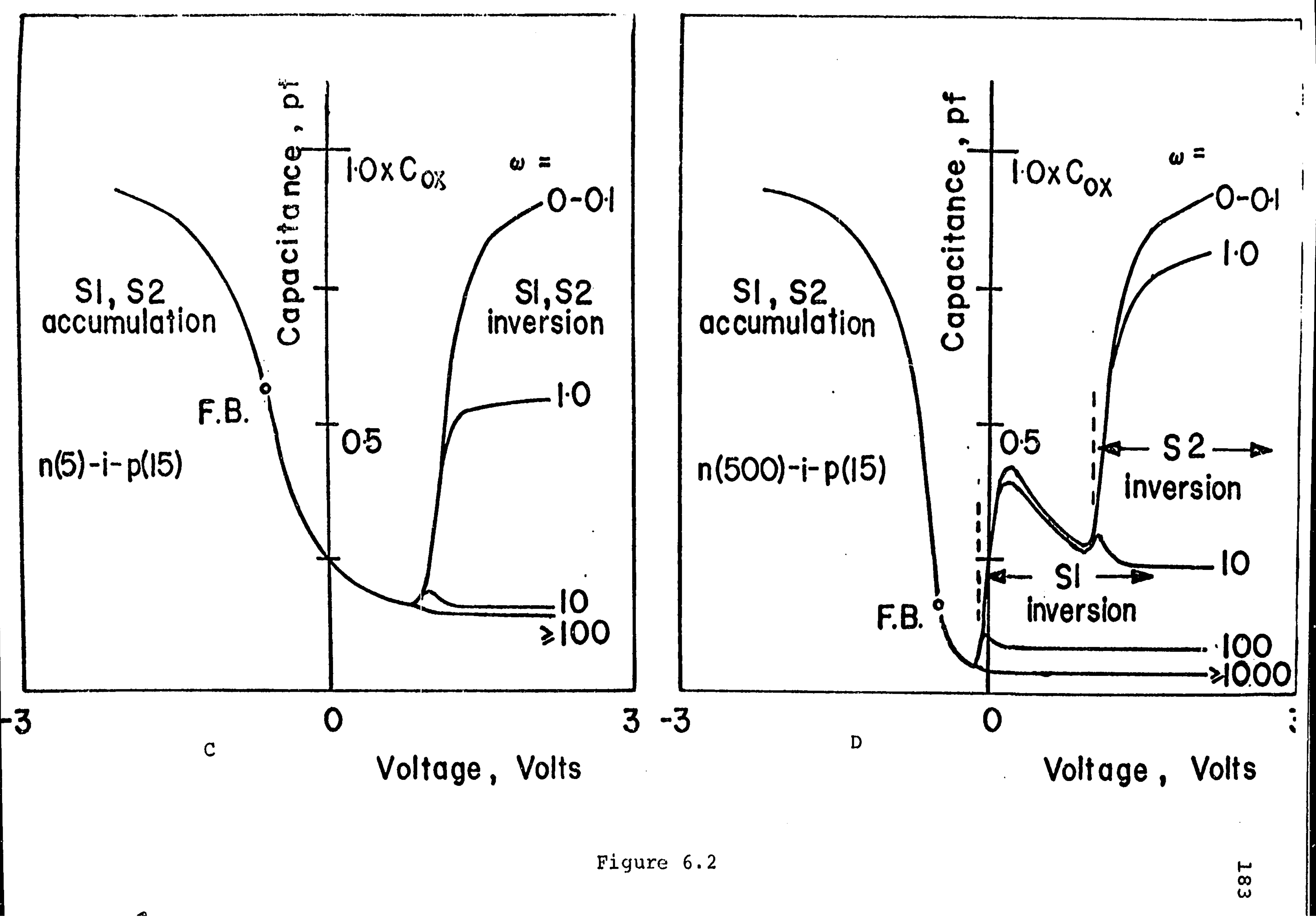


Figure 6.2

is to be expected since both semiconductors are simultaneously in depletion where frequency effects are negligible. Fig. 6.2b shows the effect of employing two n-type semiconductors having different doping densities. For this n(500)-i-n(5) device, two depletion minima can still be observed but their respective magnitudes differ considerably, reflecting the difference in doping density.

Ideal p(Si)-i-p(Si) structures with doping densities similar to those of the previous two n-type devices behave in an analogous fashion and, consequently, their C-V characteristics are not shown. Marked differences can be observed though, in the C-V curves of n(Si)-i-p(Si) structures. For example, two separate depletion minima are not obtained with an n(5)-i-p(15) device (Fig. 6.2c). This occurs when the semiconductors are of identical doping density but of opposite conductivity-type. Due to the occurance of identical depletion effects in both semiconductors at the same voltage, only one capacitance minimum is present. It is deeper and broader than would be obtained from the depletion effects of a single semiconductor. When differing dopant densities are employed in an n(Si)-i-p(Si) device, the two depletion minima appear separately as shown in Fig. 6.2d. It should be noted in this case that the central capacitance peak is dependent on frequency. Such dispersion occurs because this peak is caused, in part, by

the inversion response of one of the semiconductors. Consequently, the peak is of a distinctly different origin from the peak which is obtained in the case of the n(Si)-i-n(Si) structure in Fig. 6.2a.

The semiconductor-insulator barrier height was assumed to be identical at both interior surfaces for the calculation of the data in Fig. 6.2, a condition which is not necessarily met in experimental situations. The work function difference, ϕ_{ss}, in an "ideal" case is given by the difference in Fermi energies of the two semiconductors. Any asymmetry in the SIS structure, as caused by differences in doping density and conductivity-type, can be expected to result in a value of $\phi_{ss} \neq 0$ and, therefore, in a change in the flat band point (marked F.B. in Fig. 6.2) from zero.

Further changes in the F.B. point will result from the presence of any non-ideal influences. It is well known that surface state and oxide charge are present in a practical device [23]. The result of these effects is a lateral shift and distortion in voltage of all or part of the MOS diode's C-V curve. Similar effects will be seen in theoretical SIS C-V curves. It will also be shown that a single F.B. point can no longer be obtained, as each semiconductor reaches the flat band condition at a different value of applied bias. These biases will be indicated for semiconductors 1 and 2 by the points F.B. 1 and F.B. 2 respectively.

The effects of surface states on MOS device conductance are similarly well known [71]. Under the application of d.c. bias, the semiconductor Fermi level at the O-S interface can be swept through the energy gap of the semiconductor. The response of surface states in the midgap energy region to an a.c. signal superimposed on this bias voltage is such that a conductance peak due entirely to these states will be obtained in the G-V characteristic. With two O-S interfaces and two sets of surface states the SIS device normally shows two conductance peaks both theoretically and experimentally.

6.3 Device Fabrication

Of several methods considered for fabrication of the SIS structure depicted in Fig. 6.1a, the "contact" technique was found the most suitable for experimental purposes. In this technique two polished oxidized wafers are brought together, oxide to oxide. If these oxides are forced into intimate contact by means of pressure, SIS device characteristics can be obtained. If the insulator is reasonably thin and charge free and sufficient pressure is applied (typically 100 Kg/sq.cm.) fields applied to one wafer are able to penetrate the second wafer with sufficient strength to establish the necessary depletion and inversion layers.

The semiconductor chips employed were cut from commercially polished silicon wafers. After being cleaned, oxidized and given ohmic contacts to the back side, each chip was mounted on brass blocks that provided both electrical contact and an even distribution of uniaxial stress. The blocks were then mounted in a specially constructed pressure apparatus.

All electrical measurements on the device were carried out with an automatic plotting capacitance-conductance bridge [38] employing phase-sensitive detection to

separate in-phase and quadrature components of the signal generated by the test diode.

The value of oxide capacitance was found to vary with increasing pressure but eventually reach a limiting value. An effective insulator thickness, d_{eff}, was calculated from the observed oxide capacitance of a device, C_0, assuming the entire insulator was SiO_2. Values of d_{eff} generally were found to be two or three times greater than the sum of the individual oxide thicknesses, $d_{01} + d_{02}$, which was obtained independently after completing SIS measurements. The cause of the rather large difference between d_{eff} and $d_{01} + d_{02}$ was attributed to an interface layer of air (with relative dielectric constant of 1/4 that of SiO_2). For example, an air gap of $\sim d_{01}/2$ results in a $d_{eff} = 4d_{01}$ where $d_{01} = d_{02}$.

Two other fabrication techniques were successfully employed to construct SIS devices [17]. These were a contact fusion process in which the oxides of both wafers were fused together by a high temperature processing step, and a vacuum evaporation process involving suitable semiconductors such as CdS. Neither process proved as versatile for our purposes as the pressure contact technique.

6.4 Experimental Results and Discussion

Typical experimentally observed C-V and G-V characteristics of two different symmetric pressure contact SIS structures are presented in Figs. 6.3 and 6.4. For the n(10)-i-n(10) device in Fig. 6.3a two frequency dependent depletion minima appear on either side of a relatively frequency independent capacitance maximum centered close to zero bias. Several non-ideal features can also be noted. The height and breadth of the central capacitance maximum are greater than would be expected from theory for a silicon device of low doping density (Fig. 6.2a). This is principally due to the presence of positive charge in the oxide. This charge,when located near the interior surfaces of both semiconductors,has the effect of creating an initial positive surface band bending that represents the accumulation of majority carriers at these surfaces. Hence, the voltage at which the semiconductor reaches a flat-band condition is no longer identical to the voltage at which the second semiconductor reaches a flat-band condition. There is a resultant shift to larger absolute voltages of the positions of the two low-frequency capacitance minima. This shift has the effect of increasing the height and width of the central capacitance peak and, for large amounts of oxide charge, the

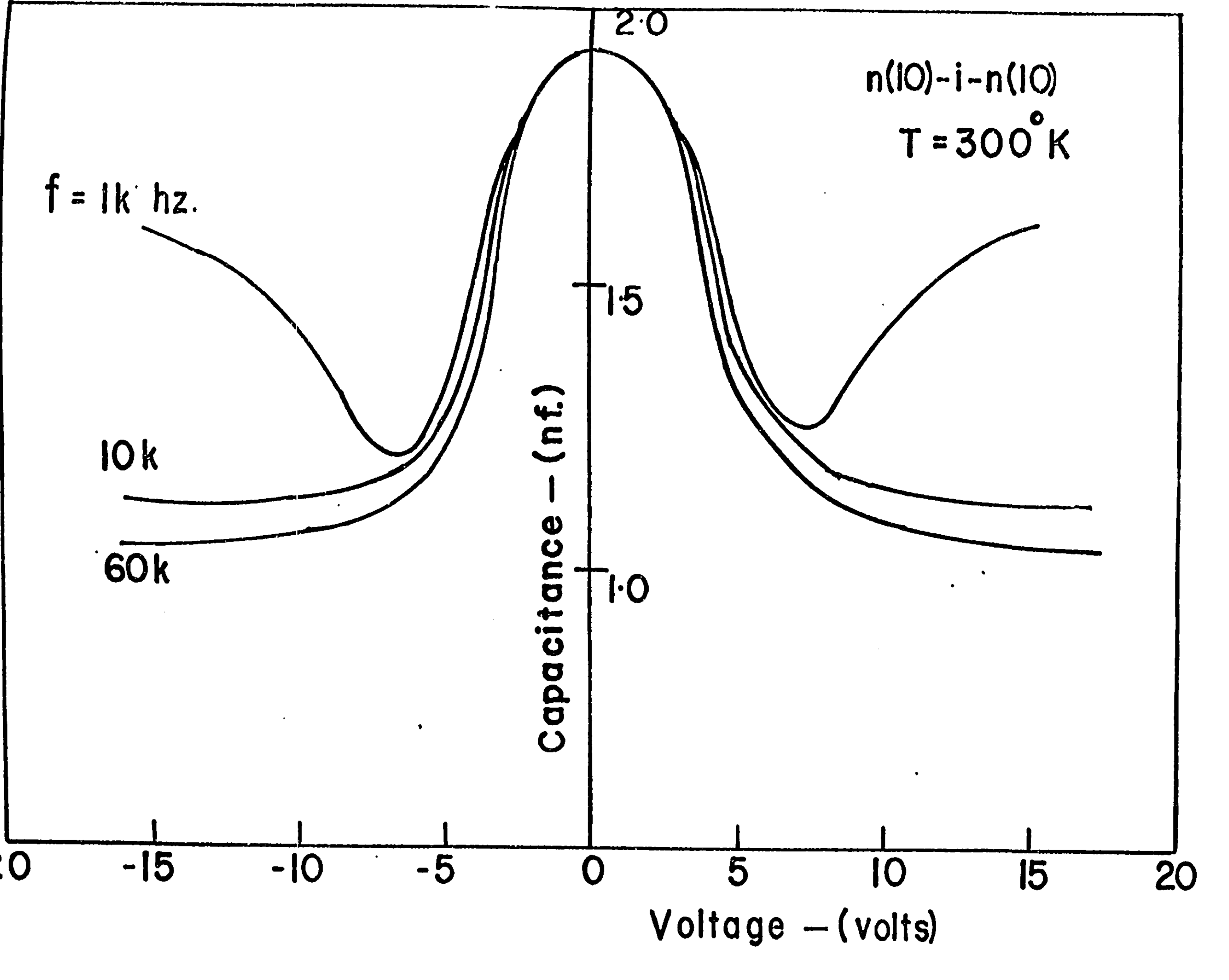


Fig. 6.3a Typical experimental C-V (5a) and G-V (5b) curves as a function of frequency for an n(10)-i-n(10) contact device under uniaxial pressure

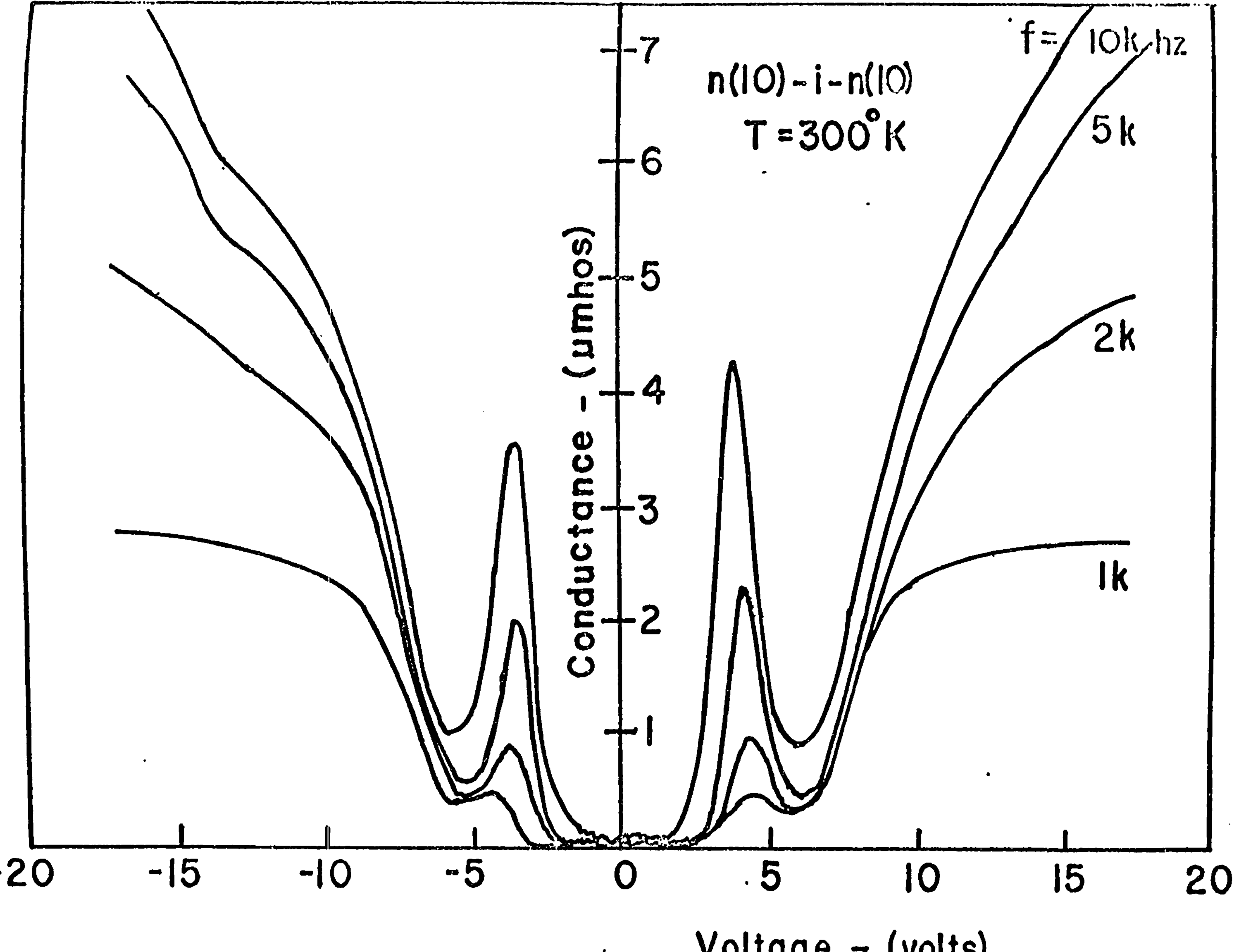


Fig. 6.3b Typical experimental C-V (5a) and G-V (5b) curves as a function of frequency for an n(10)-i-n(10) contact device under uniaxial pressure

magnitude of the capacitance peak can approach the oxide capacitance. Any small differences in the amounts of oxide charge near the two O-S interfaces can result in a shift of the capacitance peak off zero bias. This is probably the explanation for the small shift that can be observed in Fig. 6.3a.

The corresponding G-V experimental results (Fig. 6.3b) for the n(10)-i-n(10) device also show a reasonable symmetry about zero bias. In the inversion voltage regions a large conductance, relatively independent of bias (except at high frequencies), can be observed. The magnitudes of these plateaus were found to be pressure sensitive.

Surface state effects can also be seen in the C-V and G-V data in Fig. 6.3 at applied voltages $V_a \simeq \pm 4$ V. The central capacitance peak is widened by structure, appearing on either side of the peak, which represents frequency-dependent surface state capacitance. Two conductance peaks appear in the G-V data at $V_a \simeq \pm 4$ V. The magnitude and position of these peaks depend on frequency in a manner typical of conductance peaks due to surface states [71].

Another non-ideal feature that should be noted in Fig. 6.3 is the abnormally high frequency at which inversion capacitance response is obtained without illumination of the device. In the same inversion voltage region, the magnitude of the conductance plateaus is unusually large as well as

being rather more voltage dependent than expected. Results were obtained from admittance measurements on an MOS capacitor under uniaxial stress which suggests that these phenomena are related to pressure-induced bulk effects. The work of several groups [72,73] points to an explanation for such pressure effects in terms of either a pressure-induced creation of S.R.H. centers or an energy level shift of existing S.R.H. centers. The fairly substantial trap densities required theoretically to produce the observed capacitance and conductance effects lends support to the former hypothesis.

The admittance characteristics of a second symmetric SIS device, a p(10)-i-p(10) pressure contact diode, can be seen in Fig. 6.4. The radical difference between this data and that shown in Fig. 6.3 for an n(10)-i-n(10) diode can be attributed almost entirely to the presence of positive charges in the oxide. The same oxide charge condition which resulted in the broadening of the ideal capacitance peak for the n(Si)-i-n(Si) device can cause the elimination of the central peak in a p(Si)-i-p(Si) device. In place of a maximum, a capacitance minimum is observed which is due to the series combination at zero bias of two depletion capacitances and the oxide capacitance.

The 0.4 khz C-V curve seen in Fig. 6.4a contains an interesting double capacitance peak. The position in voltage

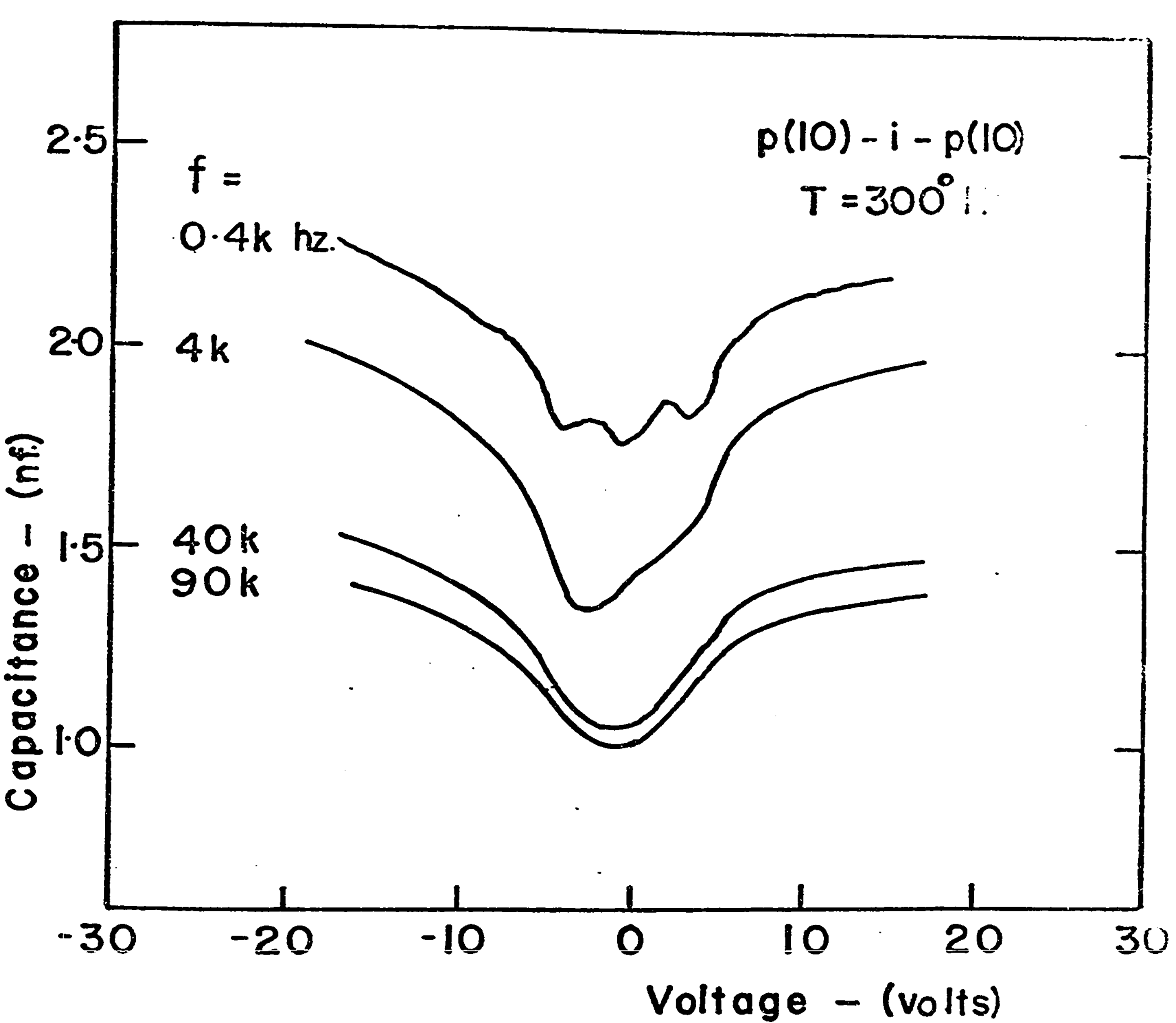


Fig. 6.4a Typical experimental C-V (6.6a) and G-V (6.6b) curves as a function of frequency for a p(10)-i-p(10) contact device under uniaxial pressure

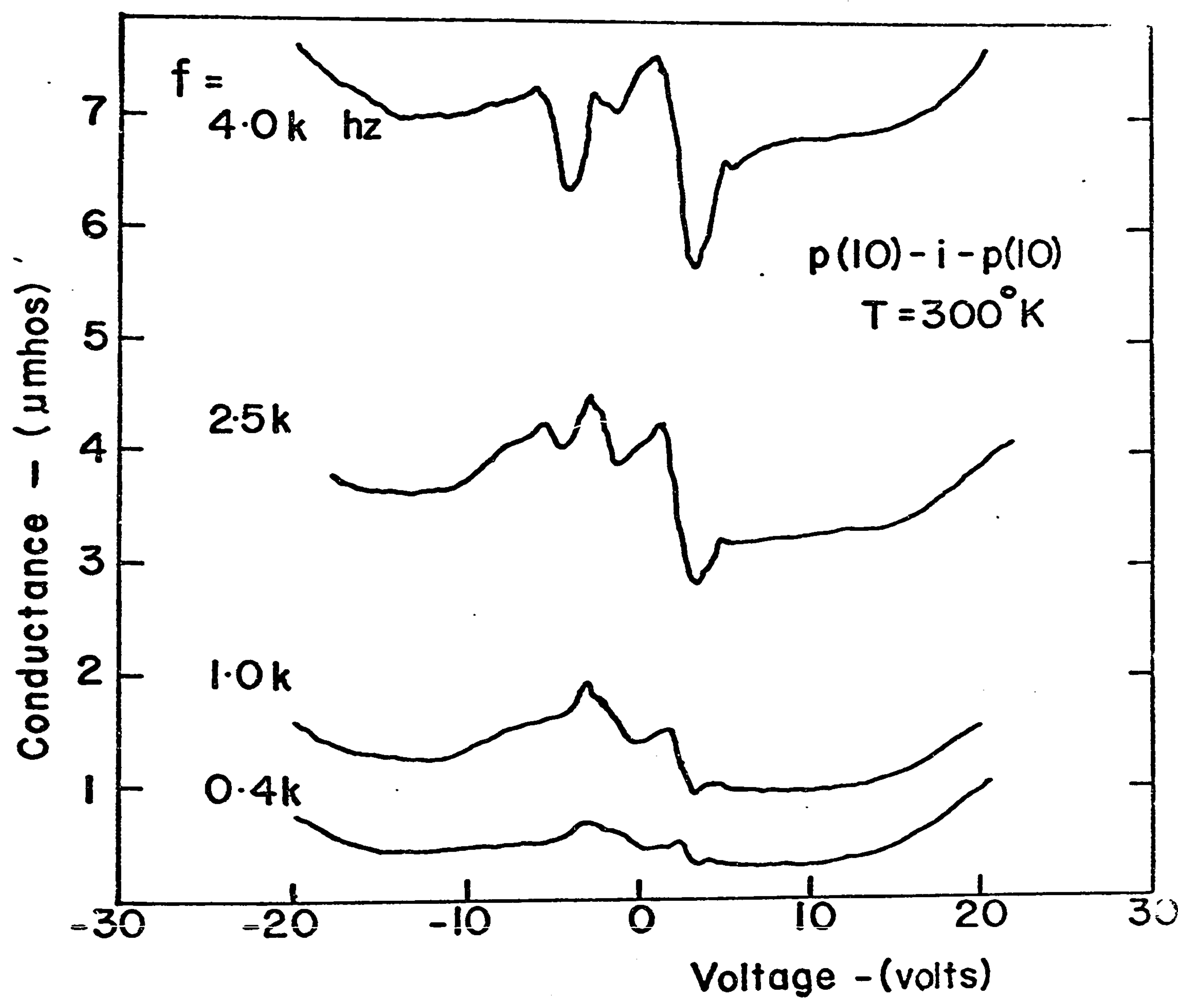


Fig. 6.4b Typical experimental C-V (6.6a) and G-V (6.6b) curves as a function of frequency for a p(10)-i-p(10) contact device under uniaxial pressure

of these smaller peaks, with respect to the walls of the capacitance minimum, makes such structure difficult to explain in terms of surface state response. A more likely cause of the structure, corroborated by theoretical calculations to be presented later, is the natural inversion response that can give rise to small capacitance peaks at voltages in the depletion-inversion regions (on either side of zero bias) at the appropriate frequency (i.e., Fig. 6.2a, ω = 10 radians/sec.). The increased minority carrier response of the stressed devices can account for the C-V structure being observable at higher values of signal frequency.

With the information gained from the C-V measurements on the p(10)-i-p(10) device, the observed G-V results for this structure (Fig. 6.4b) can be interpreted to some extent. The overall frequency dependence of the background conductance (increasing with frequency) is to be expected since at least one semiconductor is in inversion at all biases and, therefore, contributing a pressure dependent conductance. Some of the peaks closest to zero bias are probably due to a combination of the stress-induced loss in each semiconductor. Two of the remaining peaks should be due to surface states but since these peaks are obscured by the background conductance, they cannot be properly identified without resorting to a comparison with the theory.

Many of the non-ideal features discussed in the preceeding paragraphs can be simulated theoretically by employing the computational methods outlined in Ref. 18. Figure 6.5a shows theoretical results calculated for an n(10)-i-n(10) device having surface states, oxide-charge and S.R.H. centers, while Fig. 6.5b gives the admittance characteristics of a corresponding p(10)-i-p(10) device having similar non-ideal influences. The calculation parameters assumed for the n-silicon device are listed in Table 6.1. A positive oxide charge density, $N_{ox} = 1.9 \times 10^{+15}$/sq.m. at both O-S interfaces in the n(Si)-i-n(Si) device (Fig. 6.4a) broadens the central capacitance peak sufficiently to make this computation comparable with experimental data (Fig. 6.3a). The introduction of S.R.H. centers of density $N_T = 4 \times 10^{+19}$/cu.m. located at an energy near midgap and with a trap capture cross-section $\sigma = 2 \times 10^{-17}$ m^2 has significantly increased minority carrier response. "Zero" frequency C-V data can be obtained for frequencies as high as $\omega = 10^2$ radians/sec. The presence of these same recombination centers is responsible for the conductance effects observed at voltages greater than 6 volts.

In Fig. 6.5a surface states can be observed to cause frequency dependent conductance peaks and capacitance structure located at $|V_a| \sim 4$ V. In order to obtain these results,

Fig. 6.5 Theoretical C-V and G-V curves generated to show qualitatively the features in the experimental data of the n(10)-i-n(10) pressure contact device (Fig. 6.3) and the p(10)-i-p(10) pressure contact device (Fig. 6.4). FB_1 and FB_2 refer to the voltages at which flat band conditions are reached in semiconductors 1 and 2 respectively. Appropriate parameters for the calculations are listed in Table 6.1

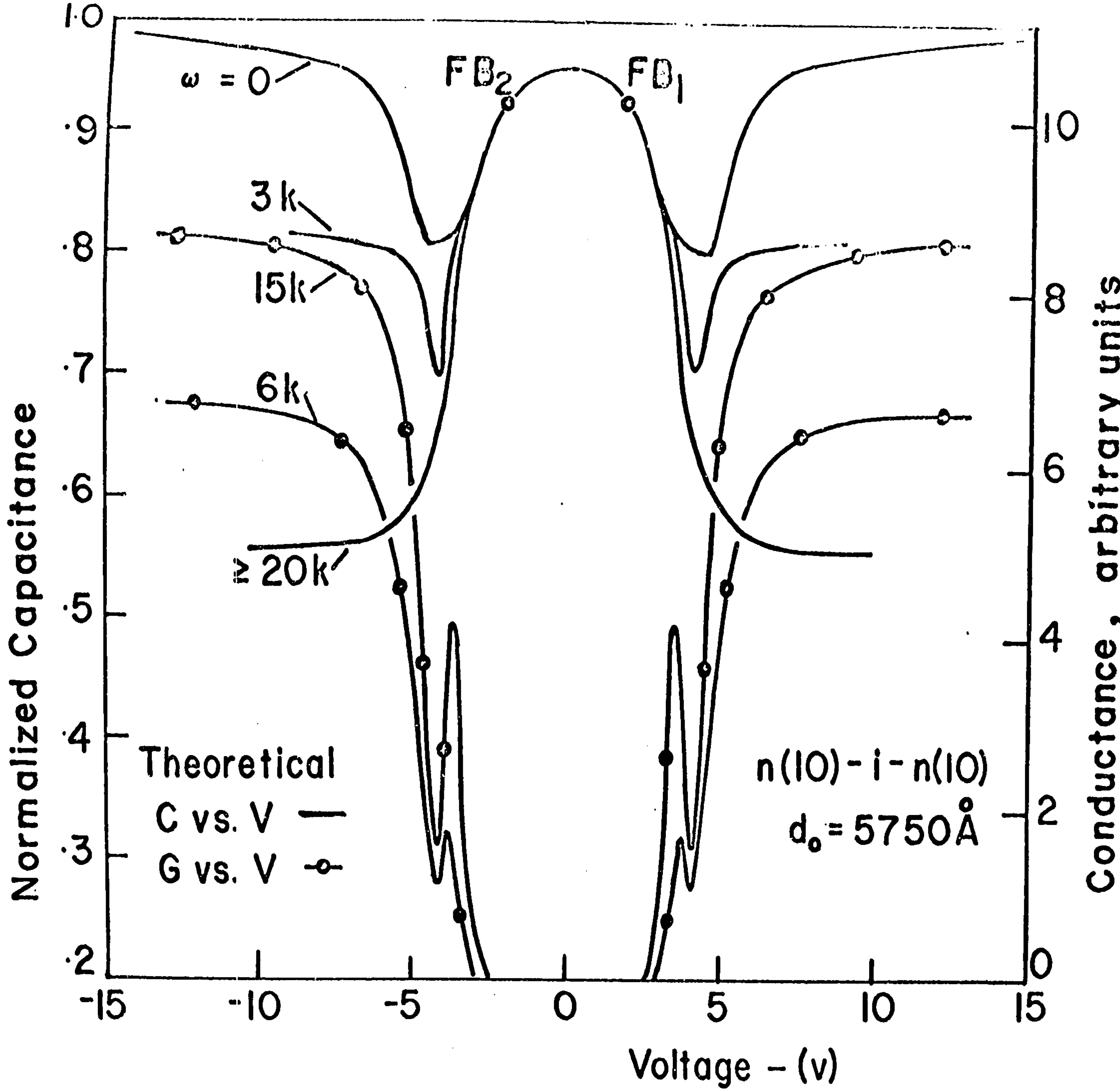


Figure 6.5

Figure 6.5

TABLE 6.1

Parameters assumed for the theory of the n(10)-i-n(10) device presented in Fig. 6.4a. Any differences from the parameters assumed for the p(10)-i-p(10) device are discussed in the text.

Parameter	Value
Electron effective mass, m_e^*	1.18
Hole effective mass, m_h^*	0.81
Electron mobility, μ_e	0.14 m^2/V-sec.
Hole mobility, μ_h	0.05 m^2/V-sec.
Surface state density at midgap, N_{ss}	1×10^{15}/sq.m./eV
Total surface state concentration, N_{sT}	1.93×10^{15}/sq.m.
Oxide charge density at each O-S interface, N_{ox}	1.9×10^{15} sq.m.
Trap density, N_T	4×10^{19}/cu.m.
Trap energy, $E_T = E_{gap}/2$	0.56 eV
Trap capture cross-section, σ	2×10^{-17} m^2
Oxide thickness, d_0	5750 Å
Temperature, T	300°K

a density of surface states $N_{ss} \sim 1 \times 10^{15}$/sq.m./eV was assumed to be present in the midgap energy region at the interior surfaces of each semiconductor.

The theoretical admittance characteristics for a p(10)-i-p(10) device with surface states, oxide-charge and S.R.H. centers are shown in Fig. 6.5b. The parameters assumed in order to calculate this data are those listed in Table 6.1 with the following exceptions. The oxide charge density was increased to $N_{ox} = 3.1 \times 10^{15}$/cu.m., the oxide thickness employed was $d_0 = 6500$ Å and the capture cross section for the S.R.H. centers was assumed to be $\sigma = 4 \times 10^{-17}$ m^2. This last assumption was made in lieu of changing the trap density, N_T, since trap density and capture cross section effects are exchangeable in a theoretical calculation. The C-V data (Fig. 6.5b) agrees qualitatively with the corresponding experimental results (Fig. 6.4a) The capacitance peaks (marked A) occurring at $|V_a| = 4$ V in the capacitance minimum (for $\omega = 3k$ radians/sec) correspond to similar peaks obtained experimentally. A relatively featureless high frequency capacitance minimum is also obtained. Theoretical conductance data, however, do not correspond to the same extent with experiment. The large theoretical surface state conductance peaks seen at $V_a = \pm 5.5$ V appear to correspond to smaller structure in the experimental data (Fig. 6.4b) at the same voltages. The

central conductance peak in the theoretical curves appears to correspond to the two 4 khz peaks at $V_a \sim 1.5$ and -2.5 V respectively. The reason for this split in the experimental conductance maximum is not known at present. The frequency dependence of the background conductance in Fig. 6.4b is greater than that predicted theoretically. It is interesting to note that in theory the rate of increase in the background conductance with frequency is quite sensitive to trap density, N_T. If the trap capture cross section is not greatly dependent on trap density, an estimate of N_T should be possible by comparing the experimentally observed rate with theory.

Surface state and pressure effects similar to those for symmetric devices, can be seen for the asymmetric n(10)-i-n(.8) diode in Fig. 6.6. The fact that the central capacitance peak is no longer centered as near to zero bias as was the peak for the symmetric n-Si device can be attributed, in part, to a work function difference, ϕ_{ss}, that should exist in this device. Such a shift of the peak towards voltages associated with the capacitance minima of the higher doped material is predicted for the ideal device [18].

The experimental measurements obtained for an n(10)-i-p(10) pressure contact device were presented in Fig. 6.7. For a device of this type in which the doping

Fig. 6.6 C-V and G-V curves as a function of frequency, observed for an n(10)-i-n(0.8) contact device under uniaxial pressure

Figure 6.6

Fig. 6.7 C-V and G-V curves as a function of frequency observed for an n(10)-i-p(10) contact device under uniaxial pressure

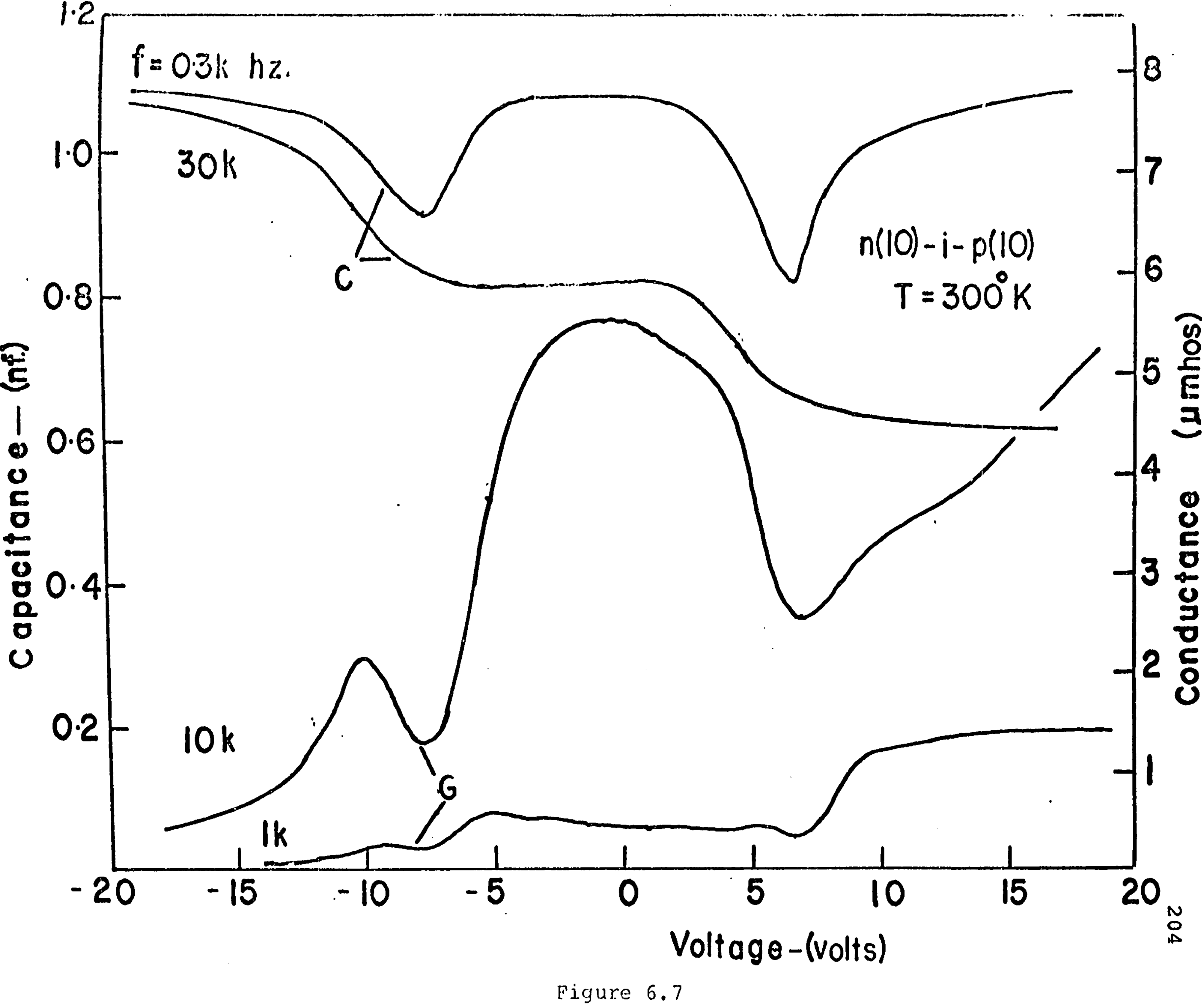


Figure 6.7

densities of the two semiconductors are of the same order, it is possible for both semiconductors to be in accumulation or depletion-inversion together. The C-V data would, therefore, be expected to show only a single capacitance minimum. The presence of oxide charge can considerably alter this picture though. The C-V data taken at a signal frequency of 30 khz indicates that the transition of the p-type material from accumulation to inversion occurs at $V_a \sim -11$ V while the n-type semiconductor does not make the same transition until a voltage $V_a \sim 5$ V is reached. The asymmetry of the above transition points, with respect to zero bias, is principally due to the combined effects of surface states and oxide charge. The low frequency capacitance peak that can now be observed at zero bias as a result of the separation of the two minima is due to the inversion capacitance response of the p-silicon.

If the above interpretation of the C-V results is correct, the conductance data in Fig. 6.7 can be more readily understood. A surface state conductance peak is visible at $V_a \simeq -10$ V and to a lesser extent at $V_a \simeq +4$ V. These peaks can be associated with the surface states at the O-S interface of the p and n-type semiconductors respectively. The stress-induced losses in the bulk semiconductors result in the other G-V features.

The varied types of capacitance behaviour that can be obtained with the different SIS devices discussed in this thesis indicate that a large variety of parametric capacitors can be created. One possible use for a voltage-symmetric capacitance has been pointed out by Schiek et al.[70]. They maintain that an "even" or symmetric C-V relation and, therefore, an "odd" charge-voltage characteristic is useful in a frequency multiplier for generating only odd harmonics of a signal frequency. This eliminates the need for proper termination of the even idler frequencies. They also considered the relative merits of two types of "even" C-V curves: the low average capacitance case and the high average capacitance case. Both types of capacitance behaviour (i.e., Fig. 6.3 and Fig. 6.4) can be realized with an SIS device.

6.5 Theoretical Tunnel I-V Characteristics of the SIS Device

A form of tunnel structure that has received little attention to-date is the SIS tunnel diode [13,14]. Interest in these diodes has been primarily due to the possibility of forming a negative resistance device suitable for circuit applications. Unfortunately fabrication techniques available to the author proved inadequate to produce such devices. A fabrication method which offers considerable promise is vacuum evaporation. This is indicated by the success of Esaki in manufacturing evaporated MIS tunnel diodes with sufficiently sophisticated evaporation techniques [74]. Certainly the evaporated diode would be far more commercially attractive than the pressure contact devices discussed in the previous sections [17]. The only drawback in such diodes would be the necessity of employing polycrystalline semiconductors, the physical properties of which are poorly characterized.

Being unable to present experimental data on the SIS tunnel structure, comments here are restricted to a review of the theoretical I-V properties of these diodes [14,33], relating these properties to those of the previously discussed MIS tunnel diode.

Since the top electrode in an SIS diode is a semiconductor, new tunnel current components must be considered. The main contributors to the total current are depicted in Fig. 6.8 in the usual fashion. Adopting a nomenclature similar to that employed earlier we define a current $J_{cc'}$ as being an electron flow from the conduction band of semiconductor 1 to the conduction band of semiconductor 2 (signified by c'). In a similar fashion the other intraband tunnel components $J_{c'c}$, $J_{vv'}$ and $J_{v'v}$ can be defined. As both electrodes now contain two separate bands, equi-energy interband transitions are also possible resulting in the currents $J_{cv'}$, $J_{v'c}$, $J_{vc'}$ and $J_{c'v}$. In place of the two surface state tunnel currents considered in the MIS diode, ten can now be defined for the SIS diode. These are given by $J_{cs'}$, $J_{vs'}$, $J_{sc'}$, $J_{ss'}$, $J_{sv'}$ and their converses.

Formulation of the current expression for the current components of an SIS diode is a fairly straightforward problem. Employing the theory set down in Chapter 2 it is only necessary to insert the appropriate definitions of semiconductor Fermi function and momentum vectors into Eq. 2.1 in place of the terms employed previously to describe the metal electrode. The limits of integration over energy are determined from a calculation of the appropriate voltage distribution.

Fig. 6.8 Energy band picture of SIS diode under positive and negative bias conditions. Various tunnel currents are defined by arrows and subscripts. For example, $J_{c'c}$ defines the current flow of electrons from the conduction band of S_2 to the conduction band of S_1

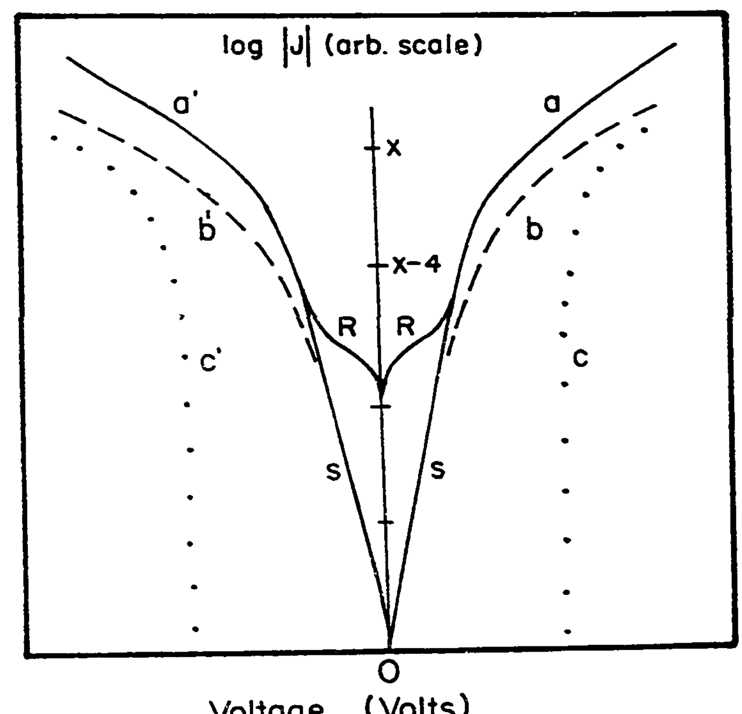
Figure 6.8

The qualitative log I-V characteristics of typical SIS diodes are shown in Fig. 6.9. Current-voltage curves for two non-degenerate silicon devices, n-i-n and p-i-n diodes, are seen in Fig. 6.9a while those of a degenerate silicon diode are presented in Fig. 6.9b.

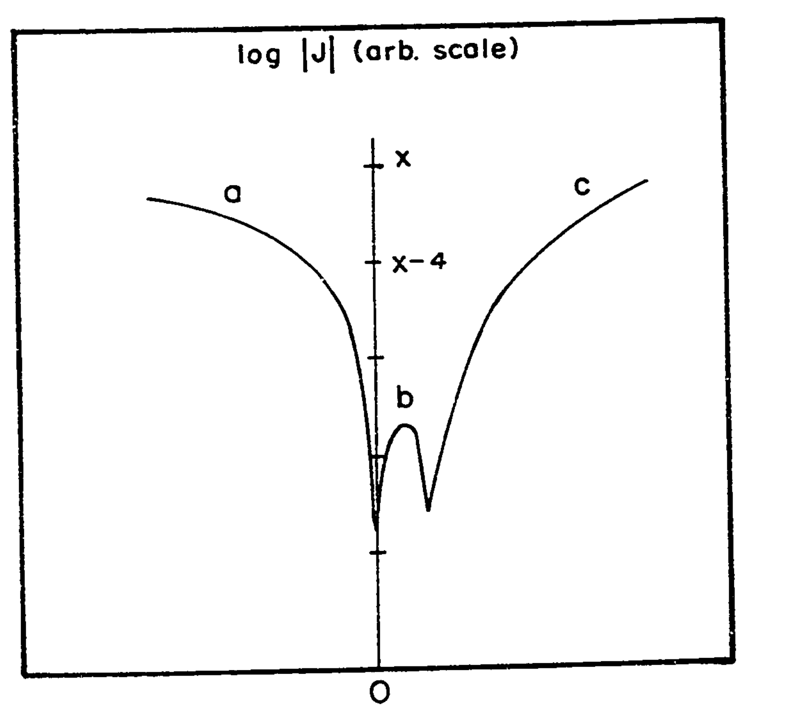
In the case of the non-degenerate diodes, the symmetry of the I-V characteristics is immediately obvious. Such symmetry could, of course, be expected for a diode employing two semiconductors of identical type. The symmetry, though, is also apparent in the I-V characteristics of the p-i-n diode as well. This is a result of the identical behaviour under applied bias of non-degenerate semiconductors with either dopant species. Such behaviour was noted in Chapter 3 where non-degenerate n-Si and p-Si MIS diodes were seen to have quite similar I-V characteristics.

Although not demonstrated, the effects of surface states and oxide charge are similar to those already demonstrated for the MIS diode. That is, these effects are limited to small biases (i.e., $-1\ V \lesssim V_a < 1\ V$), for the most part affecting only the slope and magnitude of the current voltage curves in this region [33].

Of more interest, perhaps, are the currents of SIS diodes fabricated with degenerate semiconductors, in particular, with semiconductors of opposite dopant species. A qualitative example of the I-V characteristics of such



a



b

Fig. 6.9a Qualitative log I-V characteristics of non-degenerate semiconductor n-i-n (R) and n-i-p (S) diodes. The various component currents of the total tunnel current are: $J_{c'c}$ (a), $J_{v'v}$ (b), $J_{v'c}$ (c), $J_{cc'}$ (a'), $J_{vv'}$ (b'), $J_{vc'}$ (c')

b Qualitative log I-V characteristics of degenerate semiconductor p-i-n diode showing the dominant currents $J_{cc'}$ (a), $J_{c'v}$ (b) and $J_{c'c}$ (c)

degenerate p-i-n diodes is shown in Fig. 6.9b. In such diodes the interband tunnel currents are responsible for a negative resistance characteristic at small positive biases (applied to the p-type semiconductor). As the voltage increases from zero bias, the interband current first increases then, after reaching a maximum, is cut-off as the transitions between the p-silicon valence band and the n-silicon conduction band become forbidden. This behaviour is quite analogous to that of the p-n tunnel diode [2]. Several advantages though, of the SIS diode over the p-n tunnel diode, have been proposed [14]. The insulator barrier of the former device eliminates diffusion currents. These currents are replaced by less prominant intraband tunnel currents. A second advantage proposed is the capability of a wider adjustment of negative resistance cut-off voltage in the former device over that possible in the p-n junction tunnel.

6.6 Summary

Theoretical capacitance-voltage data have been presented for the ideal SIS diode. The principal characteristic of this data is a capacitance peak centered near zero bias with a frequency dependent capacitance minimum on either side. The shape, frequency dependence, and position in voltage of the capacitance peak and minima are functions of semiconductor doping density and conductivity type.

The pressure contact fabrication technique was found adequate for the purposes of confirming the C-V behaviour of the SIS device. While minority carrier response appeared to be significantly increased by pressure effects in such structures, no distortion of the C-V data due to pressure was observable. As the application of pressure appeared to create S.R.H. recombination - generation centers which cause considerable increases in the observed conductance, the above cannot be said of the G-V curves.

Non-ideal influences such as surface states and oxide charge, inherent to some degree in any oxide-semiconductor structure,were observed in the C-V and G-V characteristics of these devices. It was found that positive oxide charge at the oxide-semiconductor interfaces of an n(Si)-i-n(Si)

device resulted in an enhancement of the central capacitance peak in height and width. A similar charge density at the oxide-semiconductor interfaces of a p(Si)-i-p(Si) device resulted in the replacement of this peak (at high frequencies) by a capacitance minimum. Generally, surface states were observed to cause two conductance peaks rather than the single peak obtained with an MOS device. Frequency dependent capacitance structure, at voltages corresponding to the conductance peak positions, could be observed in the C-V curves. When such non-ideal influences were incorporated into the SIS theory, calculated characteristics showed a reasonable qualitative fit to the experimental SIS admittance characteristics of several devices.

No experimentally determined d.c. characteristics of the SIS diode were presented. However, the general I-V features of these diodes, proposed by Temple and Shewchun [15], were discussed. As with the C-V and G-V results, the I-V characteristics of non-degenerate SIS structure exhibited a marked symmetry about zero bias. This symmetry was present even in p-i-n diodes, reflecting the similarity in I-V behaviour seen between p and n-type MIS diodes. An SIS diode can be envisaged [13,14], fabricated from degenerate semiconductors, which would exhibit a negative resistance region in its I-V characteristics. This possibility provides the main inducement to further research on this structure.

CHAPTER 7

CONCLUSIONS

In this thesis the electrical transport properties of such insulator dominated structures as the MIS and SIS diode have been investigated, both experimentally and theoretically. Of particular interest were the d.c. tunneling characteristics of these diodes.

In Chapter 2 the approximations associated with the reduction of Harrison's [10] general tunnel current expression to a numerically tractable form were discussed. Calculations of the carrier tunnel probability were performed employing both the WKB and WFM (wave function matching) approximations. Comparison of the resulting predicted I-V characteristics indicated little or no difference in relative current-voltage curve shape. This was particularly true in the case of conduction band carriers of indirect band gap materials such as silicon.

Associated with the calculation of the tunnel probability are several assumptions concerning the insulator barrier. In this work a two band insulator model was assumed employing two mass parameters, m^*_{vb} and m^*_{cb}. Variations in the magnitude and ratio of these masses were shown to have significant effects on the predicted I-V curve shapes. This fact is important since it is through

curve shape, rather than absolute current magnitudes, that the experimental I-V characteristics are analyzed.

Also studied theoretically were the effects on I-V curve shape due to variations in oxide thickness, field penetration of the electrodes and space charge tunneling; the latter providing a significant additional tunnel current only for degenerate semiconductor diodes (i.e., P_{26} diodes). Surface states were also seen to provide additional channels for tunneling. The influence of the additional tunnel current and the d.c. surface state charge on the main band tunnel currents was seen to be prominent mainly in the depletion region with $0 > V_a > -1$ V. The latter influence proved to be the dominant surface state contribution in most of the diode characteristics (with the exception of the P_{26} diode) presented in this thesis.

In Chapter 3 the fabrication of MIS tunnel diodes was considered and the methods of determining oxide thickness, d_0, discussed. It was found that d_0 provided only an upper limit for the true tunnel thickness, d_T. An estimate of d_T was determined experimentally to be given by $d_T \sim 0.7\ d_0$

Experimentally measured I-V, C-V and G-V characteristics of a range of "equilibrium" MIS tunnel diodes were presented; included were characteristics of both non-degenerate and degenerate p and n-type structures. Tunneling mechanisms in the degenerate MIS diodes were

confirmed by means of the superconducting electrode test. From a comparison with corresponding theoretical curves it was determined that the conduction band tunnel currents, J_{mc} and J_{cm}, were dominant in all but degenerate p-type diodes (with $N_A \geq 10^{26}/m^3$). In the latter type of diode it was seen that J_{vm}, a valence band current, and J_{ms}, a surface state current, dominated under positive and small negative ($0 > V_a > -1$ V) biases respectively. Good agreement between theory and experiment was obtained in most bias regions, with discrepancies appearing only in the relative magnitude of J_{mc} at large negative biases. This fit was obtained with insulator masses $m^*_{cb} = 1$ and $1 < m^*_{vb} < 2.5$.

In Chapter 4 the influence of non-equilibrium conditions in the semiconductor, on the I-V characteristics of an MIS diode, was considered. Tunnel induced minority carrier deficiencies at the semiconductor surface were seen to result in a current saturation in the I-V curves of non-degenerate diodes. In n-silicon diodes this saturation occurred (under negative bias) in the majority carrier flow J_{mc}. The magnitude of this saturation current was found to be sensitive to initial band bending conditions at the semiconductor surface. In p-silicon diodes the saturating current (under positive bias) was seen to be a minority carrier flow, J_{cm}. This current, representing a direct measure of the minority carrier supply rate, was

correspondingly smaller in magnitude and more temperature dependent than the saturating current of the n-type diode.

In general, the observation of the above non-equilibrium effects was found to be a function of oxide thickness, minority carrier supply rate and semiconductor doping density. Due to the former effect, saturating I-V characteristics were obtained, predominantly in diodes with d_0 less than a critical value (i.e., $d_0 < 30$ Å). In n-silicon diodes, from the effects on the saturating current-voltage curves of external stimuli such as light or injection from a second MIS diode, it was seen that this value of critical thickness was a function of minority carrier supply rate. In p-silicon diodes, with a minority carrier current dominating the saturation current, no "equilibrium" characteristics would be obtained were it not for an extremely large lateral minority carrier flow. Such lateral flows are typical of thermally oxidized p-silicon MIS diodes.

Semiconductor doping density increases were seen to eliminate the effects of non-equilibrium conditions on the I-V curves of the n-type MIS diode. Such an influence was interpreted to imply that the net charge density, whether from static or mobile charges, was the controlling factor in determining the extent of the non-equilibrium effects observed. On the other hand, no effect on the saturation of J_{cm} in p-type diodes from an increased semiconductor

doping density could be expected. Rather, elimination of saturation results from the relative increase and eventual dominance (i.e., for $N_A \gtrsim 10^{26}/m^3$) of the majority carrier flow, J_{vm}, with increasing doping density. Majority carrier flow in diodes with doping densities $N_A > 10^{26}/m^3$ would not saturate for reasons similar to those given above for the degenerate n-silicon diodes.

Employing a deep depletion model of tunneling, theoretical I-V characteristics were calculated which exhibited an excellent qualitative fit to experimental data. The assumption of a minority carrier density at the surface, $p_n \leq p_{nsc}$, provided the appropriate current saturation in non-degenerate diodes (n-type at least) for $p_{nsc} << N_D$. This theoretical saturation current was seen to be affected by the assumption of excess minority carrier densities in the bulk (i.e., $\phi_p - E_{FSEM} \neq 0$) in a fashion similar to the experimentally observed effects of diode illumination.

The ability to control the saturation current magnitude of non-degenerate n-silicon diodes by means of minority carrier injection suggests a new type of transistor structure is feasible, the Surface Oxide Transistor or SOT. Employing structures consisting of two formed $A\ell$-SiO_2-(n-Si) diodes in a suitable lateral geometry, two types of transistor action were observed. The first type (type 1) was characterized by common base current gains $h_{FB} > 1$ and

oxide thicknesses 20 Å < d_0 < 30 Å, while the second (type 2) was characterized by $h_{FB} \leq 1$ and $d_0 > 30$ Å. The indication that tunneling mechanisms still dominated in the currents of diodes in a type 1 transistor, permited the application of the "non-equilibrium" theory discussed in Chapter 4. Transistor gain $h_{FB} > 1$ was, therefore, attributed to a current multiplication $\alpha_{IC} > 1$ in the collector contact. A second model was proposed to explain the characteristics of type 2 transistors. This model was based on the formation of small area, Schottky barrier-like, diodes in certain regions of the contact. An effective barrier height 0.8 eV $\lesssim \phi_B \lesssim$ 1.0 eV was calculated for these devices from activation energy plots of log I/T^2 versus $1/T$. The presence of the oxide in type 2 transistors is thought to result in an increased minority carrier injection ratio associated with the emitter, due to the large effective barrier height and small effective area of the formed contact. The dependence of the common emitter gain, h_{FE}, of type 2 transistors on collector bias and contact separation was consistent with a Schottky barrier model of the diodes of this type of transistor.

In Chapter 6 methods of fabricating thick oxide SIS diodes were discussed. The experimentally observed admittance properties of these diodes were presented and compared with theory. The dominant feature of C-V curves of a symmetric SIS structure was seen to be a central capacitance peak with

a frequency dependent inversion capacitance minimum on either side. The peak was found to be sensitive to the influence of surface states and oxide charge. In particular, the presence of such charges was seen to result in an enhancement of the central capacitance peak in height and width. The presence of positive oxide charge in the insulator of a p-i-p diode was shown to result in the replacement of the central peak by a frequency dependent capacitance minimum. The predictions of the SIS theory were seen to be in good qualitative agreement with these results.

Although no experimental data concerning d.c. transport in the SIS diode was presented, the qualitative features of the expected SIS tunnel current-voltage characteristics were discussed. The major interest in such diodes is due to the feasibility of a new type of negative resistance device.

APPENDIX A

Employing a time dependent perturbation approach[10,75,76], the probability of making a transition from the state k to the state k' can be written as

$$W_{kk'} \simeq |M_{k'k}|^2 \ f(t,\omega_{k'k})/\hbar^2 \qquad \text{A.1}$$

where

$$f(t,\omega) = \left| \int_0^t e^{i\omega\tau} \, d\tau \right|^2$$

$$= 2(1 - \cos\omega t)/\omega^2 \quad . \qquad \text{A.2}$$

The function $f(t,\omega)$ is very sharply peaked about $\omega=0$ and, therefore,

$$f(t,\omega) \underset{t\to\infty}{\sim} 2\pi t\delta(\omega) \quad . \qquad \text{A.3}$$

Equation A.1 can then be written as

$$W_{kk'} = |M_{k'k}|^2 \ \frac{2\pi}{\hbar^2} \ t\delta(\omega_{k'k}) \quad . \qquad \text{A.4}$$

This result can be generalized to consider the probability of transition to a group of states of neighbouring energies. This must be done when considering transitions to a continuous spectrum of states rather than a discrete level. To accomplish the generalization it is necessary to introduce a density of states k' at energy E given by

$$\rho_{k'}(E) = n(k')\left(\frac{dE}{dk'}\right)^{-1} \qquad \text{A.5}$$

where n(k'), a normalization constant, is given by

$$n(k') = \frac{L_{k'}}{\pi}$$

and $L_{k'}$ is the length of the material in which we are considering the state k'.

To first order in the perturbation, the transition probability is then

$$W_{kk'} \simeq \int |M_{k'k}| \rho_{k'} \frac{2\pi}{\hbar^2} t\delta(\omega_{k'k}) dE$$

$$\simeq \frac{2\pi}{\hbar} |M_{k'k}|^2 \rho_{k'}(E_{k'})t \quad . \qquad \text{A.6}$$

The probability per unit time for a transition is then given by

$$p = \frac{dW_{kk'}}{dt} = \frac{2\pi}{\hbar} |M_{k'k}|^2 \rho_{k'} \quad . \qquad \text{A.7}$$

Before employing Eq. A.7, it is first necessary to consider the probability of occupation f_k, $f_{k'}$ of the states k, k'. If these states are then taken to represent the system with an electron in material 1 and 2 respectively, the probability per unit time of the electron making a transition from 1 to 2 is given by

$$P_{12} = \frac{2\pi}{\hbar} |M_{12}|^2 \rho_2 f_1(1-f_2) \quad . \qquad \text{A.8}$$

The tunnel current density resulting from such transitions is given by

$$J_{12} = 2q \sum_{k_{1T}} \sum_{k_{2T}} \int P_{12} \rho_1 dE$$

$$= \frac{4\pi q}{\hbar} \sum_{k_{1T}} \sum_{k_{2T}} \int |M_{12}|^2 \rho_1 \rho_2 \, f_1(1-f_2) dE \qquad \text{A.9}$$

where k_{1T} and k_{2T} are the transverse wavevectors in materials 1 and 2 respectively. The total transmitted current assuming $|M_{12}|^2 = |M_{21}|^2$ can be seen to be

$$J_T = J_{12} - J_{21} = \frac{4\pi q}{\hbar} \sum_{k_T} \int |M_{12}|^2 \rho_1 \rho_2 \, (f_1 - f_2) dE \qquad \text{A.10}$$

where assuming specular transmission as well, we have made $k_{1T} = k_{2T} = k_T$ (i.e., we have assumed the conservation of

transverse momentum). Substitution of an integration over transverse energy E_T for the more awkward summation over transverse wavevector gives

$$J_T = \frac{8\pi^2 qm}{\hbar^3}\int_E \int_{E_T} |M_{12}|^2 \rho_1\rho_2 (f_1-f_2)dEdE_T \qquad \text{A.11}$$

where we have used the fact that

$$\sum_{k_T} = \sum_{k_y} \sum_{k_z} = \iint dk_y dk_z$$

$$= \int_{-\infty}^{\infty} k_T dk_T \int_0^{2\pi} d\theta$$

$$= \frac{2\pi m}{\hbar^2} \int dE_T \qquad \left(\text{for } E_T = \frac{\hbar^2 k_T^2}{2m}\right) .$$

The transition probability (Eq. A.7) can be related to the more classical picture of a transmission coefficient D(E) times the frequency with which the electron strikes the oxide barrier (i.e., the velocity of the electron normal to the barrier divided by the length L of the material). One can, therefore, define

$$p = D(E_x) \frac{1}{\hbar} \frac{\partial E}{\partial k_1} \frac{1}{L_1} . \qquad \text{A.12}$$

Employing A.12 and A.7 gives

$$D(E_x) = 4\pi^2 |M_{12}|^2 \rho_1 \rho_2 \quad . \tag{A.13}$$

A simplified form of A.11 can now be written as

$$J_T = \frac{4\pi qm}{h^3} \iint [f_2 - f_1] D(E - E_T)\, dE\, dE_T \quad . \tag{A.14}$$

At this point only the transmission coefficient $D(E_x)$ need be defined and current calculations can be carried out. For this we must return to the definition of the matrix elements

$$M_{12} = \int \Psi_2^* \, V(x) \Psi_1 \, dx \quad . \tag{A.15}$$

A knowledge of the eigenfunctions Ψ_1 and Ψ_2 is necessary and can be obtained only by solving Schrodinger's equation for the heterojunction given by

$$[-h^2 \nabla^2/2m + V_p(x) + V_e(x) - E]\Psi_E(x) = 0 \tag{A.16}$$

where $V_p(x)$ and $V_e(x)$ are the periodic and electrostatic potentials respectively. Solution of such an equation is quite formidable. It is, therefore, convenient to work in the effective mass approximation [77,3] where we write

$$\Psi_E(x) = \sum_k F_n(k)\phi_{nk}(x) \qquad \text{A.17}$$

with

$$F_n(k) = \frac{1}{\sqrt{\Omega}} \int e^{ikx} F_n(x) d^3x \quad . \qquad \text{A.18}$$

$F_n(x)$ is the solution of

$$[E_n(-i\nabla) + V(x)]F_n(x) = EF_n(x) \qquad \text{A.19}$$

and $\phi_{nk}(x)$ is the solution of Eq. A.16 for the periodic potential alone. The energies E_n specify the bulk one electron energies as a function of distance in k space away from the minimum (or maximum) located at $k = k_0$ and Ω is the volume of the system. The effective mass approximation involves the use of the envelope function $F_n(x)$ in the solution of the matrix elements. This simplifies the problem considerably. Thus, assuming a quadratic expansion of the band energy as well as the most general mass in (i.e., $m = m(x)$), Eq. A.19 becomes

$$-\beta^* \frac{\hbar^2}{2m} \sum_{ij} \frac{\partial}{\partial x_i} \left(\frac{m}{\beta^* m^*(x)}\right)_{ij} \frac{\partial}{\partial x_j} \beta F + \beta(E_0 + V(x))F = E\beta F. \qquad \text{A.20}$$

The parameter β is employed to maintain continuity between the wave functions. It is generally set equal to 1. Further

simplification is possible by considering only abrupt changes in m^* at the interfaces. Therefore,

$$- \frac{\hbar^2}{2m} \nabla^2 F + [E_0(x) + V(x)]F = EF \quad . \qquad \text{A.21}$$

Solutions to Eq. A.21 can be obtained by either a WKB or WFM approximation [10]. In the former case one can write the left and right propagating waves in the barrier as

$$F_L = \frac{c_L}{\sqrt{k_b}} \exp[- \int_{x_1}^{x_2} \eta_b dx] \qquad \text{A.22}$$

$$F_R = \frac{c_R}{\sqrt{k_b}} \exp[- \int_{x_1}^{x_2} \eta_b dx] \qquad \text{A.23}$$

where η_b is the barrier propagation vector given by

$$\eta_b^2 = \frac{2m_b^*}{\hbar^2} (V(x) - E + E_T) \qquad \text{A.24}$$

and k_b is an average of this quantity given by

$$k_b = \frac{1}{x_2 - x_1} \int_{x_1}^{x_2} \eta_b dx \quad . \qquad \text{A.25}$$

The potential $V(x)$ for a one band model would be simply $\phi_{c_b}(x)$ in Fig. 2.2. Employing a more convenient form of M_{12} Eq. A.15 is given by

$$M_{LR} \equiv \frac{\hbar^2}{2m} \{F_L^* \frac{dF_R}{dx} - F_R \frac{dF_L^*}{dx}\}$$

we obtain

$$M_{LR} = \frac{\hbar^2}{m} c_L^* c_R \exp - \int_{x_1}^{x_2} \eta_b dx \qquad A.26$$

where

$$c_L = [\frac{k_{1x}}{m_1^* \, 2L_1}]^{1/2} \quad \text{and} \quad c_R = [\frac{k_{2x}}{m_2^* \, 2L_2}]^{1/2} \quad . \qquad A.27$$

Equation A.13 can now be written as

$$D(E) = \exp(-2 \int_{x_1}^{x_2} \eta_b dx) \qquad A.28$$

giving for the WKB approximation

$$J_T = \frac{4\pi qm}{h^3} \int_E \int_{E_T} (f_1 - f_2) \exp(-2 \int_{x_1}^{x_2} \eta_b dx) \, dE dE_T . \qquad A.29$$

If the wave functions are matched across the interfaces, then it can be shown that

$$D(E) = \frac{16 \frac{m_1}{k_1} (\frac{m_b}{k_b})^2 \frac{m_2}{k_2}}{\{(\frac{m_1}{k_1})^2 + (\frac{m_b}{k_b})^2\}\{(\frac{m_b}{k_b})^2 + (\frac{m_2}{k_2})^2\}} \exp(-2 \int_{x_1}^{x_2} \eta_b dx) \qquad A.30$$

where m_b is the barrier mass. In the case of a two band model of the insulator, two masses are normally used given by m^*_{cb} and m^*_{vb}. For insertion in the prefactor of the exponential in Eq. A.30 it is necessary to define an average mass given by

$$(m_b)^{1/2} = \left(\int_{x_1}^{x_2} \eta_b dx\right) / \left(\int_{x_1}^{x_2} \eta_b dx\Big|_{m_{cb} = m_{vb} = m}\right). \qquad A.31$$

The wave vector in the semiconductor (for indirect bands centered at $k = k_0$) is given by

$$k_2 = [k_0^2 + 2k_0\left(\frac{2m_s^*}{h^2}(\varepsilon - E_T)\right)^{1/2} + \frac{2m_s}{h^2}\,\varepsilon]^{1/2} \qquad A.32$$

where $\varepsilon = E - E_c$

$$k_0 = \frac{2\pi}{a}\,(0.85,0,0) \text{ for silicon}$$

Insertion of A.30 into A.14 gives the required WFM current expression which is

$$J_T = \frac{64\pi q m}{\hbar^3}\int_E \int_{E_T} \frac{(f_1 - f_2)\frac{m_1}{k_1}\left(\frac{m_b}{k_b}\right)^2 \frac{m_2}{k_2}\exp\left(-2\int_{x_1}^{x_2}\eta_b dx\right) dE\, dE_T}{\left\{\left(\frac{m_1}{k_1}\right)^2 + \left(\frac{m_b}{k_b}\right)^2\right\}\left\{\left(\frac{m_b}{k_b}\right)^2 + \left(\frac{m_2}{k_2}\right)^2\right\}}.$$

A.33

In both A.30 and A.33, one further approximation can be made without loss of accuracy. Because of the sharply peaked nature of the integrand at $E_T = 0$ in these equations, we will

assume that the prefactor can be calculated with $E_T = 0$ while the exponent of the exponential tunnel probability can be expanded about $E_T = 0$. The result of this in the general case gives

$$D(E-E_T)(f_1-f_2)dEdE_T = \left. \frac{D(E)(f_1-f_2)dE}{\int^{x_2} \frac{d\eta}{dE_T}\, dx} \right|_{E_T=0} . \quad \text{A.34}$$

APPENDIX B

Having defined the tunnel current equations in Appendix A, it remains only to specify the limits of integration, as determined by the voltage distribution, in order to perform actual calculation. The method of Temple and Shewchun [29,30], employed for the calculations of this voltage distribution, is reviewed here.

When a given static voltage is applied across the MIS diode, a portion of this voltage appears across the oxide and the remainder across the semiconductor. The corresponding charge density variations that result from the latter voltage must obey Poisson's equation for the semiconductor given by

$$\frac{d^2\psi(x)}{dx^2} = \frac{q\rho(x)}{\varepsilon_s kT} \qquad \text{B.1}$$

where $\psi(x) = -qV/kT$ is a convenient unit of band bending (i.e., electrostatic potential), ρ is the charge density, ε_s is the dielectric constant of the semiconductor and q is the electronic charge. The total charge density $\rho(x)$ can be written as

$$\rho(x) = \sum_i \rho_i + \sum_j \rho_j + \rho_{imp} \qquad \text{B.2}$$

where i sums over conduction bands (i = 1 in our calculations) and j over valence bands (also = 1 in our calculations).

In calculating $\rho(x)$, regions of exact analytic solution exist [78] that are used where appropriate. Thus in the depletion region, the charge density closely approximates the impurity dopant density

$$\rho = \rho_{imp}(x) \qquad \text{B.3}$$

and leads to the familiar quadratic dependence of ψ on x for the case of a constant density $\rho_{imp}(x)$. In regions of modest accumulation or depletion

$$\rho = c_1 \exp(c_2 (x)) \qquad \text{B.4}$$

and the closed form solutions to Poisson's equation are of the form [78]

$$\psi(x) = \frac{1}{c^2} \ln\{A^2 \operatorname{sech}^2[A(B + \sqrt{|k_1|}\, x)]\} \quad . \qquad \text{B.5}$$

In all other regions numerical solutions are obtained by approximating the charge density ρ by a staircase function. ψ is then obtained by integrating twice. The slices of different ρ are joined by assuming ψ and $d\psi/dx$ are continuous. In effect, one obtains a series of parabolas, each increasing the band bending by an amount e/RkT where R is

an arbitrarily large integer. The accuracy of the approach is controlled by R.

APPENDIX C

Employing the approach of Freeman and Dahlke [33], the expressions for surface state tunnel current can be derived in a fashion analogous to that for band currents presented in Appendix A. For a discrete surface state level a density of states can be defined such that

$$\rho_s = 2N_i \, \delta(E - E_i) \qquad \text{C.1}$$

where N_i and E_i are the density and energy of the ith state level. Furthermore c_R is now given by

$$c_R^2 = 2\eta_b\Big|_{x=x_2} \eta_{ss} \qquad \text{C.2}$$

where $\nu_b(x_2)$ is the barrier propagation constant at $x = x_2$, and η_{ss} is given by

$$\eta_{ss} = \frac{\eta_b \eta_s}{\eta_b + \eta_s} \quad . \qquad \text{C.3}$$

This quantity represents an average of η_b and a two band semiconductor propagation constant η_s given by

$$\eta_s^{-2} = \eta_{c2}^{-2} + \eta_{v2}^{-2} \qquad \text{C.4}$$

with

$$\eta_{c2}^2 = \frac{2m_{c2}}{\hbar^2}(E_{c2} - E_i) \quad \text{and} \quad \eta_{v2}^2 = \frac{2m_{v2}}{\hbar^2}(E_i - E_{v2}) . \qquad \text{C.5}$$

If a capture cross-section σ_i is introduced, the current to the ith level using a WKB approach is given by

$$J_i = \frac{4q}{\pi\hbar} \left. \frac{\sigma_i N_i (f_1 - f_i) \eta_b(x_2) \eta_{ss}(x_2) \exp(-\int \eta_b dx)}{\int \frac{d\eta_b}{dE} dx} \right|_{E_T=0} \qquad \text{C.6}$$

Apart from the more exact treatment of the denominator integral, this result is similar to the current expression of Ref. 33.

It is now a simple matter to propose a WFM current expression replacing k_2 and m_2 in Eq. A.30 by η_{ss} and m^*_{ss} where the former quantity is defined by Eqs. C.3 and C.4, while the latter is an average mass given by

$$m^*_{ss} = \left(\frac{\eta_{ss}}{\eta_{ss}\big|_{m_c=m_v=m}} \right)^2 . \qquad \text{C.7}$$

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