ULTRA-THIN SINGLE-CRYSTALLINE SILICON MEMBRANE SOLAR CELLS AS A LIGHT-TRAPPING TEST PLATFORM

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BY

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A THESIS

SUBMITTED TO THE DEPARTMENT OF ENGINEERING PHYSICS

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

Master of Applied Science (2012) McMaster University

Engineering Physics Hamilton, Ontario, Canada

TITLE: Ultra-thin single-crystalline silicon membrane solar cells as a light-trapping test platform

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Abstract

The photovoltaics (PV) research community is currently pursuing many approaches to reduce the cost of PV and increase the energy conversion efficiency. Single-crystalline silicon (sc-Si) solar cells are able to achieve high efficiency but have a higher cost relative to other technologies.

It may be possible to drastically reduce the cost of sc-Si PV by fabricating solar cells which are an order of magnitude thinner than conventional solar cells, i.e. thinner than 30 μm. Aside from new fabrication paradigms, ultra-thin sc-Si solar cells require advanced light-trapping techniques to enhance the absorption of long-wave radiation which is otherwise transmitted through the cell.

In this thesis, a novel process flow for the fabrication of ultra-thin sc-Si solar cells in the laboratory was designed and implemented with the aim of testing light-trapping structures in the context of actual ultra-thin sc-Si devices. The process flow uses 10 μm thick sc-Si membranes, 0.95 cm in diameter, fabricated on silicon-on-insulator wafers using double-sided processing.

The best fabricated device incorporated a back surface field, a white paint diffuse rear reflector and a silicon nitride antireflection coating. It achieved a fill factor, efficiency, short circuit current and open circuit voltage of 0.67, 9.9%, 27.9 mA cm^{-2} and 0.53 V respectively. Simulations suggest the device efficiency can approach 15.4%

without light-trapping and 16.5% with a diffuse rear reflector as a light trapping structure.

This process flow is intended to be used as a platform on which to test further light-trapping structures with the continuation of this project.

Acknowledgements

I would like to extend my thanks to the following: Rafael Kleiman for his guidance on this project and for allowing me the freedom to pursue my own ideas; The NSERC Photovoltaic Innovation Network for funding this work; Fellow members of the Kleiman group for their insights and suggestions at our weekly meetings; Clea Berwick for his help in designing the etching apparatus; Jacek Wojcik for ellipsometer and tube furnace training; Shahram Tavakoli for helping me get the tube furnace back online; Zhilin Peng for numerous training sessions; Doris Stevanovic for training; Dixon Paez and Edgar Huante-Ceron for their help with solar simulator measurements; Josh Rideout and Martin Gerber for their help with EQE measurements; and Justin Sacks for help with reflectance measurements.

Notation and abbreviations

J_{SC}	Short circuit current density
V_{OC}	Open circuit voltage
J_{MPP}	Current density at maximum power point
V_{MPP}	Voltage at maximum power point
η	Efficiency
FF	Fill factor
J_0	Dark saturation current density
n	Diode ideality factor *or* refractive index
J_L	Illuminated diode photocurrent density
R_S	Series resistance
R_{SH}	Shunt resistance
θ	Angle of incidence
MPP	Maximum power point
SOI	Silicon-on-insulator
SOM	Silicon-on-metal
PSI	Porous silicon process
BSR	Back surface reflector
PDR	Pigmented diffuse reflector
sc-Si	Single-crystalline silicon
c-Si	Crystalline silicon
a-Si:H	Hydrogenated amorphous silicon
poly-c-Si	Polycrystalline silicon
CZ	Czochralski
FZ	Float zone
ARC	Antireflection coating
TIR	Total internal reflection
SRV	Surface recombination velocity

RIE	Reactive ion etching
DBR	Distributed Bragg reflector
KOH	Potassium hydroxide

Contents

Chapter 1

Introduction

1.1 Introductory remarks

The broad aim of the photovoltaics (PV) research community is to facilitate the widespread adoption of solar photovoltaics as an energy generation technology. Presently, the main barrier to achieving this aim is the relatively higher cost per unit energy of PV when compared with other energy resources, such as fossil fuels.[1] A key role of scientists and engineers in surmounting this barrier is to develop solar photovoltaic technologies that are not only lower in cost but also highly efficient.

It should be stressed that this really is a dual-requirement, low-cost *and* high-efficiency. This is because a solar cell is only one component in a solar installation and, although a solar cell may be inexpensive, the cost of other components indirectly depend on the efficiency, mainly by way of the need for greater solar module area to produce an equivalent power. Consequently, for inefficient solar cell technologies

[1] It should be noted that there are a number of ancillary costs associated with our fossil fuel dependency that would not show up on an energy bill.

there is increased cost for module materials, mechanical racking, land-use, labour, processing and shipping. Costs saved at the cell-level are likely result in increased expenses at the module and system level.

Of the inorganic technologies, crystalline silicon (c-Si) is an ideal solar cell material in many ways. Silicon is the second most abundant material on the planet and can be found virtually everywhere. Its bandgap is not far from the optimum value and is therefore capable of achieving a high efficiency. Its electrical properties are good. Importantly, there already exists decades of Si processing experience from the microelectronics industry. As a result, c-Si is by far the dominant solar cell material on the market today and will most likely continue to be in the foreseeable future. However, c-Si PV, single-crystalline Si (sc-Si) specifically, is not currently considered to be a low-cost technology.

The relatively high-cost of sc-Si solar cells comes from the energy-intensive processing which takes sand and turns it into high-purity semiconductor grade silicon ingot. This ingot can then be cast, as is the case with polycrystalline silicon (poly-c-Si), or used to grow a single-crystalline silicon (sc-Si) boule through either Czochralski (CZ) or float zone (FZ) methods. It follows that it may be possible to reduce the cost of sc-Si PV simply by using less material during fabrication. The obvious way to do that is by making thinner solar cells.

There already exists a strong movement towards thinner c-Si solar cells in industry for this reason. Improved sawing methods have been developed not only to reduce the amount of wasted silicon during wafer sawing, called kerf losses, but also to make wafers thinner. However, there exists a trade-off. Thinner wafers are more susceptible to breakage and therefore the cost saved by using less material must be

balanced against cost incurred by wafer breakage during processing. Furthermore, there exists a real physical limit to how thin one can saw a wafer. It seems that a factor of two thickness reduction from the conventional 300 μm is achievable.

Over the past 15 years researchers have also been investigating an alternative approach: ultra-thin sc-Si solar cells which are more than an order of magnitude thinner (< 30 μm) than is conventional. This area shows much promise as ultra-thin sc-Si cells have already achieved efficiencies as high as 15.4% [1] with only the standard commercial features. Theoretical studies suggest efficiencies higher than 20% for devices as thin as 10 μm [2]. Moreover, new fabrication paradigms for fabricating these cells have already been demonstrated at both the lab and pilot production line level.[2] Full-scale commercial deployment does not yet seem to be a reality, at least partly because the ultra-thin sc-Si PV cell efficiencies are still low when compared to their conventional counterparts.

The decreased efficiency of ultra-thin sc-Si cells is a consequence of silicon's indirect bandgap which makes it a poor absorber of light. Some of the long wavelength solar radiation would not be absorbed by an ultra-thin cell and this would give rise to a lower photocurrent. This is shown in Figure 1.1 which plots the reflectance, transmittance and absorbance of a 10 μm layer of sc-Si. Calculations were done according to [3].

The situation is not as drastic as one might imagine. Figure 1.2 shows the normalized photon absorption (α_n) as a function of thickness referenced to the AM1.5 spectrum. The normalized photon absorption is defined here as the number of photons absorbed by a given thickness of bulk silicon (including front and rear surface

[2]Notable commercial players in ultra-thin sc-Si fabrication are AstroWatt (Austin, TX), Silicon Genesis (San Jose, CA) and Twin Creeks Technologies (San Jose, CA).

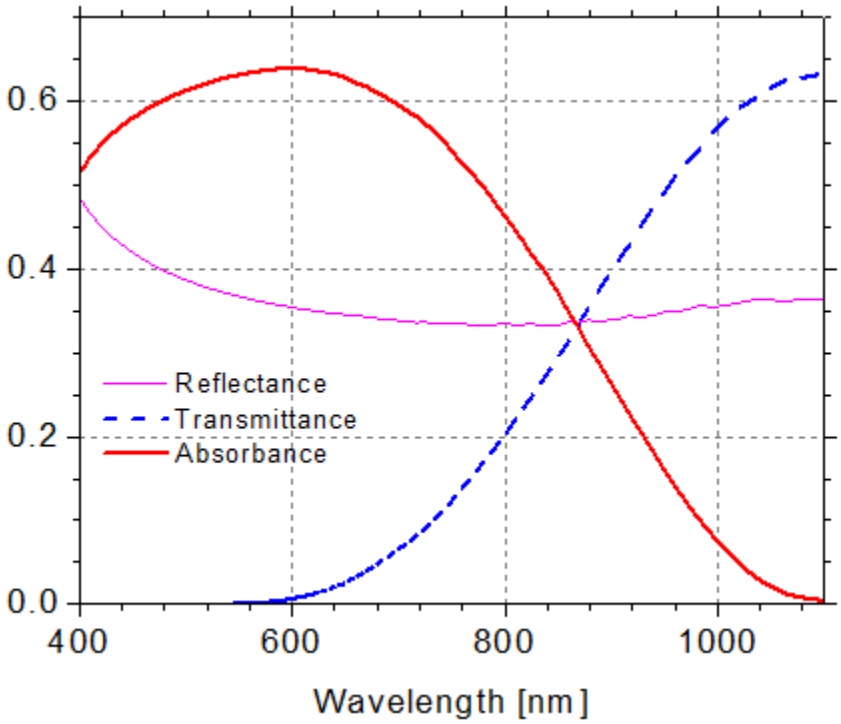


Figure 1.1: Reflectance, transmittance and absorbance are plotted for a 10 μm layer of sc-Si. Interference fringes have been removed with a simple averaging algorithm for the sake of clarity. Above 600 nm, an increasing percentage of light transmits through the sc-Si.

reflections) over the total number of photons which have an energy above the silicon bandgap. This is normalized to remove reflectance losses such that infinite thickness has an absorption of 1.

It is possible to recover some of those long-wave photons, and thereby increase efficiency, by making use of advanced light-trapping features. With light-trapping, the absorption of light inside a semiconductor can be enhanced by a up to factor of $4n^2$ [5], where n is the refractive index of the semiconductor. This means that a solar cell which is physically thin can behave optically as if it were much thicker. As will

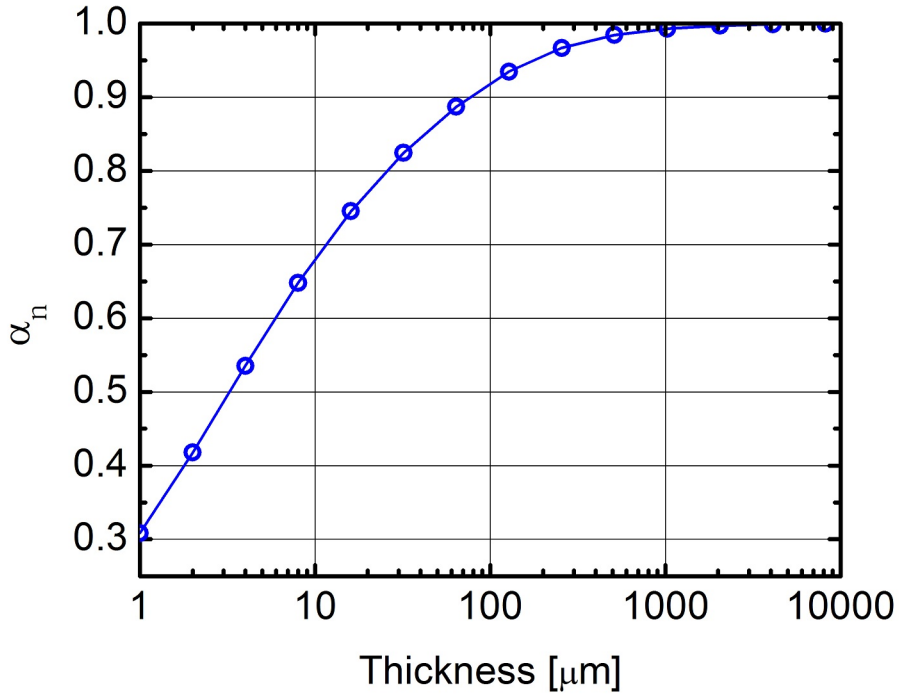


Figure 1.2: The normalized absorption of 10 μm thick sc-Si is approximately 68% of the infinite thickness limit while that of 300 μm thick sc-Si is approximately 97%. Despite a 30× reduction in thickness, the 10 μm thick sc-Si absorbs approximately 2/3 the amount of light as 300 μm thick sc-Si [4].

be discussed later on in this document, there are a variety of ways in which light-trapping can be implemented in PV device. The relevant point for this work is that there is much experimental work still to do in terms of implementing light-trapping, specifically in the context of actual ultra-thin sc-Si devices.

1.2 Aim

The aim of this thesis was to design and implement a laboratory process flow capable of fabricating 10 μm thick ultra-thin sc-Si solar cells. The solar cells fabricated using

this process flow could then be used as a platform on which to investigate light-trapping structures in the context of actual solar cell devices both in this thesis and in the continuation of this project.

The process flow developed in this thesis is novel. Solar cells were fabricated using an ultra-thin 10 μm thick sc-Si membrane created from a silicon-on-insulator (SOI) wafer and shown schematically in Figure 1.3. Note that the solar cell in Figure 1.3 has both an antireflection coating (ARC) and back-surface field (BSF). The main benefit of the ultra-thin membrane approach is that it allows high temperature dual-side processing. This allows for a wider variety of light-trapping architectures and other high-performance coatings, crucial for optimal device performance. Essentially, the processing issues associated with fabricating ultra-thin sc-Si are decoupled from the study of light trapping because using the ultra-thin membrane approach allows conventional solar cell processing techniques.

The solar cells fabricated using this process flow should be a good platform on which to investigate light-trapping in ultra-thin sc-Si solar cells. In total, four devices were fabricated, each with an improved performance to the prior device. A diffusely reflecting white paint rear reflector was investigated in this work as a light-trapping structure on the rear of a membrane solar cell.

1.3 Overview of thesis document

Chapter 2 will provide background information regarding light-trapping concepts. The background information in this chapter is rather thorough because an adequate review could not be found anywhere else. For the reader familiar with light-trapping, this section could be skipped without much loss of content. Chapter 3 will look

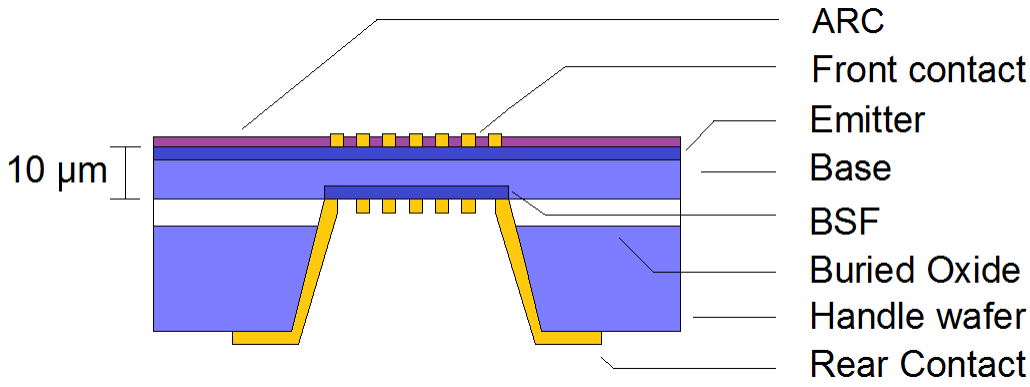


Figure 1.3: Cross-section of ultra-thin sc-Si membrane solar cell fabricated in this thesis. Rear-reflector is not shown.

specifically at ultra-thin sc-Si solar cells that have been fabricated in the literature.

To fabricate the ultra-thin sc-Si cells used in this study a variety of experimental methods were used, including: potassium hydroxide (KOH) etching, sputter deposition, electron beam deposition, RTA and tube furnace annealing, wet thermal oxide growth, RCA cleaning, ellipsometry and ion-implantation. Custom parts were also fabricated. Information on solar cell processing and relevant experimental techniques can be found in Chapter 4.

The solar cells were characterized with EQE measurements and J-V curve measurements. An overview of these set-ups and also of data analysis is presented in Chapter 5. Chapter 6 presents the experimental data and Chapter 7 provides a discussion of those results. The document concludes with Chapter 8.

Chapter 2

Background I:

Light-trapping

As stated in Chapter 1, the main technical issue associated with ultra-thin sc-Si solar cells is that sc-Si is not a strong absorber of light due to its indirect bandgap. Figure 1.2 showed that at a thickness of 10 μm about 68% of available photons are absorbed, compared to 97% at 300 μm neglecting reflectance in both cases.

The difference in absorption between a conventional and ultra-thin cell can be easily seen in external quantum efficiency (EQE) plots. Figure 2.1 shows the EQE plots for the passivated emitter and rear with locally diffused contacts (PERL) cell[1] compared to that of a 6 μm ultra-thin cell. It is clear that the absorption of the longer-wave photons is affected. Light-trapping can be utilized to enhance absorption and improve the long-wavelength EQE.

The aim of light-trapping is to enhance the optical path length of light inside a solar cell such that the cell absorbs light as if it were physically thicker. It is based on

[1]This is the most efficient single-junction Si solar cell.

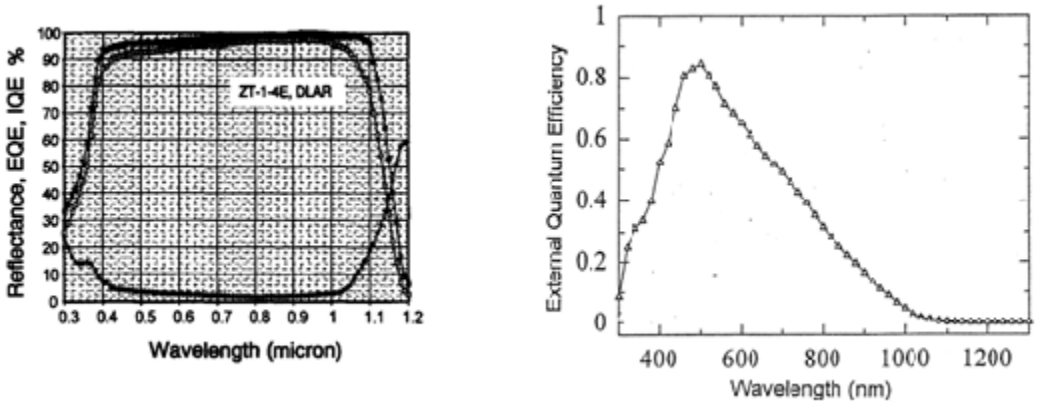


Figure 2.1: The EQE of an ultra-thin cell (right) [6] without light-trapping shows a poorer long-wave response than a cell of conventional thickness (left) [7].

three operating principles: (i) rear surface reflection, (ii) angular incoupling of light and (iii) total internal reflection.

Rear surface reflection forces outgoing photons back into the solar cell, at least doubling the optical path length. Light which travels through the solar cell at an angle must necessarily travel a larger distance than if it were travelling normal to the surface. This increases optical path length but also enhances reflection at the front or rear surfaces. If light is incoupled into the cell at an angle and also, reflected at the rear, then it may undergo total internal reflection at the front surface and be effectively "trapped" inside the cell.

This chapter will look at each of the principles of light-trapping in greater detail. Figure 2.2 shows a chart organizing what is discussed in this section. There are several important distinctions and it may be helpful to refer back to this figure when reading through each section.

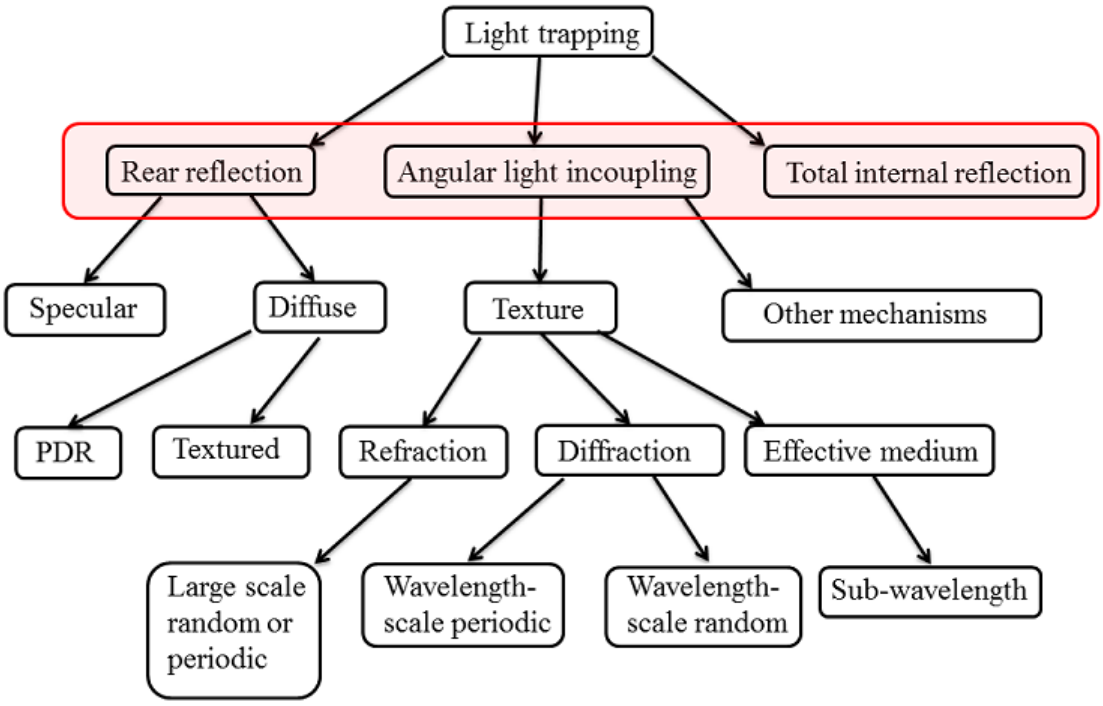


Figure 2.2: Light trapping is based on three principles: (i) rear reflection, (ii) angular incoupling of light and (iii) total internal reflection. Rear reflectors can be specular or diffuse. Diffuse reflectors can be pigmented (PDR) or textured. It is possible to incouple light angularly by using texture. Texture operates on the principles of refraction or diffraction. Large-scale texture is based on refraction. Wavelength-scale texture is based on diffraction. Sub-wavelength-scale texture is an effective medium. Total internal reflection can occur at the front surface to further enhance optical path length.

2.1 Rear reflector

The usefulness of a rear reflector is conceptually straightforward. It is a means of keeping light in the cell which would have otherwise been transmitted right through. At the bare minimum, it would double the optical path length for those photons which undergo reflection. Rear-reflectors can be classified as being specular or diffuse.

Specular reflectors reflect light such that the incident angle of light is equal to the reflected angle. Under normal solar cell test conditions light is parallel to the surface normal. A specular reflector would reflect light back into the cell such that it is also parallel to the surface normal. Examples of specular reflectors are dielectric materials and metallic materials. Metallic reflectors are somewhat lossy and dielectric reflectors have a wavelength dependence resulting from the wavelength-dependent refractive index.

Diffuse reflectors reflect light over a distribution of angles, or at least at a non-specular angle, rather than just at the angle of incidence. Diffuse reflectors may not do this perfectly and some specular reflection may still be present. Examples of diffuse reflectors are pigmented reflectors and textured reflectors. A pigmented diffuse reflector (PDR) approaches the Lambertian ideal (i.e. equal radiation intensity in all directions) and it is simple as a layer of white paint. The pigment molecules in the paint absorb light and then re-radiate it in all directions.

Various types of surface textures have been developed and they will be further discussed in the sections to come. Surface texture is normally applied to the front of the cell but can be applied to the rear as well. In this case, rather than transmitting light into the cell at an angle, as it would do at the front surface, it reflects light back into the cell an angle. In the latter case, light-trapping principles (i) & (ii) are accomplished in the same step. An important consideration here is that front surface texture can also reduce front surface reflection but the rear surface texture can not.

2.2 Angular incoupling of light

Angular incoupling of light is normally accomplished by texturing the front surface but texture actually serves three purposes that benefit the solar cell. Firstly, texture forces light to be transmitted through the cell at non-normal angles and this means it must travel a larger distance to reach the rear of the cell. This increases optical path length. Secondly, a larger angle of transmission increases reflection at the rear surface and can increase the total internal reflection effect. Lastly, texture can reduce the front surface reflection of incident light.

To understand how a texture is able to incouple light at angle into a solar cell it is necessary to make two distinctions. The first distinction regards whether the texture is random or periodic texture. Random texture has no periodicity to it and one would see a distribution of feature sizes, positions and perhaps shapes. Periodic texture has periodically occurring features of uniform size and shape. The two different types of texture are shown in Figure 2.3.

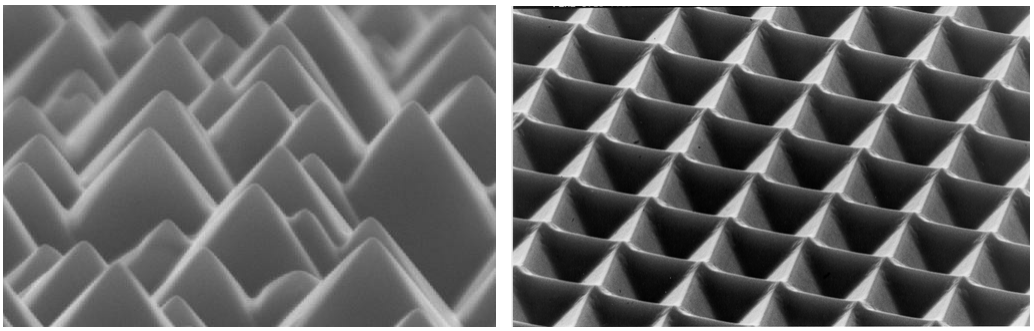


Figure 2.3: Large scale random upright pyramidal textured achieved by alkaline etching (left). Large scale inverted pyramidal texture obtained using photolithography (right). Both images are from [8].

The second distinction regards the scale of the texture when compared to the wavelength of visible light. A random pyramidal texture with feature heights greater

than ∼1-2 microns would be considered large. A random texture composed of features which have heights and widths on the order of several hundreds of nanometers or near a micron would be considered wavelength-scale. Textures with feature sizes much smaller than the wavelength of light, called sub-wavelength texture, would be considered very small.

For large-scale textures that are random or periodic one thinks of the angular incoupling of light in terms of refraction. For small-scale periodic or non-periodic textures one thinks of it in terms of diffraction. When the texture size gets much smaller than the wavelength of light, the texture can be modelled as an effective medium with a refractive index gradient. Sub-wavelength textures can be good antireflection coatings (ARCs) but will not incouple light into the solar cell at an angle and therefore not be a good-light trapping structure.

2.2.1 Large scale random or periodic texture

For large scale random or periodic texture, like the textures shown in Figure 2.3, the incoupling of light at large angles is based on refraction. Light is thought of as a ray and its behaviour at an interface is described by Snell's Law, shown in Equation 2.1.

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 \tag{2.1}$$

The process is shown in Figure 2.4. When a large-scale pyramidal texture is added to the front surface of a silicon solar cell, the ray may appear to be normally incident on the surface to the naked eye but it is actually not because there is local variation in the orientation of the surface caused by the texture. The ray then has some non-normal angle of incidence at the surface and it will be refracted into the silicon due

to the difference in refractive index between Si and the medium from which the light was incident according to Snell's law. The result is that the light ray is transmitted into the silicon at an angle.

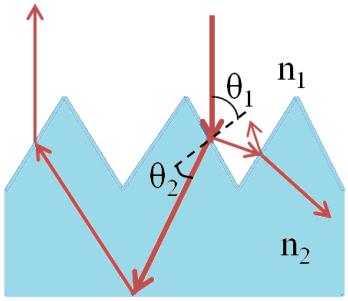


Figure 2.4: The incident light is refracted as it is transmitted into the solar cell. That light can then reflect from the rear. If the light is poorly absorbed it will reach the front surface again where some is reflected and some is transmitted back out of the cell. The original incident light that is reflected at the front surface texture will hit an adjacent pyramid and have a second chance at being absorbed. This is called the double-bounce effect.

Some of the light hitting the texture will also be reflected. The angle of reflection will equal the angle of incidence. The percentage of light reflected is governed by the Fresnel equations. However, this reflected ray is not lost. It will hit another pyramid and receive a second opportunity to be transmitted into the cell. The amount of light reflected from the first pyramid will actually by greater than that reflected by a flat interface but the effect of this so-called "double-bounce" is to reduce the overall reflection from the surface.

2.2.2 Wavelength-scale periodic texture

For large scale random and periodic textures, the incoupling of light at oblique angles is based on Snell's Law. The approximation of light as a ray is only valid when the

texture feature size is large compared to the wavelength of propagating light. As the feature size gets smaller, this approximation is no longer valid and the wave nature of light becomes most important. One of the important consequences of the wave nature of light is the phenomenon of diffraction. It is through diffraction that wavelength scale periodic textures can incouple light obliquely into well defined modes. Example 1-D and 2-D wavelength-scale textures are shown in Figure 2.5.

Figure 2.5: A 1-D rectangular diffraction grating (left), a triangular grating (centre) and a 2-D honeycomb grating (right) [9].

The diffraction of light through a periodic grating on the surface of a solar cell is a complex problem. Maxwell's equations must be solved with the boundary condition of the surface texture profile. This is generally done in two dimensions. Several papers have conducted these studies [10–14]. It is more useful for the purposes of this thesis to explain the physics of light incoupling through diffraction gratings in a simpler more qualitative manner.

Towards this end, consider an idealized diffraction grating placed at an interface of air and silicon. This is shown in Figure 2.6. Light is incident from the air, some transmits through the silicon and some is reflected from the grating back into the air. If the grating period is a suitable value then the light will be reflected and transmitted into mathematically well-defined diffraction modes.

For normally incident light, the equation for the angles of the various diffraction modes of the transmitted light is shown in Equation 2.2 and that for reflected light is Equation 2.3 (both equations from [15]). These equations will only indicate the angle of the diffraction mode and not the intensity. For that quantity, a more rigorous calculation procedure is necessary.

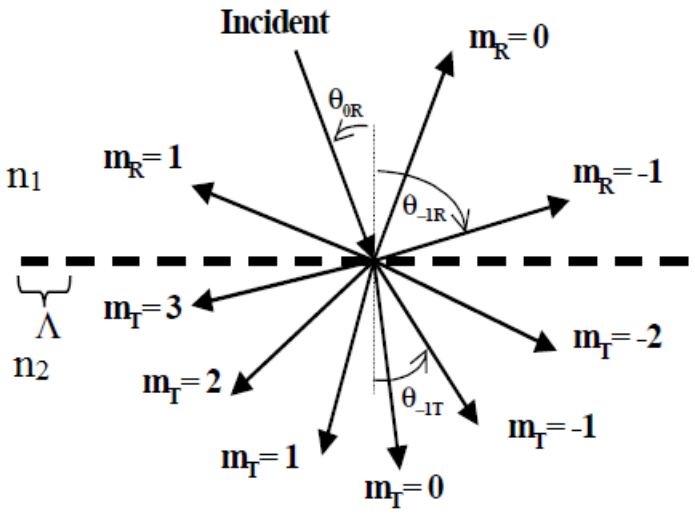


Figure 2.6: Idealized diffraction grating [16].

$$\theta_{T,m_T} = \sin^{-1}\left(\frac{m_T\lambda}{n_2\Lambda}\right) \tag{2.2}$$

$$\theta_{R,m_R} = \sin^{-1}\left(\frac{m_R\lambda}{\Lambda}\right) \tag{2.3}$$

2.2.3 Wavelength-scale random texture

Two regimes have been discussed so far, that of large-scale random and periodic textures and that of wavelength-scale periodic textures. Next we consider wavelength-scale random textures. The theory connecting the surface morphology of a wavelength-scale random texture and its light scattering ability appears not to be well-developed [17, 18].

Starting from the beginning, if one is to think about such surfaces it needs to be in the context of diffraction theory as it would be the interference effects introduced by the surface texture which cause the incoupling of light at oblique angles. Attempts at understanding the relationship between surface morphology and enhanced absorption in thin cells have been made [19]. However, a more qualitative explanation is offered here.

In the case of a periodic diffraction grating the diffraction modes are at well-defined angles. However, for a random texture the distance between adjacent texture minima/maxima occur as a distribution of values. Thus, one would expect an angular distribution of diffraction modes. Equation 2.4 [20] is an example of how this may look quantitatively but it must be understood with caution as the actual situation is not so simple.

$$\theta_{m,i} = \sin^{-1}\left(\frac{m_i \lambda}{d_i n}\right) \tag{2.4}$$

In this equation, i is an index that represents two adjacent features on the given texture, θ is the diffraction angle, m_i is the diffraction order, n is the refractive index of Si, d_i is the distance between the minima of the adjacent features and λ is the wavelength of light. One can see that, for a given wavelength of light, θ can take

on a distribution of values because d_i will take on a distribution of values. A proper theoretical analysis would need to go much further of course, but this equation is offered as a conceptual justification regarding why and how wavelength-scale textures scatter light.

The scattering of light by a wavelength-scale texture can be described by its angular distribution function for transmitted radiation (ADFTR). It shows how the intensity of incident light is transmitted through a texture into various angles. An example ADFTR is shown in Figure 2.7. Each curve represents a different texture in an a-Si:H cell.

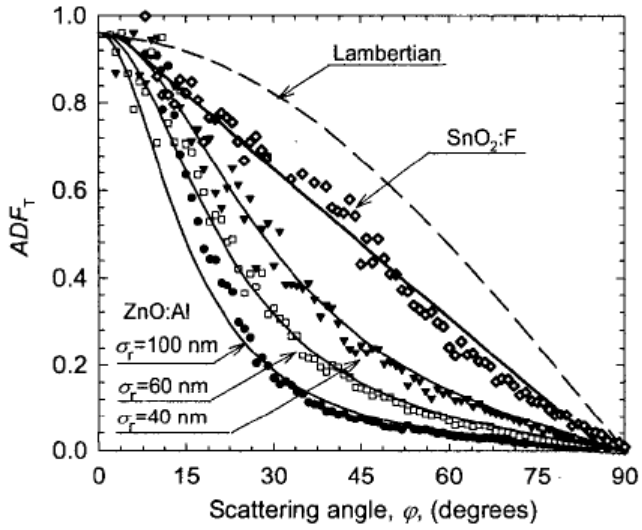


Figure 2.7: The angular distribution function for transmitted radiation describes how light is scattered by a given texture. This is normally invoked for a-Si:H cells where the texture is more commonly at the wavelength scale [21].

Surfaces are also often characterized by their roughness (σ_r), a parameter describing the statistical variation of feature sizes, but again, the surface roughness will not allow you to determine the ADFTR or any other useful parameters as the theory does not yet seem well-developed.

2.2.4 Textures much smaller than the wavelength of light

As the texture feature size gets much smaller than the wavelength of light, the local morphology of the surface becomes less important and the texture can be thought of as an effective medium [22, 23] with a refractive index intermediary between silicon and the medium from which the light was incident (ie. air).

The idea is that the volume of the cell which the texture occupies is viewed as being composed of a stack of layers. Each layer in the stack has a refractive index related to the proportion of silicon in that layer and the proportion of the other medium. Since texture features often get smaller as they travel upwards, the effect of this is that the uppermost layers have a refractive index nearest to the incident medium and the lowermost, the silicon. The middle layers gradually change in refractive index from the two extremes. This is like a multiple layer AR coating. Extremely low front-surface reflection due to this effective medium effect has been observed in many studies [24].

The physics of various textures for light trapping has been explained qualitatively. The results of the discussion is summarized in Table 2.1.

2.3 Total internal reflection at front surface

Total internal reflection (TIR) comes as a consequence of Snell's Law. In the case of light incident from a higher refractive index medium (n_2) Snell's law can be solved to obtain the refracted angle (θ_1). This shown in Equation 2.5.

$$\theta_1 = \sin^{-1}\left(\frac{n_2}{n_1}\sin\theta_2\right) \tag{2.5}$$

Table 2.1: Light-trapping texture physics summary

Regime	Angular light incoupling	AR mechanism
Large-scale (periodic or random)	Refraction	Double-bounce effect
Wavelength-scale periodic	Diffraction	Effective medium
Wavelength-scale random	Localized diffraction	Effective medium
Texture much smaller than wavelength (random or periodic)	None	Effective medium

However, the argument of an inverse sine can not be larger than 1. Since n_2 is greater than n_1 this may happen. The angle θ_2 where the argument of the inverse sine is equal to 1 is called the critical angle (θ_c). Rather than refraction, total internal reflection takes place. The expression for θ_c is given in Equation 2.6.

$$\theta_c = \sin^{-1}\left(\frac{n_1}{n_2}\right) \tag{2.6}$$

If the refractive index of Si is taken to be 3.8 and a flat air/Si interface is assumed then the critical angle is 15.2°. Therefore, if light is reflected from the rear of a solar cell and travels towards the front surface at an angle greater than 15.2° it will undergo TIR assuming there is no ARC or passivation layer.

2.4 Light-trapping in the literature

In the previous section the physics behind light-trapping was discussed. This section will look at how the various principles of light-trapping are being explored in the

literature. The organization of the following sections will be similar to the first half of this chapter. Literature regarding rear-reflectors will be first discussed. It will then be followed by a discussion on large-scale texture, wavelength-scale periodic texture, wave-length scale random texture and sub-wavelength scale texture.

2.4.1 Rear-reflectors

The various types of reflectors previously discussed have been evaluated in the literature. Berger, Inns and Aberle [25] compared five different types of rear-reflectors implemented in a 1 - 2 μm thick poly-c-Si solar cell on the basis of short circuit current measurements.

They investigated a metallic rear-reflector, a silicon-air interface, a TCO/Al stack, a detached metallic rear-reflector and a white paint PDR. These reflectors were implemented on solar cells with a textured front surface and without. They found that the metallic reflector was the worst and white paint PDR was the best, offering a 20% short circuit current enhancement over an Al reflector. The improvement approached 40% when the volume concentration of pigment molecules was optimized.

Müller et. al. compared the short circuit current of cells with either a metallic rear-reflector or a TCO/metallic stack [26]. They found that a dielectric/metallic stack was better than a straight metallic reflector and that Ag was better than Al.

From the literature it seems that a straight metallic reflector is actually the worst alternative. A white paint PDR appears to be a good option and is also experimentally straightforward to apply.

2.4.2 Large-scale random and periodic texture

As stated in a previous section, large-scale texture incouples light into a solar cell at an angle based on the principle of refraction. It also has antireflective benefits from the double-bounce effect. Large-scale texture can be either random or periodic but both function on the same principle. Most of the research surrounding large-scale texture is aimed at reducing the front surface reflection of conventional thick Si cells. It is therefore difficult to determine the relative merit of these sorts of textures for light-trapping in ultra-thin sc-Si solar cells but some insights can still be gained.

Large-scale periodic texture normally involves lithography. Inverted pyramidal texture is possible when an anisotropic etchant, such as potassium hydroxide (KOH), is used. A honeycomb texture is possible when an isotropic etchant is used [27, 28]. Lithography is normally not considered to be amenable to large-scale fabrication processes but certain types of lithography, such as interference lithography, may be more amenable than others because in such cases there is no need of an actual lithography mask.

Large-scale random texture is normally achieved by anisotropic etching of Si without a lithography mask [29–33]. This is the industry standard for texturing. It produces a random pyramidal texture. This texture has been applied in actual ultra-thin sc-Si solar cells [1, 34]. It appears to be the only texture that has thus far been applied to such cells.

The main issue in using such texture is the amount of material that is removed. At least several microns of material are removed before a texture is formed and the feature size of the texture is typically several microns as well. This is of course not useful for ultra-thin solar cells on the scale of 10 μm. It may be possible to get a

smaller scale texture, on the order of 3 μm, by adding a surfactant [35] but there is still the issue of bulk material removal before the texture begins to form.

Large-scale random inverted pyramidal texturing with minimal material is possible. There appears to be at least two ways of implementing it. The first method involves depositing a poor quality oxide on the surface of Si wafer and then etching that wafer in KOH. The oxide will form pinholes which creates something like a mask but without the effort of lithography [36]. The second method involves using silver nanoparticles to create pits on the surface of Si which can then be opened up into inverted pyramids with alkaline etching [37]. It is not clear how much material is removed in the latter method.

Laser etching of Si may also be an option to create large-scale features [38]. Such a texture can have a front surface refletance of 7% throughout the useable solar spectrum. However, the utility of it for light-trapping is not clear.

It seems that the conventional random upright pyramidal texture is not appropriate for the thickness of cells considered in this work due to the amount of material that is removed. Large-scale periodic textures based on interference lithography may be useful for ultra-thin sc-Si as may other unique texturing methods which produce random inverted pyramids.

2.4.3 Wavelength-scale periodic texture

The physical basis for light scattering from wavelength-scale periodic textures was said to be a result of diffraction. The simple model used to qualitatively explain how these textures work was a diffraction grating on the front surface of the solar cell. This is actually not the only configuration that is being considered in the literature.

Researchers are also considering diffraction gratings on the rear of the cell and also so-called integrated diffraction gratings which are on both the rear and the front of the cell. Furthermore, diffraction gratings can be either one-dimensional or two-dimensional and within each of those categories a number of profiles are possible. Thus, the number of potential diffraction-based light-trapping structures is quite large.

Wavelength scale textures must be realized using a lithographic method. Interference lithography and wet chemical etching is an option. Another option is natural lithography where a surface is coated with colloids hundreds of nanometers in diameter which naturally create a lithographic pattern on the surface. Pattern transfer is then possible with reactive ion etching (RIE) or optical photolithography and wet chemical etching.

It seems that there are a large number of papers on this subject that have been published in the last decade. The large majority are theoretical and are concerned with simulating a specific diffraction grating structure. Other theoretical papers seek to optimize diffraction grating profiles. The small minority of papers are experimental and are concerned with implementing a diffraction grating in an actual solar cell or determining the reflectance of a certain grating.

An important consideration when sorting through this body of research concerns what useful information can be taken from them. The experimental papers are very useful because they will give some indications of how an actual grating will perform in a solar cell. Papers that seek to optimize grating profiles via simulations are useful because they will provide guidance for experimentally fabricating optimum structures.

The papers which simulate a specific structure (which constitutes the large majority) are less useful because they all seem to promise a large increase in performance but, because they are based on simulations, it is not necessarily possible to compare the results of one paper to the next. At best, it seems that these papers can give experimentalists an idea of what is possible, what design features may be most important and what may be likely to perform well. Thus, the quantitative results of papers which simulate specific structures will not be given, rather, they will be treated collectively and probed to discern any useful design lessons.

Front surface

Front surface diffraction gratings can be either one-dimensional or two-dimensional. The most common one-dimensional diffraction gratings of interest to researchers are rectangular and triangular gratings. Both were shown in Figure 2.5.

Theoretically, ideal grating parameters have been determined and are similar to the results for integrated gratings. Abouelsaood et. al. found that the optimum anti-reflective and light diffusive properties of a rectangular grating occurred for a period of 650 nm, a height of 200 nm and a duty cycle of 50% [39]. Catchpole and Green also found optimal diffusive light transmittance in 1D rectangular diffraction gratings at a period of 650 nm and a height of 300 nm [40]. There seems to be some agreement as to what an ideal rectangular grating should look like.

Zaidi et. al. [9] fabricated rectangular and triangular diffraction gratings on a standard crystalline silicon wafer using photolithography and RIE. Their rectangular grating had a period of 500 nm, a duty cycle of approximately 25% and a grating height of 1000 nm. They then performed experiments to measure IQE and reflectance

and compare the results with those from the same cell but with no grating. The IQE is improved by as much as 2.5 times in the red end of the spectrum, as expected, but diminished slightly in the blue. The researchers claim this is due to RIE damage which may degrade the recombination velocity at the front surface where the blue-end of the spectrum is absorbed.

Several researchers have investigated RIE through a colloidal mask to produce a two-dimensional periodic front-surface texture [41–46]. This texture has not been implemented in an ultra-thin sc-Si cell so far as the author is aware. It is seen as a potentially viable texturing alternative for multi-crystalline Si solar cells as these cells can not be textured using the conventional random alkaline etch.

Front surface reflectance values from this texture as low as 1.5% were obtained [44]. Of those studies where this texture was tested in an actual solar cell, the efficiency gains were relatively low, at most 0.6 percentage points and this was in a multi-crystalline silicon cell [42]. One of the drawbacks of RIE texturing is that it causes damage to the front surface and this can degrade its electrical properties. Thus, RIE texturing can be an optimization experiment between optical and electrical properties.

Rear surface

Attention has been paid recently to using diffraction gratings as rear reflectors. Metallic rear diffraction gratings have been examined theoretically by Campa et. al. [47] and Chen et. al. [48]. Campa et. al. found that while the rear-diffractive structures served to scatter light back into the cell into various diffraction modes, the overall reflectance of the rear-reflector was reduced from the case of a flat interface. In

some cases the overall reduction was up to 40%. This effect could be reduced with the choice of appropriate grating profile. Campa et. al. suggested certain optimal parameters for the rear diffraction gratings that theoretically allowed absorbance increases of up to 180%. Triangular gratings seemed favourable to them because they could be implemented at larger periods and this is presumably easier.

Chen et. al. analyzed the reflection of light from rectangular, trapezoidal and triangular rear-surface diffraction gratings of various profiles into the various diffraction modes. The aim was to see what type of grating would suppress the zeroth order and couple the most light into higher orders. While all structures saw some coupling into higher orders, this seemed to be done best by the optimized triangular grating, at least at normal incidence.

Rear-diffraction gratings incorporating distributed Bragg reflectors (DBR) were investigated in [49–51]. Feng et. al. [50] simulated and optimized a rectangular rear-surface diffraction grating with a DBR situated directly on the gratings rear. The purpose of the DBR was to reflect back in any light that was not reflected by the grating. Their simulations suggest that a 10 μm cell with optimized rear-surface rectangular diffraction grating, AR coating and DBR can get an efficiency of greater than 15% where a flat cell with no light-trapping of the same thickness would get less than 10%.

Blazed gratings have been looked at by Chiou et al [52] and Heine et al [15]. Glessing et al theoretical analyzed 2D rear-side diffraction gratings [53].

Integrated

Integrated diffraction gratings are more common in the context of thin-film cells like a-Si:H than ultra-thin sc-Si cells because an integrated diffraction grating would be the most straightforward to implement in those cells. The common approach is to deposit a transparent conductive oxide (TCO) on a glass superstrate and then create a diffraction grating in the TCO. The thin film cell is deposited on the TCO and the grating pattern is copied into both the front and the rear of the cell.

Optimal grating parameters have been determined theoretically to be similar to those for a front surface grating. Dewan and Knipp found that maximum short circuit current occurred for a feature height of 300 nm and a period of 600 nm for an integrated diffraction grating in a 1 μm cell assuming a 50% duty cycle [12]. Campa et. al. numerically optimized a similar type grating and found and optimal period of 300 nm, a height of 300 nm and a duty cycle of 50% [54].

Experimentally, the research again seems sparse. Stiebig et. al. [55] experimented with a range of periods and feature heights on 1 μm thick micro-c-Si:H cells with integrated diffraction gratings. Unfortunately, they did not come near the theoretically optimum values for period and feature height. They found that the short circuit current of a cell with an intgrated diffraction grating was intermediate between no grating and a random texture.

Eisele et. al. [56] determined the reflectance and diffraction order intensities for a-Si:H integrated diffraction gratings. They fabricated gratings of various periods and found that for a 980 nm period and 160 nm height the front surface reflectivity in the range of visible was lower than wavelength scale random texture.

2.4.4 Wavelength-scale random texture

RIE can be used to produce a variety of feature shapes and sizes, from thin needles to larger pyramids. It can be difficult to classify RIE textures as either wavelength-scale or sub-wavelength scale because the feature sizes really do seem to come in a continuum of values. Furthermore, there would be no sharp divide where one RIE texture may be diffractive and another purely an AR coating. Thus, there is necessarily some overlap in the remaining sections of this chapter.

Agarwal et. al. fabricated a wavelength-scale texture on Si composed of pores 400 - 700 nm large [57]. The texture achieved by Moreno using RIE had larger feature sizes, closer to the micron scale [58]. Yoo et. al. fabricated a unique texture composed of cylindrical-like features several hundreds of nanometers in diameter [59]. Other wavelength-scale RIE textures were studied by Fukui et. al. [60], Zaidi et. al. [61, 62] and Ruby et. al. [63, 64].

In most of these studies a low front-surface reflectance is observed. However, the relative light-trapping merit of these textures is not often studied because such textures are usually intended to be applied in conventional multi-crystalline Si solar cells where light-trapping is less of a concern. Nonetheless, it seems like a technology that may be amenable to ultra-thin sc-Si solar cells because it is possible to form a variety of surface profiles with only minimal material removal, unlike alkaline etching.

2.4.5 Sub-wavelength-scale texture

Sub-wavelength-scale texture can be very useful as an antireflection coating but it is not useful as a light-trapping structure because it will not cause normally incident light to enter the cell at an angle. It is included in this discussion for the sake of

completeness in terms of different types of texture.

This sort of texture is possible with metal-assisted wet chemical etching [65–68], maskless RIE [59, 69–71], vapour texturing [72], electrochemical etching [73] and acid etching [74].

2.4.6 Plasmonic light-trapping

A final approach to light-trapping comes from the field of plasmonics. It is only mentioned briefly here for the sake of completeness. A plasmon is the quantization of an electron wave in a similar way a phonon is the quantization of a lattice vibration. Metal nanoparticles display a plasmon resonance and this can be utilized to scatter light and enhance absorption. The resonance is tuneable by manipulating the nanoparticle size and shape. There are numerous papers on this subject in the literature, as an example see [75, 76].

2.5 Summary

Light-trapping must play an integral role in any ultra-thin sc-Si device because it can enhance absorption. Light-trapping was discussed on the basis of three principles. Firstly, light must be incoupled into the solar cell at an angle because this will increase the distance light must travel to reach the rear of the cell. Secondly, there must be strong reflection at the rear of the cell. This will at least double the optical path length for those photons which are reflected. Lastly, light may undergo total internal reflection at the front surface of the solar cell and be effectively trapped.

The most experimentally important of these principles is incoupling of light at

an angle. This can be accomplished by texturing the front or rear surface or with plasmonic nanoparticles. The physics of how this is done depends on the scale of the texture. Large scale textures operate based on refraction. Wavelength-scale textures operate based on diffraction and sub-wavelength-scale textures act as an effective medium which does not scatter light.

The number of options for implementing texture is immense. Sorting through this body of literature so as to glean useful insights is difficult because most of the literature is not in the context of ultra-thin sc-Si solar cells but rather other thin film cells or multi-crystalline cells. The main constraint imposed by ultra-thin cells is that the texture ought to be relatively small and involve minimal material removal. This eliminates the conventional random pyramidal texture as an option. Ideally, the texture would also not involve complicated lithographic steps because this is considered prohibitive for large-scale manufacture although, interference lithography may still be an option because it is simpler.

This leaves a number of options: inverted pyramidal or honeycomb textures from interference lithography or pinholing, metal-assisted inverted pyramidal texture, 1-D or 2-D front, rear or integrated diffraction gratings of various profiles and sizes obtained from interference lithography or natural lithography and RIE, wavelength-scale random texture with various surface profiles from maskless RIE or possibly even sub-wavelength textures to produce ultra-low reflectance front surfaces (but here there is minimal light-trapping value and there is the danger of degrading surface electrical properties).

More research needs to be done before the utility of these textures for light-trapping in ultra-thin sc-Si solar cells can be established. Currently, it seems only

one sort of texture has been implemented in ultra-thin sc-Si and that is the random pyramidal texture on a 25.5 μm solar cell already mentioned.

Chapter 3

Background II: Ultra-thin sc-Si solar cells in the literature

This chapter reviews ultra-thin sc-Si cells that have been fabricated in the literature. A variety of different procedures have been used by different researchers. They are listed below.

1. Cell fabrication on the device layer of a silicon-on-insulator (SOI) wafer which is then, in some cases, transferred to another substrate
2. Wafer thinning using KOH etching
3. Layer transfer techniques
4. sc-Si epitaxy on a foreign substrate using a seed layer
5. KOH lateral undercutting to release thin sc-Si layers

3.1 Cell fabrication on device layer of SOI

Perhaps the most straightforward way to construct an ultra-thin solar cell is to use an SOI wafer with a device layer that is the desired thickness of the cell. It is possible to create the device entirely on the front surface by using a lateral junction architecture as has been done in [77–79] or transfer the device layer to another support as in [6, 80].

Among these studies [80] is perhaps the most notable. It has a lateral junction architecture (Figure 3.1), is 10 μm thick and has an efficiency of 9.6%. The lateral junction is not ideal, partly because it will increase shadow losses. The front-surface is well passivated with thermal oxide. There is high local doping under the contacts. The researchers claim the adhesive which adheres the device to the substrate helps passivate the surface as well. The alumina substrate is a diffuse reflector of light and can contribute to light-trapping.

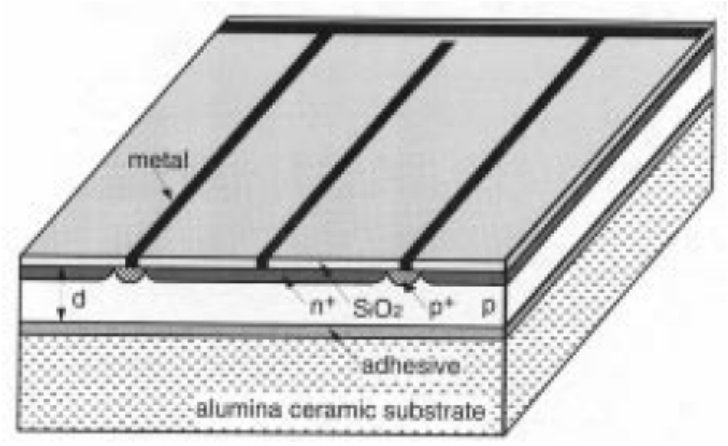


Figure 3.1: Schematic representation of device fabricated in [80].

The researchers in [6] constructed a 6 μm solar cell with the junction at the rear of the cell. It is unclear why they chose to do that. They achieved an interesting

result which points to the importance of surface passivation in ultra-thin sc-Si solar cells. Without surface passivation the cell obtained an efficiency of 2.76% but this improved to 7.96% with oxide surface passivation.

3.2 Wafer thinning using KOH etching

Thinning a thicker sc-Si to create a freestanding ultra-thin sc-Si foil is another way to create an ultra-thin sc-Si solar cell. However, this method has its limits. Firstly, repeatability might be difficult as it would not be straightforward to produce the same thickness of Si from experiment to experiment without some sort of etch stop.

Secondly, this method is probably not appropriate for cells thinner than 10 μm as handling the foil at that point is likely to damage it, prohibiting solar cell processing.

Nonetheless, this approach was used in [81] to produce a 30 μm thick freestanding flexible ultra-thin sc-Si:a-Si:H heterojunction solar cell. This structure did not incorporate any light-trapping features and had an efficiency of 12.4%.

3.3 Layer transfer

Transferring a thin layer of Si to a foreign substrate, or alternatively leaving it as a freestanding foil, is experimentally more complex than the previous methods but it is also more relevant. The previous two methods are only suitable for laboratory fabrication whereas layer-transfer approaches may be more amenable to large-scale commercial fabrication.

Layer transfer methods allow a thin layer of Si to be taken from a bulk silicon wafer which can then be reused to produce the next thin layer of Si. A review of layer

transfer process is provided in [82]. A representative layer-transfer process which explains the general approach is shown in Figure 3.2 [83].

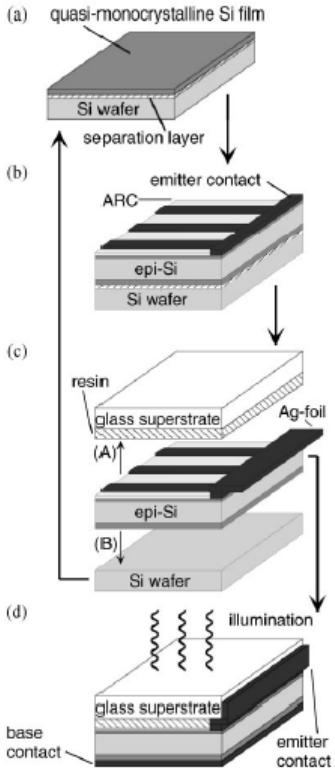


Figure 3.2: (a) A porous separation layer is created at the surface, or slightly below the surface, of a bulk Si wafer. (b) A solar structure is grown epitaxially using that wafer as a substrate. The front surface is metallized. (c) The epitaxial layer is mechanically removed from the Si substrate and adhered to a glass superstrate. (d) The rear is metallized and the Si substrate can be re-used [83].

The layer transfer approach has been used to produce ultra-thin sc-Si solar cells in a number of studies [1, 34, 83–87]. Perhaps the most notable results are those obtained by [1]. A schematic of this solar cell is shown in Figure 3.3. This solar cell is 25.5 μm thick and has an efficiency of 15.4%, the highest yet for an sc-Si ultra-thin cell. The front surface texture is random pyramidal, there is a detached metallic rear reflector and a front surface antireflection/passivation layer of silicon nitride.

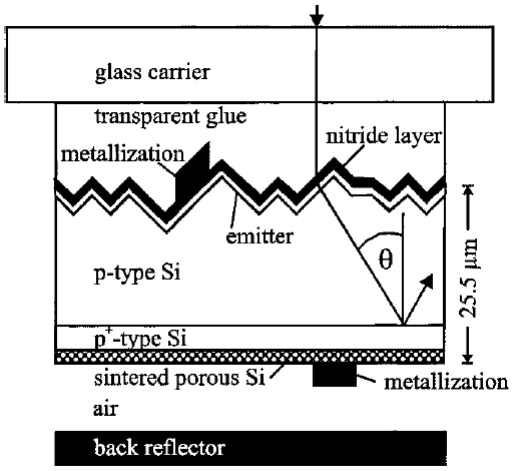


Figure 3.3: High performance ultra-thin sc-Si solar cell [1].

Brendel et. al. [34] constructed a similar cell. It was thinner, at 15.5 μm. It had a random pyramidal texture on the rear instead of the front and it had no detached rear reflector. They achieved an efficiency of 12.2%.

Notable layer transfer approaches that are approaching commercial availability and are capable of producing free standing ultra-thin foils (>20 μm) come from AstroWatt (Austin, TX) [88], Twin Creeks Technologies (San Jose, CA) and Silicon Genesis (San Jose, CA) [89]. A 25 μm sc-Si foil is shown in Figure 3.4.

AstroWatt uses their Silicon on Metal (SOM) process which is able to produce ultra-thin Si foils by using a metallic layer which introduces strain and facilitates foil exfoliation. Twin Creeks Technologies and Silicon Genesis used high energy ion-implantation to produce a weakened layer that allows a foil to be exfoliated.

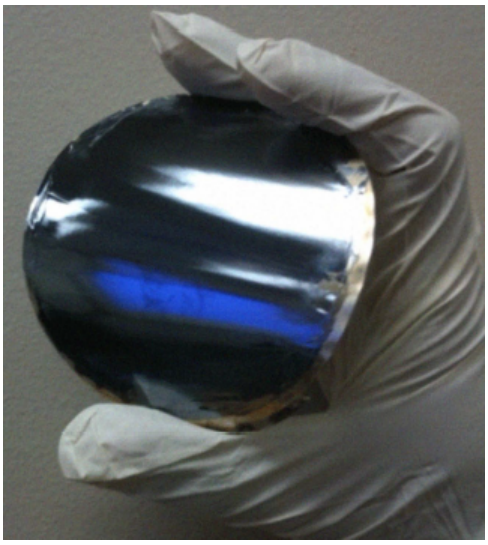


Figure 3.4: Flexible 25 μm thick sc-Si foil [88].

3.4 sc-Si epitaxy on foreign substrate

This method appears to be used almost exclusively by Gordon et. al. [90–92]. In these studies, the researchers deposit a Si seed layer on an inexpensive substrate like glass which is then the template for epitaxial growth. The cells made using this method thus far have been basic, shown in Figure 3.5, but have achieved a reasonable efficiency. A 10 μm cell with no light-trapping has achieved an efficiency of 11%.

3.5 KOH lateral undercutting

An alternative approach to fabricating ultra-thin sc-Si solar cells using basic laboratory procedures has been developed in [93]. In this study the researchers use extensive lithography and are able to release ultra-thin sc-Si solar cells from a substrate by KOH lateral etching. The result is a rear contacted 14 μm thick device that is 14.9% efficient. Because this process relies on lateral etching, it is likely to be limited to very

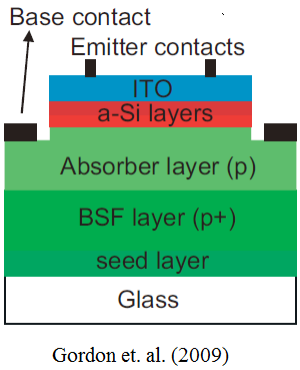


Figure 3.5: An ultra-thin sc-Si solar cell can be epitaxially grown on a glass substrate by using an Si seed layer [91].

small area solar cells. In this study, the cells were only 250 μm wide.

3.6 Summary of ultra-thin sc-Si cells in the literature

From reviewing the ultra-thin sc-Si cells that have been fabricated in the literature, it is clear that light-trapping as it has been presented in the previous chapter has yet to be adequately explored in the context of ultra-thin sc-Si cells. Most of the cells presented here did not incorporate texturing and of those that did, it was the random pyramidal texture which may not be ideal for cells of this type.

There is much experimental work still to be done. With this aim in mind, a simple process flow that is versatile enough to allow for the implementation of various light-trapping schemes but does not involve any complicated experimental techniques would be of real value.

3.7 Membrane-based process flow developed in this thesis

The main aim of this thesis was to design and implement a process flow capable of fabricating ultra-thin sc-Si silicon solar cells. It is clear that there exist several process flow options from the scientific literature. However, some of these were not possible to implement at McMaster and others were not ideal.

McMaster does not have the capabilities to perform sc-Si silicon epitaxy from a seed layer. The Porous Silicon Process also involves silicon epitaxy and thus, was not possible. Ultra-thin wafer exfoliation from high-energy ion-implantation used by Silicon Genesis or Twin Creeks Technologies was not likely to be possible at McMaster and, even if it was it would require extensive experimental work to determine the correct processing parameters. The process information for the SOM process used by AstroWatt was also not widely available.

Wafer thinning approaches would make it very difficult to achieve thickness repeatability and in addition, it would limit the device thickness capable of being studied. It now seems possible to purchase ultra-thin wafers directly[1] but this has the down side of high-cost and handling difficulties at very low thicknesses. The KOH lateral undercutting approach is only useful for extremely small device sizes and there would be several limitations in terms of processing and characterization.

The remaining option was then to use the device-layer of an SOI wafer to create a demonstration device that could have, in theory, been made using some of the processes more amenable to large-scale fabrication. This is the route that was pursued in this thesis and is the subject of the following chapter.

[1] University Wafer, 66 N St., Boston, MA

Chapter 4

Experimental

A process flow for the fabrication of ultra-thin sc-Si solar cells was developed as a component of this thesis. It has been presented in [4]. This chapter will discuss the process flow in greater detail by first giving an overview and then a step-by-step breakdown in subsequent sections. Also discussed will be the resulting solar cell devices fabricated using this process flow.

4.1 Overview of process flow

A schematic of the process flow developed in this thesis is given in Figure 4.1. The process flow started with a p-type (boron) silicon-on-insulator (SOI) wafer ordered from Ultrasil Corporation.[1] It was cleaved into 2 cm $\times$ 2 cm sections. The device layer thickness was 10 μm, the handle wafer thickness was 400 μm and the buried oxide thickness was 2 μm. The resistivity of the device layer was 1 - 20 Ωcm.

The sample was cleaned using the RCA (also called Standard Clean) procedure.

[1] Ultrasil Corporation, 3527 Breakwater Ave., Hayward, CA 94545

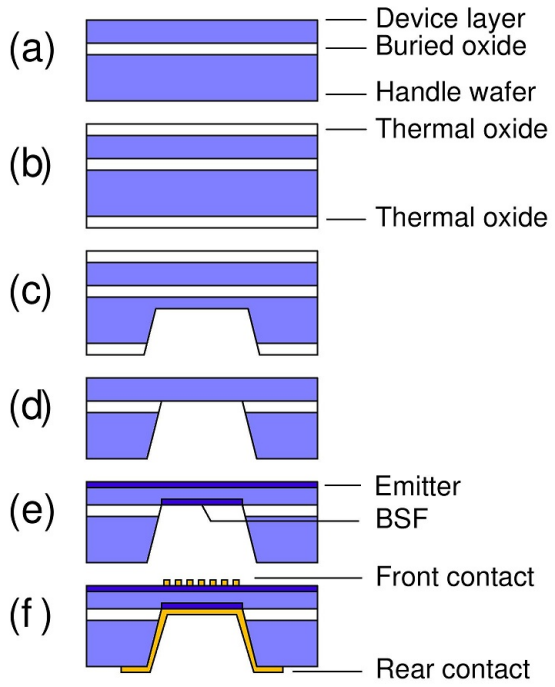


Figure 4.1: (a) Started with a low-doped p-type SOI wafer, device layer of 10 μm; (b) Cleaned wafer and anneal to grow a thermal oxide; (c) & (d) Etched circular area into SOI handle wafer to expose thin membrane; (d) Removed oxides in buffered hydrofluoric acid (BHF); (e) Emmiter and back surface field (BSF) doped with ion-implantation; (f) Cell was cleaned, annealed and metallized.

After cleaning, a thermal oxide approximately 200 - 400 nm thick was grown on the sample using a tube furnace with a steam/oxygen ambient at 1000 °C. This oxide served as an etch mask during subsequent processing.

Using a custom made etching apparatus, a circular area of material, approximately 0.95 cm in diameter, was removed from the rear of the handle wafer in a 20 wt% potassium hydroxide (KOH) solution at 95 °C. The etching apparatus was used to remove most of the material from the rear. As the etch approached the buried oxide, the sample was taken out of the apparatus and etched openly in the KOH solution using the thermal oxide to mask the front surface of the sample.

When the buried oxide was reached, the sample was rinsed in deionized (DI) water and left in BHF so as to remove the buried oxide and the front surface thermal oxide. The result of the processing was a 10 μm thick solar cell membrane 0.95 cm in diameter supported by a thicker Si frame. An isometric view is shown in Figure 4.2. All further solar cell device processing was done on this membrane without any additional mechanical support.

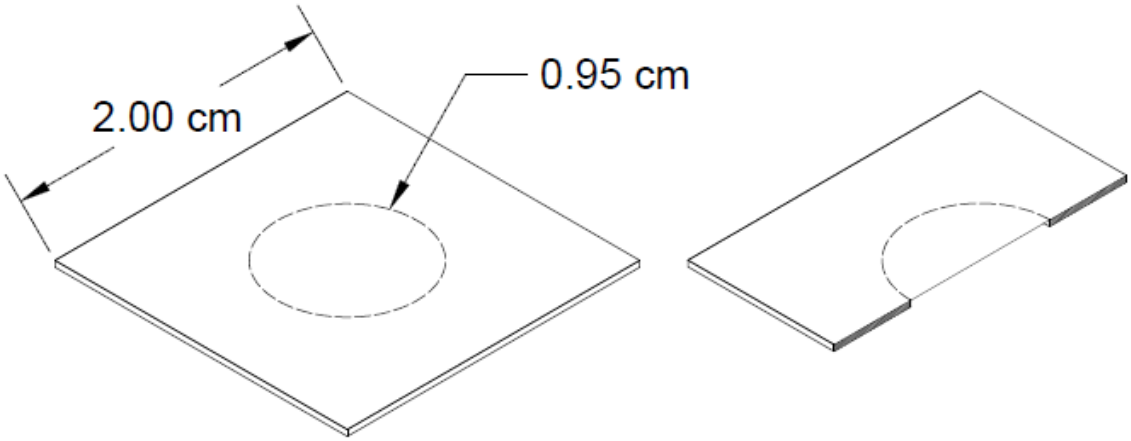


Figure 4.2: Isometric topside view of 10 μm thick sc-Si membrane with diameter of 0.95 cm. The dotted line indicates the membrane position. On the right is a cross-sectional view.

An n-type emitter and p+ back surface field (BSF) was then doped into the sample using ion-implantation at McMaster University. The emitter was doped using phosphorous ions at a dose of 2×10^{15} cm^{-2} and an implant energy of 12 keV. The BSF used boron ions at a dose of 5×10^{15} cm^{-2} and an implant energy of 35 keV. This was followed by another RCA clean and then a 3-step annealing procedure in a tube furnace with nitrogen gas ambient. It consisted of two hours at 550 °C, 15 minutes at 850 °C and then, another two hours at 550 °C. This annealing step activated the dopants and fixed lattice damage.

The final step was metallization. Ti/Pt/Au contacts were deposited through a custom designed shadow mask in an e-beam evaporation system. The first cells constructed had a completely metallized rear and a later cell had isolated rear contact fingers so as to implement a rear reflector.

The following sections will elaborate on each step of the process flow.

4.2 RCA clean

The RCA clean was developed in 1970 [94] and is still accepted as the standard laboratory procedure for silicon wafer cleaning. The chemistry of the cleaning procedure is thoroughly discussed in [95]. Intensive cleaning is necessary before high-temperature processing steps to prevent surface contaminants, specifically metal ions, from being driven into the Si where they may degrade electrical performance.

There are two main parts to the RCA clean. The first step (RCA-1) removes organic contaminants. Within this step, the Si sample is immersed in a mixture of 5:1:1, water, hydrogen peroxide and ammonium hydroxide solution heated to 70 °C. The hydrogen peroxide in this mixture oxidizes the Si surface and then the ammonium hydroxide etches the oxide, undercutting organic contaminants and releasing them from the Si surface.

The second step (RCA-2) removes metal ions and other particulates. Within this step, the Si sample is immersed in a mixture of 5:1:1, water, hydrochloric acid and hydrogen peroxide solution heated to 70 °C. The total cleaning procedure, including RCA-1 and RCA-2 steps, is listed below.

Cleaning procedure

1. Sample is placed in clean teflon dip basket; All glassware is clean
2. Dip basket is successively immersed in trichlorothethylene, acetone and then methanol, for approximately 5 minutes each
3. Flowing DI water for 5 minutes
4. RCA-1 solution for 10 minute (heated to 70 °C on a hot plate and then removed when sample is immersed)
5. Flowing DI for 5 minutes
6. BHF solution for approximately 1 minute
7. Flowing DI water for 5 minutes
8. RCA-2 solution for 10 minutes (heated to 70 °C on a hot plate and then removed when sample is immersed)
9. Flowing DI water for 5 minutes
10. Sample removed from dip basket with a different set of plastic tweezers (tweezers are designated "clean" and used only for this purpose)
11. Blow dry with nitrogen gas (if cleaning a membrane the regulator needs to be decreased to less than 10 psi)

4.3 Thermal oxide growth

A thermal oxide was used as an etch mask. The oxide was grown in a Lindeberg Hevi-Duty tube furnace. It was grown in a steam/O_2 ambient because of the faster

growth times and lower temperatures required. The tube furnace temperature was 1000 °C and growth was done for 2 hours. The chemical reaction is shown in Equation 4.1. A schematic diagram of the set-up and a description of the process is given in Figure 4.3.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{4.1}$$

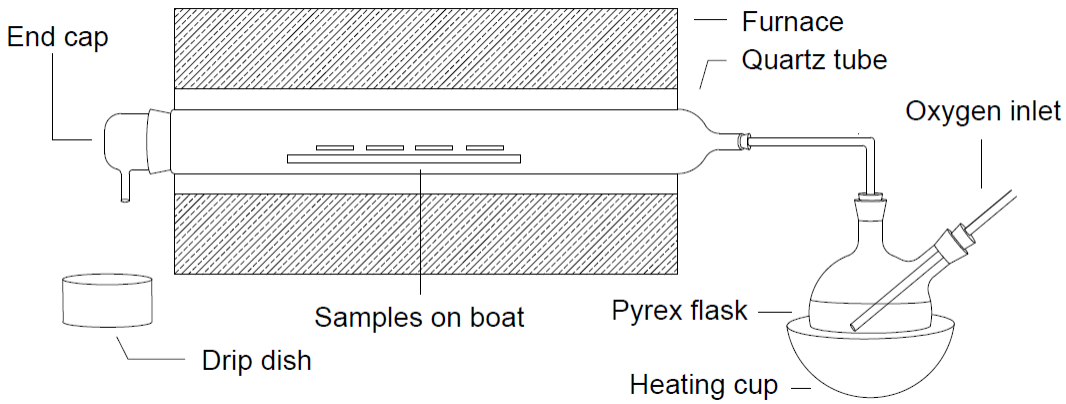


Figure 4.3: The pyrex flask is partially filled with DI water. It is heated by the heating cup. Oxygen comes in through the inlet and bubbles up through the DI water. This creates a steam/oxygen ambient which flows into the quartz tube which is heated up to 1000 °C by the furnace. The wet thermal oxide grows on the samples in the sample boat. The steam condenses at the end cap and drips into the drip dish.

This set-up is not ideal for precision oxide growths as there were several imperfections in the system, some of which were: there was no thermometer or PID temperature control on the DI water, the oxygen flow gauge was not sized properly for the system making it difficult to accurately know the oxygen flow rate and one of the heating elements in the tube furnace was not functioning (far left in Figure 4.3) which would cause a temperature gradient in the system. However, all that mattered for the purposes of this thesis was that the oxide was sufficiently thick to act as an

etch mask during KOH etching and this was achievable.

The Si/SiO_2 selectivity at 70 °C and 20 wt% KOH solution is 400 [96]. If 50 μm of Si needs to be removed, assuming this is how thick the handle wafer is when the sample is taken out of the etching apparatus, then the oxide needs to be at least 125 nm. The thermal oxides grown on these samples were typically 200 to 400 nm thick.

Before growing an oxide on actual SOI samples a calibration curve was first obtained experimentally. It is shown in Figure 4.4. Thickness measurements were taken on a J. Y. Horiba PZ2000 single-wavelength ellipsometer. Also shown is the theoretical curve obtained from [97].

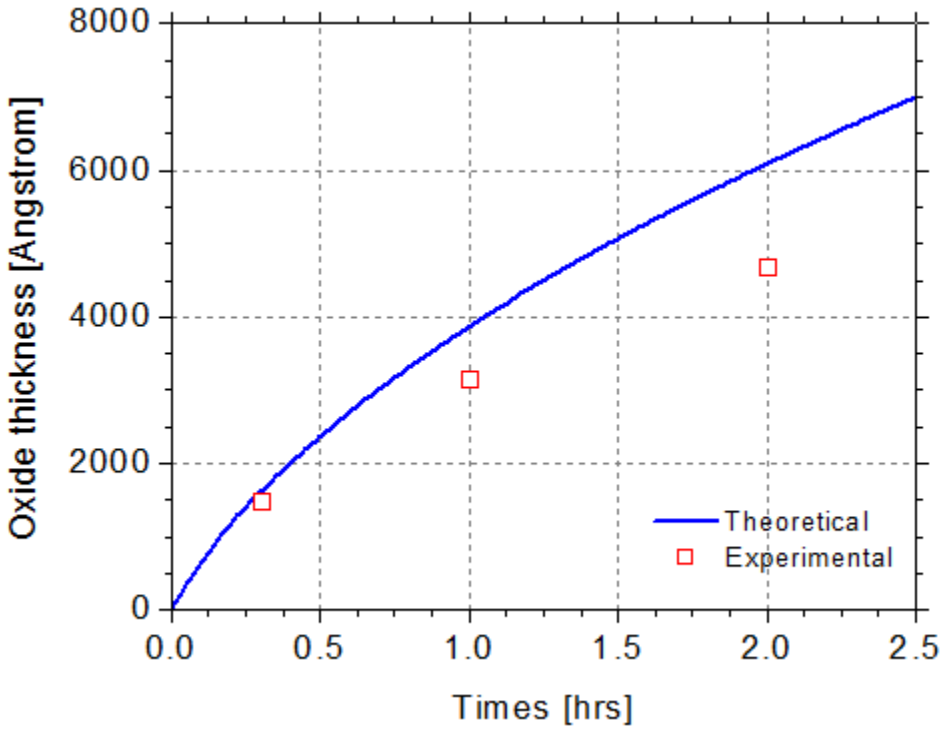


Figure 4.4: Experimental oxide growth is slower than theoretically predicted. Experimental values will vary greatly due to the inability to control several variables.

4.4 Etching apparatus and KOH etch

The etching apparatus is necessary to protect the front surface of the sample while the handle wafer is etched and also to isolate the area where the material is removed from the handle wafer. This could also be accomplished with lithography however, the etching apparatus was a straightforward and versatile solution.

Etching apparatuses similar to that used in this study have been reported elsewhere. Figure 4.5 shows one type of etching apparatus. The interior vessel contains the etchant and the exterior contains a heated water bath. There is a small circular opening at the bottom of the interior vessel where a sample can be placed. It is sealed in the stop by an O-ring which is compressed by tightening the screws. The light at the bottom of the vessel helps to gauge the progress of the etch. At some point some of the long-wavelength visible light will transmit through the sample and it will glow red.

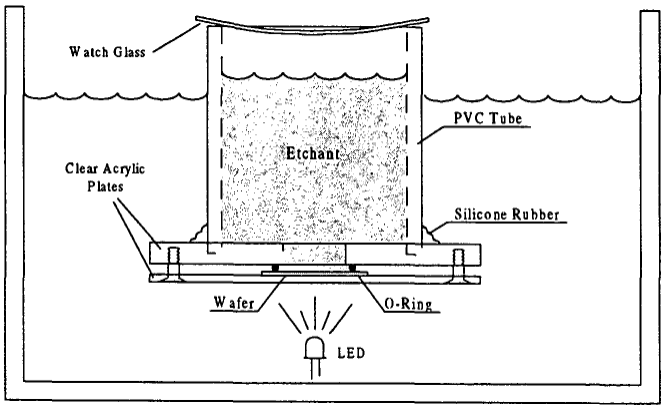


Figure 4.5: Dual etch vessel for one-sided etching from literature [98].

An alternative etching apparatus is shown in Figure 4.6. It is made of teflon and is designed to be completely submersed in an etching bath. The O-rings mechanically prevent the etchant from etching one side of the wafer. Nitrogen is pumped in between

the two O-rings to create a pressure gradient, further preventing fluid from seeping in.

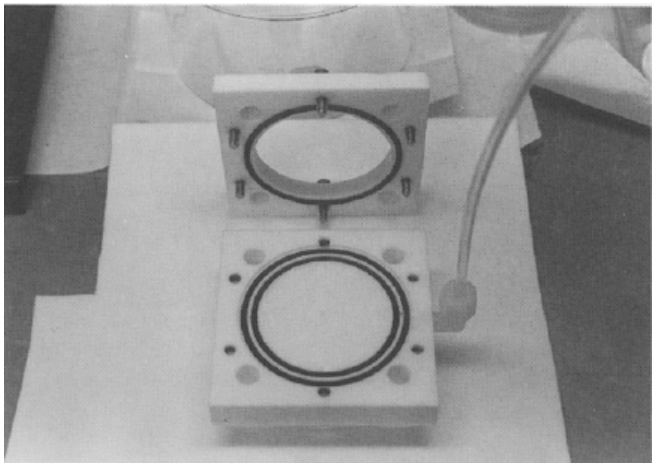


Figure 4.6: Teflon etching apparatus is designed to be totally submersed in etchant for one sided etching [99].

The etching apparatus designed in this thesis was similar the latter of the two. However, there were a few important design changes. The original intent was to adhere the front surface of the SOI sample to a glass support using a transparent epoxy because it was not clear whether or not the Si membrane would be structurally stable. This required that the interface between the glass and sample be mechanically protected as well. This would not be the case with apparatus shown in Figure 4.6 because the etchant has access to the sides of the wafer. It was therefore, desirable to have the sample fully enclosed with only a small circular area open to the etching solution.

The second change was a transparent window which would allow for the implementation of the LED thickness detection system used in the first apparatus. The last change involved a switch to radial O-ring seal which would easily allow samples of different thicknesses. The resultant etching apparatus designed with the aid of the

manufacturing shop at McMaster University is shown schematically in Figure 4.7. A full mechanical drawing is available in Appendix A. The full etching set-up is shown in Figure 4.8.

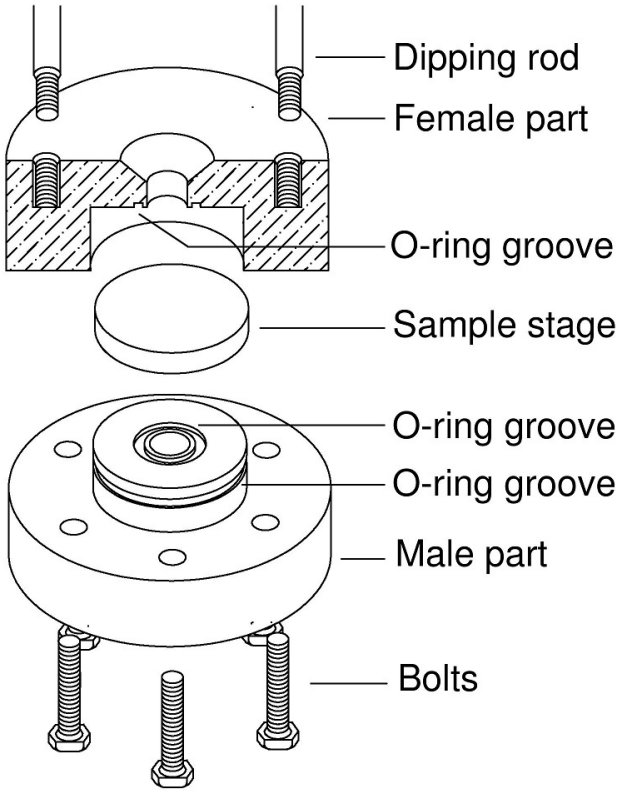


Figure 4.7: This etching apparatus was custom designed for this thesis. It is constructed of Teflon and is designed to be completely submersed in a KOH etching solution. The sample sits on the sample stage. When the bolts are tightened, the O-rings compress and the sample is mechanically sealed into the vessel with the exception of the small hole on the female part which allows etching of a small circular area of the sample. The small hole at the centre of the female part goes right through the apparatus. If a transparent stage is used then an LED thickness detection system could be implemented. This was seen to not be necessary. The radial O-ring on the male part allows samples of various sizes to be used while still mechanically protected the sample.

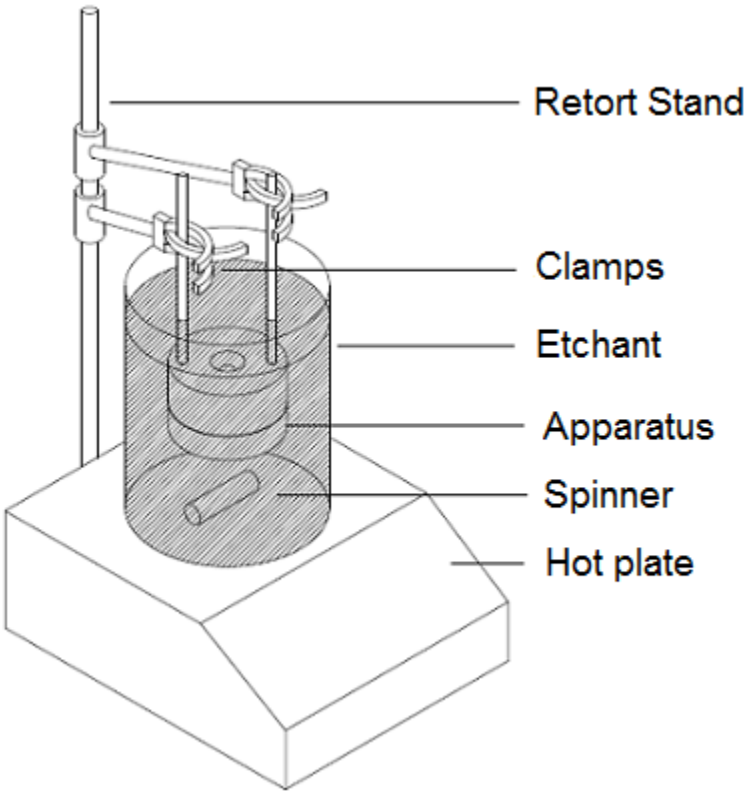


Figure 4.8: A large beaker with the KOH etchant is heated on a hot plate. The etching apparatus is suspended in the etching solution by the clamps attached to the dipping rods. A magnetic stirrer stirs the solution from the bottom of the beaker.

The etching procedure is given below.

Etching Procedure

1. Sample with thermal oxide mask was placed, device layer facing down, in the etching apparatus. Bolts were tightened to finger-tight but not over-tight (so long as the O-rings are somewhat compressed, there is a seal). Dipping rods were screwed in the top of the apparatus.

2. A solution of 20 wt% KOH was prepared in a large pyrex beaker and heated to 95 °C on a hot plate. A large mechanical spinner was placed in the beaker and

set to 150 rpm. The apparatus was suspended in the beaker by using clamps attached to a retort stand tightened around the dipping rods. See Figure 4.8.

3. Beakers containing DI water were placed on another hot plate and also heated to 95 °C. These were used to replenish the water that evaporates during the etch. The easiest way to do this was to make a mark on the large beaker where the top of the solution was and then periodically top up the solution to that line with the heated DI.

4. The first phase of the etch removed the thermal oxide from the rear of the cell (thermal oxide grew over entire surface, not just front surface) . This depends on the thickness of the oxide but should take less than an hour as the etch rate of SiO_2 in 95 °C 20 wt% KOH solution is several hundred nanometers an hour [96]. It is important to watch the apparatus so that a timer can be started when the etch through the oxide is complete. The exposed Si will begin to bubble vigorously when this happens. The timer was started when this was observed.

5. The next phase of the etch removed the bulk of the material from the handle wafer. This was a timed etch for 2 hours and 5 minutes, using a 400 μm handle wafer. The Si etch rate under these conditions is reported to be about 250 μm/hr [96] but lower etch rates were observed in this experiment. The etching time was determined experimentally. The membrane had a tendency to break when left in the etching apparatus for the whole etch. Thus, it was removed from the apparatus before the etch was finished and etched openly for the remainder. To find the appropriate time for this etch, one sample was put in the apparatus and etched until the membrane broke. Subsequent etches were

then stopped about 15 minutes before that time, in this case the overall etch time was determined to be 2 hours and 5 minutes.

6. After the given time had elapsed, the sample was carefully taken out of the apparatus and placed in a dipping basket. The solution was allowed to cool to below 70 °C (a lower etch rate is better at this point) and etching continued until there were no longer bubbles coming from the Si surface. This meant the etchant had reached the buried oxide. There was a clear visual difference between the exposed buried oxide and silicon. This usually took between 1 and 2 hours.

7. The sample was taken out and rinsed in DI. To remove the oxides, the sample was left in BHF for one hour at room temperature. After another rinse in DI, the result was a 10 μm thick sc-Si membrane approximately 0.95 cm in diameter and supported by a thicker Si frame.

4.5 Ion implantation and annealing

Ion implantation parameters were determined from [100]. The n-type emitter was doped with phosphorous ions at a dose of 2×10^{15} cm^{-2} and energy of 12 keV. The back surface field was doped with boron ions at a dose of 5×10^{15} cm^{-2} and energy of 35 keV.

Four samples were mounted on a 10 cm diameter silicon wafer and implanted at the same time. Samples were mounted using Apeizon Wax W. An important consideration here was that the entire rear-side of the sample was not sealed to the mounting wafer because this would cause the membrane to break when under vacuum.

The wax was only melted over three of the sample corners, allowing the fourth to make direct contact with the silicon wafer to allow surface discharge. This would affect the incident angle of ions and thus, the ion implantation depth. However, this effect was not considered. The mounting procedure is shown in Figure 4.9.

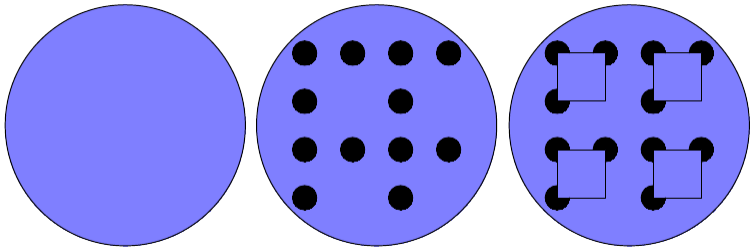


Figure 4.9: The sample mounting procedure: Start with 10 cm diameter silicon wafer (left); Place small amounts of Apeizon Wax W on wafer such that four samples can be mounted and, in each case, only three corners are attached with the Wax (centre); Carefully mount samples on the dry wax pieces and then place in a pyrex dish on a hot plate causing the wax to soften, ensure the remaining corner of each sample makes contact with the wafer (right).

To remove the samples from their mount, the wafer was quartered such that each quarter had one sample mounted on it. One at a time, the quartered pieces were placed in a large dip basket and soaked in trichloroethylene to dissolve the wax. Once the wax was dissolved the dip basket was subsequently immersed in acetone, then methanol, to prevent a film from forming on the sample.

The samples were then cleaned using the RCA procedure and annealed in flowing nitrogen in a tube furnace, also according to [100] and also [101] . The anneal had three steps: 2 hours at 550 °C, 15 minutes at 850°C and another 2 hours at 550 °C. This annealing procedure was seen to be necessary in [100] to preserve the minority carrier diffusion length of the sample. The three step anneal is represented schematically in Figure 4.10.

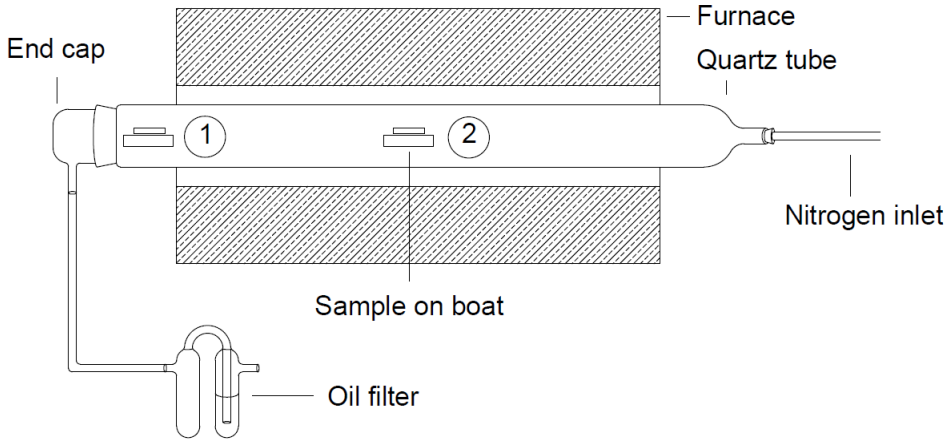


Figure 4.10: The sample is in position 1 when the furnace is ramping up or down. It is moved to position 2 during an annealing step. For example, the sample rests at position 1 until the temperature of the furnace hits 550 °C. It is then moved to position 2 for 2 hours at which point it is moved back to position 1 while the tube furnace heats to 850 °C and so on.

4.6 Metallization shadow mask

Metallization was accomplished by using e-beam deposition or RF sputter deposition through a shadow mask. There were two different shadow masks used for the front contact. Samples 1, 2 and 3 (of 4) used the front contact design shown in Figure 4.11.

Finger width, busbar width and finger spacing were determined by the optimization calculations given in [102]. The optimization considered resistive power losses in the emitter layer and the metallization versus the shadow losses of the metallization. This mask was designed with the intent of adhering the solar cell membrane to a front glass support as shown in Figure 4.11. However, the front glass support was deemed to be unnecessary.

Samples 1 and 2 had a completely metallized rear. However, Sample 3 and 4 used a contact pattern on the rear as well, so as to implement a rear reflector. It was observed that Sample 3 had a higher series resistance due in part to the rear

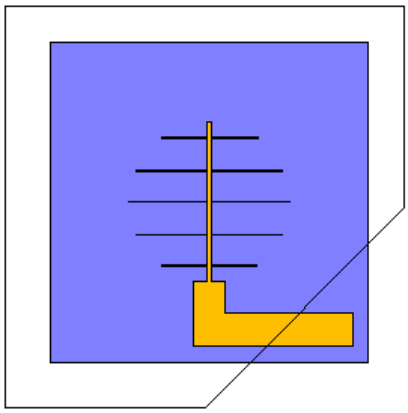


Figure 4.11: Front contact pad design for Samples 1, 2 and 3. fingers are 50 μm wide, spaced 2 mm apart and the busbar is 240 μm wide. The original intent was to adhere the solar cell to a supporting front glass (shown here with a corner cut off) and the contact pad was designed to extend onto an area of silicon that would not be covered by the glass.

contact fingers. Thus, an improved shadow mask with lowered series resistance was fabricated for Sample 4. The new front contact pattern is shown in Figure 4.12. The major difference is that with this contact pattern the busbars are moved outside the illuminated area, allowing them to be widened. There are decreased shadow losses as well as the new contact pattern lets about 3% more light into the cell. The rear contact pattern used for Sample 4 is shown in Figure 4.13.

One important thing to note about both front and rear metallization is that the contacts extend off the surface of the membrane and onto the thick Si frame. This allows the cell to be probed without breaking the membrane.

4.7 Metallization

Sample 1 used Cr/Ag front contacts and an Al rear contact. All were RF sputtered to a thickness of approximately 500 nm (Cr thickness was 10 nm as an adhesion

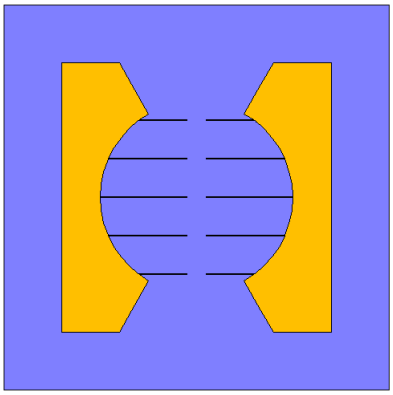


Figure 4.12: Improved contact design with lowered series resistance used for Sample 4. It has the same contact finger width and spacing but a much thicker busbar.

layer). This cell did not have a BSF and therefore, the Al would not make a good contact to the low-doped semiconductor without a heat treatment. This cell used a heat treatment of 400 ^{o}C for 5 minutes in an RTA and a good contact was achieved. A lower temperature anneal at 350 °C was not successful.

Samples 2, 3 and 4 used Ti/Pt/Au contacts on both the front and rear. This metallization scheme allowed for contacting without a heat treatment. These contacts were deposited by e-beam evaporation in the Centre for Emerging Device Technology (CEDT) cleanroom at McMaster University to a total thickness of 500 nm.

It was important to ensure that metal was not deposited on the sides of the solar cell because this would create a current shunt and degrade performance. Initially, the sides of the samples were just diced off post metallization but this resulted in the occasional broken sample. A better approach was to prevent metal from being deposited on the sides of the cell in the first place. This was accomplished using Al foil for additional masking where the original mask did not cover the sample.

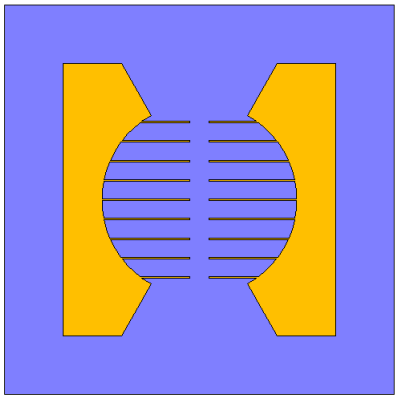


Figure 4.13: The rear of Sample 4 had contact fingers so as to implement a rear reflector. The Ti/Pt/Au contact pad came out onto the thicker Si frame to make mounting straightforward. Fingers are 80 μm wide, spaced 0.92 mm apart and the busbar is greater than 2 mm wide

4.8 ARC Deposition

The ARCs for all samples were deposited using sputter deposition of silicon nitride. The approach to designing this ARC was simple. Test samples were made to determine the sputter deposited silicon nitride refractive index. This information was then used to determine the required thickness to get quarter-wavelength interference at a given wavelength; in this case 500 nm was chosen because that is about the peak of the solar spectrum. More rigorous optimization can be used to get a better coating.

Spectroscopic ellipsometer measurements on a J. A. Woolam Co., Inc. M2000UI ellipsometer indicated that the refractive index of the Sample 1 ARC varied from 1.52 to 1.72 from 400 nm to 1100nm. This is quite low, likely indicating that the layer is porous. The thickness was 85 nm.

The ARCs for the four solar cell samples were not deposited at the same time. Therefore, some variation in the coating thickness and refractive index was expected. Indeed, this was observed and will be discussed further in the Results and Discussion

chapters.

4.9 Sample mounting

For testing, samples were mounted on copper clad circuit board with silver paste. The silver paste was dried on a hot plate at 80 °C for 10 minutes and cured at 100 °C for 15 minutes.

4.10 Fabricated samples

After the fabrication process was established, four membrane solar cells were created. The four samples are shown schematically in Figure 4.14.

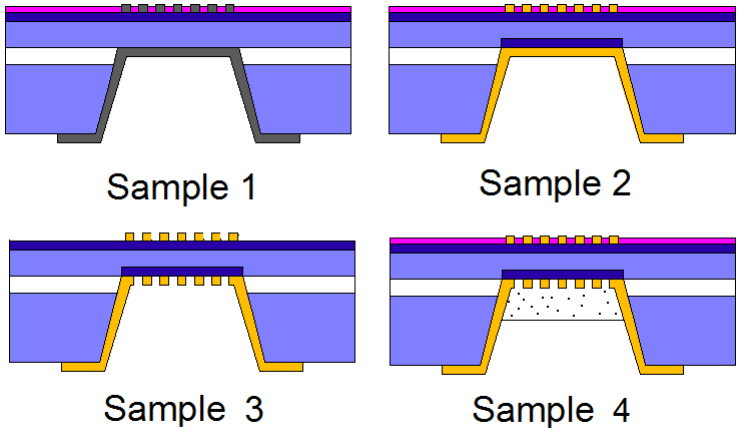


Figure 4.14: Refer to Figure 4.1 for appropriate labels. Sample 1 has a SiN_x ARC, no BSF, Cr/Ag front contacts and an Al rear contact. Sample 2 has Ti/Pt/Au contacts on front and rear, a SiN_x ARC and a BSF. Sample 3 has Ti/Pt/Au front and rear contacts, a BSF and rear contact fingers instead of a full metallization but it has no ARC (the sample was damaged before it could be implemented). Sample 4 is similar to Sample 3 but it uses the improved front and rear contact pattern, has an ARC and also has the white paint PDR.

4.11 Rear-reflector experiment

Since Sample 3 had contact fingers on the rear of the cell instead of uniform metallization, it was possible to test the performance of different rear reflectors. Towards this end, four different rear reflectors were tested: a detached Al mirror, a detached black reflector, a detached white reflector and lastly, the white paint PDR applied directly to the rear surface of the solar cell (see Figure 4.15).

The only reflection from the detached black rear reflector should be from the Air/Si interface at the rear of the cell. The white paint PDR, as described in Section 2.4.1, is anticipated to have the highest J_{SC} because of the light-trapping effects introduced by its diffuse reflectance.

The J_{SC} of each of these reflectors were measured under 1 sun AM1.5. They were compared against each other and also, against Sample 2 which is a comparable device but with a metallic rear reflector.

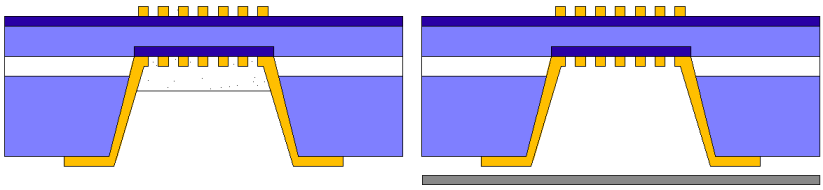


Figure 4.15: The white paint PDR is applied directly to the rear of Sample 3 (left). Detached reflectors are situated approximately 2 mm from the rear of Sample 3 (right).

Chapter 5

Measurements and Data Analysis

This chapter is split into two main sections, one which describes the measurement apparatuses and another which discusses how the data was analyzed.

5.1 Measurements

The solar cells fabricated in this thesis were characterized using one sun illuminated current-voltage (J-V) curves and external quantum efficiency (EQE) curves.

5.1.1 J-V curve measurement

A 96000 series Newport solar simulator was used to illuminate the cell. It was calibrated with a PVM 298 reference cell from PV Measurements, Inc. The reference cell had been calibrated by the National Renewable Energy Laboratory (NREL). A two-point probe source meter controlled by a LabView program was used to record the curves. A schematic of the J-V set-up is shown in Figure 5.1 (Figure adapted from [103]).

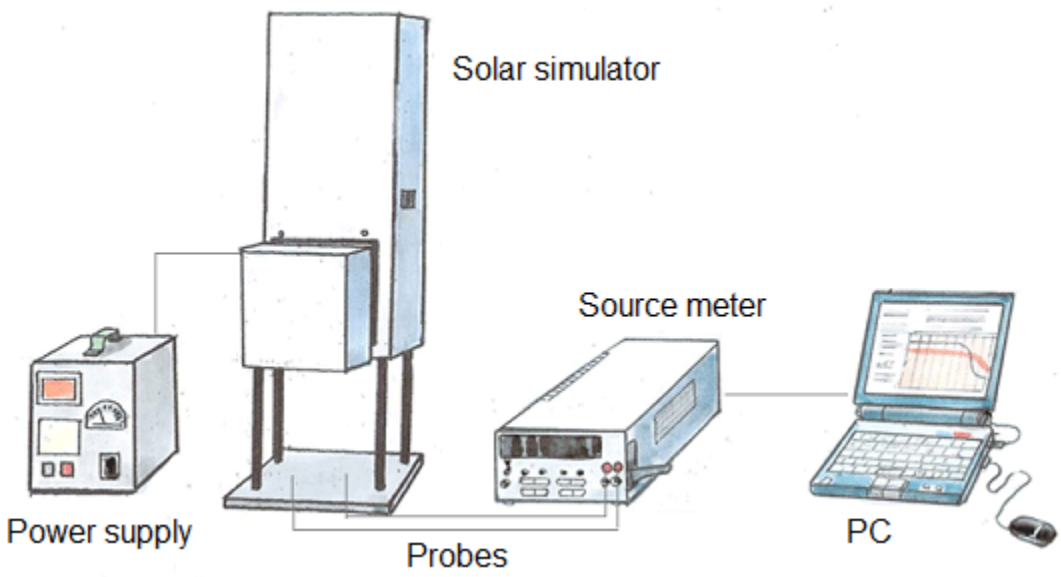


Figure 5.1: The contact probes are attached to a solar cell illuminated by the solar simulator. The PC prompts the source meter to source a voltage and measure a current and the J-V curve is traced.

A stainless steel mask was used to shade the periphery of the solar cell and allow only the area with contact fingers to be illuminated. This allowed the area to be known with accuracy for efficiency calculations. It is shown in Figure 5.2.

5.1.2 J-V set-up calibration

The solar simulator was calibrated to 1 sun for the J-V curve measurements using the calibrated reference cell but issues of beam spot uniformity were a problem. The calibrated cell was 2 cm $\times$ 2 cm and it was seen that it gave a reading of 1 sun $\pm$ 4% if the cell was placed in the middle of the beam spot $\pm$ 0.5 cm.

The solar cells tested in this thesis were less than a quarter of the surface area of the reference cell and as such, they were more sensitive to beam spot nonuniformity. This is because a larger cell surface area would tend to average out local nonuniformities.

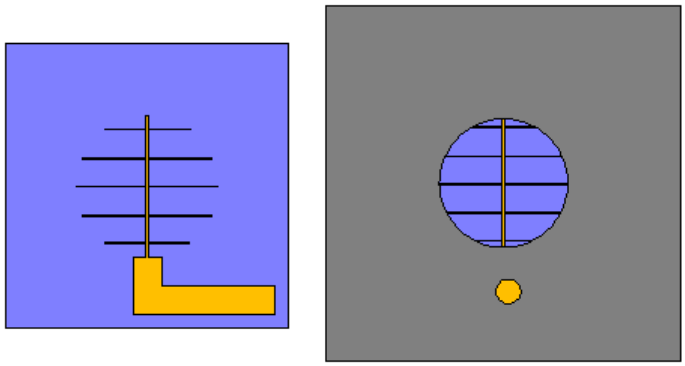


Figure 5.2: This mask was used for I-V measurements of Sample 1 and 2 and only allowed light to hit the area with the contact pad. A similar mask was employed for Sample 3.

To judge the effect of beam spot nonuniformity the short circuit current of a membrane cell was measured in the beam spot centre and approximately 0.5 cm to the left and right. It was found that short circuit current varied to within approximately $\pm$ 10% of the centre value. Thus, if the centre of the beam spot is assumed to be at 1 sun (as calibrated from the reference cell) the error in the illumination for the tests cells is estimated to be approximately $\pm$ 10%. Measurements for absolute performance have this error associated with them.

The beam spot had one position with the highest illumination, approximately 1.1 sun. It could be found by moving the cell in the beam spot while monitoring the current with an ammeter. When the cell current was maximal it was in the position of greatest illumination. All measurements were taken at this position in the beam spot and then a conversion was applied to shift the curve down to 1 sun illumination. The conversion is straightforward and invokes the superposition principle and the linearity of J_{SC} with irradiance. In this way all measurements were taken at the same illumination level and can therefore be compared to eachother with accuracy. That

illumination level is known with a ± 10% margin of error as discussed in the previous paragraph.

5.1.3 EQE measurements

EQE plots describe the efficiency of a solar cell at the spectral level. At each wavelength, the EQE curve gives a ratio of electrons out vs. photons in. This can be very useful in understanding solar cell performance. An ideal EQE would be unity for all above bandgap photons (below approximately 1100 nm for silicon).

However, this is never achieved in practice. Front surface recombination deteriorates the EQE in the UV and rear surface recombination, optical losses and poor carrier collection deteriorates the EQE in the IR. Front surface reflection reduces EQE across the entire spectrum.

EQE plots were taken using a custom-built set-up brought online by Joshua Rideout and Martin Gerber at McMaster University. A schematic of the quantum efficiency set-up is shown in Figure 5.3.

The sample is placed underneath the aperture. It is illuminated with a bias lamp with an intensity of approximately 0.5 sun. This brings the solar cell up to near working conditions. Light from an arc lamp passes through a monochromator to isolate given wavelengths. This monochromatic light than passes through a chopper and exits the lamp housing.

A blocking high pass filter at the lamp housing output ensures there are no second order diffraction peaks at half-wavelength. The light reflects from a mirror and passes through an aperture which defines the spot size on the sample. In this experiment, a spot size slightly smaller than the illumination mask opening was used.

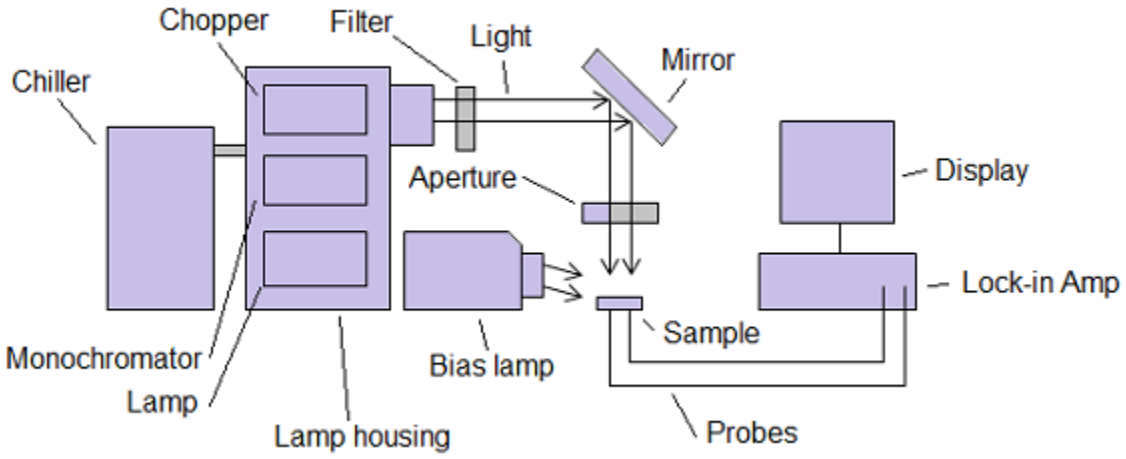


Figure 5.3: Schematic diagram of EQE set-up.

The current signal from the solar cell is then composed of two signals, a large DC signal from the bias lamp and a much smaller square wave AC signal from the chopped monochromatic light. The AC signal is separated from the DC by the lock-in amplifier which measures the AC signal amplitude at the chopping frequency. The display shows a reading in mV which can then be converted back to a current reading.

A current measurement is taken in approximately 20 nm wavelength increments throughout the solar spectrum. This gives the solar cell current as a function of wavelength.

To calculate EQE the incident power also needs to be known (this can be easily converted to incident photons). For this purpose, a Si detector is placed in the sample position and a power reading is recorded for the same wavelengths. This is done directly after the previous measurement. It is then possible to calculate the EQE with this information.

5.2 Data Analysis

5.2.1 Equivalent circuit model of a solar cell

Solar cells are modelled using equivalent circuits. Either a one or two diode equivalent circuit is often used. Shunt and series resistances are included in the equivalent circuit model of any real solar cell. A schematic of the equivalent circuit is shown in Figure 5.4 [104].

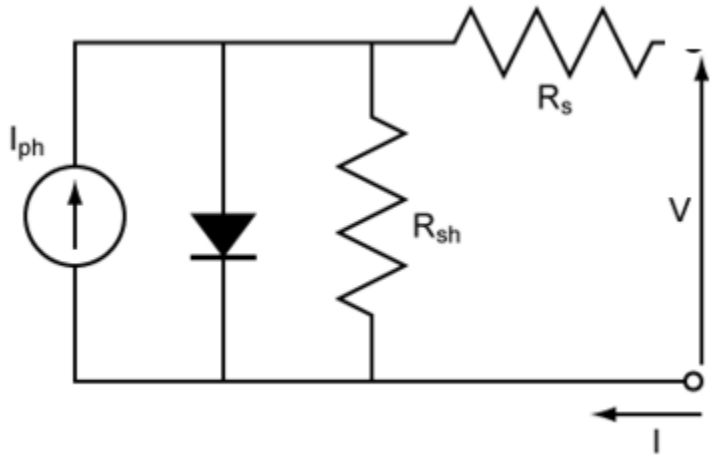


Figure 5.4: The solar cell current comes from an illumination-dependent current source. The voltage results from that current flowing through the diode. Parasitic resistance cause losses in voltage (series) or current (shunt).

The single-diode equation is more often invoked because it is simpler and captures the basic device physics sufficiently. Additional diodes can correct for non-idealities in the single-diode model. However, this is done at the cost of an increased parameter space. The single-diode model is used in this thesis. The expression for this model is given in Eq. 5.1.

$$J = J_L - J_0 \left(\exp\left(\frac{V + JR_s}{nV_T} \right) - 1 \right) - \frac{V + JR_s}{R_{sh}} \tag{5.1}$$

The parameters in Eq. 5.1 are as follows:

- J is the current density in units [A cm^{-2}]
- J_L is the illuminated photocurrent density in units [A cm^{-2}]
- J_0 is the reverse saturation current in units [A cm^{-2}]
- V is the voltage in units [V]
- R_S is the series resistance normalized to cell area in units [Ω cm^2]
- n is a unitless quantity called the ideality factor
- V_T is the thermal voltage in units [V] (also expressed as $k_B T$ where k_B is the Boltzmann constant)
- R_{SH} is the shunt resistance in units [Ω cm^2]

5.2.2 Solar cell performance parameters

While these parameters define the J-V curve, the performance of a solar cell is summarized by introducing four other parameters: the fill factor (FF), the efficiency (η), the open circuit voltage (V_{OC}) and the short circuit current density (J_{SC}). These parameters are determined under 1 sun AM1.5 illumination. These can be understood with the aid of Figure 5.5 [105].

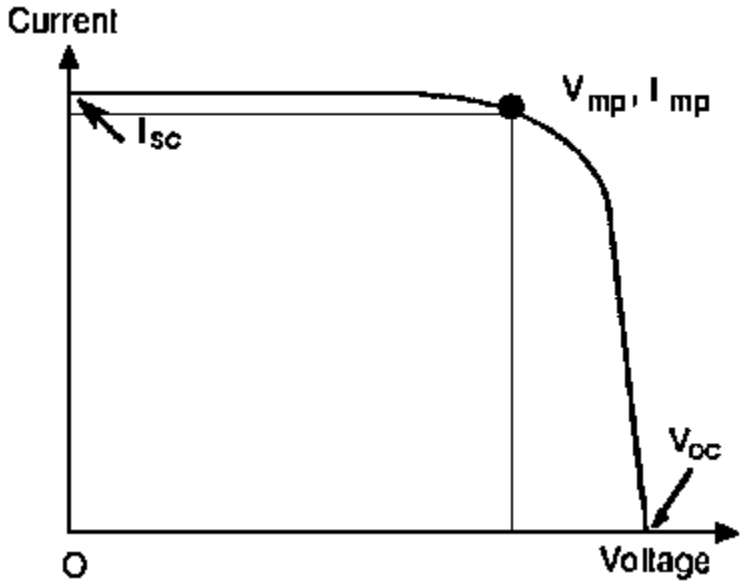


Figure 5.5: Relevant performance parameters are obtained from these four points: V_{OC}, I_{SC}, V_{MPP} and I_{MPP}.

The fill factor helps to quantify the shape of the J-V curve (and thus, the parasitic resistances). The efficiency describes the total power produced over that which was incident. The FF and η are given in Eq. 5.2 and 5.3 respectively.

The open circuit voltage is the operating point where no current is produced and the short circuit current is the operating point where no voltage is produced. The maximum power point (MPP) is the operating point at which maximum power is produced, given by J_{MPP} and V_{MPP}.

$$FF = \frac{V_{MPP}J_{MPP}}{J_{SC}V_{OC}} \tag{5.2}$$

$$\eta = \frac{V_{MPP}J_{MPP}}{GA} \tag{5.3}$$

In Eq. 5.3, G is the irradiance (equal to 1000 [W m^{-2}] for the AM1.5 G spectrum) and A is the solar cell surface area in units [m^2].

It is clear that FF, η, V_{OC} and J_{SC} are straightforward to obtain from a 1 sun J-V curve measurement. This is not the case with parameters of the 1-diode equivalent circuit described in Eq. 5.1. Various methods of extracting these parameters have been extensively treated in the literature (examples are shown in [106, 107]). In this thesis, the 1-diode equivalent circuit parameters are obtained using a Lambert W function method.

The Lambert-W function (LamW(y)) is defined for all complex values of y and is described in Equation 5.4. It is normally helpful in solving equations of the form shown in Equation 5.5, where A is a constant, because it can reduce the equation to something that can be solved analytically, Equation 5.6.

$$y = \mathrm{LamW}(y)e^{\mathrm{LamW(y)}} \tag{5.4}$$

$$A = f(x)e^{f(x)} \tag{5.5}$$

$$f(x) = \mathrm{LamW}(A) \tag{5.6}$$

With some algebraic manipulation the 1-diode model of a solar cell can be simplified using the Lambert-W equation [108–110].

5.2.3 J-V curve parameter extraction

The Lambert W function, shown in Eq. 5.7, can turn the implicit solar cell curve into a more tractable function where J can be isolated and expressed in terms of only V and the other solar cell parameters. This makes fitting experimental J-V data in a mathematics software package such as Maple or MATLAB straightforward.

$$J = \frac{nV_T}{R_s}\ \mathrm{LamW}\left(\frac{R_s R_{sh} J_0}{nV_T(R_s + R_{sh})}\exp\left[\frac{R_s(V + J_0 R_s)}{nV_T(R_s + R_{sh})}\right]\right) + \frac{V - J_0 R_s}{R_s + R_{sh}} \tag{5.7}$$

The drawback of this method is that there exist many local minima in the parameter space and there is no guarantee that the fitting procedure will find the global minima. To find the global minima the initial guesses at parameter values must be relatively accurate. To accurately determine these parameters a graphical technique is used.

The graphical method used to determine initial parameter values is based on the semi-log J-V plot. Eq. 5.8 puts the dark diode curve in the first quadrant. Ignoring the parasitic resistances, the solar cell equation in the dark is given in Eq. 5.9. In forward bias, Eq. 5.9 reduces to Eq. 5.10.

$$J = J_0\left(\exp\left(\frac{V - JR_s}{nV_T}\right) - 1\right) + \frac{V - JR_s}{R_{sh}} \tag{5.8}$$

$$J = J_0\left(\exp\left(\frac{V}{nV_T}\right) - 1\right) \tag{5.9}$$

$$J = J_0 \exp\left(\frac{V}{nV_T}\right) \tag{5.10}$$

If the natural logarithm is applied to both sides of Eq. 5.10, then the $\ln(J)$-V curve is linear. The slope is given by $(nV_T)^{-1}$ and the y-intercept by $\ln(J_0)$. This is shown in Eq. 5.11. It is clear that in the case of an ideal solar cell it would be straightforward to find J_0 and n from the semi-log plot.

$$\ln J = \ln(J_0) + \left(\frac{1}{nV_T}\right) V \tag{5.11}$$

However, when parasitic resistances are included the semi-log plot deviates from linearity. At high bias the shunt resistance term is negligible and the semi-log expression reduces to:

$$\ln(J) = \ln(J_0) + \left(\frac{1}{nV_T}\right) V - \frac{JR_s}{nV_T} \tag{5.12}$$

This is not yet helpful. To remedy this, the series resistance effects can be removed from the J-V data by transforming voltage data (V) into a new data set ($V' = V + JR_s$) and then plotting the semi-log J-V$'$ curve. With the series resistance removed, the whole region for >0.4 V is linear. Eq. 5.12 reduces to Eq. 5.13 which is equivalent to Eq. 5.11. This allows J_0 and n to be extracted.

$$\ln(J) = \ln(J_0) + \left(\frac{1}{nV_T}\right) V' \tag{5.13}$$

This approach requires knowledge of R_S that is not directly available. It is sometimes approximated as the inverse slope of the J-V curve evaluated at V_{OC} but this is not accurate enough. Rather, R_S, n and J_0 can be found simultaneously by using the

observation that the slope of the semi-log J-V′ plot in the region of >0.4 V is linear when the effects of R_S are removed. The process is described below:

1. An initial guess for R_s is made
2. The illuminated J-V data is transformed to J-V′ so as to remove the effects of R_S and the data is shifted up by J_{SC} such that the curve crosses the zero point
3. ln(J) vs. V′ is plotted
4. For >0.4 V the semi-log plot should be completely linear, if not, R_S can be adjusted and the process is repeated iteratively

An example is given in Figure 5.6. The value of R_S which gives the best linear least-squares fit in the region >0.4 V of the ln(J)-V′ plot is the correct value. Also, since series resistance has been removed, Eq. 5.8 is valid for >0.4 V and therefore n and J_0 can be known. R_{SH} can be estimated as the inverse slope of the J-V′ curve at J_{SC}.

These parameters can then be used as the initial values in a Lambert W J-V curve fitting procedure in Maple or MATLAB and the 1-diode equivalent circuit parameters can be extracted. Aside from its simplicity, the benefit of this procedure is that it helps avoid local minima by getting reasonably accurate initial guesses.

5.2.4 EQE data analysis

The EQE is a ratio of electrons out over photons in as a function of wavelength when the solar cell is operating at short circuit. From current measurements and incident power measurements the EQE should be calculated using Equation 5.14.

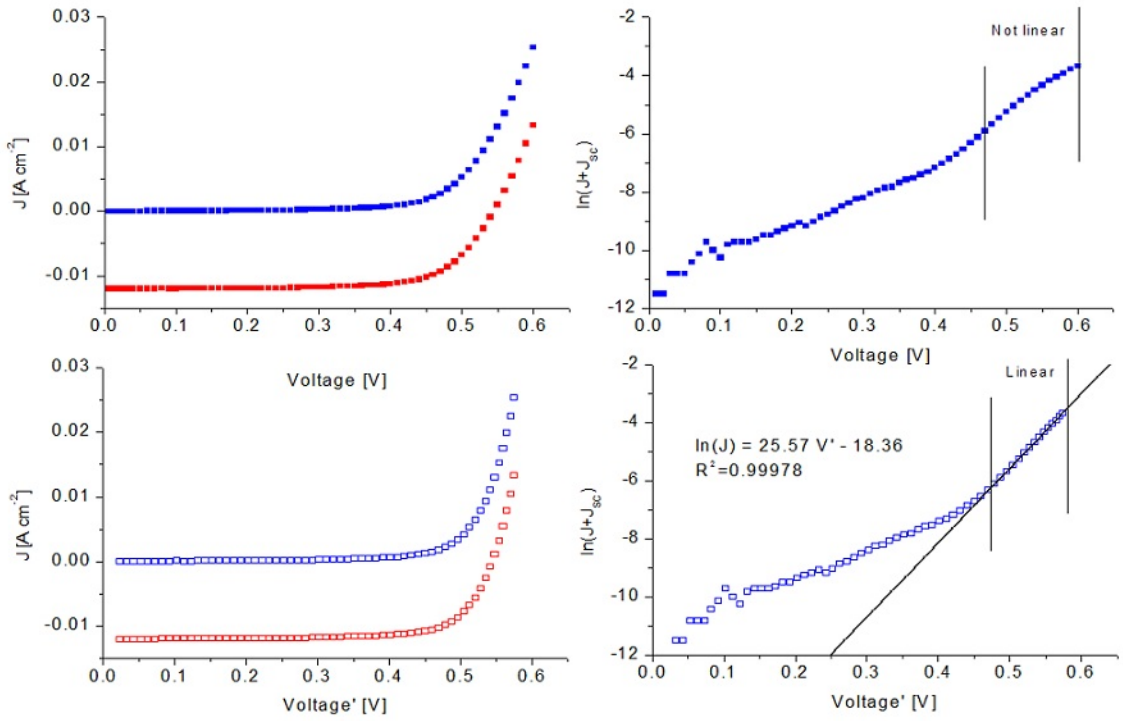


Figure 5.6: Top left: The light J-V curve is shifted up into the first quadrant without adjusting series resistance. Top right: When plotted on a log-scale the effects of series resistance are an obvious nonlinearity in the high bias regime. Bottom left: The effect of series resistance is removed from the curve and it is shifted into the first quadrant. Bottom right: The high bias region is now highly linear indicating that the appropriate value of series resistance was removed. In reality, a few values of series resistance must be tried iteratively to get the best least squares fit. It is now possible to extract n and J_0 from the curve as well.

$$\mathrm{EQE}(\lambda) = \frac{hc}{q\lambda}\frac{I(\lambda)}{P(\lambda)} \tag{5.14}$$

In this equation :

- h is the Planck constant
- c is the speed of light
- λ is the wavelength
- q is the electron charge
- $I(\lambda)$ is the current from the solar cell under illumination from a given wavelength
- $P(\lambda)$ is the incident power

Equation 5.14 was not used however due to an as yet unidentified systematic error affecting the magnitude of the EQE measurements. The EQE set-up gives the correct shape, when compared with the reference cell, but the absolute values do not agree exactly. To get the EQE as accurate as is possible a scaling factor (γ) was used such that when the EQE curve was integrated with the AM1.5 spectrum over all wavelengths, the result is the short circuit current. This is shown in Equation 5.15. The EQE curves presented in the results is then actually $\gamma\mathrm{EQE}(\lambda)$. The value of γ for the measured solar cells ranged from 0.95 to 1.05.

$$\mathrm{I_{SC}} = \gamma \int_{\lambda} \mathrm{EQE}(\lambda)\mathrm{AM1.5}(\lambda)\mathrm{d}\lambda \tag{5.15}$$

The relative EQE enhancement (REE), used to compare two EQE plots, is calculated using Equation 5.16.

$$\mathrm{REE}(\lambda) = 100\% \times \left(\frac{\mathrm{EQE}_1(\lambda)}{\mathrm{EQE}_2(\lambda)} - 1 \right) \tag{5.16}$$

Chapter 6

Results

The ARC used on Sample 1 was measured using spectroscopic ellipsometry at an angle of 45°. This is a close approximation to reflectance at normal incidence. It was found that the film thickness was 85 nm and the refractive index varied between 1.52 and 1.72 in the solar wavelength range (300 - 1100 nm). The reflectance of the ARC is shown in Figure 6.1. A straightforward numerical integration with the AM1.5 spectrum indicated a solar weighted reflectance (400 nm - 1000 nm) of approximately 13%. Reflectance measurements on the remaining samples did not yield good data. However, it is clear that the reflectance minima shifted closer to 600 nm for Sample 4. This is a repeatability issue with the sputter deposition apparatus.

J-V curves for Samples 1, 2 and 4 are shown in Figures 6.2 - 6.4. The figures show both the illuminated and dark curves on both a linear and a semi-logarithmic scale. The J-V curve of Sample 3 is not shown because it did not have an ARC and is therefore not comparable with the other samples. According to convention, the illuminated J-V is shifted up by the J_{SC} for semi-log plots and the reverse bias portion of the curve uses absolute values of current.

Also shown is a fit of the dark data from which the ideality factor and dark saturation current were determined. Relevant performance parameters are given for each device in Table 6.1.

Figure 6.5 plots the illuminated J-V curves of all samples on the same axes and, in this case, with quadrant one as the power producing quadrant.

The EQE of Samples 1, 2 and 4 is plotted on the same axis in Figure 6.6. Ideally, the difference between the EQE curves of Samples 2 and 4 would be solely the result of the different rear reflectors. However, this does not appear to be the case. The EQE of Sample 4 should not improve over that of Sample 2 until after approximately 600 nm, when the light begins to transmit through and the PDR begins to enhance absorption. However, the enhancment occurs well before that. This is likely to be due to an improved ARC deposited on Sample 4. To isolate the effect of the PDR alone, the relative EQE enhancement of Sample 3 (having the PDR rear-reflector) with respect to Sample 2 (prior to ARC deposition) is plotted in Figure 6.7. There is a clear EQE enhancement in the red end of the spectrum as shown by the relative EQE enhancement plot also in Figure 6.7.

The results of the rear-reflector experiment discussed in Section 4.9.4 are shown in Figure 6.8. Plotted is the relative J_{SC} enhancement of various rear reflectors over that of a base case with a completely metallized rear (Sample 2 prior to ARC deposition). The reflectors are: a detached aluminum mirror (Al D), a detached black reflector (Black D), a detached white reflector White D and a white paint PDR applied directly to the rear of the cell. The white paint PDR applied directly to the rear of the cell provided the greatest enhancement of 12%.

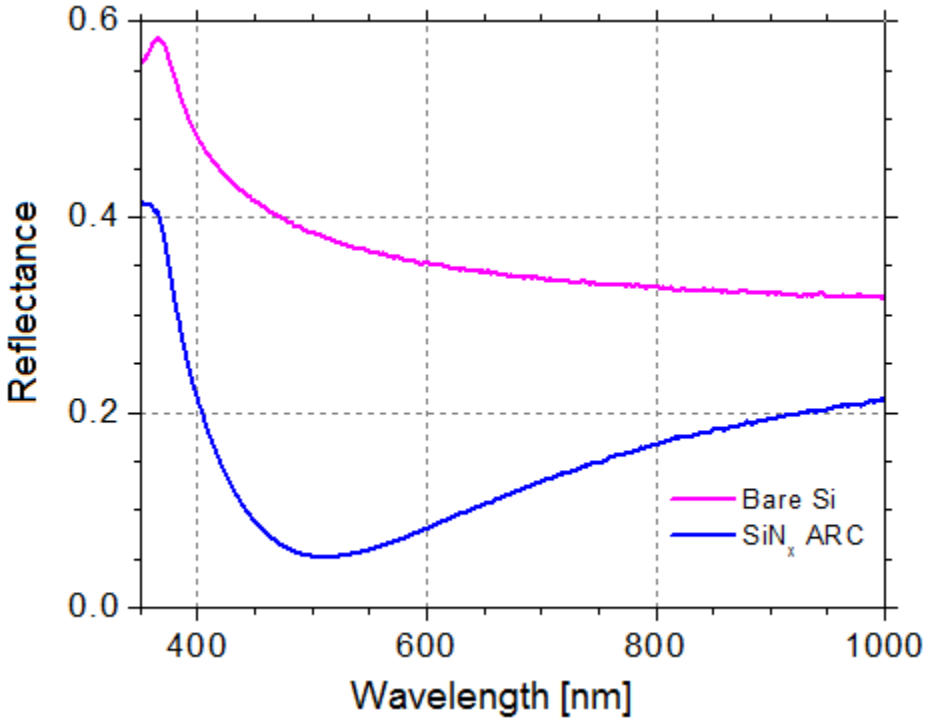


Figure 6.1: The ARC has its maximum destructive interference at approximately 500 nm, near the peak of the solar spectrum.

Table 6.1: Summary of solar cell performance parameters

Sample	V_{OC} [V]	J_{SC} [mA cm^{-2}]	FF -	η [%]	R_S [Ωcm^2]	R_{SH} [Ωcm^2]	J_0 [A cm^{-2}]	n -
1	0.43	18.8	0.63	5.1	2.16	2833	1.35e-8	1.26
2	0.55	22.9	0.67	8.4	1.38	1214	1.31e-8	1.57
4	0.53	27.9	0.67	9.9	1.40	733	7.26e-9	1.42

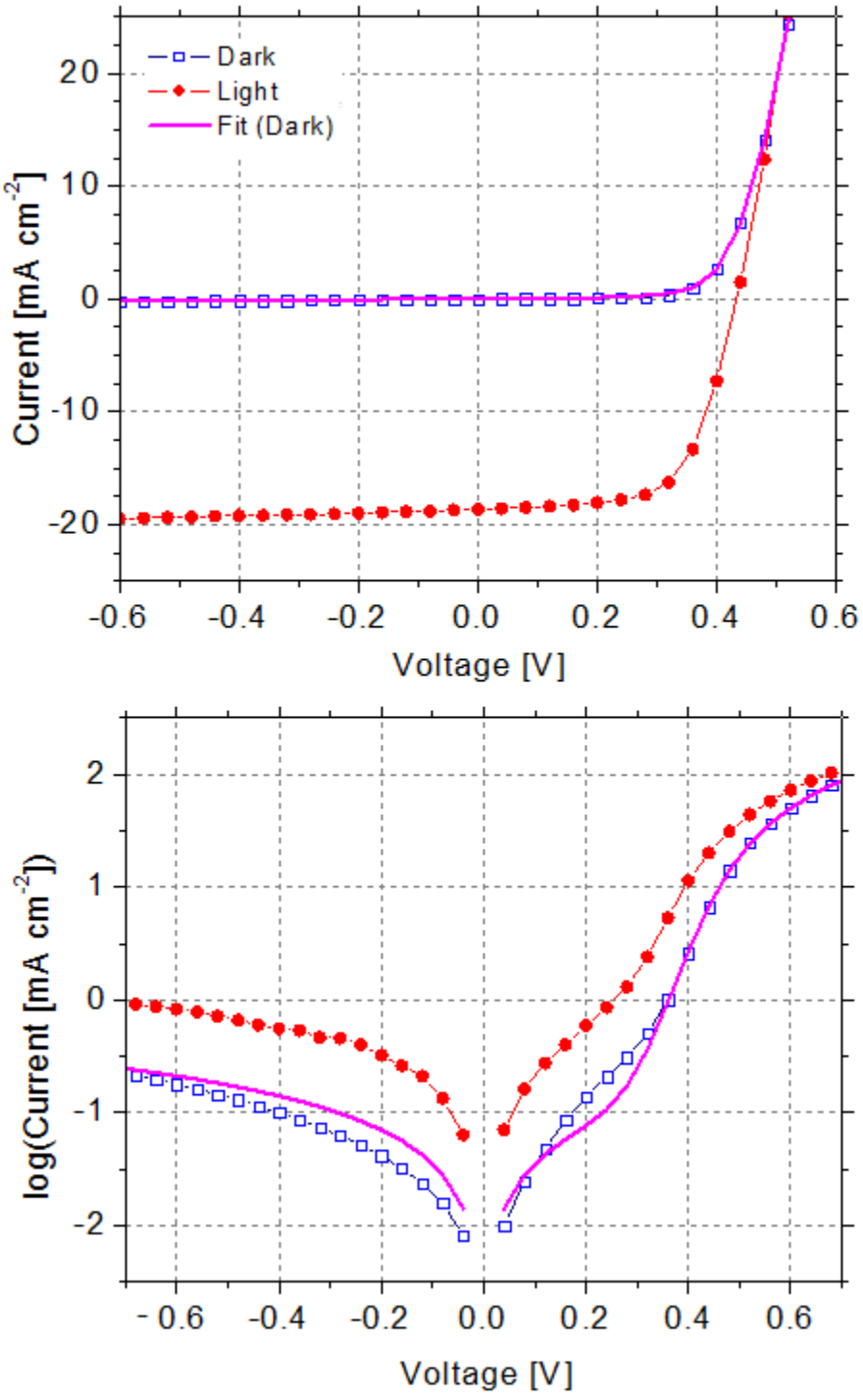


Figure 6.2: Experimental illuminated and dark J-V curves of Sample 1. The fit is determined from the dark diode curve.

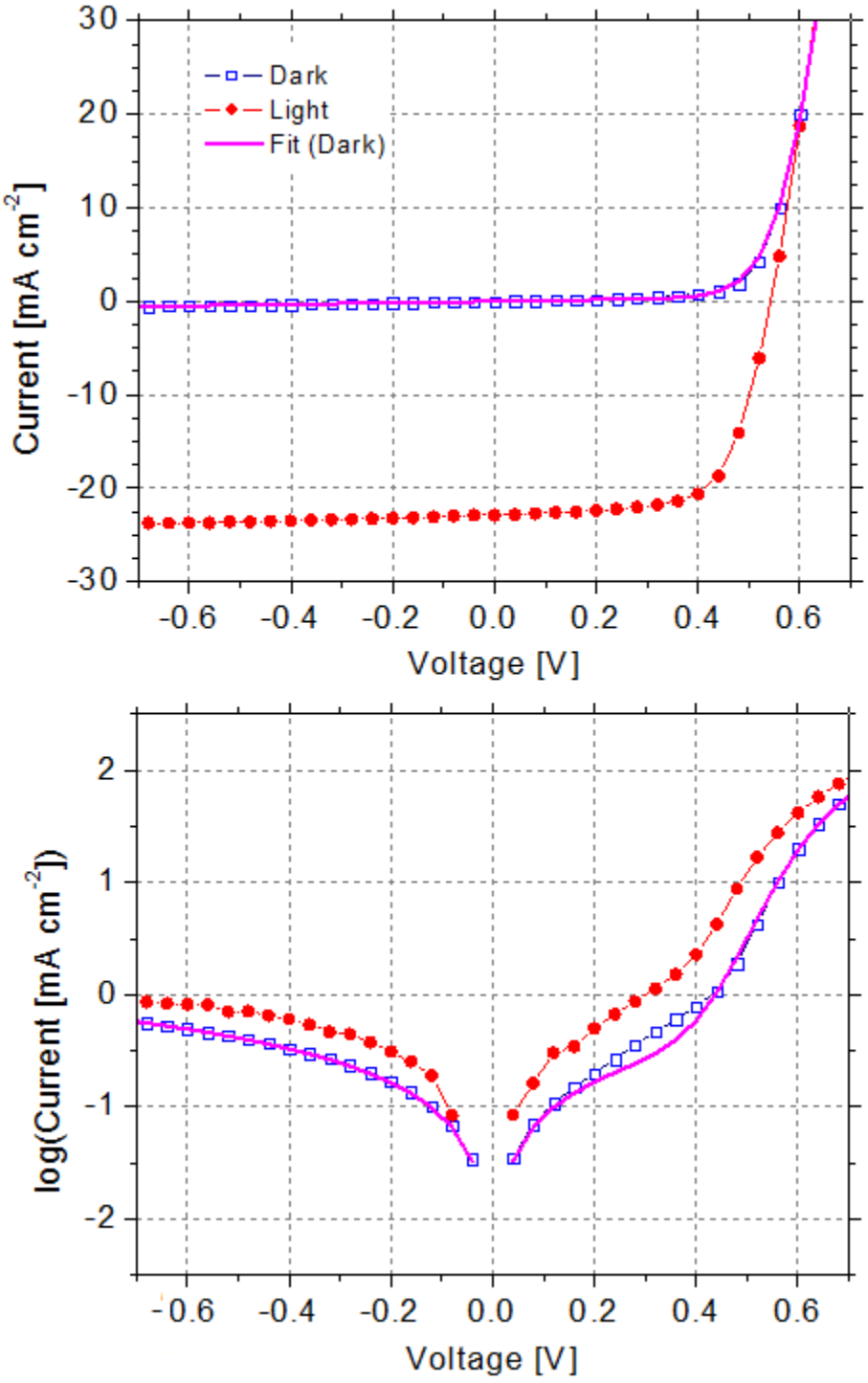


Figure 6.3: Experimental illuminated and dark J-V curves of Sample 2. The fit is determined from the dark diode curve.

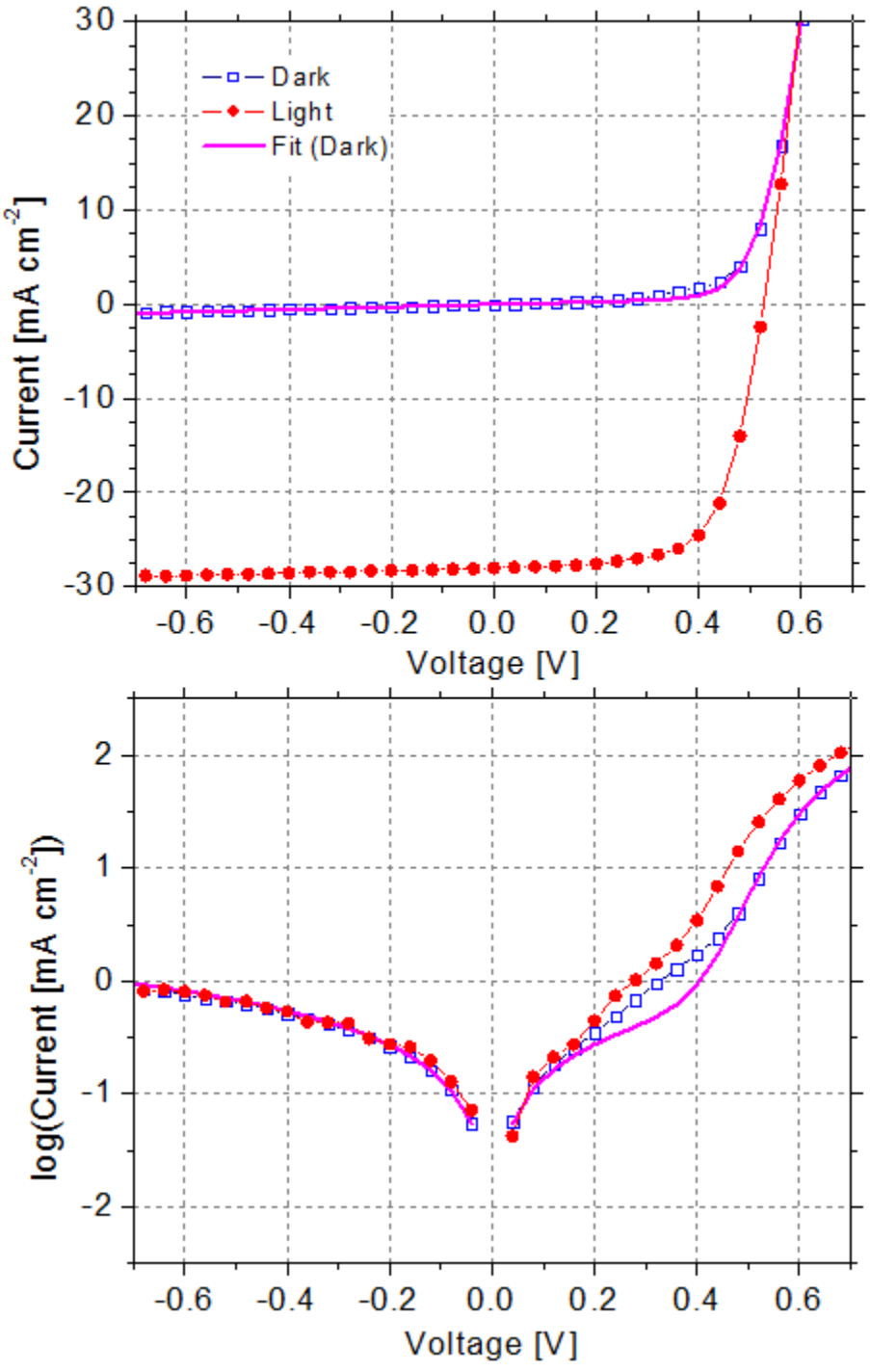


Figure 6.4: Experimental illuminated and dark J-V curves of Sample 4. The fit is determined from the dark diode curve.

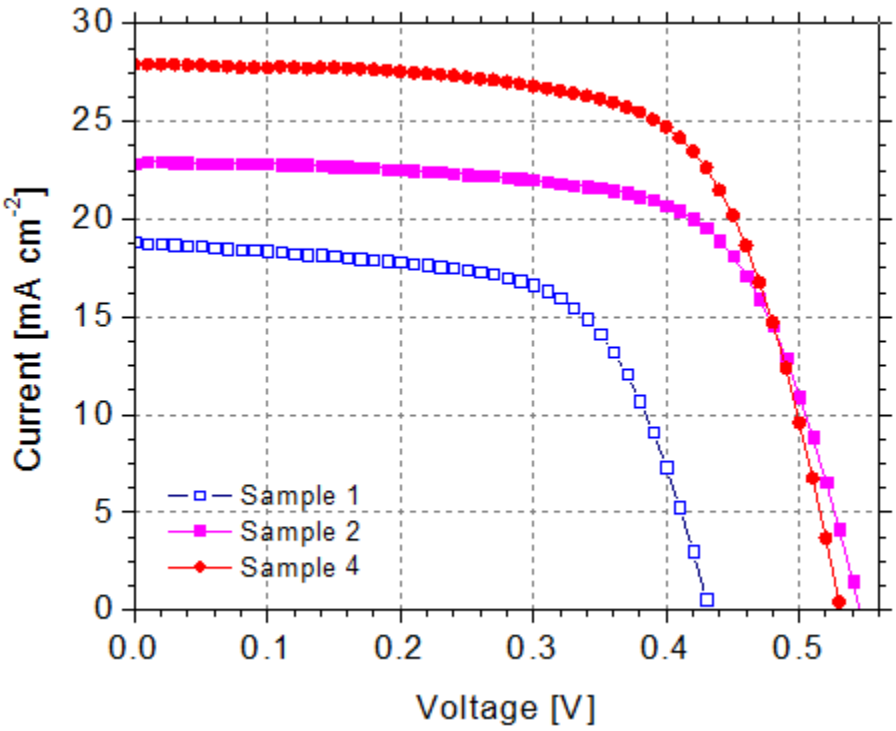


Figure 6.5: Comparison of J-V curves from Sample 1, Sample 2 and Sample 4.

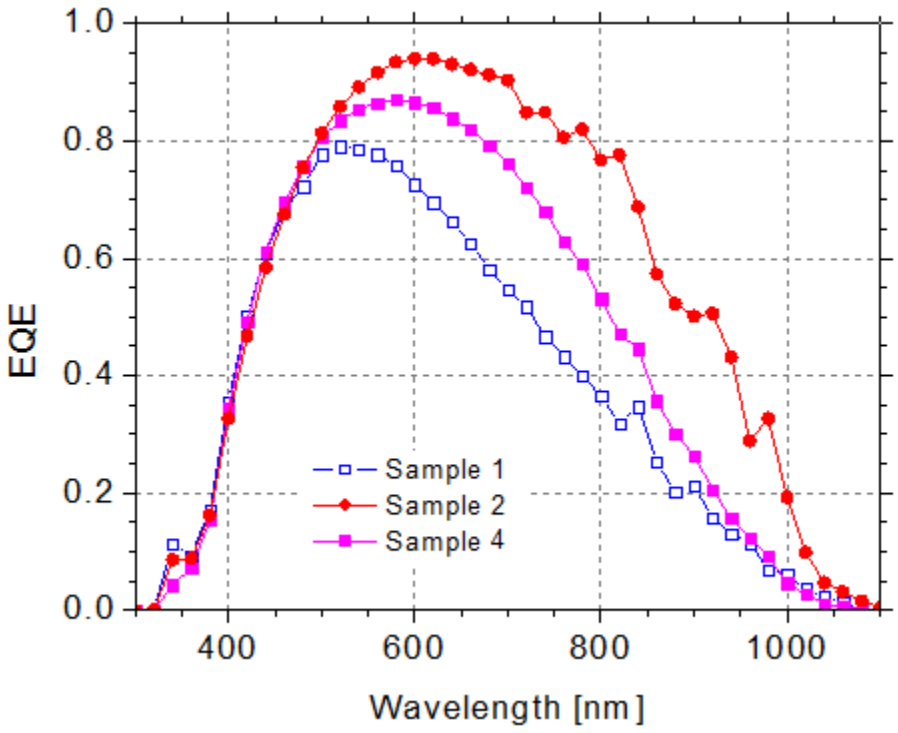


Figure 6.6: The EQE of Samples 1, 2 and 4.

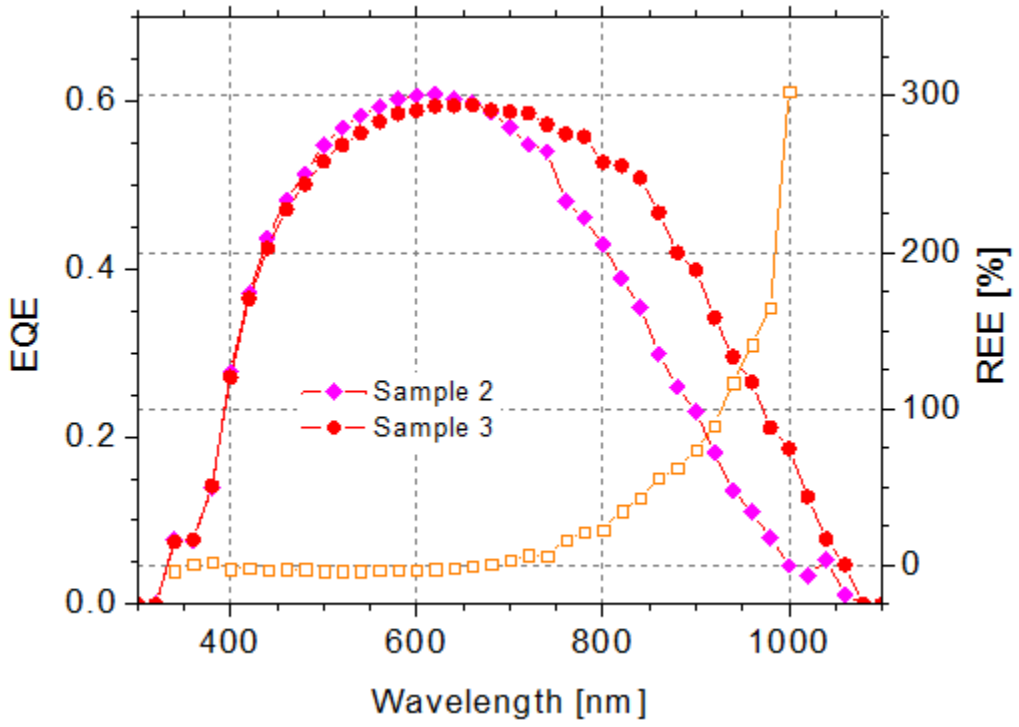


Figure 6.7: The EQE of Samples 2 and 3. This measurement was taken prior to ARC deposition on Sample 2. The EQE improvement for longer wavelengths is clearer and not affected by differences in ARCs.

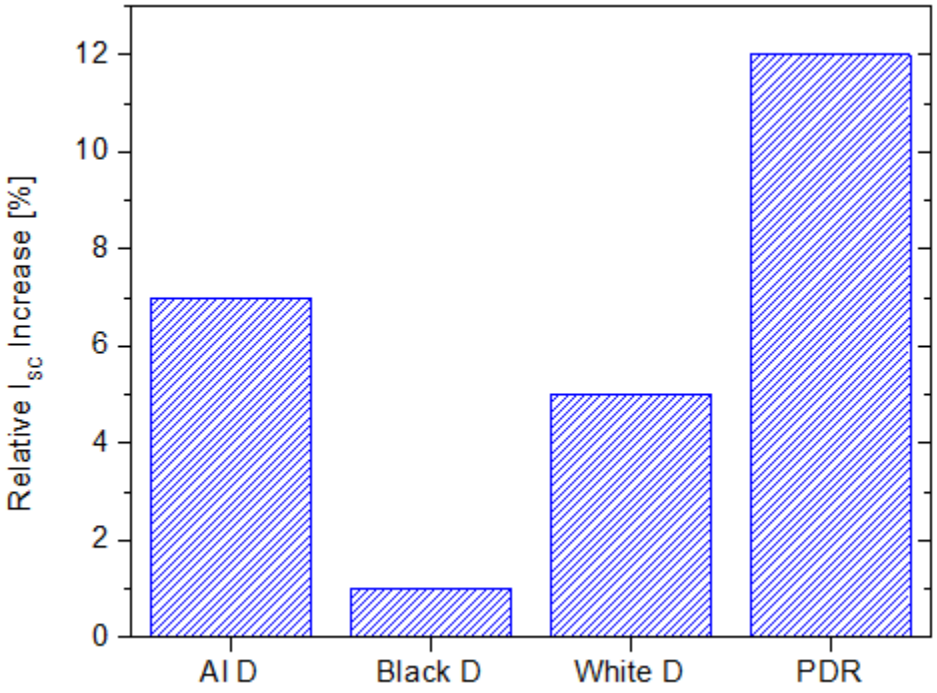


Figure 6.8: The relative increase in J_{SC} over a comparable case with a completely metallized Ti/Pt/Au rear has been plotted for a variety of rear reflector configurations using Sample 3.

Chapter 7

Discussion

This chapter will first address important observations from the experimental data and then discuss in greater detail problems encountered during the fabrication process and potential improvements.

7.1 J-V curves

This section will attempt to explain some of the important features of the J-V curves presented in the Results section. Towards this end, the simulation program PC1D is employed. Comparisons between simulations and the experimental data are intended to be more qualitative than quantitative in this regard.

7.1.1 BSF, surface recombination velocity and V_{OC}

It is clear from Figure 6.2 that Sample 1 has a very poor open circuit voltage. To remedy this, a back surface field (BSF) was employed in subsequent samples. The back surface field promotes surface passivation by providing an energy barrier at the

rear of the cell which prevents minority carriers from reaching the surface where there is a high concentration of gap state recombination centres.

The increase in V_{OC} was large, from 0.43 V to 0.55 V. However, 0.55 V can still be improved upon. At least two factors are important here: 1) surface recombination velocity (SRV) and 2) base resistivity.

To better understand the open circuit voltage increase, a comparable solar cell was simulated in PC1D. The comparable cell has a high SRV (10^6 cm/s), an ARC that gives 13% reflection, a background base doping of 7e14 cm^{-3} (20 Ω cm) and a 200 nm uniform emitter with a doping concentration of 1e19 cm^{-3}. The remaining parameters of this solar cell, and of other simulated solar cells, are given in Appendix B.

According to PC1D, if the base doping is changed to 1e16 cm^{-3} (1 Ω cm) then the V_{OC} increases markedly, see Figure 7.1. If a BSF 1 μm in thickness with a doping of 1e19 cm^{-3} is added then the V_{OC} increases to about the same value regardless of base doping. The increase is on the same scale as what was observed experimentally and the very low initial V_{OC} could be a result of a low base doping (high base resistivity). The SOI wafers had a base doping of 1 - 20 Ω cm so this seems reasonable. Figure 7.1 also shows that a large increase in current should be expected from implementing the BSF.

It is clear why the I_{SC} ought to improve with a BSF, specifically, if there are less carriers recombining at the rear surface then more carriers can be collected at the junction. It is more difficult to see why the V_{OC} should improve but a simple argument is offered. The V_{OC} is strongly dependent on J_0. The analytic equation for J_0 shows a dependence on the diffusion length of the absorber material and thus,

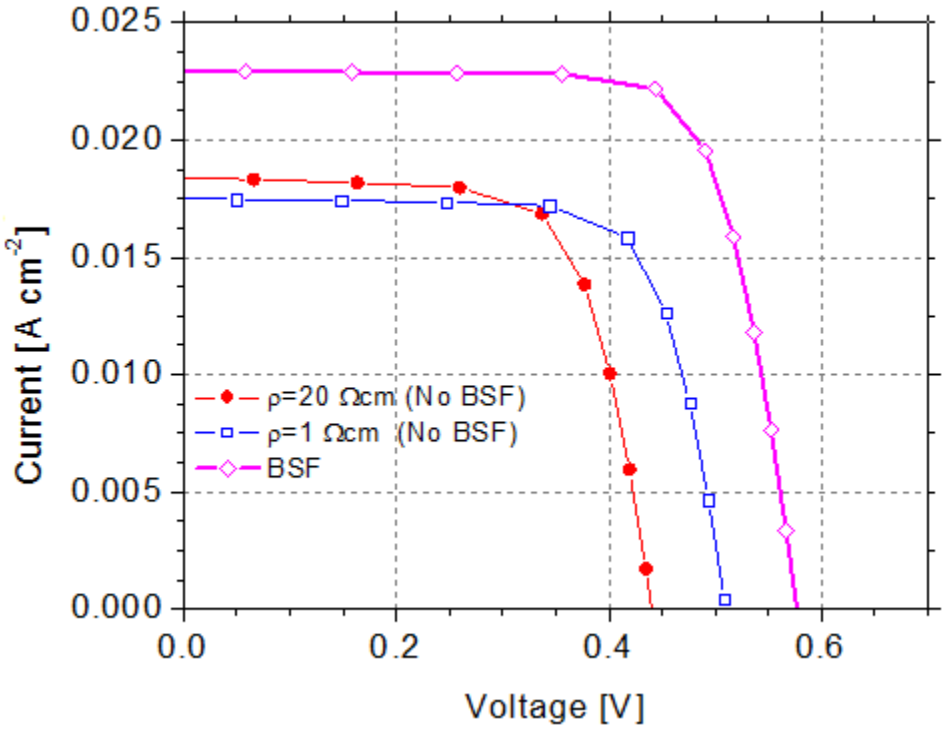


Figure 7.1: The low V_{OC} of Sample 1 may be due to high base resistivity. The addition of a BSF in the simulation increased the V_{OC} of the cell comparably to experiment.

indirectly, on the recombination in the device. The relationships are such that if the photogenerated carrier recombination is reduced then the dark saturation current decreases and V_{OC} improves.

With surface passivation added in addition to the BSF, the V_{OC} can still increase notably. Figure 7.2 shows simulated J-V data for the comparable case with the BSF and also with three other scenarios: rear surface passivation, front surface passivation and both surfaces passivated. In the simulation a passivated surface has an SRV of 100 cm/s.

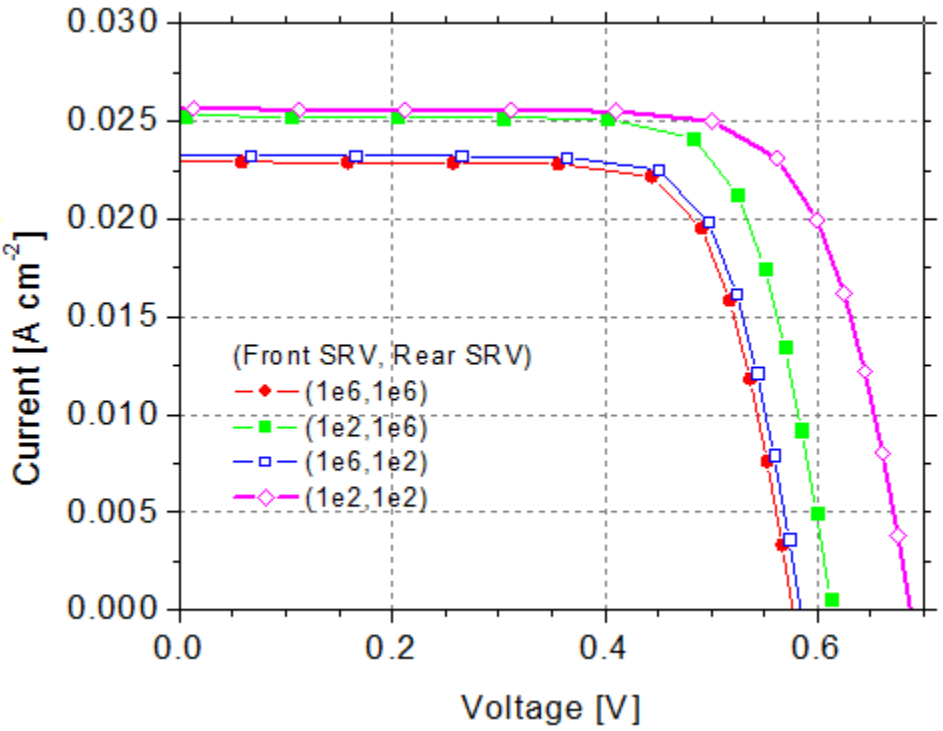


Figure 7.2: PC1D simulations suggests that passivating both surfaces in addition to the BSF can still increase I_{SC} and V_{OC} notably.

It is clear from the arguments presented in this section that low SRVs are necessary for optimal device performance. In addition to the BSF, both front and rear surface

passivation layers can greatly increase performance.

7.1.2 Deviation from superposition

It might be concluded from first glance of the linear J-V curves presented in Figures 6.2 - 6.4 that the solar cells obey the superposition principle but the semi-log plots clearly show a different curvature between dark and illuminated J-V curves. This difference is exacerbated in Sample 1, is present to a smaller degree in Sample 2 but is only minimally present in Sample 4.

A common reason for the deviation from superposition is the presence of series resistance. At low forward bias in the dark the cell does not pass much current and therefore the effects of series resistance are not obvious but under illumination, a large current may be present in this same region.

This explanation is likely to be satisfactory for Sample 2 and Sample 4 but it is useful to verify it with PC1D simulations. Using the comparable device from Figure 7.1, with high SRV and a BSF, the light and dark J-V curves were plotted on semi-log plot both with and without series resistance (Figure 7.3).

It is clear that the series resistance causes a deviation from superposition at medium to high forward bias while there is no deviation in reverse bias. This is more or less what was observed for Sample 4. However, there may be another effect present for Sample 2.

The deviation from superposition in Sample 1 can not be explained as a series resistance effect because the deviation is most pronounced in reverse bias and low forward bias. It appears as though the shunt resistance is degraded with illumination but current shunts are supposed to be independent of illumination.

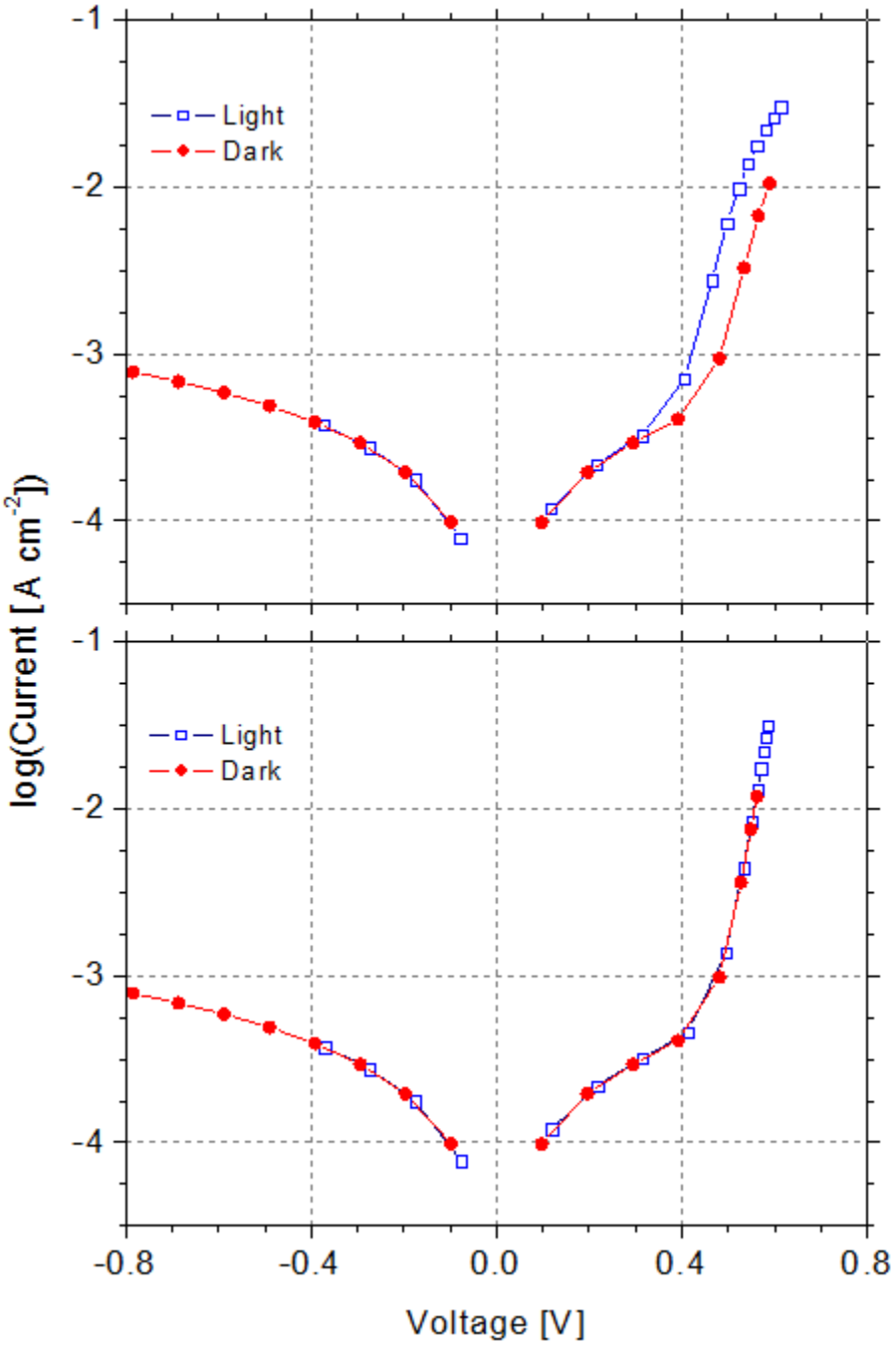


Figure 7.3: Light and dark simulated of Sample 1 J-V curve on semi-log plot with series resistance (top) and without (bottom).

It is likely that this is not actually a change in shunt resistance but something more complicated. Figure 7.4 shows the J-V results of a theoretical simulation of Sample 1, as discussed previously, but this time with and without a BSF. It appears that it is the BSF that makes this superposition deviation go away, pointing to the fact that the main issue here is the rear surface recombination velocity.

Further PC1D simulations show that this effect is present to a much a smaller degree in conventional thickness cells as well. A simple physical argument as to why the J-V curve changes shape in this way, is not readily apparent but the physics of it is contained in the semiconductor equations and gets washed out with the analytical diode expression.

The deviation from superposition of Sample 1 indicates that the 1-diode fit is probably not appropriate to describe the physics of this device. This is clear from Figure 6.2 where the fit does not appear to be good.

7.1.3 Specular vs. Diffuse Reflectors

The theory behind PDRs is discussed thoroughly in [25] and [111]. The scattering of light by a PDR is described by Lorentz-Mie theory and there are three optimization parameters: refractive index contrast between scattering particles and binder, volume concentration of pigment molecules and pigment diameter. None of these factors were considered in this thesis, where the intent was to apply a simple light-trapping structure. A white paint PDR was applied in a straightforward manner by using commercially available white spray paint.

Despite the lack of optimization the results seem quite good with a 12% short circuit current enhancement over the case of a completely metallized rear. This

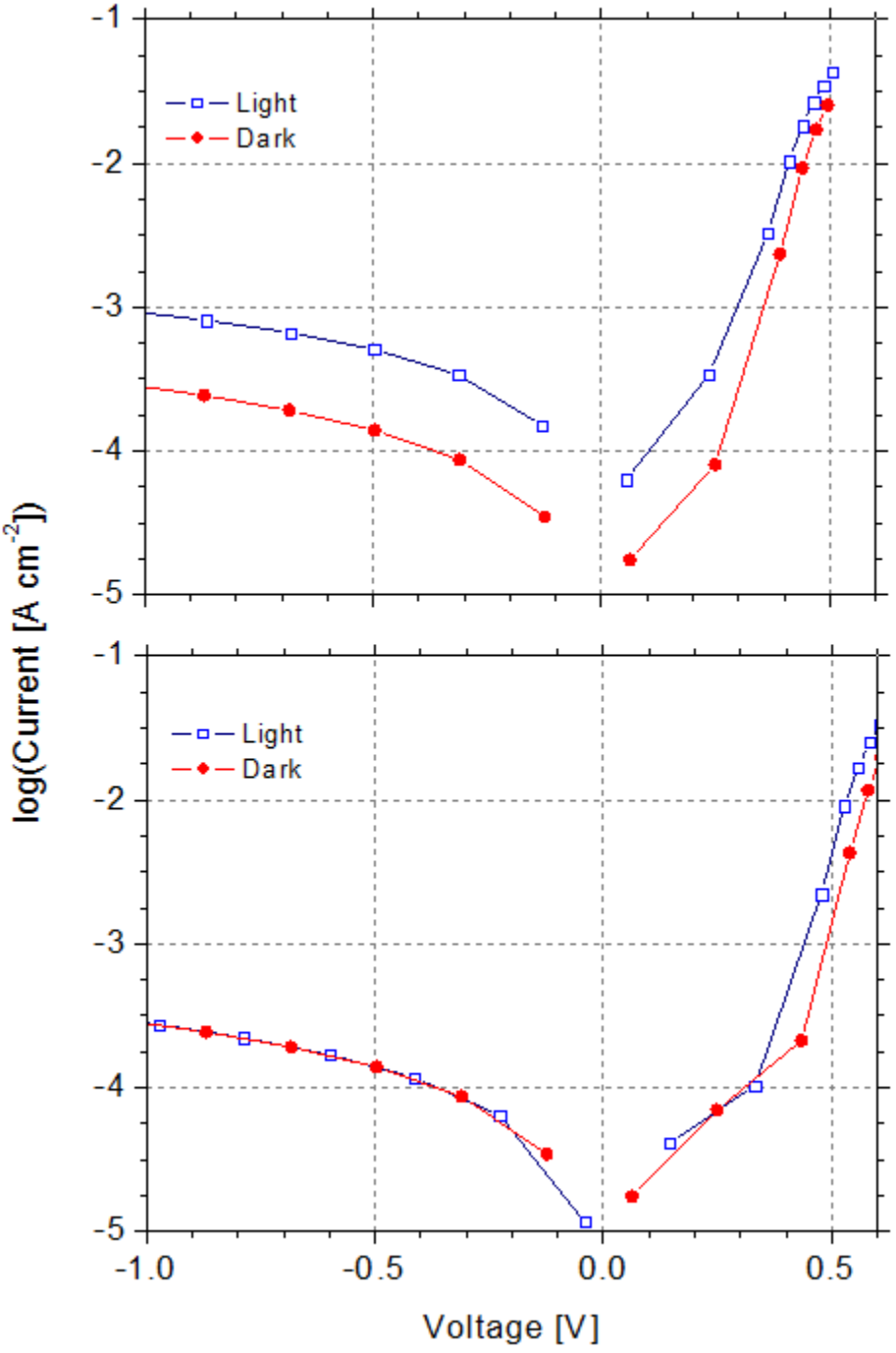


Figure 7.4: Light and dark simulated J-V curve of Sample 1 on semi-log plot without BSF (top) and with BSF (bottom).

enhancement is due to increased absorption in the longer wavelength regime because it is these wavelengths that have lower absorption and can benefit from a diffuse reflector. This is clear from Figure 6.7.

It is difficult to compare the EQE enhancement results with other light-trapping structures in the literature because often the data is available because the focus of most textures is on reducing the reflectance of conventional thick cells. EQE enhancement data is available in [25] and [111], both PDR studies, but in the former case the cell thickness is 1 - 2 μm and in the latter it is 65 - 90 μm. These results are shown in Figure 7.5 and 7.6.

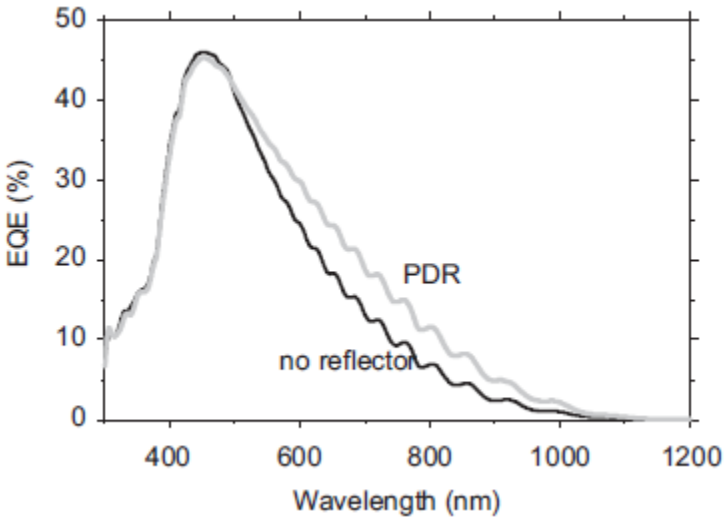


Figure 7.5: EQE plot of 1 - 2 μm thick poly-c-Si solar cell with and without PDR.

A thicker cell ought to see less of an improvement and a thinner cell more. Qualitatively, it seems that the EQE improvement seen in this thesis was comparable to that seen in [25] even though the solar cell in that study had a poorer EQE to begin with. The EQE improvement seen in [111] extended over less of the spectrum then was seen in this work which was expected because the researchers in that study used

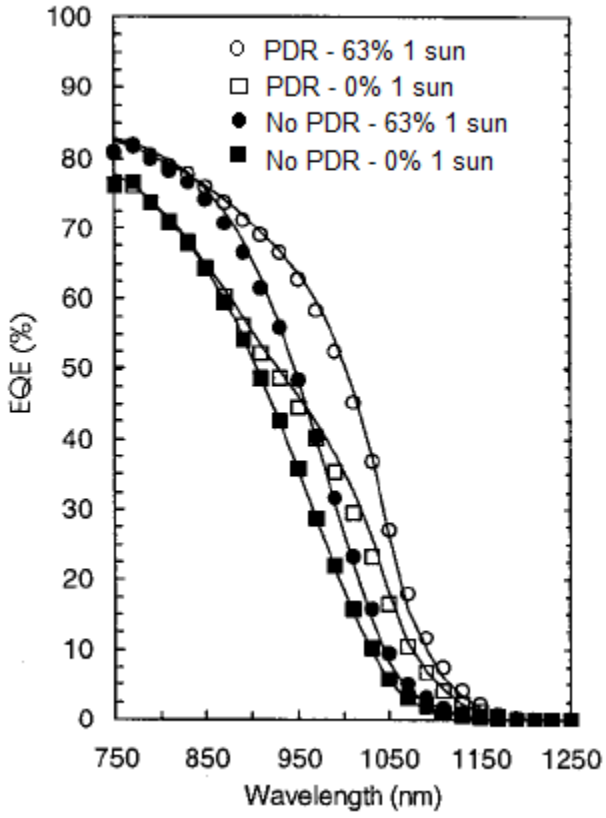


Figure 7.6: EQE plot of 65 - 90 μm thick poly-c-Si solar cell with and without PDR and at two different illumination intensities. Solid lines are theoretical predictions.

a much thicker solar cell.

A potential weakness of this experiment is that the repeatability of device performance parameters has not been established and, as a result, the lower performance of the completely metallized rear comparable case may be due to some other reason. This is most likely not the case. Firstly, the open circuit voltage of both devices (Sample 2 and Sample 4) are comparable indicating comparable electrical performance. Secondly, the trends observed agree with what was seen in [25].

In that study, the researchers looked at the short circuit current enhancement of a 1-2 μm poly-c-Si solar cell device with various rear reflectors. They observed that: 1) a completely metallized rear (Al) was slightly worse than no reflector at all, 2) a detached Al mirror yielded about a 15% short circuit current improvement and 3) a PDR yielded a 20% improvement. This was all for a planar cell. They observed a greater improvement than was seen in this experiment in part because they used a thinner cell which ought to respond better to light-trapping. However, the trend is approximately the same. The researchers also observed a 40% improvement in short circuit current by optimizing pigment volume concentration.

One of the interesting results of this experiment and that in [25] is that an Al rear reflector is actually quite poor. One might expect it to have a reflectance of above 90% when implemented as a back surface reflector. However, this is not the case. The detached black rear reflector used in this experiment would have a total reflectance of about 35% due to the Si/Air interface and this performed better than the Al back surface reflector (BSR). This indicates that the Al BSR is likely to have a reflectance below this value. Furthermore, the effect is likely to be optical and not electrical as no change in open circuit voltage was observed. This all suggests that the Al BSR is

absorbing light. This is somewhat supported by the drastic reduction in performance observed by Berger when the Al BSR was implemented with a textured substrate, allowing multiple bounces at the Al/Si interface.

7.1.4 Simulated J-V curves

It useful to verify the experimental J-V curves with simulation of comparable devices. The intent here is more to determine if the J-V curves are within reason and less so to rigorously simulate a perfectly accurate representation of the device. With this in mind simplified device structures comparable to Sample 1, Sample 2 and Sample 4 were simulated in PC1D. The specific simulation parameters are given in Appendix B.

J-V simulation results and experimental results are given in Figure 7.7. The simulated and experimental curves agree sufficiently. However, the fill factors and open circuit voltages of experimental devices seem poorer in all cases.

PC1D simulations can also provide a device performance target. From simulation, it seems possible that a device efficiency of 15.4% using reasonable parameters is possible with this device without using any light-trapping. This goes up to 16.5% with a diffuse rear reflector. To achieve this value Sample 2 or Sample 4 simulation parameters can be adjusted in the following way: a front surface reflectance of 10% (or lower), SRVs of 100 cm/s, low resistivity wafer (1 Ω cm), a strong rear-reflector (0.95) and a low series resistance (<1 ohm cm^2).

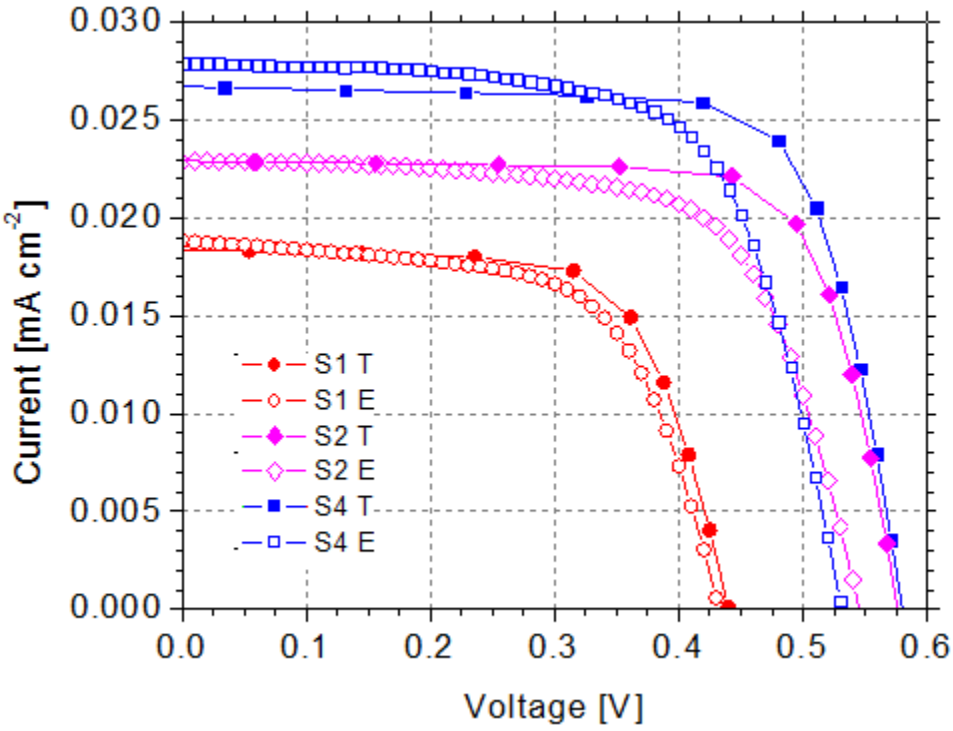


Figure 7.7: Comparison of experimental (E) and theoretical (T) J-V curves from the three samples fabricated in this thesis.

7.2 Problems encountered with process flow design and implementation

The SOI-based process flow presented in this thesis has several advantages. The membrane approach allows high-temperature dual-side processing and in essence, allows ultra-thin solar cells to be processed in the lab in almost the exact same way as with thick cells. This should allow a wide variety of high-performance design features and light-trapping to be implemented. The device thickness is easily repeatable and a range of device thicknesses are possible by using SOI wafers with varying device thicknesses. SOI wafers are available off-the-shelf at relatively low-cost to the researcher. All of the solar cell-processing is straightforward and it is not necessary to use lithography, although it still remains a possibility. Although a 10 μm sc-Si sample needs to be supported it should be easy to produce free-standing ultra-thin sc-Si wafers with larger device thickness (25 μm) using thermal oxide masking. Results thus far indicate that the 10 μm sc-Si membrane solar cell is quite robust and it should be possible to produce thinner devices.

An obvious question to ask when looking at this process flow is: why is the etching apparatus even necessary, as this step could have been done using very simple lithography? The answer is that the initial plan was to first adhere the front surface of the SOI to a glass support using a transparent epoxy because it was thought that without such a support the device would certainly break. It would then be necessary to protect the epoxy from the etching fluid as it seemed unlikely to hold up during a long KOH etching procedure. The etching apparatus was the solution. Using the etching apparatus to create a sc-Si membrane adhered to a glass support was

straightforward.

This approach had one very serious disadvantage. It was possible to dope and anneal the emitter prior to etching but the epoxy would prevent high temperature processing post-etch and that meant no BSF or other high-temperature rear-side processing. This problem was heightened by the fact that to get ohmic contact to low-doped p-type Si a heat treatment of around 400 °C is necessary. Tests suggested that the epoxy would not hold up to this temperature. Thus, it would not be possible to get good electrical contact on the rear of the solar cell.

There were two obvious solutions: 1) purchase custom implanted SOI with a BSF already in the device structure or 2) not use a permanent epoxy for the front glass support. The first solution would result in high-cost and long lead times. It seemed that the second solution ought to be attempted before resorting to the first.

The first attempts at forming a solar cell membrane with no glass support failed, with the membrane breaking. It seemed that the high etching rate used to remove the handle wafer put pressure on the membrane. To alleviate this pressure the etching rate was slowed near the end of the etch by lowering the temperature. This was sometimes successful at forming a membrane but the majority of the time it was not.

At that point, a good route forward seemed to be the use of a temporary adhesive and glass support which could be removed after the etch. Cyanoacrylate-based (ie. Superglue or Krazyglue) adhesives seemed ideal for this purpose as they could withstand the etching temperature of 95 °C but would also dissolve in acetone. This was a good solution to the membrane breakage during the etch. However, the membrane had a tendency to break during the release step.

The fundamental problem seemed to be that the membrane had a tendency to

break if it was in the etching apparatus near the end of the etch although it was difficult to discern why this ought to be the case. The solution then seemed to be to remove the sample from the etching apparatus before it reached the end of the etch. Some sort of mask could then be used to protect the front surface as the sample was etched openly in KOH. Black wax was first used for this purpose, as it is marketed as a KOH etch resist, but it was not suitable even with etching temperatures well below its softening point.

Ultimately, this led to the solution of using a thermal oxide mask formed prior to etching as has already been presented. This worked excellently.

7.3 Moving forward with process flow

This process flow has not been optimized. The main optimization variables would be the emitter/BSF implanting parameters and the post-implant annealing parameters. These were taken from a solar cell ion-implantation optimization paper [100] and this may not be the area in which to focus in terms of greatest cost/benefit.

To get a high-performance solar cell additional steps are necessary. An optimized ARC coating is necessary, perhaps weighted more to the blue end of the spectrum as all the red end will not be absorbed. This can be somewhat of an afterthought as it can simply be deposited over the metallization as the last step. The sputtered nitride ARC in Sample 1, 2 and 4 offered good current enhancement but this can be improved upon.

Surface passivation certainly is necessary to improve the V_{OC}. A thick thermal oxide could be grown post ion-implant but this would affect the junction and BSF and not allow the three-step annealing procedure which is believed to be necessary.

This oxide would need to be opened up with lithography for metallization. It is also possible to use low-temperature passivation layers like silicon nitride or amorphous silicon without disrupting the three-step anneal. These would also need to be opened up using lithography so as to metallize the cell. These approaches could combine ARC and passivation in one step.

An alternative would be to grow a thin thermal oxide during the three-step anneal by doing the 850 °C portion of the anneal in wet conditions. It should be possible to get 17.5 nm thermal oxide within 15 minutes at 850 °C [97]. This may improve the surface quality. If this were done then lithography would be needed to open up the oxide for metallization.

It is also important to consider other light-trapping structures. Non-lithographic texturing procedures could be applied post-membrane formation without difficulty. If lithography is to be used then some preliminary work would be necessary so as to determine how best to implement it on the membrane structure. Plasmonic nanotexture coatings should be possible on the front or rear without the membrane structure posing any problems.

7.3.1 Summary

With the aid of the simulation program PC1D and also, results from the scientific literature, key observation from the J-V curves of fabricated solar cells have been analyzed. The low V_{OC} of Sample 1 was described to result from a high base resistivity and a high surface recombination velocity. The V_{OC} gain by introducing a BSF was simulated and it was comparable to what was seen experimentally. Simulations also suggest that large gains in performance can be achieved by adding surface passivation

layers.

Deviations from the superposition principle were observed in all solar cells. In Sample 2 and Sample 4 the deviation could largely be explained in terms of the series resistance. Sample 1 had a much stronger deviation from superposition and it was seen to be a consequence of a higher rear surface SRV.

The results of the rear reflector experiment agree with what has been observed in the literature with the white paint PDR outperforming the metallic BSR by a notable quantity.

Simulations of comparable solar cell devices in PC1D have been conducted and suggest that the experimental solar cell J-V curves are reasonable. Using realistic parameters, PC1D simulations suggest that this device can achieve efficiencies near 15% without light trapping. Achieving this target experimentally means good front and rear surface passivation, a good ARC and rear reflector.

This chapter explained the evolution of the ultra-thin sc-Si fabrication process flow design from initial conception to final implementation. The process flow has several advantages and as it stands could be used as a platform to test light-trapping in ultra-thin sc-Si solar cells. Furthermore, several additional process steps have been proposed that have the potential to greatly increase the solar cell performance.

Chapter 8

Conclusion

Ultra-thin sc-Si solar cells, an order of magnitude thinner than is conventional, are one potential route to low-cost high-efficiency photovoltaics. To achieve this goal, advanced light-trapping strategies need to be employed to boost the absorption of long-wave radiation which is otherwise transmitted through such thin devices. Light-trapping was seen to be based on three principles: angular propagation of light inside the solar cell device, rear reflection and total internal reflection.

The angular propagation of light within the device is normally accomplished through texture. The physics of the texture depends on the texture size and periodicity. A variety of textures is under study in the literature and it is normally implemented through wet or dry etching. Rear-reflectors can be specular (ie. metallic or dielectric) or diffuse (ie .PDR or textured). Metallic reflectors were seen to be rather lossy and pigmented diffuse reflectors were seen to be quite good. Solar cells are not normally engineered to enhance total internal reflection at the front surface but nonetheless it is an important component of light-trapping.

There is a number of light-trapping structures under analysis in the literature

but rarely have these been applied to ultra-thin sc-Si devices. It is useful for the development of ultra-thin sc-Si cells to implement some of these structures in the context of actual ultra-thin solar cells. However, ultra-thin sc-Si solar cells can be rather involved to fabricate, requiring complicated procedures such as metal-assisted Si foil exfoliation, Si epitaxy on a porous Si substrate or seed layer and also, very high-energy ion-implantation. To support the investigation of light-trapping structures in actual ultra-thin sc-Si devices, this thesis developed a much simpler laboratory process flow for the fabrication of such devices.

The novel process flow is based on the formation of ultra-thin sc-Si membranes which can be processed into solar cells using conventional processing techniques. There are many advantages to this approach. Aside from its simplicity, a major advantage is that dual-side high-temperature processing is possible, something not necessarily possible with other methods. This allows a wider variety of high-performance coatings to be implemented and makes the ultra-thin membrane devices a good platform on which to test light-trapping.

Four devices were fabricated in total. Each was 10 μm thick. The best device achieved an efficiency, FF, V_{OC} and J_{SC} of 9.9%, 0.67, 0.53 V, 27.9 mAcm^{-2}. It incorporated a BSF, PDR, optimized contact pattern and an SiN_x ARC. Strong EQE improvements were seen with the addition of a BSF and a PDR.

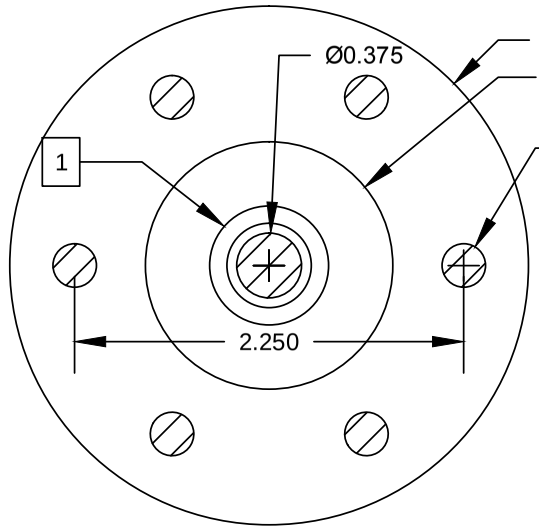
Experimental results were seen to agree reasonably well with PC1D simulations. Furthermore, simulations suggest that device efficiencies approaching 15.4% are possible with 10 μm devices without the implementation of light-trapping and up to 16.5% with a diffuse reflector. The important high-performance features include: passivation for low recombination velocity surfaces, low front surface reflection, low

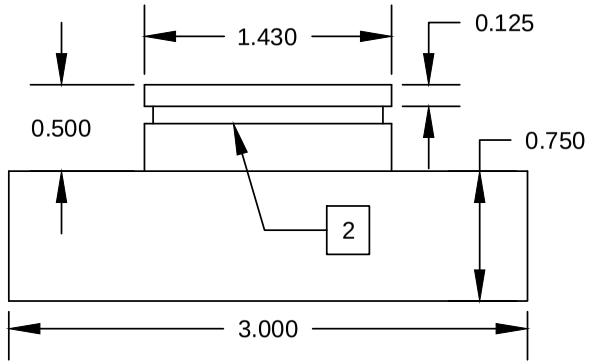
base resistivity and high rear reflection.

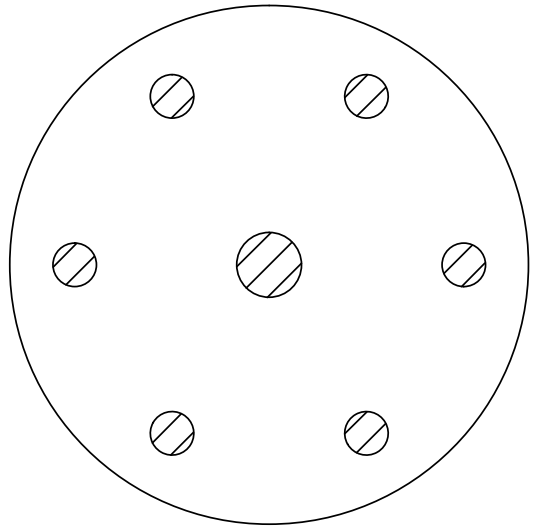
Several adjustments to the process flow were suggested for future work and may allow the ultra-thin membrane approach to reach the high-efficiency predicted by simulation. Furthermore, the device structure is already suitable as a platform to test light-trapping structures.

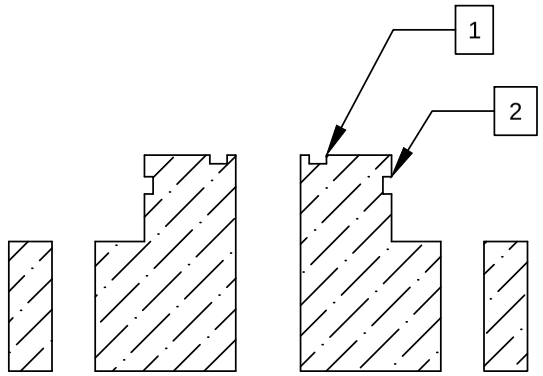
Appendix A

Etching apparatus mechanical drawings









McMaster University

Engineering Physics Dept.
1280 Main St. W, JHE A315
Hamilton, ON
L8S 4L8

Title:
Teflon Etching Jig Male Part

Drawn By:
Erik Janssen

Scale:	Date:	Drawing No:
1:1	03/11/12	2 of 5

Description:

Notes:
-Top left: Top view
-Top right: Side view
- Bottom left: Bottom view
- Bottom right: Side cross-section
(1) Groove sized for 1/16" CS o-ring with ID 0.489" (1/2")
(2) Groove sized for 1/16" CS o-ring with ID=1.301" (1-5/16")

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Engineering Physics Dept.
1280 Main St. W, JHE A315
Hamilton, ON
L8S 4L8

Title:
Teflon Etching Jig Threaded Rod

Drawn By:
Erik Janssen

Scale: 1:1

Date: 09/11/2011

Drawing No: 4 of 5

Description:
Need two of these. Part threads into Jig Female Part. Made of ¼" teflon rod stock

Notes:

McMaster University

Engineering Physics Dept.
1280 Main St. W, JHE A315
Hamilton, ON
L8S 4L8

Title:
Sample Stage

Drawn By:
Erik Janssen

Scale: 1:1

Date: 09/11/2011

Drawing No: 5 of 5

Description:

Notes:

Appendix B

PC1D simulation parameters

PC1D device simulation parameters are given in Table B.1. PC1D comes with default parameters for a Si PV device. If a parameter is not mentioned in the table then it has not been changed from the default.

Further justification for some of the choice of value for some of these parameters is here offered. The background doping of 7e14 cm^{-3} corresponds to a base resistance of approximately 20 Ω cm and is within reason. Surface recombination velocities of 1e6 cm/s are for poor quality unpassivated surfaces. Contact resistance values come from experimental values, as do shunt conductance values. External reflectance is 0.13 with an ARC as measured experimentally. Reflectance of bare Si is approximately 0.35. Internal reflectance at the front surface matches the external reflectance. It is specular. Internal rear reflectance of Sample 1 and Sample 2 is 0.35 because the metallic rear reflector is slightly worse than just a Si/Air interface. The internal rear reflectance of Sample 3 is 0.95 and diffuse because a white paint PDR is used.

Table B.1: PC1D device simulation parameters

Parameter	Sub-parameter	Units	Sample 1	Sample 2	Sample 4
Thickness	-	μm	10	10	10
First front doping	Type	-	n-type	n-type	n-type
	Profile	-	uniform	uniform	uniform
	Depth	μm	0.2	0.2	0.2
	Concentration	cm^{-3}	1e19	1e19	1e19
Background doping	Type	-	p-type	p-type	p-type
	Concentration	cm^{-3}	7e14	7e14	7e14
First rear doping	Type	-	-	p-type	p-type
	Profile	-	-	uniform	uniform
	Depth	μm	-	1	1
	Concentration	cm^{-3}	-	1e19	1e19
Front Surface SRV	n & p	cm/s	1e6	1e6	1e6
Rear Surface SRV	n & p	cm/s	1e6	1e6	1e6
Area	-	cm^2	1	1	1
Texture	-	-	no	no	no
Contact Resistance	Emitter	Ω cm^2	2.16	1.38	1.40
	Base	Ω cm^2	0	0	0
Shunt Conductance	-	Ω cm^2	0.00035	0.00082	0.0014
External Reflectance	Front	-	0.13	0.13	0.13
Internal Reflectance	Front	-	0.13	0.13	0.35
	Rear	-	0.35	0.35	0.95 (diffuse)

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