

LATERAL DIFFUSION LPE GROWTH OF SINGLE CRYSTALLINE
SILICON FOR
PHOTOVOLTAIC APPLICATIONS

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PHOTOVOLTAIC APPLICATIONS

By

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A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfillment of the Requirements

for the Degree

Doctor of Philosophy

McMaster University

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DOCTOR OF PHILOSOPHY (2012)
(Engineering Physics)

McMaster University
Hamilton, Ontario

TITLE: Lateral Diffusion LDLPE Growth of Single Crystalline Silicon

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NUMBER OF PAGES: XVI, 158

Abstract

The success of the solar cell industry in the last decade is attributed to technology improvement and cost reduction. Thin film solar cells comprise an increasing market share because they have the advantage of low cost over crystalline silicon technologies. However crystalline silicon solar cells dominate the market, due to the mature silicon based integrated circuits technologies and the well understood knowledge of silicon. Among all the commercial low cost solar cells, single crystalline silicon solar cells have the highest efficiency record of 21%.

A modified liquid phase epitaxy (LPE) technique, called lateral diffusion LPE (LDLPE), is invented for low cost and high efficiency solar cell applications. Potentially, LDLPE is able to produce single crystalline silicon wafers directly from the raw material, rather than cutting wafers from single crystalline silicon ingots, therefore reducing the cost by avoiding the cutting and polishing processes.

By using a traditional LPE method, the silicon is epitaxially grown on the silicon substrate by cooling down the saturated silicon/indium alloy solution from a high temperature. The silicon precipitates on the substrate since its solubility in the indium solvent decreases during the cooling process. A SiO₂ mask is formed on the (111) substrate with 100µm wide opening windows as seedlines. Silicon is epitaxially grown on the seedline and forms thick epitaxial lateral overgrowth (ELO) layers on the oxide mask. The ELO layers are silicon strips with an aspect

ratio of 1:1 (width: thickness), approximately. The strip grows both laterally in width and vertically in thickness.

The concept of LDLPE is to intentionally block the silicon diffusion path from the top of the seedline, but leave the lateral diffusion path from the bulk indium melt to the seedline. Theoretically, by using the LDLPE method, the silicon strip should have a larger aspect ratio, because the laterally growth in width is allowed but the vertical growth in thickness is limited. In addition, single crystalline silicon wafers can be achieved if the strip grows continuously.

A graphite slide boat is designed to place a plate over the seedline to block the diffusion path of silicon atoms from the top of the seedline. After one growth cycle, silicon strips grown by LDLPE are wider than LPE strips but have similar thicknesses. The aspect ratios are increased from 1:1 to a number larger than 2:1. A Monte-Carlo random walk model is used to simulate the change of LDLPE strip aspect ratio caused by placing a plate over the seedline. Strips grown on single seedline substrate have rougher surfaces than those grown on multiple seedline substrates. Because the small growth area on single seedline substrate cannot accommodate the large supersaturation, which could cause terraces and vacancies on the silicon strip.

Wetting seedline by indium melt is very critical for a successful growth. Due to the small space between the plate and seedline and the surface tension of the indium melt, the indium melt cannot flow into the small space. A pre-wetting

technique is used to fill the space prior to loading the graphite boat into the tube furnace and solve the wetting problem successfully.

The structure of a LDLPE silicon strip is characterized by X-ray diffraction. The electrical properties are characterized by Hall Effect measurement and photoconductive decay measurement. LDLPE silicon strips are (111) orientated single crystal and are the same orientation as the substrate. For the growth temperature of 950°C, the LDLPE strip has an estimated effective minority carrier lifetime of 30.9 μ s. The experimental results demonstrate that LDLPE is feasible for photovoltaic application if continuous growth and scaling up can be achieved.

Acknowledgements

I would like to express the deepest appreciate to my supervisor Dr. Adrian Kitai, whose enthusiasm encouraged me throughout the project, made every step exciting and enjoyable. His wealth of knowledge and optimism made me learn even from failures. I would to say, this thesis could not have been completed without his valuable guidance and support. His personal fascination has a profound impact on me, which is believed to be greatly positive for my future career and life. I would also like to thank the members of my supervisory committee: Dr. Ray LaPierre and Dr. Rafael Kleiman for their support and helpful suggestions.

I would like to thank the staff of the Department of Engineering Physics and members of Center of Emerging Device Technology who provided technical support throughout my years in graduate school.

In the end, I would like to dedicate this thesis to my wife, Shasha Zhao and my parents as a special gift to appreciate their unconditional support and understanding.

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Table of Abbreviations

Acronym	Definition
UV	Ultraviolet, wavelength 10nm-400nm
TCO	Transparent Conductive Oxide
ITO	Indium Tin Oxide
VTD	Vapor Transport Deposition
CSS	Closed Space Sublimation
PVD	Physical Vapor Deposition
RF	Radio Frequency (5-30MHz)
VHF	Very High Frequency
ARC	Anti-reflection Coating
EFG	Edge-defined Film-fed Growth
ZMR	Zone Melt Recrystallization
LTP	Layer Transfer Process

Chapter 1. Introduction

1.1 Commercialized Semiconductor Growth Techniques for Photovoltaic Applications

Among several types of photovoltaic technologies currently in use for PV solar panels, two have become the most widely adopted: crystalline silicon solar cells and thin film solar cells. If one classifies these technologies by the semiconductor materials and their growth methods, the major market players are single-crystalline silicon (sc-Si), multi-crystalline Si (mc-Si), cadmium telluride (CdTe) thin film, copper indium gallium selenide (CIGS) thin film and amorphous Si (a-Si) thin film.

Development of thin film solar cells is one of the solutions to reduce the cost in materials and energy during the production processing thin film solar cells are made by depositing thin layers of semiconductor material on various substrates, usually on glass and stainless steel.

1.1.1. Cadmium Telluride Thin Film

Cadmium telluride is a compound semiconductor material with a 1.44 eV(300K)[1] direct band gap which corresponds to an infrared wavelength of about 860nm. It ideal for making solar cells since the CdTe material can absorb sunlight in the range from near-infrared to UV, where the sunlight distributes the most energy. Cadmium is a hazardous heavy metal material which is mostly

obtained as a by-product of zinc refining. However CdTe is a chemical stable compound material and it is proved that there is no cadmium emission during standard operation of CdTe PV systems and negligible cadmium emission even in exceptional cases like accidental fire or broken panels[2]. Therefore, considering the low cost process introduced below, CdTe is an ideal material for PV applications.

CdTe is usually a p-type material which is used for the absorber layer, and a low resistance, n-type, wide band gap material is required as the window material. The most widely used window material cadmium sulfide (CdS) which has a band gap of 2.42 eV (transparent for wavelengths longer than 520nm). Therefore the CdTe-based thin film solar cell is normally a hetero-junction device. The typical structure consists of glass/SnO₂/CdS/CdTe/back contact and it is shown in Figure 1.1.

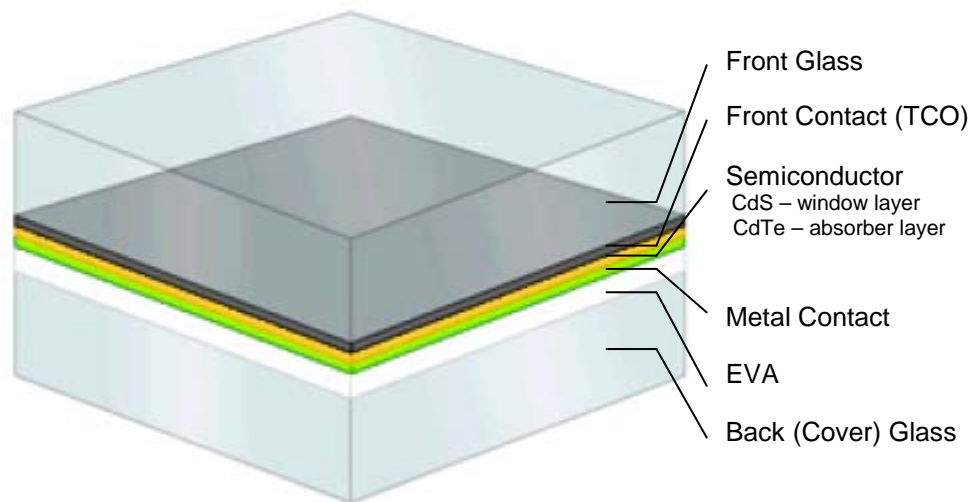


Figure1.1 Device structure of CdTe thin film solar cell[3]

The processing sequence is: a transparent conductive oxide film(TCO) is deposited on the glass substrate by sputtering; the window layer, a thin film of CdS is then deposited and then followed by a heat treatment in a reducing atmosphere (H_2 or HCl) or in the presence of $CdCl_2$; then, the absorber layer p-type CdTe thin film (1.5-3.0 μm) is deposited on the CdS layer, and a post-deposition heat treatment with $CdCl_2$ is required to promote recrystallization and increase the minority carrier lifetime[4-6]; finally, the metal back contact is deposited on the CdTe thin film.

Varieties of deposition techniques are used for CdTe thin film solar cell fabrication. The CdS window layer can be deposited by using closed space sublimation (CSS) and chemical-bath deposition (CBD) method. CdTe film is typically deposited at a substrate temperature between $550^\circ C$ and $650^\circ C$ for high-performance devices (i.e., 14%-16% efficiency). 12% efficiency cells are also made at a substrate temperature of $\sim 400^\circ C$. Because CdTe is a near congruent sublimating material, commercialized CdTe thin film cells are mostly fabricated using very low cost CSS (Antec Solar)[7-9] and VTD (Vapor Transport Deposition) (First Solar) methods[3, 10, 11]. The device-quality CdTe absorber layer is deposited at a very high deposition rate (tens of $\mu m/min$) [3, 7-11]. Electrodeposition, MOCVD, screen printing, PVD and sputtering are also used in research and achieve cell efficiency from 10% to 14%[3].

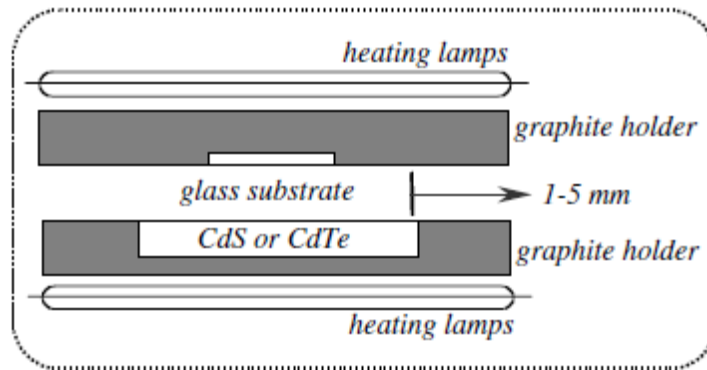


Figure 1.2 Conceptual schematic of the CdTe/CdS close space sublimation process[12]

The concept of the CSS process is shown in figure 1.2. The CdS CSS deposition is carried out at a pressure of a few torr in an atmosphere composed of Ar and O₂. The sublimation source (CdS or CdTe) is evaporated at a very small distance from the substrate (a few millimeters). The gas phase CdS/CdTe precipitates on the substrate with CdO and/or CdSO₃ in the grain boundary and on the CdS surface. The oxide in the grain boundary is helpful for grain boundary passivation, and the oxide on the CdS surface has to be removed by H₂ treatment in order to allow CdS to interact with CdTe and form a CdS/CdTe junction.

The concept of the VTD process is shown in figure 1.3. The VTD system is usually operated at a pressure on the order of 10 torr with an inert carrier gas (N₂ or Ar). The CdTe source is heated to a temperature around 850°C and sublimated. The gas phase CdTe saturates the carrier gas and is brought to the glass substrate which is much cooler than the CdTe source (400~550°C). Since

the saturation pressure of CdTe decreases by approximately by one order of magnitude per 100°C[13], the CdTe is rapidly deposited on the substrate and the gas phase CdTe is depleted at the outlet of the carrier gas.

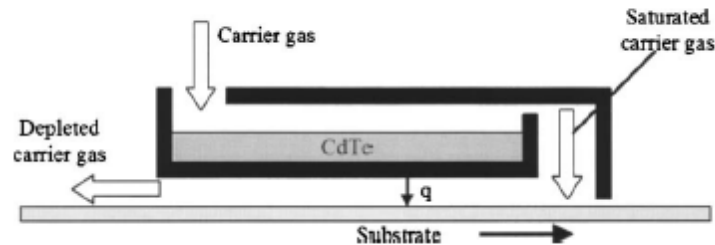


Figure1.3 Conceptual schematic of the CdTe vapor transport deposition process[13]

1.1.2 Copper Indium Gallium Selenide (CIGS) Thin Film

CuInSe_2 and CuGaSe_2 are chalcopyrite compound semiconductor materials with bandgaps of 1.0eV and 1.7eV respectively. The compound material $\text{Cu}(\text{In}_x\text{Ga}_{1-x})\text{Se}_2$ can be alloyed to obtain an intermediate bandgap around 1.15eV[14]. Thin film CIGS solar cells combine the low cost advantage of thin film technology with the efficiency and stability of conventional crystalline silicon solar cells. CIGS solar cells hold the highest efficiency (over 20%)[15] record among all thin film technologies, and the commercialized CIGS solar cell modules made with a low cost process achieve an efficiency over 12%[16]. All these features caused CIGS to attract intense interest and research, and promise it a growing PV market share.

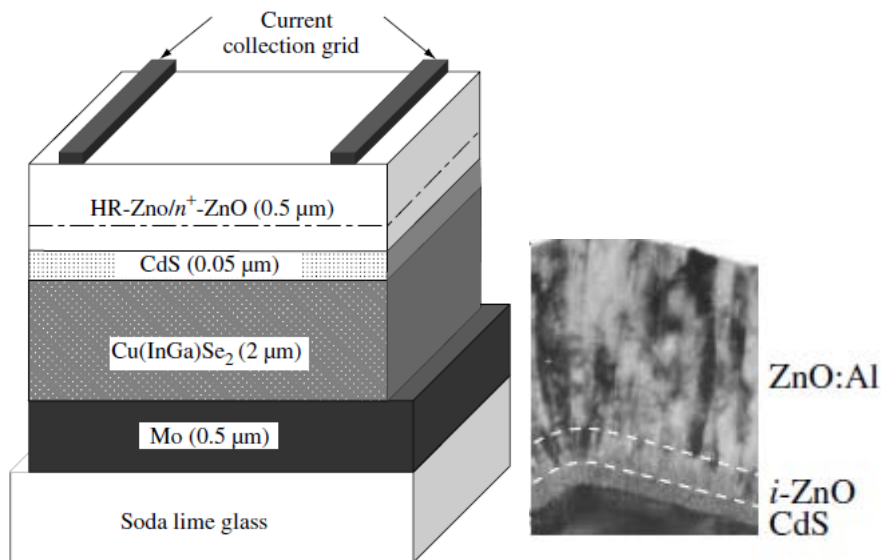


Figure 1.4 Typical device structure of the Cu(InGa)Se₂ solar cell [17]

Although a variety of processing technologies are employed, all CIGS solar cells are fabricated around a Cu(InGa)Se₂/CdS junction on a substrate with a Molybdenum (Mo) back contact. Besides polyimide and stainless steel which are used as flexible substrate, soda lime glass is the most widely used substrate for CIGS solar cells, since an intentional sodium diffusion from the soda lime glass can improve the cell performance [18, 19]. Figure 1.4 shows the typical structure of a Cu(InGa)Se₂ solar cell schematically. Mo is sputtered on the substrate functioning as the back contact. After Cu(InGa)Se₂, a thin layer (no more than 50nm) of CBD-CdS is deposited on the Cu(InGa)Se₂ to form the junction. Then two ZnO layers are deposited by sputtering or chemical vapor deposition (CVD): a buffer layer of high resistivity ZnO followed by a TCO (transparent conductive oxide) film of doped highly conductive ZnO. Finally, a metal electrode is deposited for current collection or device interconnection.

There are many approaches for the depositing the $\text{Cu}(\text{InGa})\text{Se}_2$ absorber layer, however two of them are considered as the most promising approaches which have been used to demonstrate high device efficiency, low cost and are implemented in pilot scale manufacturing.

The first approach is vacuum coevaporation, scaled up for production by Ascent solar, Würth Solar etc[16, 20, 21]. An efficiency of 12% has been achieved. It is a single growth process, in which all the constituents Cu, In, Ga and Se can be evaporated simultaneously to form the $\text{Cu}(\text{InGa})\text{Se}_2$ alloy on the substrate heated to $400\sim 600^\circ\text{C}$ [15, 18, 19].

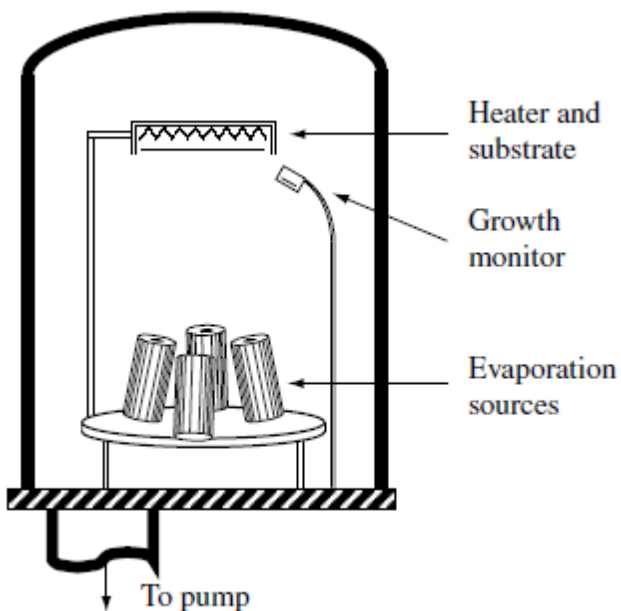


Figure 1.5 Conceptual schematic of $\text{Cu}(\text{InGa})\text{Se}_2$ multisource coevaporation system[22]

Figure 1.5 illustrates the concept of the $\text{Cu}(\text{InGa})\text{Se}_2$ coevaporation system in which Cu, In, Ga, Se are delivered from independent evaporation

sources. Each of the four sources is designed for each element with a specific evaporation temperature. The typical temperature ranges are 1300°C to 1400°C for Cu, 1000°C to 1100°C for In, 1150°C to 1250°C for Ga and 300°C to 400°C for Se. The deposition process may include a specific evaporation sequence and the evaporation flux for each element can be time dependent. The deposition rates can vary from 20~200 nm/min for a Cu(InGa)Se₂ film thickness of 2µm.

The second approach is usually referred to as two-step processing or selenization. Generally, a metal precursor thin film is deposited on the Mo coated substrate followed by a Se containing atmosphere (H₂Se or Se vapor or H₂Se/H₂S) followed by annealing/reaction. The precursors usually are in the form of Cu/In alloy or bilayer (Cu-Ga alloy/In) or trilayer (Cu/Ga/In), or even a stacked multilayer of Cu/Ga/In[23], and the precursor layer can be deposited by various methods, such as sputtering, electrodeposition[24], screen printing[25], and thermal or electron beam evaporation[26]. However, sputtering is the most attractive for precursor deposition and is adopted by Solar Frontier (subsidiary of Showa Shell Sekiyu K.K), Avancis etc. for commercialized CIGS solar cells production[27, 28]. Sputtering equipment is well developed commercially and is able to produce good uniform thin films over large scale areas with high deposition rates.

1.1.3. Amorphous Si Thin Film

Device grade amorphous Si (a-Si) is actually a hydrogenated a-Si or hydrogen/a-Si alloy in which the hydrogen passivates the dangling band defect in the a-Si therefore significantly improving the electrical properties. The hydrogen/a-Si alloy usually is referred as a-Si:H, however a-Si is also recognized as a-Si:H, since non-hydrogenated a-Si is seldom studied.

The a-Si thin film deposition becomes a competitive technology for photovoltaic applications for many reasons. First of all, this material has many interesting properties. For example, due to the direct bandgap, it has a high absorption coefficient in the visible solar spectrum range and is able to absorb 90% of usable solar energy in a thickness of 1 μ m. Second, a-Si thin film large scale manufacturing (up to 5.7m²) can be realized by plasma enhanced chemical vapor deposition (PECVD)[29]. Third, but not the least important reason, the a-Si thin film PECVD technology has been well studied and widely adopted for commercial large scale production, mainly for thin film transistors on liquid crystal displays. Therefore, the deposition technology and equipment is ready for production and no extra research and development costs are needed. Furthermore, flexible a-Si solar cells on metal foil and Polyimide substrates can be made because PECVD is a low temperature process, and the substrate temperature is usually between 150°C and 350°C

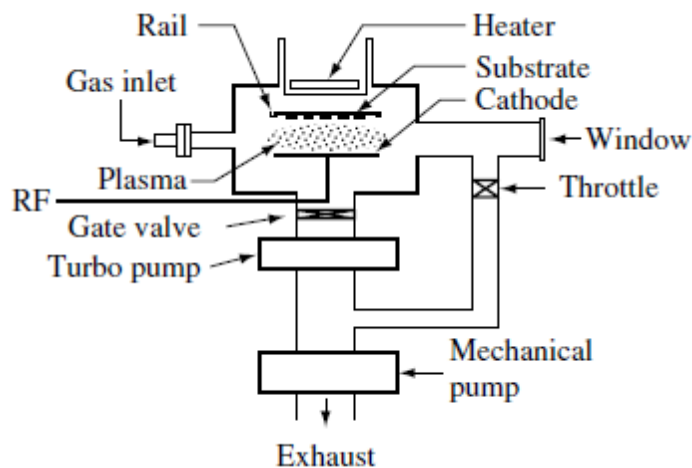


Figure 1.6 Schematic of a typical RF PECVD system[30]

Figure 1.6 shows the schematic of a typical RF PECVD system which is the most popular technique for a-Si deposition among all PECVD techniques (such as: DC PECVD, VHF PECVD, microwave PECVD). Turbo-molecular pumping ensures a good background vacuum. The pressure is then set by the pressure control system and source gas delivery system to be in the range of 0.05 to 2 Torr[30]. After a series of physical and chemical reaction processes including source gas diffusion, electron impact dissociation, gas-phase chemical reaction, radical diffusion, the a-Si is deposited on the substrate.

Solar cells based on a-Si employ many structures, for example, the p-i-n, multi-junction, and tandem junction. All these structures which consist of different a-Si alloys and doped a-Si layers can be obtained by PECVD deposition using a mixture of SiH₄ and other gases. For example, dilute H₂ is used for hydrogenated a-Si, GeH₄ is used for a-SiGe/a-Si heterojunction, phosphine (PH₃) is used for p-

typed doping and diborane (B_2H_6) is used for n-type doping. Although the source gas composition can be adjusted in real time and all different layers can be deposited in a single chamber, multi-chamber PECVD system is used in industry for large-scale manufacturing to improve throughput and yield.

1.1.4. Crystalline Silicon wafers

Silicon is the second most abundant material on the earth and it is a 1.1eV indirect bandgap semiconductor. Thanks to the development of the semiconductor industry, silicon has been well studied and the manufacturing processes from mining to wafer have been well established. Because of these benefits from the semiconductor industry, crystalline silicon solar cells dominate the photovoltaic market.

Silicon exists in the form of a compound with oxygen, forming silica and silicates. Solar grade silicon production mainly follows the routine adopted by semiconductor grade silicon production: 1) metallurgical grade silicon, typically with a purity over 98.5%, is produced by the carbothermic reduction of silica, 2) metallurgical grade silicon is crushed into fine particles (in the 40 μ m range) and then used to prepare volatile silicon hydride, trichlorosilane or silane ($SiHCl_3/SiH_4$) which are then purified by fractional distillation[31]; 3) high purity polycrystalline silicon is produced by decomposition of the silicon hydride, usually by the Siemens process (using $SiHCl_3$) or Union Carbide process (using SiH_4)[31, 32].

The solar grade poly-Si is then made into solar cell wafers, single-crystalline (sc-Si) or multi-crystalline (mc-Si). At the early stage, the Si solar cell wafers were mainly single-crystalline. Because the microelectronic industry upgraded single crystal production equipment for large wafers, the small size equipment used for PV industry is at an attractive price. As the PV market grows, specific crystal growth equipment are designed and used for solar cells, especially multi-crystalline production equipment.

Single-crystalline Si ingots are made through two approaches: Czochralski (CZ) and Float Zone (FZ). Figure 1.7(a) shows the schematic of the sc-Si CZ puller and basic principle. The CZ puller consists of a vacuum chamber, hyperpure quartz crucible in which the feedstock, solar grade silicon is melted, RF heating coils, and a thermal shelter which helps to stabilize the temperature and reduce energy loss. After the feed stock silicon is completely molten and the temperature of the melt is stabilized to achieve the required temperature, a seed crystal, usually $\langle 100 \rangle$ for PV, is dipped into the melt. Then the seed is slowly withdrawn vertically associating a proper rotation at the meanwhile, the liquid Si crystallizes at the interface of the melt and the seed crystal. Shortly before the seed grows to the desired diameter, the pulling velocity is raised to the specific value at which the crystal grows with the desired diameter. During the CZ sc-Si pulling process, the pulling velocity, rotation speed and an argon inert atmosphere (5-50 mbar) must be precisely controlled to ensure a success growth[33]. The standard pulling speeds in the ingot body range is 0.5-

1.2mm/min and the diameter of the crystal for solar cells is chosen between 100-150mm.

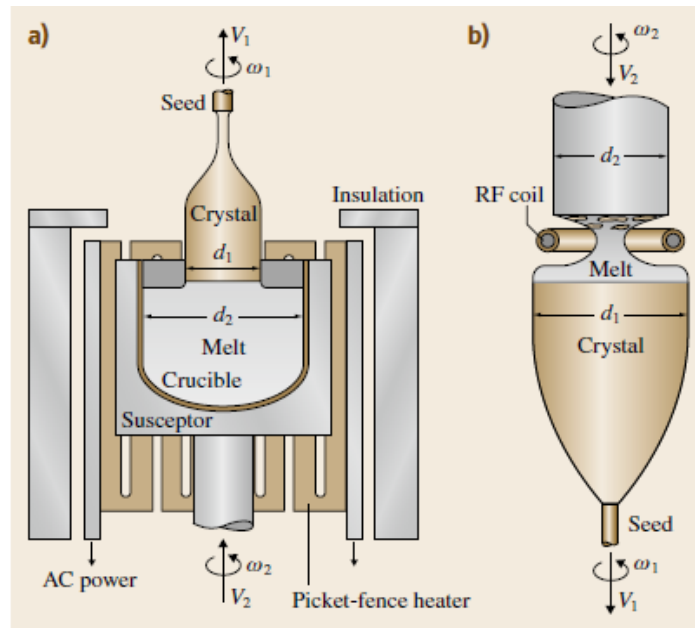


Figure 1.7 Schematic of (a) Czochralski growth; (b) Float Zone growth[34]

Figure 1.7(b) shows the schematic of the sc-Si Float Zone system and its principle. The Float Zone process is carried out in a large growth chamber with an overpressure argon atmosphere. The feedstock poly-Si rod is preheated and then the lower end of the rod is heated by the RF coil which works at 2.5-3.5 MHz frequency[35], until the surface melts, forming a melt drop hanging on the rod by surface tension. Then, the seed is moved upwards until it touches the melt drop. After it is melted back slightly, the seed is moved downwards and a monocrystalline neck is formed with all dislocations removed. Then, by slowing the seed pulling rate, and increasing the RF power and feeding rate, the diameter of

the growing crystal can be increased to the desired size. In the meanwhile, the feedstock poly-Si rod and the seed are rotated at a proper rate.

Because of no contact between molten Si and crucible, and also taking the advantage of small segregation coefficients of many impurities, the Float Zone process can produce very high purity single-crystalline Si, which is used by making solar cells with world record efficiency of 25%[36].

Due to the large demand for silicon for solar cells and the requirement of lowering the cost, mc-Si which is only made for solar cells earns more and more PV market share, although the disadvantage is 1-2% less efficiency. The technique used in industry for making mc-Si ingot is directional solidification which is normally realized through two approaches: the Bridgman process and the block casting process. With both processes, high quality multi-crystalline Si ingot with weight 250-300kg, with dimensions of up to 70x70cm², and height of 30cm[37] can be produced.

In the case of the Bridgman process, the feedstock poly-Si is molten in a silicon nitride (Si₃N₄) coated quartz crucible within the crystallization furnace which is equipped with the inductive heating or a resistive heating element. The solidification is realized by slowly moving the Si melt-containing crucible out of the hot zone to lower the temperature below the Si melting point (1410°C). Now the crystallization front, which is the solid-liquid interphase moves vertically, upwards through the crucible.

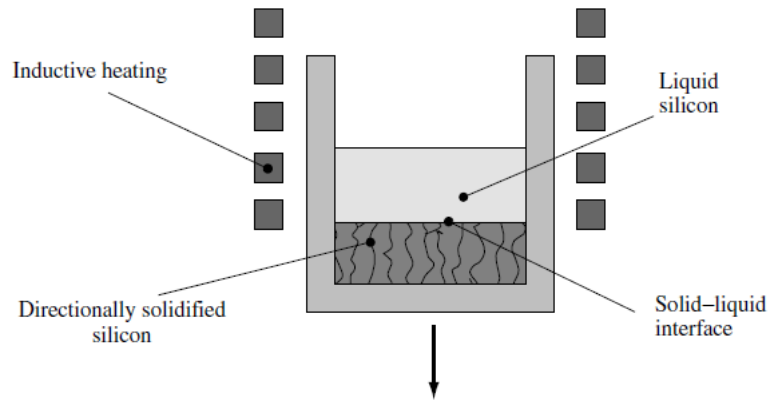


Figure 1.8 Schematic of mc-Si Bridgman process [38]

For the block-casting process, the feedstock poly-Si is melted in a non-coated crucible and poured into a Si_3N_4 coated crystallization crucible, rather than using only one crucible for both melting and crystallization as in the Bridgman process. The crystallization crucible is surrounded by heaters which can be adjusted during the crystallization process, making the crystallization front move in a vertical direction, upwards through the crucible, after the solidification starts in the bottom region.

The directional solidification intentionally achieved by either the Bridgman process or the block-casting process results in a columnar crystal growth and consequently the adjacent wafers made out of the ingot have nearly the same defect structures such as grain boundaries and dislocations. The crystallization speed of the Bridgman process is normally set to be 1 cm/h, and that of the block-casting usually is much higher [37]. The mc-Si ingots are then trimmed off the outside layer and chopped into the wafer size. The impurity concentration is too

high in the outside layer which contacts to the crucible during the crystallization process. Then the outside layer of the ingot is refined and used as the feedstock.

The sc-Si or mc-Si ingots are then sliced into wafers, using the modern wiresaw, the schematic of which is shown in figure 1.9. The cutting is achieved by the abrasive slurry which is supplied to the wire and carried by the wire into the cutting channel. The wiresaw is sophisticatedly controlled for wire tension, slurry temperature, wire speed, ingot feed rate and many other parameters. By using very thin wire and fine silicon carbide (SiC) slurry, several hundreds of wafers with the thickness of 150-200 μ m can be sliced in one cutting cycle which is around 5-8 hours[39]. However, the cutting causes kerf loss almost as much as wafers and wafer surface damage which has to be removed by further processes.

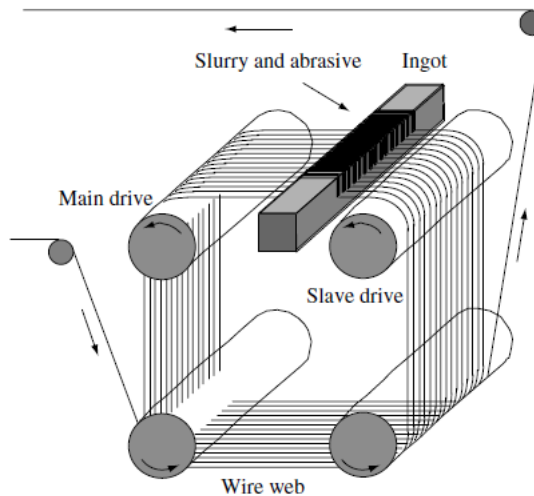


Figure1.9 Schematic of modern wiresaw for crystalline Si[40]

Most crystalline solar cells are fabricated by using the low cost, reliable and high yield process based on screen printing. An industrial crystalline Si solar cell with screen printing contact is shown in Figure 1.10.

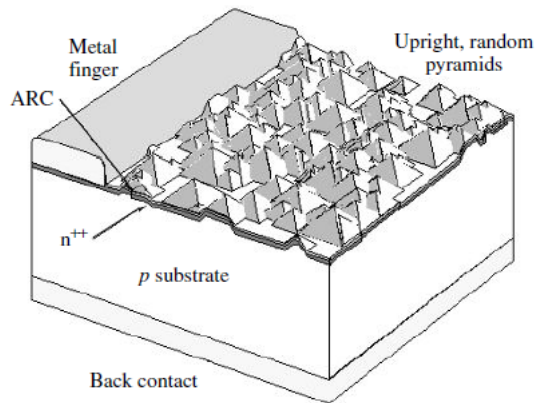


Figure 1.10 Typical structure of a crystalline Si solar cell with screen printing contacts (not to scale)[41]

Solar wafers are first etched off about 10 μ m in alkaline solution to remove the surface damage caused by sawing. Then a pyramid texture is formed on the wafer surface to improve the light absorption by dilute NaOH etching. The PN junction is formed by phosphorus diffusion in a diffusion furnace through gas dopant (POCl_3 carried by N_2) or solid dopant source sprayed or screen printed on the wafer. Since the edges of Si wafers are also p-type doped with phosphorus, causing interconnection between front contact and back contact, the edge is dry-etched by plasma in highly reactive fluorine compound gas (CF_4 , SF_6) to isolate the junction. To reduce light reflection, titanium dioxide (TiO_2) is deposited on the front side of the wafer as the anti-reflection coating (ARC) by atmospheric

pressure chemical vapor deposition (APCVD). Si₃N₄ deposited by PECVD is also adopted for the ARC.

The silver-based paste is screen printed in a grid pattern on the front side of the cell and dried in an in-line furnace. The same operations are performed at the backside of the cell, except that the paste contains both silver and aluminum and the back contact is continuous or in a mesh pattern. Finally, the cell is finished with the co-firing process which is performed to achieve metallization and ohmic contacts on both sides.

1.1.5 Silicon Ribbon

More than 29% of the cost of the silicon wafer is in the sawing process which also causes a material loss[42]. Many technologies of silicon ribbon growth have been developed to crystallize silicon directly and utilize all silicon feedstock in principle without sawing. However, only two of them have been commercialized for large scale manufacturing. They are edge-defined film-fed growth (EFG) and string ribbon technologies which are shown in figure 1.11 and figure 1.12 respectively.

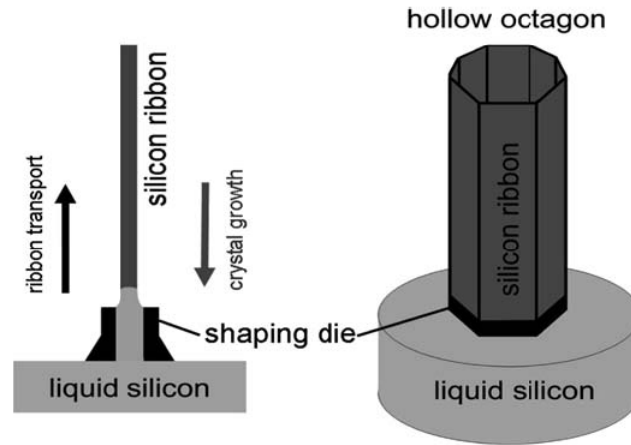


Figure1. 11 Schematic of EFG technology (commercialized by Schott Solar)[43]

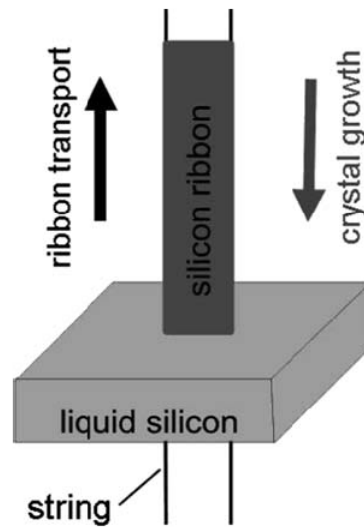


Figure1.12 Schematic of string ribbon technology (commercialized by Evergreen Inc)[43]

In the EFG process, a die is wetted by molten silicon contained in a crucible which is continuously supplied with up to 200kg silicon during a growth run. The liquid silicon rises up to reach the die top and connects to a seed, due to the capillary effect. As the seed is pulled up (at a rate of ~2cm/min), the top

portion of the liquid is lifted up and continually solidifies, maintaining the shape of the die channel and adding multi-crystalline silicon growth to the seed. In Scott Solar (Formal ASE American), silicon grown by EFG is in the form of a closed octagon tube with a wall thickness of about 300 μm . Then wafers (12.5 x12.5 cm^2) are cut from a faces of the octagon tube, using a Nd:YAG laser, with less than a 10% loss in starting material. Considering the recycling of silicon rejected in the crystal growth and laser cutting, it is possible to produce EFG wafers with less than a 5% loss of silicon from the starting feedstock material[44, 45].

In the string ribbon process, two thin graphite filaments enter the bottom of the molten silicon-containing crucible through small openings, pass through the molten silicon and are bridged above the melt by a seed plate. As the filament and seed plate are pulled up, the molten silicon is lift up by surface tension, forming a film between the two filaments. The liquid silicon film rises up with the filaments and solidifies continually, forming a multi-crystalline silicon ribbon between them. The ribbon growth rate is ~2cm/min[45], which is similar to the EFG process. 100 μm thick silicon ribbons have been achieved and commercially available string ribbon silicon wafers are 15 x 8 cm^2 , with a thickness of ~300 μm .

The advantages of silicon ribbon technologies are that they avoid the costly sawing process and reduce kerf loss significantly. However, technically, all silicon ribbon technologies face challenges of 1) stress which arises due to the cooling gradients near the solid-liquid interface of the order of 500 $^{\circ}\text{C}$; 2) carbon and other impurities associating with the strings and die. Therefore, the payback

is that the efficiency of silicon ribbon solar cells is 3-4% less than that of crystalline silicon solar cells, and the efficiency of commercialized silicon ribbon solar cells is 14-15%[44-46].

1.2 Research Progress on Thin Film Crystalline Si Solar Cells

The thin film crystalline silicon solar cell comprises a completely different approach. The active material has a thickness in the micrometer range. Therefore, potentially, it could both have the high efficiency advantage of c-Si technologies and the low cost advantage of thin film technologies. As the silicon is an indirect band gap material, optical designs are needed to overcome the low absorptivity of this material.

Using inexpensive foreign substrates is the key for the low cost advantage of the c-Si thin film technology. A large variety of deposition techniques, substrate and cell design are currently under the investigation for fabricating c-Si thin film solar cells. Three approaches are usually adopted: 1) growing Si thin film on low temperature substrates; 2) growing Si thin film on high temperature substrates; 3) using the layer transfer process to transfer the thin film layer epitaxially grown on silicon wafers to inexpensive foreign substrates. However, most of these developments are still in the laboratory phase, and the resulting devices are a few square centimeters in area and with efficiencies in the range of 5%-14% [47-50].

1.2.1 Crystalline Si Thin Film on Low Temperature Substrates (LTS)

When the Si thin film is grown by plasma enhanced chemical vapor deposition (PECVD) on a substrate at a low temperature up to 550°C, low cost window glass could be used as the substrate. To improve light absorption, the planar glass is usually textured by wet chemical etching or a chemo-mechanical texturing process[51]. An alternative is to coat the planar glass with textured ZnO or SnO[52-54], since the TCO layer is required for the contacts, and the wet chemical etching process is just a small extra step.

Solid-phase crystallization is an approach to deposit the c-Si active layer. The process was developed by Sanyo Group: a-Si thin film is deposited by PECVD on glass using hydrogen-diluted SiH₄ at a temperature around 600°C; After an annealing process at 600°C for 10 hours, the initial a-Si transforms into microcrystalline Si(μc-Si). Since the P-doping enhances the nucleation rate, the bottom of the a-Si is highly doped, with the result that all crystalline nuclei are located at the bottom of the film and columnar grains grow from the bottom to the top, with a typical grain size of 1.5μm[55, 56].

PECVD deposits μc-Si rather than a-Si with a low silane concentration (SiH₄/(SiH₄+H₂)). For example, Si deposition at 225°C by very high frequency (VHF) glow discharge at 70MHz yields films at silane concentrations <7% which are microcrystalline, while those at concentrations >7% are amorphous[57]. Two favored proposed mechanisms: 1) strained bonds are etched by atomic hydrogen; 2) the surface diffusion length of growth precursors is enhanced due to the

hydrogen saturation of the growth surface[58-61]. The deposition rate is reduced by a low silane concentration but can be increased by high plasma power. However, high plasma power results in poor electric properties of the thin film. Thus, VHF deposition (higher than 50MHz) is used in contrast to conventional 13.6MHz to overcome these problems[62]. The typical growth rate for $\mu\text{c-Si}$ thin film is $10^{-2}\mu\text{m}$. The typical grain size is typically 20nm[57, 63].

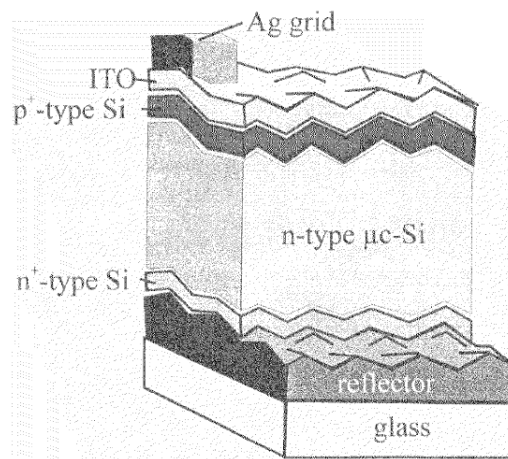


Figure 1.13 Schematic of a $\mu\text{c-Si}$ thin film with textured surface, enhanced absorption and back reflector, with a total thickness of 1-5 μm [64].

The efficiencies of $\mu\text{c-Si}$ thin film solar cells are usually lower than 10%. 9.2% cell efficiency is achieved by Sanyo on a device based on a 10 μm poly-Si thin film, fabricated by using a solid-phase crystallization process. Single junction $\mu\text{c-Si}$ thin film solar cell with 3 μm active layer and textured TCO achieved 8.5% cell efficiency[65]. Higher efficiency is achieved by optimum cell design with textured surface, enhanced absorption and back reflector, which is illustrated in figure 1.13.

The device consists of glass/ Al reflector/ 300nm-thick n⁺ type μ c-Si/ 1-5 μ m slightly doped n type μ c-Si/ 30nm-thick p⁺ type/ textured ITO/ Ag electrode grid. The design of the textured ITO surface and Al reflector reduces the light reflection and increases the light travelling path. The absorption layer is slightly doped or intrinsic to reduce recombination. Therefore, an efficiency of 10.1% is achieved[64].

1.2.2 Crystalline Si Thin Film on High Temperature Substrates (HTS)

Substrates which could withstand temperature higher than 1000°C, or even the silicon melting point, allows the high temperature deposition of c-Si from chlorosilanes to be feasible. The growth rate is much faster than the low temperature deposition processes, up to 5 μ m/min.

Due to the very high temperature, the substrate material is required, firstly, to be thermal resistant and inert in order to not to react with Si at high temperature; secondly, to match the thermal expansion of the poly-Si, which is $3.9 \times 10^{-6} \text{ K}^{-1}$ at 1000°C; thirdly, to be a dielectric material, allowing the integrated series connection; fourthly, to be a high purity material, avoiding contamination; and finally, but not the least important, to be inexpensive. Of course, to be highly reflective or transparent is a plus for light trapping designs. Table 1.1 shows the materials used for high temperature substrates and their properties.

Table1. 1 Substrate materials used for c-Si thin film solar cells with the HTS approach

	Insulator	Reflector	Cost	Cell Efficiency	Reference
Mullite	yes	yes	low	8.2%	[66, 67]
Graphite	no	no	high	11%	[67, 68]
High-T glass	yes	yes*	high	7.5%	[69]
Si-infiltrated SiC	no	no	low	8.0%	[67, 70]
Ribbon Si	no	no	high	11.2%	[67]

* combined with Al mirror evaporated on the glass substrate

The c-Si layer grown by high temperature deposition typically has a thickness of 5-40 μ m and grain sizes of 1-5 μ m [66-70]. The c-Si layer grown on oxidized Si wafers doesn't yield a higher efficiency, indicating that contaminations from the substrate are not the limiting factor, but the grain boundary recombination limits the cell performance[71].

To increase the grain sizes and reduce the grain boundary recombination, zone melt recrystallization (ZMR) process is used, thus increasing the cell efficiency. The ZMR apparatus is illustrated in figure 1.14. A halogen lamp at one focus of an elliptical mirror melts a narrow region of the mc-Si film which has been deposited on the substrate. The temperature gradient is reduced by heating the substrate with the heaters underneath the substrate. The molten zone moves

with the lamp, crossing the substrate with a velocity of 1-30mm/s. The grain sizes are increased from micron range to millimeter range, up to 5mm [66, 67, 71].

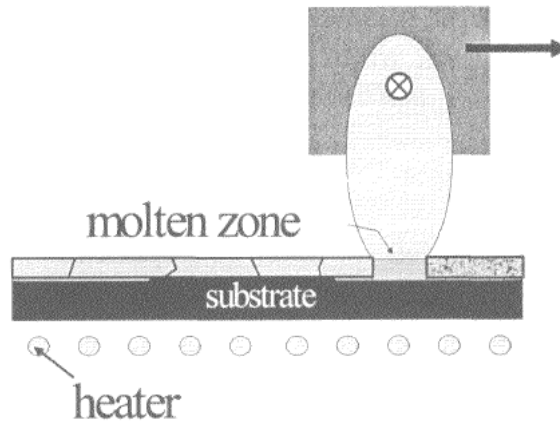


Figure 1.14 Schematic of a zone melting recrystallization (ZMR) apparatus [72]

A diffusion barrier of SiC or silicon oxide/silicon nitride/silicon oxide (ONO) is deposited prior to the deposition of the Si layer in order to reduce impurity diffusion from the substrate to the silicon layer during the recrystallization process. A cell fabricated by recrystallization of a 10 μ m-thick Si thin film on the mullite substrate with 8.2% efficiency is reported [66, 67]. A higher efficiency of 11% is achieved by the cell fabricated on a graphite substrate with a SiC diffusion barrier [67].

1.2.3 Layer Transfer Process

The layer transfer process (LTP) permits the transfer of the device layer from a re-usable substrate to a low cost device carrier by growing the device

layer on the substrate with a special surface condition which most commonly adopts an oxide mask and a porous structure.

The LTP for solar cell fabrication was first used to reduce the cost of GaAs cells which is an expensive material[73]. A carbonized photoresist mask with stripe openings is fabricated on the GaAs substrate. The openings function as seeds during the thin film growth. 10 μ m-thick single-crystalline GaAs thin films are grown by vapor phase epitaxy on the re-usable GaAs substrates. The GaAs lateral overgrowth on the openings yields a continuous single-crystalline thin film. Then the film is bonded to a glass carrier and cleaved from the substrate. 17% efficiency is achieved by the cell based on this single-crystalline GaAs thin film[74].

Besides carbonized photoresist, SiO₂ is commonly used as the mask for the sc-Si thin film growth. It provides a surface condition allowing thin films to be transferred from the substrate to the device carrier via chemical etching or mechanical forces.

Figure 1.15 shows a LTP process using via hole etching for the separation of thin film (VEST process)[75, 76]. A large-grained polycrystalline Si thin film with 1-3 μ m thickness is fabricated on the pre-oxidized sc-Si wafer by chemical vapor deposition (CVD) and zone melt recrystallization (ZMR). The layer is then thickened by CVD and textured by KOH etching. Holes of 100-300 μ m diameter are etched on the poly-Si layer with a separation distance of 1-2mm via a lithography process. The SiO₂ layer is etched through these holes by chemical

etching and the poly-Si layer is detached. Through these processes, the emitter is formed by vapor phase diffusion and contacts are fabricated by sputtering. Poly-Si cells with thickness 80 μm are fabricated through this process and achieved 16% efficiency on areas of 100 cm^2 and 13% on areas of 924 cm^2 [77].

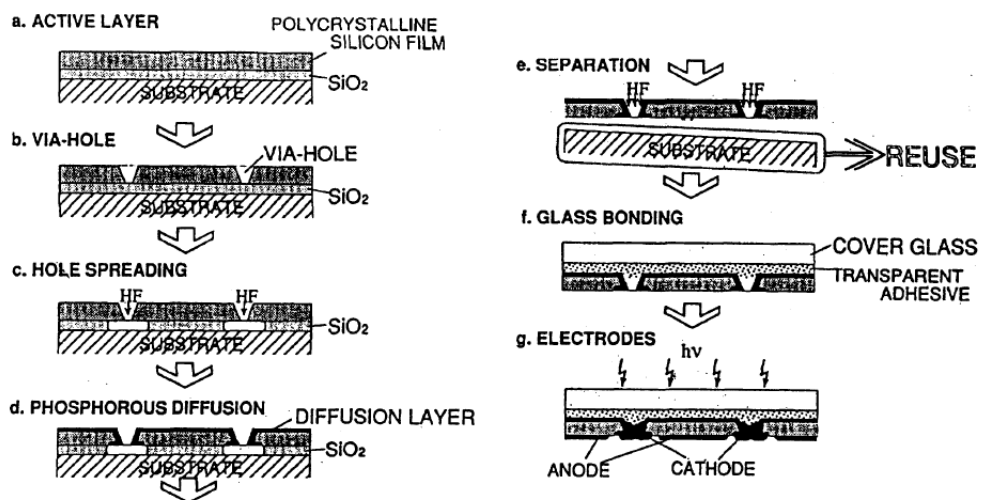


Figure 1.15 LTP via hole etching for separation of thin film investigated by Mitsubishi [75]

Another LTP process using oxide mask called epilift is less complex. The process starts on sc-Si substrates with mesh patterned seeds. The patterned seeds are along (110) directions and are fabricated by lithography [78, 79]. Single-crystalline Si thin films are grown on these seeds by liquid phase epitaxy. Lateral overgrowth makes the film become a continuous mesh structure. The cross section of the Si thin film mesh is diamond-shaped when a (100) substrate is used, as shown in figure 1.16. For the Si thin film mesh on a (111) substrate, the cross section is a parallelogram, as shown in figure 1.17 and figure 1.18. The

epilift layers usually have a thickness from a few microns to a few tens of microns [78-81]. Cells based on the epilift layer have an efficiency of 13% on 1cm^2 areas and 10.9 on 50cm^2 areas[80].

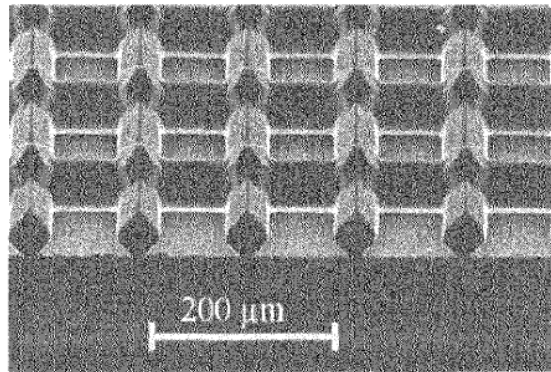


Figure1.16 SEM image of an LPE Si mesh on (100) sc-Si substrate[78]

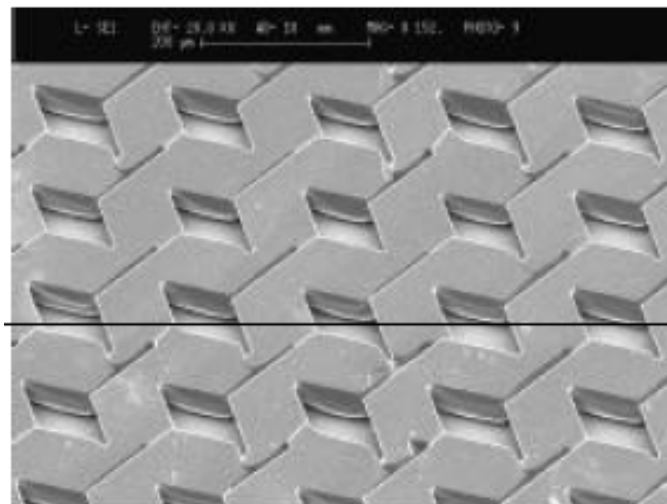


Figure1.17 SEM image of an LPE Si mesh on (111) sc-Si substrate[80]

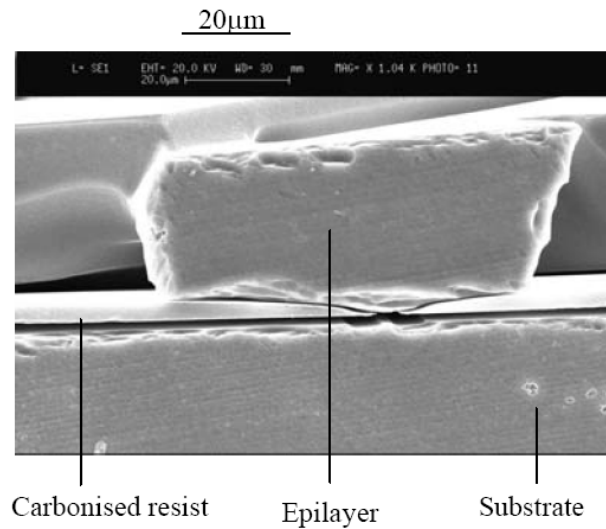


Figure 1.18 Cross section SEM image of an LPE Si layer on a carbonized photoresist mask[81]

In both the VEST process and the epilift process, only one side of the epitaxial layer is accessible before the layer is detached. Therefore both contacts of the cell have to be on the top surface. The holes on the epitaxial film are used to form emitter-warp through structure[80, 82]. However this structure increases the complexity of the cell fabrication.

Porous silicon technique is also adopted to provide convenience for the LTP process. A porous silicon layer is formed by electrochemical anodisation of the sc-Si substrate in an HF-based solution. The porous layer is usually a few to ten microns thick and has a low porosity at the surface and a high porosity at depth, and therefore allows high epitaxy growth quality and easy subsequent detachment of the epitaxial layer. CVD and LPE are used to epitaxially grow sc-Si layers on the porous structure[83, 84]. The epitaxial layer is detached by attaching it to a foreign substrate, and applying a mechanical force at the high

porosity layer such as a water jet, ultrasonic vibration or mechanical tensile force[85].

1.3 A Conclusion of Material Growth Techniques for Photovoltaic Applications

Among all commercialized solar cell techniques, crystalline silicon dominates the market, because of the relative high efficiency of 18%-24% and the mature technology which is already widely adopted and thus offers low cost. Lots of effort has been invested to lower the cost of the wafer, since it represents more than 40% of the module cost and more than 60% of the cell cost. There is not much room to reduce the cost of the traditional wafering process, since it has been developed for more than 40 years, or as long as the integrated circuit industry. Reducing the thickness of the wafer can increase the wafer output from a single ingot. However, over a certain limit, the cost will increase as new techniques are used to reduce wafer thickness. Furthermore, kerf loss should ideally be avoided.

Thin film solar cells have relative low efficiencies: 12-16% for CdTe, 12% for CIGS, and 8-9% for a-Si. The advantage of thin film solar cells is low cost which is already below \$1/watt. As more fundamental studies of these materials are carried out, it is expected that the efficiencies of thin film solar cells will be further increased and therefore the cost will be reduced. However, the disadvantages of the thin film techniques are the complexity of the growth

technique and equipment, and toxic or explosive precursors used for thin film growth.

Crystalline silicon thin film is a possible alternative approach to produce low cost and high efficiency solar cells. Since the silicon is an abundant and inexpensive material, and the device layer is directly made from raw material or precursors, wafer cutting and polishing are avoided. However, the films made by high temperature substrate (HTS) processes and low temperature substrates (LHS) processes, being microcrystalline or polycrystalline, therefore yield low efficiencies. For layer transfer processes (LTP), good quality sc-Si films are epitaxially grown by CVD or LPE. However the small thickness requires optical design for good light absorption and foreign substrates for enough mechanical strength. And more, lithography and chemical etching are required for the LTP process. These disadvantages add to the complexity of the LTP and therefore increase cost.

Thus, an ideal material growth technique for solar cells should produce a continuous sc-Si layer directly from raw materials, avoiding wafer cutting processes. The sc-Si layer should have enough mechanical strength, avoiding the use of a foreign substrate as the device carrier. This suggests that a thick sc-Si layer be epitaxially grown on a re-usable substrate such that the sc-Si layer can be detached from the substrate without chemical etching and lithography.

In this thesis, the lateral diffusion liquid phase epitaxy (LDLPE) process is proposed, which has the potential to satisfy the above requirements.

Chapter 2. Objectives of Present Work

Single crystalline silicon solar cells have relative higher efficiencies than those of thin film solar cells. However, thin film technologies have the advantages of low cost and low energy consumption over single crystalline silicon technologies. Based on LPE technology, which has the capability to grow premium quality single crystal thin film, a novel technology called lateral diffusion liquid phase epitaxy (LDLPE) is invented to grow self-supported single crystalline silicon wafers/chips directly for photovoltaic applications. Potentially, LDLPE technology has the advantages of both crystalline silicon and thin film technologies in terms of high efficiency and low cost.

2.1 Lateral Diffusion Liquid Phase Epitaxy (LDLPE)

LPE is a low cost process for growing premium quality thin films of various semiconductor materials, including silicon. However most of the applications of LPE are for planar growth on substrates. Although lots of research effort has been made on silicon epi-lift LPE technology in which the lateral overgrowth of LPE is investigated, there is no publication about the technique of lateral overgrowth using techniques for limiting thickness during the lateral growth.

A modified LPE technology is proposed, which utilizes the lateral over growth feature of the LPE, however it limits the thickness increase as the silicon grows laterally. The concept of the modified LPE is illustrated in figure 2.1. Since

the lateral diffusion contributes most of the growth, this modified LPE technology is named Lateral Diffusion LPE (LDLPE).

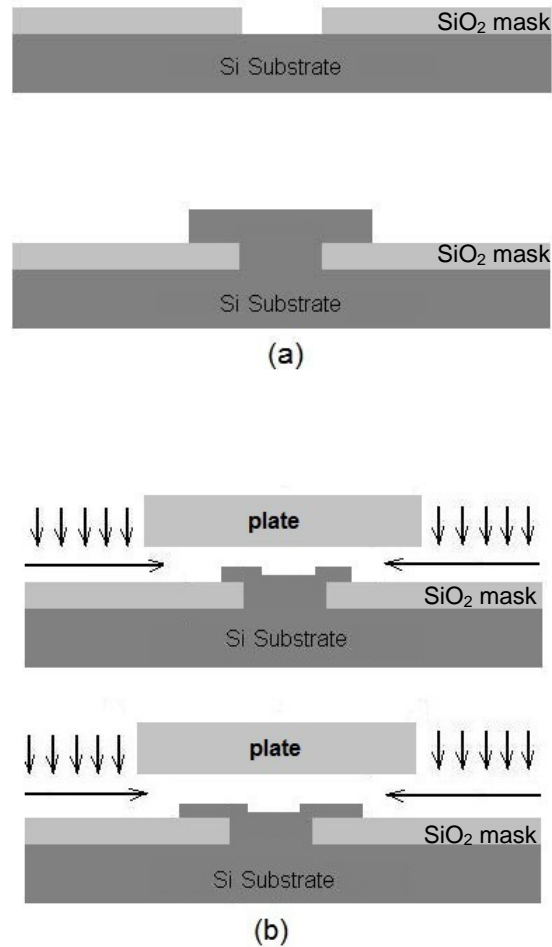


Figure 2.1 Concept of (a) conventional LPE lateral over growth (b) Lateral Diffusion LPE lateral overgrowth

With conventional LPE silicon thin film lateral over growth, shown in figure 2.1 (a), the silicon is deposited on the un-masked area (the seed) on the substrate at the beginning, and then the silicon grows laterally over the SiO₂

mask. When the un-masked area is a straight line, a silicon strip will grow on the seedline. However as the silicon strip grows laterally and increases its width, it also grows vertically and increases its thickness, since the silicon atoms diffuse toward the seedline from all directions. That means it is not feasible to produce a silicon strip with a large planar area and a small thickness which is able to be controlled within a certain value.

LDLPE, as shown in figure 2.1 (b), is a modified LPE technology. A plate is placed over the seedline, leaving a space between the plate itself and the substrate. With this configuration, as the silicon strip grows, the silicon atoms diffuse toward to the seed line basically horizontally from both sides, rather than from all directions which traditionally leads to increasing thickness and width simultaneously in a LPE growth process. In LDLPE, when the thickness of the strip reaches a certain value, it stops increasing due to the presence of the plate. But the strip can keep growing horizontally, increasing its width. Therefore, theoretically, this invention provides a method to grow silicon or other semiconductors strips with a certain thickness but having a planar surface, which is large enough for practical device fabrication, like CZ and FZ single crystalline wafers.

2.2 Features of LDLPE

As mentioned in Chapter 1 and above, solar cells made of single crystal materials show better performance than those made on non-single crystalline thin

films. However, the traditional techniques to make single crystalline material such as CZ and FZ have many disadvantages: very high temperature processes; insufficient usage of raw material; costly cutting and polishing processes and kerf loss of materials. The proposed LDLPE technology has the potential to overcome these drawbacks and provides a low cost approach to produce single crystalline silicon wafer/chips. As summarized, the features and contributions of LDLPE include the following aspects:

(1) LDLPE can produce single crystalline silicon strips at a near equilibrium condition, leading to a premium quality of the crystal.

(2) The thickness of the LDLPE single crystalline silicon planar structure is controlled by the space between the plate and the substrate. Theoretically, the strip can continuously grow laterally with a certain thickness, making itself a single crystalline wafer which is the same as CZ and FZ wafers.

(3) An appropriate thickness of the strip provides sufficient light absorption for the solar cell device, and also a sufficient mechanical strength for being handled during the device fabrication processes.

(4) The LDLPE single crystalline strips can be peeled off from the substrate and used as wafers for device fabrication.

(5) After the strips are peeled off, the substrate can be reused after being appropriately processed.

(6) LDLPE grows single crystalline silicon at a temperature much lower than 1414°C, the melting point of the silicon.

2.3 Summary of Contributions of This Thesis

(1) The concept of Lateral Diffusion Liquid Phase Epitaxy is proposed for the first time and a provisional patent was filed.

(2) A graphite boat is designed to realize silicon LDLPE growth. Ideas of scaling up and the method to realize continuous growth are proposed

(3) Single crystalline silicon strip with a thickness of 100 μ m grown by LDLPE is demonstrated. Comparing to the single crystalline silicon strip grown by conventional LPE, the aspect ratio (width: thickness) is improved from 1:1 to 1:2

(4) The mechanism of LDLPE is proved and the effect of a plate on the silicon strip thickness is demonstrated.

(5) Electrical properties of sc-Si strips grown by LDLPE are proved to satisfy requirements for solar cells wafers.

After reviewing the material growth method for PV applications, an idea of growing single crystalline silicon wafers by LDLPE is proposed. The goal of inventing this technology is to take advantage of both single crystalline technology and thin film technology. The mechanism of LPE is described in the third chapter. The details of the LDLPE concept, experimental setup, parameters and LDLPE system operating procedures are introduced in Chapter 4. The experiment results are shown and discussed in Chapter 5, including the characterization of the LDLPE single crystalline silicon strip in terms of crystallography and electrical properties. A summary of the conclusions and a

brief research plan of future work to develop LDLPE technology are presented in final section of chapter 6.

The drawing of the design of the LDLPE graphite boat and system is attached in appendix I and the code to perform the simulation of LDLPE in a random walk model is attached in appendix II.

Chapter 3. Background and Theory of Liquid Phase Epitaxy (LPE)

This chapter is devoted to the growth method referred to as liquid phase epitaxy (LPE). After a general introduction to the apparatus, materials and applications of LPE, Si LPE is specifically discussed in terms of growth methods, solvent and growth temperature selection and the lateral overgrowth which is an important feature for the development of lateral diffusion liquid phase epitaxy (LDLPE). Finally, the theoretical fundamentals of LPE are introduced, including the phase diagram, diffusion-limited growth theory, nucleation and growth modes and impurity incorporation.

3.1 Introduction to LPE

3.1.1 General Aspect of LPE

‘Liquid phase epitaxy (LPE)’ precisely describes the concept of its name: a process in which a single crystal layer is grown from a dilute molten solution onto a single crystal substrate. The term ‘epitaxy’ means ‘the deposition of a single crystal layer on a single crystal substrate in such a way that the crystalline structure of the substrate is continued into the layer’. Epitaxy is classified into homoepitaxy, when the layer and the substrate are same in chemical composition and crystal structures, and heteroepitaxy, when the layer and substrate have different chemical composition but are similar in crystallographic relations.

LPE is a mature technology and has been used for developing III-V compound semiconductor optoelectronic devices, including light-emitting diodes (LEDs), laser diodes, waveguides, amplifiers, etc, for more than 40 years[86-88]. LPE has also been applied to silicon, germanium, SiC and II-VI compound semiconductors, as well as magnetic garnets, superconductors, ferroelectrics and other optical materials. In recent decades, LPE has been used for developing III-V and sc-Si thin film solar cells[74, 79-81, 86, 89].

Technically, LPE has the following features making itself a versatile semiconductor epitaxy technology for device manufacturing and development.

i) High growth rate. LPE could achieve a growth rate in the range of 0.1/min -1 μ m/min which is 10 to 100 times faster than MBE or MOCVD. Thus, it is feasible to fabricate thick device structures with LPE

ii) The wide range of dopants available with LPE. Theoretically, the growth layer can be doped by any material to some finite degree, by intentionally adding the dopant material to the molten solution.

iii) Growth of ternary and quaternary alloys and a great range of materials are feasible with LPE.

iv) Growth of high purity materials. LPE can produce epitaxial layers with low background impurities due to the preferential segregation of deleterious impurities.

v) The point defect density in the epitaxial layer is low, because the semiconductor is deposited at a near-equilibrium condition.

vi) Multilayer structures are feasible with LPE, e.g. heterostructures, p-n junctions.

vii) Low capital equipment and operating cost.

viii) No high toxic precursors or by-products.

ix) Selective epitaxy and epitaxial lateral overgrowth with high aspect ratio can be achieved by LPE.

In recent years, although LPE is still used for low cost LEDs production, this technique becomes less favored in research, due to its disadvantages:

i) More sensitive to the crystallographic misorientation of the substrate than other epitaxy techniques.

ii) Very difficult to have abrupt or precisely controlled doping or composition profiles.

iii) Difficult to grow compositionally graded buffer layers to reduce lattice mismatch between the device layer and the substrate when heteroepitaxy is required.

iv) Difficult to control the layer thickness uniformity and reproducibility with high accuracy, especially if the layer is thinner than 100nm.

v) Not compatible with in-situ and real-time characterization and growth monitoring instruments.

vi) Not suitable for compound semiconductors when the vapor pressures of the components are very different from each other.

Generally speaking, LPE is a good platform for exploring new semiconductor materials and developing novel semiconductor devices, because it is simply based on phase equilibria rather than complex precursor chemistry, growth kinetics and mass transfer. But, due to its weakness, LPE is not competitive in large-scale production of semiconductor devices which require extremely accurate controls of the composition profile and the thickness, like superlattices, quantum wells and quantum dot devices and devices on integrated circuits.

Moreover, LPE has been developed for thick layers or bulk crystal growth by setting up continuous mass transfer between source material and seed. A temperature gradient between the source material and the seed leads to a concentration gradient thus a continuous mass transfer[90]. Also, an electrical field between the source material and the seed can drive a continuous mass transfer from the source to the seed[91]. These modified LPE techniques are named temperature-gradient liquid phase epitaxy and liquid phase electroepitaxy, respectively.

3.1.2 Equipment and Instrumentation for LPE

LPE systems are generally classified into two categories: vertical dipping systems and horizontal slideboat systems, illustrated in figure 3.1 and figure 3.3 respectively.

The vertical dipping LPE system provide an economic method for large scale production of single, thick epitaxial layer deposition, such as for solar cells, especially when the thickness control is not critical. With the use of the wafer holder made by quartz or graphite, shown in figure 3.2, a batch of wafers, up to 50~100 wafers, can be processed in a single growth cycle.

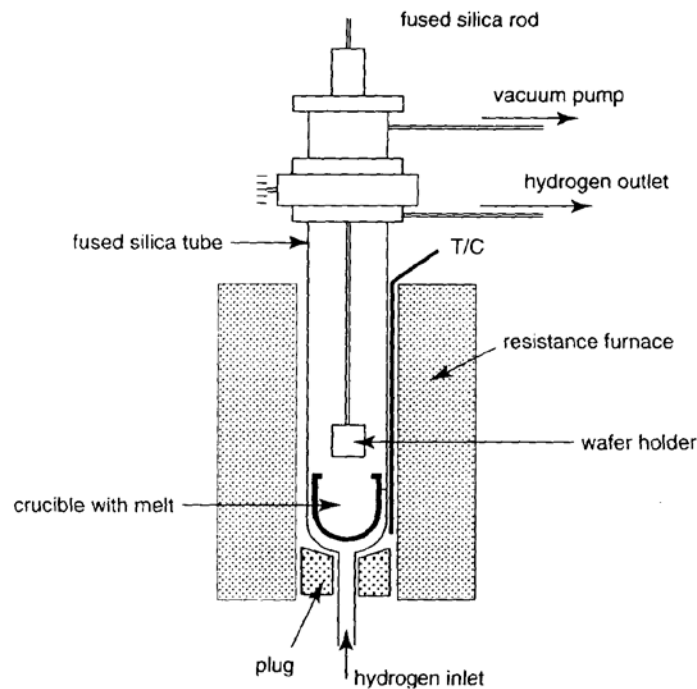


Figure3.1 Schematic of vertical dipping LPE system[89]

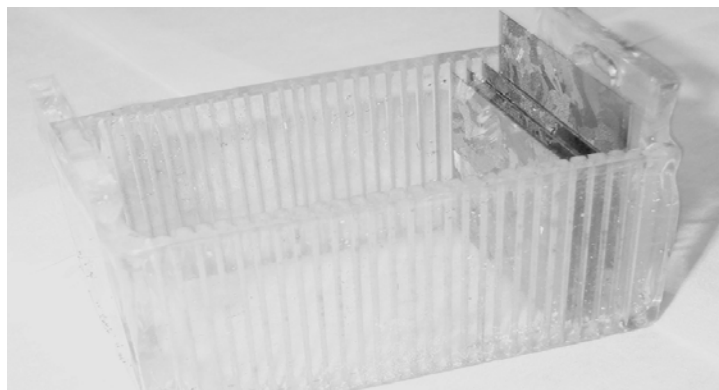


Figure3.2 A quartz wafer holder for large scale LPE production [92]

The horizontal slideboat system is the most versatile LPE growth system. It enables various LPE growth formats by applying variations and novel designs to the substrate holder or the slideboat. They include tipping systems, rotating/tipping systems, rotary crucible systems, piston slideboat systems [93-96], etc. Growth of multilayer structures such as laser diodes and double heterostructure LEDs can be achieved by using these specifically designed LPE systems.

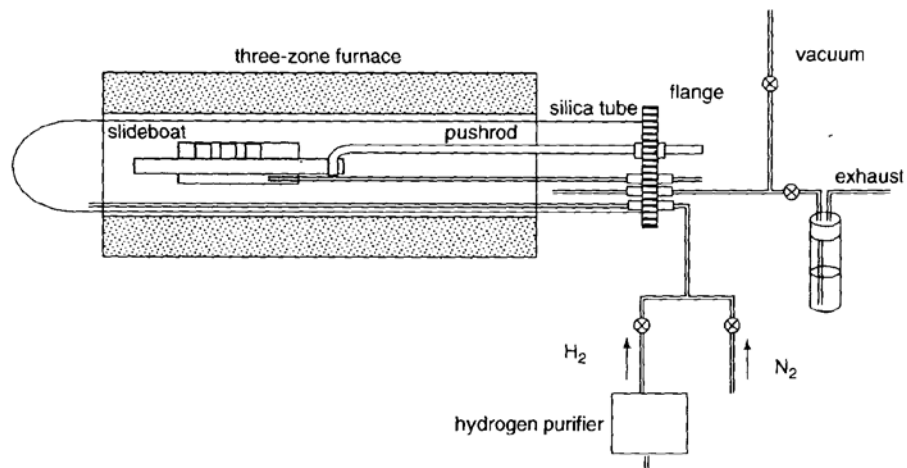


Figure 3.3 Schematic of horizontal slideboat LPE system [97]

Both the vertical dipping and horizontal slideboat systems consist of five basic elements: precise temperature controlled furnace, a reaction chamber (usually a quartz tube), substrate holder/slideboat, vacuum pump, and hydrogen inlet/outlet. In principle, the operations are the same: first, load the substrate, source semiconductor material and metal solvent into the quartz tube; second, evacuate the quartz tube and fill it with hydrogen, providing a reducing ambient; third, heat the tube to a set temperature until the molten metal is saturated with

the source semiconductor material; fourth, dip or slide the substrates into the melt, and cool down the quartz tube at a low cooling rate, so the semiconductor is precipitated and deposited on the substrate. The growth can be terminated by moving the substrate out of the melt. When the system is cooled down to the room temperature, substrates can be taken out after purging the hydrogen.

3.1.3 LPE Growth Techniques

LPE growth is driven by the supersaturation obtained by cooling the growth melt from the equilibrium liquidus temperature. The supersaturation can be obtained by many methods, briefly categorized into three types, namely the ramp-cooling, step-cooling and super-cooling techniques as shown in figure 3.4. For the ramp-cooling technique, an epitaxial layer is grown as the temperature of the melt is cooled down from the saturated temperature to a set value at a constant rate (figure 3.4(a)). For step-cooling, the melt is rapidly cooled below the saturated temperature to obtain a large supersaturation, then brought into contact with the substrate and held at a constant temperature during the growth cycle (figure 3.4(b)). The super-cooling technique has advantages of both ramp-cooling and step-cooling. The melt is first brought to a large supersaturation, and then upon contact with the substrate, the growth is continued by cooling the melt at a constant rate.

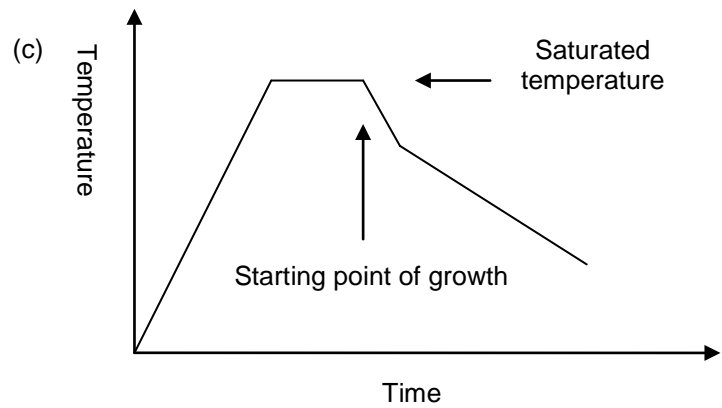
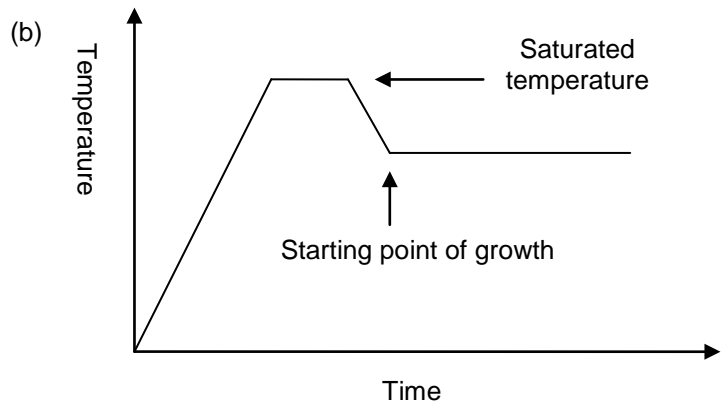
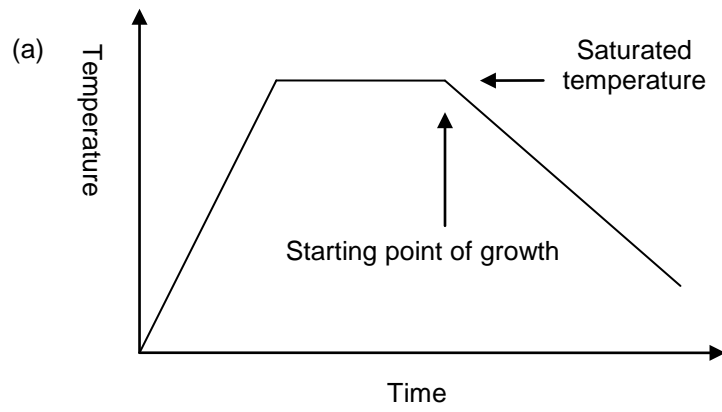


Figure3.4 Cooling process of LPE: (a) ramp-cooling; (b) step-cooling; (c) super-cooling[98]

With a suitable choice of cooling rate, a slow growth can be obtained by the ramp-cooling technique, at a near-equilibrium condition. Thus a high quality epitaxial layer can be grown. In practice, however, ramp-cooling does not offer such good results as step-cooling growth, with respect to thickness uniformity and surface topography[99, 100]. Also this growth process is more sensitive to temperature fluctuations in the furnace. Therefore, ramp-cooling is widely adopted for thick layer growth (up to tens of microns) where thickness uniformity is not critical.

The step-cooling process provides a large supersaturation, and thus a large driving force to enhance nucleation. This is very important to overcome the lattice mismatch between the substrate and the epitaxial layer[101, 102]. As the growth is taking place at a constant temperature, the variation of layer composition and impurity incorporation due to the changes of temperature can be eliminated[103]. However, for this process, only a limited super-cooling is allowed and the growth should start before spontaneous crystallization occurs. Thus, the step-cooling technique is typically used for thin layer growth (< a few microns) with good surface flatness.

Super-cooling has been widely used in the heteroepitaxy growth of III-V alloys [104-106]. Since it is a hybrid of ramp-cooling and step-cooling, it has advantages of both of them. At the early stages, the large supersaturation enhances the nucleation and at the later stages, growth is dominated by ramp-cooling, and thicker layer can be deposited.

3.2 Silicon LPE for Photovoltaic Applications

3.2.1 Introduction

LPE technology has been of interest for solar cells for three decades, both as a means for fabricating high-efficiency cells and as a low cost manufacturing method. It has been found that carrier mobilities in LPE silicon layer are only slightly lower than those in bulk silicon with similar doping[107]. Many techniques has been developed which mostly consist of processes involving silicon layer deposition on silicon substrates. Substrates used for silicon LPE solar cells include wafers cut from CZ single crystalline or polycrystalline cast ingots, silicon sheets or ribbons and recrystallized CVD deposited silicon layers on ceramics. Foreign substrates, like glass [108, 109], have been explored for LPE like solution growth of silicon, but less successfully.

Comparing the solution system for compound semiconductor LPE growth, the silicon and the metal solvent form a much less complex alloy system. Metal alloys are also used as the solvent, to achieve intentional doping or adjustment of the electrical properties of the epitaxial silicon layer. Metals and alloys successfully used for silicon LPE growth include: indium, aluminum, antimony, copper, gallium, tin, gold, bismuth, zinc, copper-aluminum, gold-bismuth, gallium-aluminum, gallium-indium, tin-aluminum, and many other combination of above metals and alloys[110].

The equipment and processes for LPE silicon solar cells are quite simple and straightforward, because for most situations, only single layer growth is

needed. The vertical dipping system, as shown in figure 3.1, is used for thick layer deposition on a large area[80, 89, 92], and the horizontal slideboat system and a simple slideboat, as shown in figure 3.3, are used for small area growth or research on new materials, new substrate and modified techniques[90, 111, 112].

Although high efficiency solar cells can be made on silicon wafers without an epitaxial layer, LPE is of interest for reducing the usage of solar grade silicon and high quality silicon wafers, due to its several important advantages. Relatively high deposition rates make LPE more likely to be used for large scale than other epitaxial technologies; during the growth, impurities segregate and are rejected into the liquid phase, therefore, the electrically active impurities at grain boundaries can be effectively avoided. On a substrate with poor quality and poor electrical properties like metallurgical-grade silicon wafers, LPE can produce a layer with less defect density, especially dislocations, and good electrical properties, satisfying requirements for high efficiency solar cells[92, 113]. More aggressively, the feasibility has been proved to use metallurgical-grade silicon as the feedstock for LPE silicon solar cells[92].

3.2.2 Solvent Selection

The most important consideration is probably the selection of solvent when a process for LPE growth of a semiconductor is being designed. Since the selection of solvent has large effect on the cost, growth parameters, and

especially the electrical properties of the epitaxial layer. For silicon LPE growth, the ideal solvent is proposed to have following properties[114]:

1) Low melting point so as to form a Si/metal alloy solution at a temperature well below the melting point, at least, less than 1200°C, the maximum temperature that the quartz tube can survive.

2) Large silicon solubility at the growth temperature and a remarkable change in silicon solubility with temperature. These are essential for minimizing the growth temperature and maximizing the growth rate

3) Not forming compounds with silicon and not reacting with crucible material.

4) Good wettability on the substrate. This is essential for removing the surface oxide, in the case of silicon substrates.

5) Low solubility of the solvent material in the solid silicon. The incorporation of the solvent atoms is in a certain range that results in an intentionally controlled doping or electrically inactive impurities in silicon.

6) Able to be removed from the grown silicon crystal by easy physical or chemical means (spinning, wiping or chemical etching).

7) Low cost for high purity material (higher than 99.99%) and low toxic.

Semiconductor properties of the epitaxial layer are closely related to the selection of the solvent. Table 3.1 summarizes the minority carrier lifetime and diffusion length, resistivity, and carrier mobility of LPE grown silicon using various

metal solvents. Overall, silicon layer grown from tin, indium and gallium could satisfy the requirements for thin film silicon solar cells.

Table3.1 Semiconductor properties of LPE silicon

Metal solvent (Growth temp. °C)	Doping concentration (cm ⁻³)	Resistivity (Ω-cm)	Carrier mobility (cm ⁻² V ⁻¹ s ⁻¹)	Minority carrier lifetime (μs)	Diffusion length (μm)	Ref.
Al (750)	10 ¹⁹		20		~3	[115]
Cu (950)	<10 ¹⁶				>100	[116]
Ga (600)	10 ¹⁸	0.42	70		1	[117]
Ga (500-900)				50-175		[118]
Ga _{0.7} Al _{0.3} (450)	1.4x10 ¹⁸	0.03	150		<1	[119]
In (920)	10 ¹⁶		90-260			[111]
In (946)	1.8x10 ¹⁶	2.17	285			[120]
In (1056)	1.2x10 ¹⁷	1.3	275			[120]
In (1250)	1.6x10 ¹⁸	0.25	206			[120]
In (900-1200)	10 ¹⁷ -10 ¹⁸				2-12	[121, 122]
In (+ Ga) (600-900)	5x10 ¹⁶ -10 ¹⁷				50-300+	[123, 124]
In (+ Ga) (947)	10 ¹⁷			2-3.5	50-65	[125]
In (+ Ga) (920)	5x10 ¹⁶		280	120	100-250	[93, 126]
Sn (950)	8-22x10 ¹⁵	0.2-0.7		0.3-1.0	15-30	[127]
Sn (900)	2x10 ¹⁶	1-2	150-300		50-60	[128]
Sn (+ Al) (930)	1.5x10 ¹⁷		100-200	8.5		[129]
Au-Bi (800-900)	10 ¹⁴ -10 ¹⁵			2-10		[121]
Pb (990)		0.2-10				[130]

Note: +Ga (with gallium dopant); +Al (with aluminum dopant); blank cell (data not available)

3.2.3 Choice of LPE Growth Temperature

From table 3.1, the growth temperature shows its close relation to the semiconductor properties of the silicon grown from metal solutions. For example, with indium as the solvent, the doping concentrations (cm^{-3}) of the LPE silicon are 10^{16} , 1.2×10^{17} and 1.6×10^{18} when the growth temperature is 920°C , 1056°C and 1250°C respectively. For the solution of indium with gallium dopant, a long carrier diffusion length can be obtained by growing the silicon at a low temperature [93, 124-126].

Generally speaking, a high growth temperature results in a high epitaxial growth rate; increased risk of contamination of the growth solution from the container material; larger post-growth strain for the heteroepitaxial growth; higher vapor pressures of solution component and dopant, and thus difficulties of composition and doping level control of the growth layer.

However, a low growth temperature also has drawbacks: poor nucleation due to the difficulties of removing surface oxide on the substrate at low temperature; low growth rate; failure to remove unwanted impurities from the solution, and therefore a higher background impurity level and lower carrier mobility.

A compromise between various factors is necessary for choosing a growth temperature for a particular application. The device structure, substrate material and other parameters also need to be considered.

3.2.4 Substrate Selection

The selection of substrate is another important consideration for the LPE silicon thin film grown for solar cells. It is closely related to not only the performance of the cell but also the cell fabrication processes. Basically, for the consideration of epitaxial layer quality, the substrate should match the lattice constant and the thermal expansion coefficient of the silicon epitaxial layer.

The low quality sc-Si wafer is a good candidate, since it is less expensive than high quality sc-Si wafer but still retains the most important advantages of a silicon substrate for silicon homoepitaxial growth: perfect lattice match and thermal expansion match between the epitaxial layer and the substrate. The sc-Si substrate only functions as the back contact and the carrier for the epitaxial layer, conducting electricity and providing mechanical support. The epitaxial layer which has better quality and semiconductor properties functions as the active layer of the solar cell. In 1995, it was reported that an efficiency of 18% had been achieved by LPE grown silicon thin film solar cells on low cost P⁻ type sc-Si substrates, and 17% is achieved on low cost P⁺ type sc-Si substrates[131, 132].

LPE silicon thin film solar cells on multicrystalline substrate have been studied by a number of groups. A group in ANU (Australian National University) successfully fabricated 15.4% and 15.2% efficiency cells on P type and P⁺ type mc-Si substrates respectively in 1997[133]. However, 16-18% efficiency solar cells can be produced in large scale on mc-Si wafer without an epitaxy layer grown by LPE. The metallurgical (MG) and upgraded-metallurgical (UMG) silicon

substrate are more interesting as the substrate for LPE silicon thin film solar cell. An efficiency of 10% was achieved by a thin film silicon solar cell on an UMG silicon substrate[134]. An improvement can be made by forming a recrystallized seeding layer (grown by CVD) on the MG/UMG substrate for the LPE growth, and 13% efficiency was achieved[135].

An alternative is to transfer the premium quality epitaxial sc-Si layers to low cost foreign substrate (e.g. glass or ceramics), called layer transferred process (LTP), which was introduced in section 1.2.3. LPE can be used for active layer deposition in the porous silicon LTP and the 'epilift' process.

Porous Silicon is formed by anodic dissolution of a highly doped p-type silicon substrate in a chemical mixture of HF and ethanol or acetic acid[85]. The porous layer is usually a few to ten microns thick and has a low porosity (10-20%) at the surface and a high porosity (50-70%) at depth, therefore allowing high epitaxial growth quality and easy subsequent detachment of the epitaxial layer. The thickness and porosity of the porous layer can be simply controlled by changing the electron current and time applied for the electrochemical etching while keeping a constant HF concentration in the chemical mixture.

Single crystalline Silicon wafers with (100) and (111) orientations are used for the epilift process. As introduced in section 1.2.3, a mask layer (SiO₂ or carbonized photo resist) with mesh patterned seeds, as shown in figure 3.5, is formed on the sc-Si substrate by thermal growth and lithography. The (100) and (111) orientated substrates results in thin films with diamond-shaped and

parallelogram-like cross-sections, respectively. The misorientation of the seed and spacing between seed are also important to the morphology of the epitaxial layer [79-81].

3.2.5 Epitaxy Lateral Overgrowth (ELO)

It has been demonstrated that the epitaxial growth of silicon and most III-V compounds using either LPE or CVD occurs preferentially in the openings (also called window, vias or seeds) defined in a masking layer on a substrate. The selective growth is an important feature of epitaxial growth that operates under near-equilibrium growth conditions, such as LPE and certain types of CVD. Since the near-equilibrium growth enables the control of nucleation and limits the growth to the opening, this thereby avoids the high supersaturation that results in extraneous nucleation and deposition on the mask. The material used for the mask is usually a layer (up to several hundred nanometers) of dielectrics, metals, or metallic compounds, deposited by various thin film deposition methods. For epitaxial selective growth of silicon, thermal grown SiO₂ is most commonly used for the masking layer.

Epitaxial lateral overgrowth (ELO) is another unique and important feature of the epitaxy under near-equilibrium growth condition, and is a consequence of selective growth. The crystal selectively grown in the openings laterally grows over the masked substrate. ELO has been investigated for more than twenty years due to the interest in the application of silicon-on-insulator (SOI)[136, 137].

LPE has demonstrated its advantages for ELO and SOI: 1) less defective growth; 2) high aspect ratio of lateral growth width to vertical growth thickness; 3) large overgrowth width.

Silicon ELO is also investigated for photovoltaic applications. Selective growth and ELO provide an approach for fabricating sc-Si thin film solar cells and reusing the substrate. In the case of silicon, the (111) plane, having the most compact atom arrangement, is the only preferred faceting surface. Thus, the ELO layer on (111) Si substrates have a planar (111) top surface, illustrated in figure 3.5

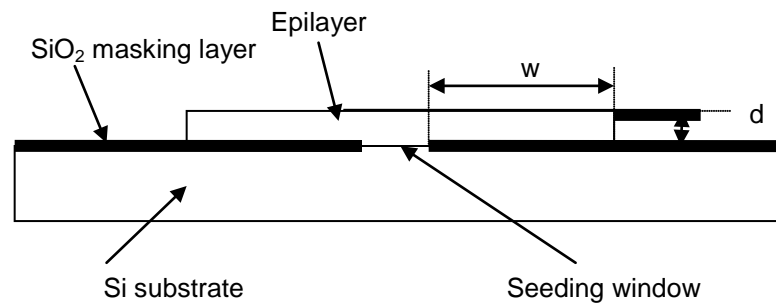


Figure 3.5 Schematic cross-section of the ELO layer (aspect ratio is defined to w/d)

The aspect ratio for VPE is typically 1-5, and the lateral extent of overgrowth is typically $\sim 10\mu\text{m}$ [138]. LPE has been demonstrated as having larger aspect ratios and lateral growth width. ELO silicon layers with a $0.2\mu\text{m}$ thickness and an aspect ratio of 80 were achieved by Kinoshita using tin solvent[137]. Also over $100\mu\text{m}$ overgrowth width was reported by Webber[81], grown by a vertical dipping LPE system from a tin melt. Tin was shown to provide larger overgrowth width than indium.

3.3 Theory of LPE

In this section, the silicon-indium solution is used as an example to introduce the theory of liquid phase epitaxy. Silicon-indium solvent is a simple system and indium results in better electronic and semiconductor properties of the epitaxial layer discussed in section 3.2.2.

3.3.1 Equilibrium Phase Diagram

The temperature-dependent silicon concentration in the indium can be found on the phase diagram shown in figure 3.6. The melting point of indium (156.6 °C) is also the eutectic point, the lowest temperature at which the silicon-indium solution exists. The temperature range from 1000°C to 800°C is generally used for LPE Si growth. When cooling down a saturated Si-In solution, the solubility of silicon in the indium decreases. The difference between the state of the Si-In solution and its equilibrium state is the driving force for silicon nucleation and precipitation. The solidus is so close to the vertical temperature axis that it is almost invisible in figure 3.5, indicating that the silicon precipitated from indium has a very low concentration of indium, shown in table 3.1. At a growth temperature of 946°C, a maximum indium concentration in silicon of 1.8×10^{16} atom/cm³ is reported[120]. The silicon grown by LPE from In/Si solution is naturally p-type doped by indium and has been reported to be used for crystalline Si thin film solar cells by many research groups [80, 112, 129].

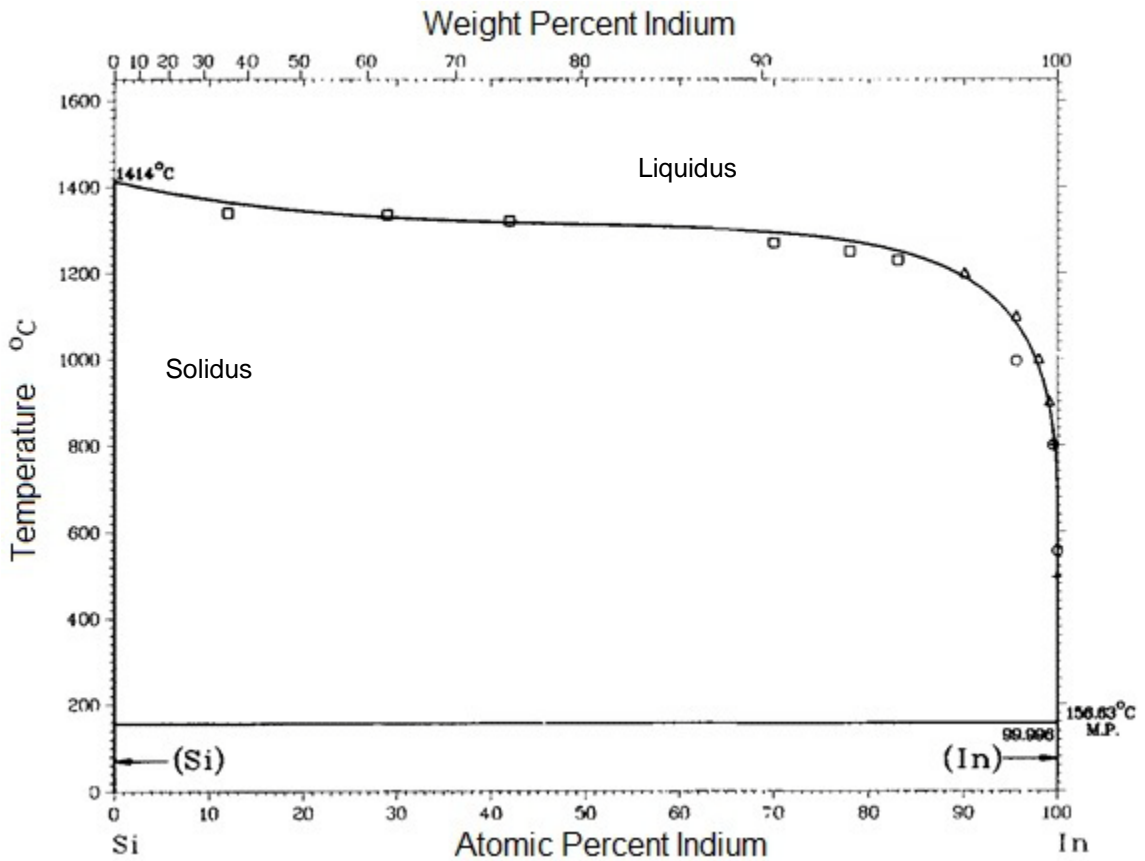


Figure 3.6 Phase diagram of the silicon-indium solution [139]

The phase diagram of the Si-In system was plotted based on the results from a series of experiments. However, to assess the thermodynamic consistency of the data and extrapolate the solubility relations into temperature ranges where it is not covered by experiments, it is useful to develop a phase equilibria model [140]. For a silicon-metal binary system, the liquidus is given implicitly by [141]:

$$-L_{Si} \frac{T_{Si}^F - T}{T_{Si}^F} - \int_T^{T_{Si}^F} \Delta C_{Si} dT + T \cdot \int_T^{T_{Si}^F} \frac{\Delta C_{Si}}{T} dT = RT \ln \gamma_{Si}^L + RT \ln X_{Si} \quad (\text{equ. 3.1})$$

where L_{Si} is the latent heat of fusion for silicon at the melting point of silicon, T_{Si}^F is

the melting point of pure silicon, ΔC_{Si} is the difference in molar heat capacities between solid and liquid silicon $\Delta C_{Si} = \Delta C_{Si}^L - \Delta C_{Si}^S$, and γ_{Si}^L is the activity coefficient of silicon in the liquid phase, indicating the nonideality of the solution. For ideal solution γ_{Si}^L is equal to 1.

$$\mu_i^{S,\theta} = \mu_i^{S,\theta}(T) + RT \ln a_i^S \quad (\text{equ. 3.2a})$$

$$\mu_i^{L,\theta} = \mu_i^{L,\theta}(T) + RT \ln a_i^L \quad (\text{equ. 3.2b})$$

In a solid-liquid two phase system, phase equilibrium is achieved when every component i has equal chemical potential both in liquid phase and solid phase $\mu_i^{S,\theta}(T) = \mu_i^{L,\theta}(T)$, where the $\mu_i^{S,\theta}(T)$ and $\mu_i^{L,\theta}(T)$ are the standard or reference chemical potential for component i in solid phase and liquid phase, respectively. The reference chemical potential is temperature-dependent and phase-independent. R is the ideal gas constant and T is the absolute temperature. a_i refers to the activity of component i in each phase. For the Si-In binary system, at equilibrium condition, the equations become:

$$\mu_{Si}^{S,\theta}(T) + RT \ln a_{Si}^S = \mu_{Si}^{L,\theta}(T) + RT \ln a_{Si}^L \quad (\text{equ. 3.3a})$$

$$\mu_{Si}^{S,\theta}(T) + RT \ln a_{Si}^S = \mu_{Si}^{L,\theta}(T) + RT \ln a_{Si}^L \quad (\text{equ. 3.3b})$$

The activities a_i can be expressed in terms of atomic fractions X_i and activity coefficients γ_i , like $a_i = X_i \cdot \gamma_i$. The equations under equilibrium conditions for each component i become:

$$RT \ln \frac{\gamma_i^L X_i^L}{\gamma_i^S X_i^S} = \mu_i^{S,\theta}(T) - \mu_i^{L,\theta}(T) \quad (\text{equ. 3.4})$$

To determine the liquidus in the Si-In binary, pure solid silicon and pure liquid silicon are chosen as the reference states for chemical potential. That is, the reference chemical potential of liquid phase silicon $\mu_{Si}^{L,\theta}(T)$ is equal to the partial molar Gibbs free energy of pure liquid silicon $\overline{G}_{Si}^{L,\theta}(T)$. Since the reference components are pure phases, the partial molar Gibbs free energy $\overline{G}_{Si}^{L,\theta}(T)$ equals the molar Gibbs free energy $\underline{G}_{Si}^{L,\theta}(T)$. It is the same for the reference chemical potential of the solid phase. Thus, the equations become:

$$RT \ln \frac{\gamma_i^L X_i^L}{\gamma_i^S X_i^S} = \mu_i^{S,\theta}(T) - \mu_i^{L,\theta}(T) \quad (\text{equ. 3.5a})$$

$$= \overline{G}_{Si}^{S,\theta}(T) - \overline{G}_{Si}^{L,\theta}(T) \quad (\text{equ. 3.5b})$$

$$= \underline{G}_{Si}^{S,\theta}(T) - \underline{G}_{Si}^{L,\theta}(T) \quad (\text{equ. 3.5c})$$

$$= -\Delta \underline{G}_{Si}^{FUS}(T) \quad (\text{equ. 3.5d})$$

All terms on the right-hand side of the equations (Equ.3.5a – Equ.3.5d) are properties of silicon which are only functions of temperature. Therefore, for a certain material, e.g. Si, the activity coefficients determine all the distinctive features of the liquidus.

Generally, the activity coefficients for components i and j of a binary system are:

$$RT \ln \gamma_i = \alpha_{ij} \cdot (1 - X_i)^2 \quad (\text{equ. 3.6a})$$

$$RT \ln \gamma_{ij} = \alpha_{ij} \cdot (1 - X_j)^2 \quad (\text{equ. 3.6b})$$

where $\alpha_{ij}(T) = a_{ij} - b_{ij}T$ is the binary interaction parameter, which is temperature-dependent (the absolute temperature, unit: Kelvin), but independent of concentration. Table 3.2 shows some references for the binary interaction parameters, of units J mol^{-1} , for metal solvents which are commonly used for silicon LPE growth.

Table 3.2 Liquid phase binary interaction parameters

Binary pair	Interaction parameter (J mol^{-1})	Reference
Al-Si	-11966	[142]
	23698	[143]
Au-Si	-21004	[142]
Cu-Si	24078	[143]
Ge-Si	6757	[142]
In-Si	36213	[142]
	39221-7.1·T	[144]
Sn-Si	26819	[142]
	82968-20.1·T	[145]

The slope of the liquidus determines the feasible temperature range for growth, as well the growth rate and the maximum amount of silicon that can be deposited for a certain amount of solution. In the case of the Si-In binary system, the equations (equ.3.6) for Si become:

$$RT \ln \gamma_{Si}^L = (a_{Si-In} - b_{Si-In} \cdot T) \cdot (1 - X_{Si})^2 \quad (\text{equ. 3.7})$$

At a low temperature, the solution is dilute in silicon, approximately a few percent of silicon. If it is assumed that $X_{Si} \rightarrow 0$, then:

$$RT \ln \gamma_{Si}^L \cong (a_{Si-In} - b_{Si-In} \cdot T) \quad (\text{equ. 3.8})$$

so that:

$$X_{Si} = X_0 \cdot \exp\left(-\frac{L_{Si} + a_{Si-In}}{RT}\right) \quad (\text{equ. 3.9})$$

where, the quantity $(L_{Si} + a_{Si-In})$ represents the enthalpy change when silicon is dissolved in the liquid metal, and can be assumed to be interpreted as the molar heat of solution ΔH^{soln} . Also,

$$X_0 = \exp\left(\frac{L_{Si} + b \cdot T_{Si}^F}{RT_{Si}^F}\right) \quad (\text{equ. 3.10})$$

Thus, the slope m of the liquidus is:

$$m \equiv \frac{dT}{dX_{Si}} = \frac{1}{X_{Si}} \cdot \frac{RT^2}{(L_{Si} + a)} = \frac{e^{\Delta H/RT}}{X_0} \cdot \frac{RT^2}{(L_{Si} + a)} \quad (\text{equ. 3.11})$$

For a transient cooling silicon LPE process, the thickness of h (in μm) of the grown silicon layer is given by:

$$h = \frac{W_{In}}{A} \cdot \frac{1}{\rho_{Si}} \cdot \frac{M_{Si}}{M_{In}} \cdot [X_{Si}(T^i) - X_{Si}(T^f)] \quad (\text{equ. 3.12a})$$

$$\cong \frac{W_M}{A} \cdot \frac{1}{\rho_{Si}} \cdot \frac{M_{Si}}{M_{In}} \cdot \left[\frac{1}{m} \cdot \Delta T\right] \quad (\text{equ. 3.12b})$$

where, A is the deposition area (cm^2); W_{In} is the mass of the indium melt (g); M_{In} and M_{Si} are the atomic masses of indium and silicon (g mol^{-1}), respectively; ρ_{Si} is the density of solid silicon (g cm^{-3}); $X_{Si}(T^i)$ and $X_{Si}(T^f)$ are the atomic fractions of

silicon in the liquid phase at temperature T^i and T^f , which are the growth initiating temperature and terminating temperature respectively (K or °C).

3.3.2 Nucleation of Silicon from Indium Melt

The driving force for nucleation and crystal growth is the supersaturation which can be simply and directly achieved by supercooling. As the status of the silicon containing metal melts deviates from the thermodynamic equilibrium and the supercooling is sufficient that the free energy exceeds the surface energy barrier required for stable nuclei formation, the nucleation starts.

The degree of the supercooling can be interpreted or measured by the free energy change, thermodynamically. It is assumed that a spherical nucleus of radius r is formed. Therefore the total free energy of an embryonic nucleus ΔG^T consists of two parts: the negative free energy change associated with the super cooling and a positive energy change associated with the formation of the Si-In interface:

$$\Delta G^T = -\frac{4\pi r^3}{3V_m} \Delta H^{sol} \frac{\Delta T}{T^{eq}} + 4\pi r^2 \gamma_{Si-In} \quad (\text{equ. 3.13})$$

where, T^{eq} is the liquidus temperature at the equilibrium condition, V_m is the molar volume and γ_{Si-In} is the interface energy between solid silicon and the Si-In melt.

To form stable nuclei, the radius r of the nuclei is required to exceed a critical value r^* , corresponding to the maximum value of total change of the free energy ΔG^* . By taking the derivative of the ΔG^T with respect to r and setting it equal to zero, the critical radius is given by:

$$r^* = \frac{2 \cdot \gamma_{Si-In} V_m T^{eq}}{\Delta H^{sol} \Delta T} \quad (\text{equ. 3.14})$$

and the critical free energy for stable nuclei formation is

$$\Delta G^* = \frac{16\pi \cdot \gamma_{Si-In}^3 \cdot (T^{eq})^2}{3(\Delta H^{sol})^2 \cdot \Delta T^2} \quad (\text{equ. 3.15})$$

A sufficient supercooling is the essential condition for nucleation, however, a supercooling larger than a certain amount will cause spontaneous nucleation. Brice[146-148] estimated the threshold supercooling for homogeneous nucleation in the bulk of the melt:

$$\Delta T^{hom} \approx \left[\frac{16\pi \cdot \gamma_{S/L}^3 \cdot T^{eq}}{210 \cdot \Delta H_{sol}^2 \cdot V_m \cdot R} \right]^{1/2} \quad (\text{equ. 3.16})$$

where $\gamma_{S/L}$ is the solid-silicon/liquid-indium surface energy and ΔH_{sol} is the enthalpy of solution which is approximately the enthalpy of fusion for silicon. ΔT^{hom} indicates the amount of supercooling that the Si-In melt can be subjected to without spontaneous nucleation in the bulk of the melt. Such a supercooling estimated for metal solvents such as aluminum, gallium, and tin are on the order of 100°C. A supercooling as high as 70°C for the silicon-tin system at 1100°C and one of 30°C for silicon-tin system at 950°C were reported[149, 150].

3.3.3 LPE Growth Modes

The most well-understood parameters that affect nucleation and the subsequent layer formation are 1) surface and interfacial free energies and 2) the state of the substrate surface, in terms of dislocations, misorientation and lattice mismatch. Therefore, the growth modes, which determine the layer perfection

and surface perfection, are mainly classified in terms of surface and interfacial free energy, shown in figure 3.7, and the state of substrate surface, shown in figure 3.8

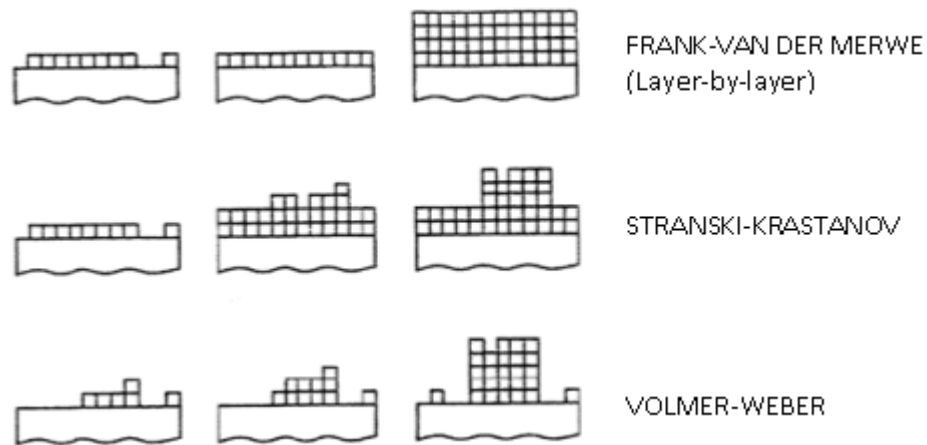


Figure 3.7 Growth modes classified by surface and interfacial energies[86, 151]

Three classical growth modes, shown in figure 3.7, were derived thermodynamically by considering the surface and interfacial free energies between the epitaxial layer and the flat substrate surface[152]: 1) the Frank-Van der Merwe (F-VM) mode, which assumes the interfacial energy between substrate and epitaxial layer is dominating, and therefore leads to layer-by-layer growth with a macroscopic interstep distance ($1\mu\text{m}$ is observed for silicon epitaxy above 1100°C)[153]; 2) the Volmer-Weber (VW) mode, which corresponds to the weakest interfacial energy, and thereby results in three-dimensional island growth and coalescence[86, 154]. 3) the Stranski-Krastanov (SK) mode, as the intermediate state between the F-VM and VW modes, in which the growth initially

starts with compact monolayer formation of layer-by-layer and then continues with three-dimensional island formation and coalescence[155-157].

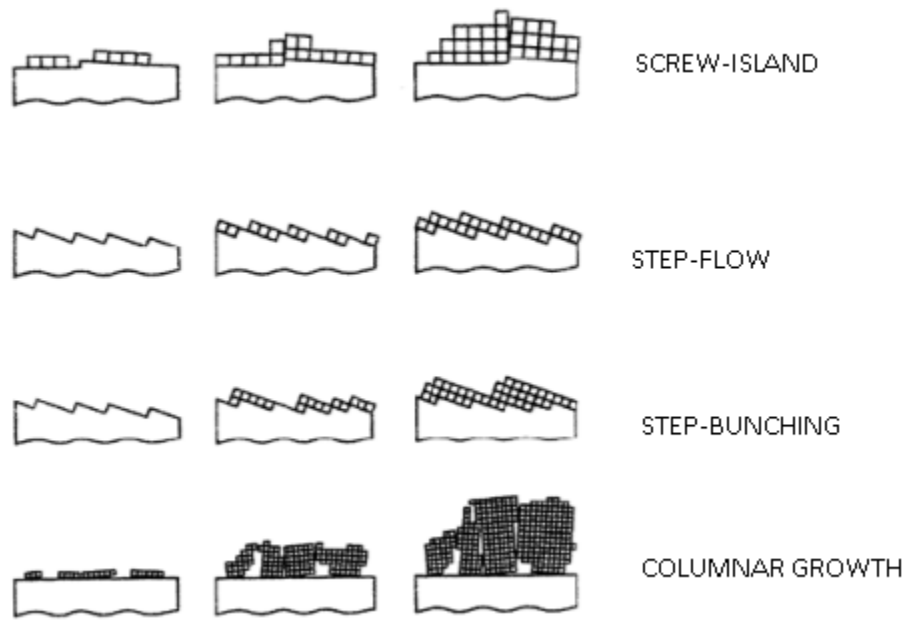


Figure3.8 Growth modes classified by state of substrate surface[86, 151]

Another four modes are classified by considering the state of the non-flat substrate surface: 4) the screw-island mode, where screw dislocation and high density of screw island growth are present on the growth layer due to the screw dislocation of the substrate[158, 159]; 5) the step-flow mode, where a precisely adjusted misorientation of the substrate (typically $0.8-2.5^\circ$) results in short interstep distances and thus prevents islands formation and improves the structure perfection, especially for the VW and SK modes growth; 6) the step-bunching mode, where a large misorientation of the substrate leads to high density step formation. These steps subsequently catch up each other and form

macroscopic steps; 7) the columnar growth mode, being, in principle, a combination of the VW and screw-island modes, or the SK and screw-island modes, where the screw dislocation results in anti-phase grain boundaries at the coalescence of islands[86].

Ideally, the layer-by-layer F-VM mode is desired for premium quality silicon layer growth. Hence, a nearly perfect substrate with misorientation $\theta \approx 0$ is required. Also the supersaturation should be limited to a small value, since the large supersaturation could cause island or cluster formation. However, island formation, step bunching or surface corrugations can be prevented by using the substrate with a precisely adjusted misorientation and microsteps. Because microsteps function as nucleation sites and promote nucleation, they therefore release the supersaturation and improve the perfection of the growth layer.

Chapter 4. Experimental Setup and Procedures

Our early LPE experiments revealed that lateral diffusion close to the substrate surface is the dominant mechanism for silicon epitaxial lateral overgrowth. Thus a growth method that utilizes this lateral diffusion but confines the diffusion from all other directions was proposed. To realize this method we named Lateral Diffusion Liquid Phase Epitaxy (LDLPE), a horizontal slide boat LPE system was built up where the graphite slide boat was specially designed for LDLPE.

4.1 Concept of Lateral Diffusion Liquid Phase Epitaxy (LDLPE)

The term of lateral diffusion LPE emphasize the fact that diffusion of silicon atom in the melt toward the seed are mostly confined to lateral diffusion intentionally, and both the growth rate and the geometry of silicon is thereby determined by lateral diffusion

LPE selective epitaxy and epitaxial lateral overgrowth have been reviewed in chapter 3. The growth is affected by various mechanisms and parameters. Supercooling and supersaturation are essential parameters for nucleation, however, in addition, substrate surface condition, surface energy and interfacial energies results in different growth modes and crystal morphologies, and surface mass transfer is important for the flatness of the epitaxial layer surface.

An experiment in our lab revealed a mechanism that greatly affects the geometry of the LPE epitaxial lateral overgrowth layer. Comparing with early work done on epilift and ELO (epitaxial lateral overgrowth), we used opening windows with 100 μm width as seeds rather than seedlines with a few micron width.

Figure 4.1 shows the epitaxial lateral overgrowth layer on (111) silicon substrate from silicon-indium melt, where the seedline width is 100 μm . After a deep etching back which removes the surface oxide and also forms an under-cut underneath the oxide mask layer, a thick (~70 μm) Si ELO layer is grown. However, it is not a continuous layer like figure 4.2, but consists of two parts which have a gap between them.

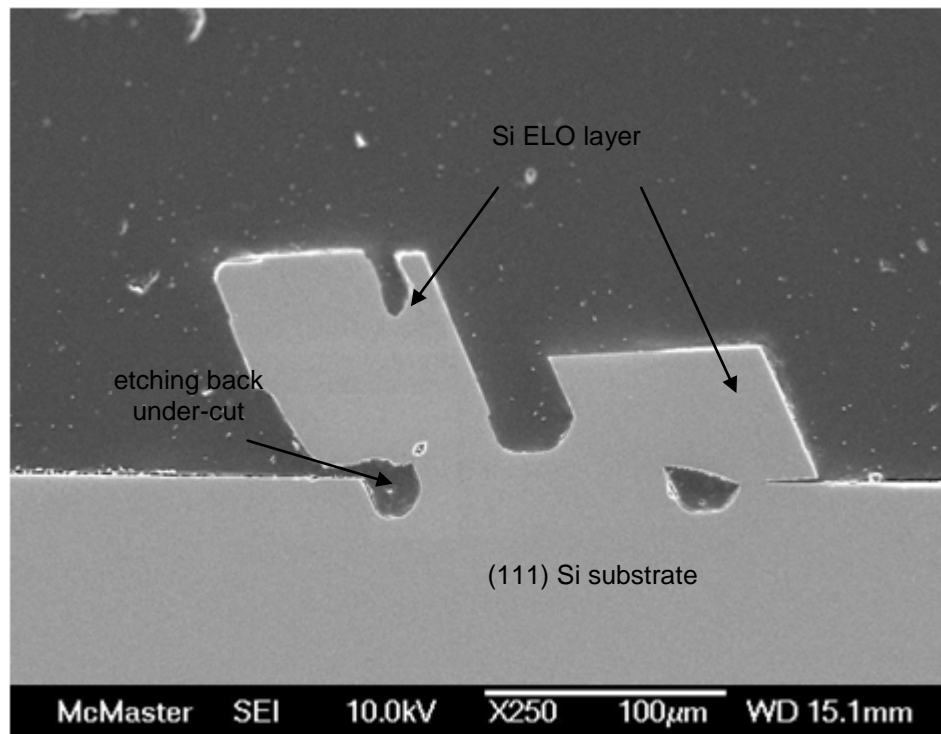


Figure4.1 SEM image of Si ELO layer on 100 μm -wide seedline (cross section)

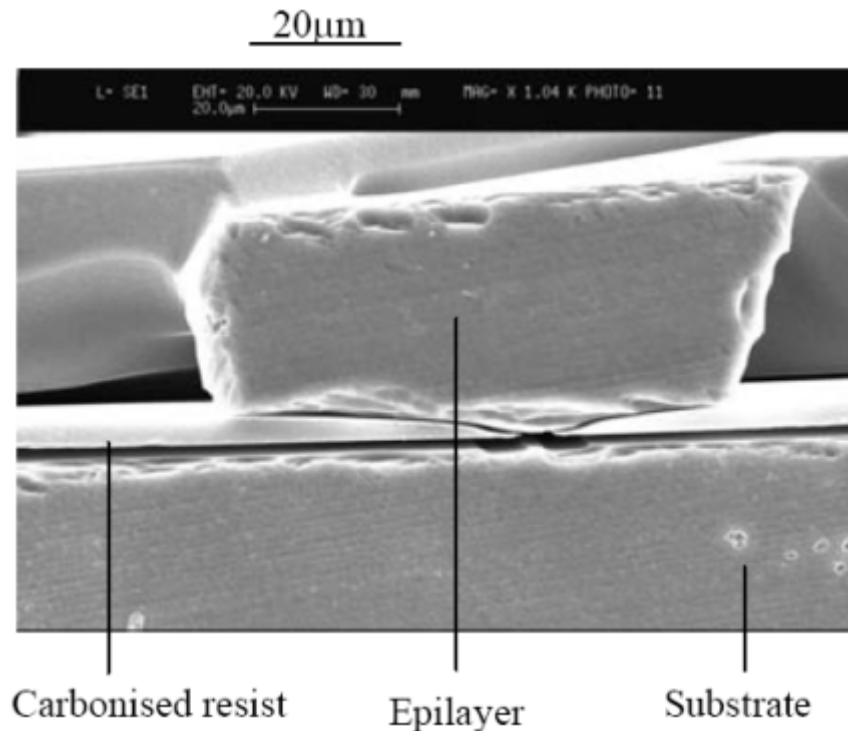


Figure4.2 SEM image of Si ELO layer on 5µm-wide seedline (cross section)[81]

Figure 4.1 shows that the substrate is etched back by at least 10µm to form a trench. Subsequently the etched-back trench is filled by growing silicon, but leaving the under-cut empty. When the epitaxial silicon exceeds the height of the substrate surface, it grows in opposite directions laterally, forming two parts with a gap between them. Ideally, the epitaxial silicon should grow layer by layer and form a continuous ELO layer without a hollow area at the centre. This indicates that after exceeding the height of the substrate surface, the epitaxial layer grows slower at the centre than its two opposite sides. This phenomenon suggests that silicon atoms diffuse to the seed mostly from the lateral directions, along the substrate surface.

Thus, ideally, if a continuous lateral diffusion is maintained but diffusion from all other directions is reduced, the silicon ELO layer will grow laterally continuously without getting thicker. The concept of maintaining lateral diffusion but confining other sources of silicon atoms is shown in figure 4.3 schematically.

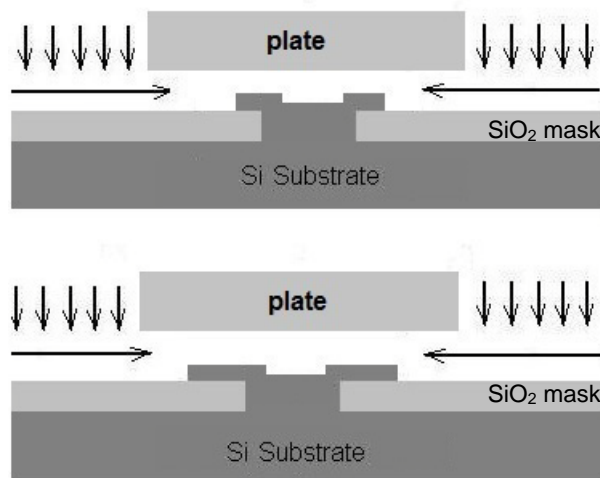


Figure4.3 Concept of lateral diffusion LPE (cross section)

A plate is placed over the seedline, leaving a space between the seedline and the plate. The plate should be made of a material on which silicon does not nucleate. Quartz or graphite is suggested. Arrows roughly indicate the direction of silicon diffusion in the melt. Silicon atoms in the growth solution diffuse to the seedline laterally, rather than from the top of the seedline; the diffusion path from the top is blocked by the plate placed over the growth area. Therefore, the ELO layer grows in width but with a limited thickness imposed by the plate.

4.2 Furnace and Graphite Boat for LDLPE

The slide boat LPE system is ideal for exploring the concept of LDLPE, since the slide boat is amenable to various designs and the horizontal tube furnace is highly versatile and offers ease of control of the movement of the slide boat. Moreover, less metal is needed by the horizontal slide boat system than by the vertical dipping system. The drawing and dimensions of the slide boat designed for LDLPE is shown in appendix I.

4.2.1 Horizontal Tube Furnace

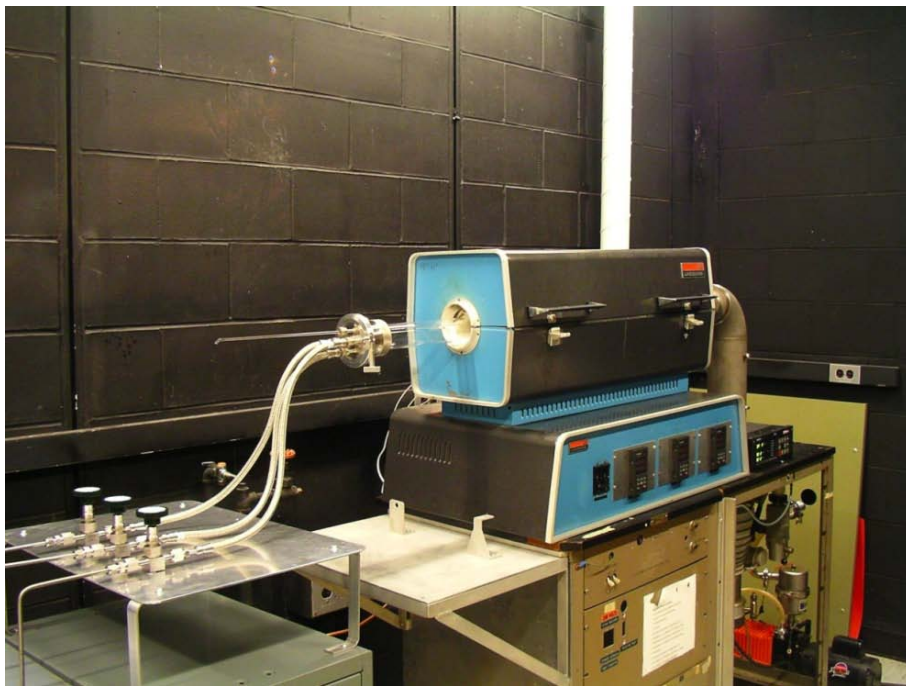


Figure4.4 Three-zone tube furnace for LDLPE

A Lindberg three-zone tube furnace (type: 59744-A) has three resistive heat elements individually controlled by three Omega 16-segment programmable

temperature controllers (model: CN4520), one for each. Thus the furnace has a virtually uniform temperature over the center 30cm length of the 2 inch diameter tube inside the furnace and excellent radial temperature uniformity. A complex temperature profile with up to four ramps can be programmed with different rising slopes, cooling rate and soak time.

Type K-type thermocouples (one per zone) and the microprocessor-based self-tuning PID temperature controllers provide accurate temperature measurement and precise temperature control ($\pm 1^\circ\text{C}$) in the temperature range of 200-1100°C.

4.2.2 Vacuum System

Preventing the formation of oxide during the LPE process at a high temperature is a critical requirement for a successful growth. Oxygen and water vapor have to be removed prior to raising the temperature of the furnace. A vacuum system is used to pump the quartz tube down to 10^{-6} torr. It consists of a diffusion pump connected with one end of the quartz tube through a compression fitting and a mechanical pump on the foreline. The high vacuum is measured and monitored by an ion gauge installed on the stainless steel tube between the compression fitting and the gate valve of the diffusion pump.

4.2.3 Gas System

LPE growth needs an inert or reducing atmosphere to prevent oxidation and reduce the vapor pressure of the metal solvent. As shown in figure 4.5, a platinum membrane hydrogen purifier is used to provide '7N' ultra-high purity hydrogen. A tank of ultra-high purity nitrogen is used for purging/flushing the tube after growth. Three high vacuum valves are used to control the purified hydrogen inlet, the nitrogen inlet and the waste gas outlet, respectively. A glass check valve and checking bottles are used between the waste gas outlet valve and the ventilation pipe to prevent gas back-flow.

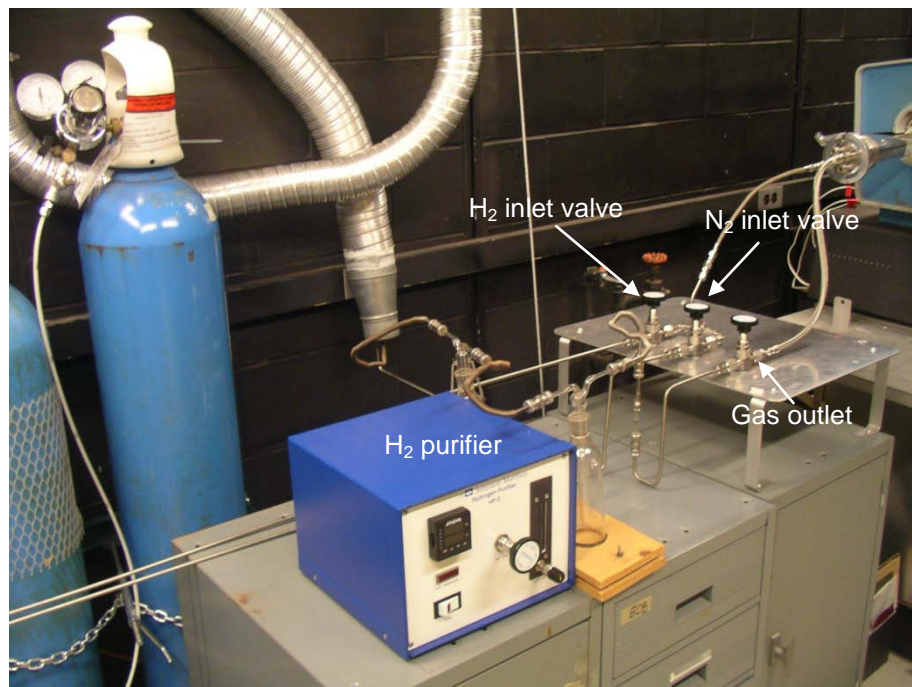


Figure4.5 Gas system for LDLPE

On the other end of the 2 inch quartz tube, a compression fitting and a clamp fitting with four welded feed-throughs on the flange allow 1/4 inch diameter gas inlet/outlet tubes to connect to the 2 inch quartz tube, and two 3/16 inch diameter quartz pushing rods to go through the fitting and control the movement of slide boat inside the 2 inch quartz tube, as shown in figure 4.6. This configuration offers excellent sealing for both vacuum and atmosphere pressure conditions, thus allows high vacuum during pumping down and leaking-free conditions during LPE growth.



Figure4.6 Four feed-throughs for gas inlet/outlet and quartz pushing rods

For safety considerations, a hydrogen leak detector is needed as a warning for hydrogen leaking in the case of o-ring failure or glass breakage. Also

the room should be ventilated well and the waste gas should be purged into the ventilation pipe.

4.2.4 Graphite Slide Boat Design for LDLPE

A frame is design and fabricated with high purity pyrolytic graphite to support an oxide silicon plate to be located over the seedline, shown in figure 4.7. With different frame dimensions, plates with different widths W can be placed over the seedline at different heights H , where H varies between 0.25mm, 0.50mm and 0.75mm. The plate used is also cut from a silicon wafer with a width of ~3mm. A SiO_2 layer is formed all around the plate surface to prevent undesired nucleation on the plate.

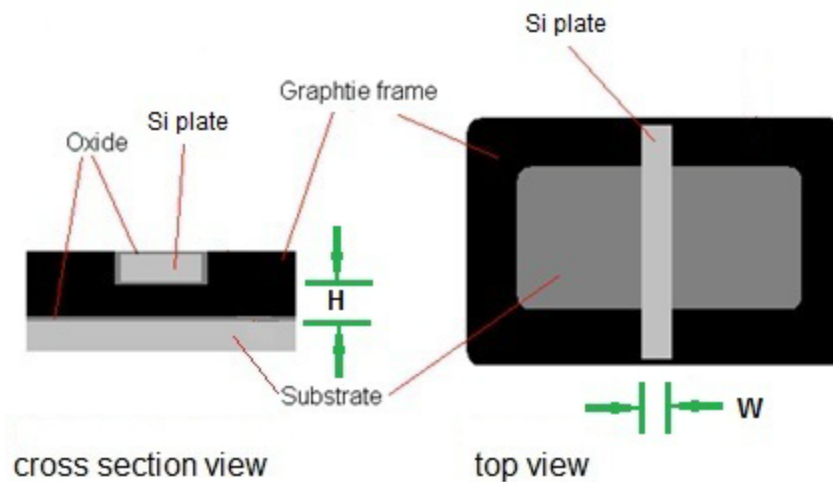


Figure4.7 Schematic of the graphite frame to support the plate over the substrate

The conventional LPE slide boat mainly consists of three parts, as shown in figure 4.8 from top to bottom: 1) the holder, which holds the container by

inserting pins through holes on the holder and container; 2) the two-bin (or multi-bin) melt container and 3) the slider, which has positions in which to place silicon source wafers and substrates. The push rod can hook the slider through the hole on its one end and move it freely without moving the container.



Figure4.8 Conventional LPE graphite slide boat

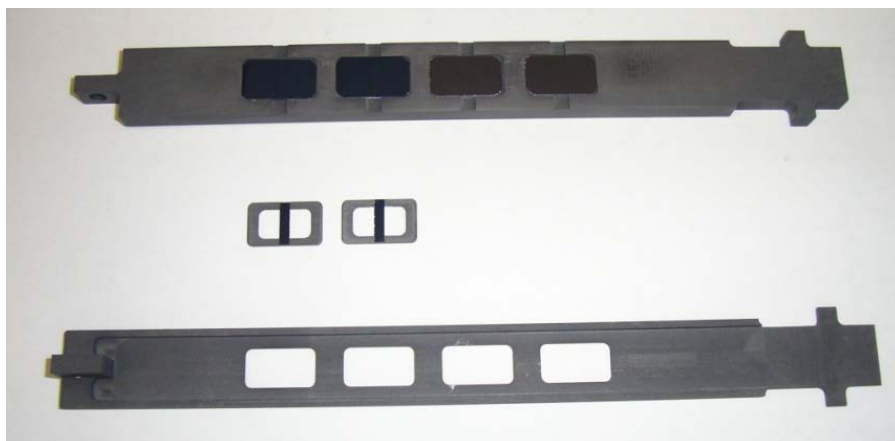


Figure4.9 LDLPE slider #1, frames with plates and slider #2, from top to bottom

The LDLPE graphite boat has the same design of the holder and the melt container as a conventional LPE graphite boat, but it has two sliders rather than

one single slider, shown in figure 4.9. Slider #1 can hold two Si substrates and two source wafers. Each of the two graphite frames holds a Si plate sitting over the substrate. Slider #2 has 4 holes and is able to hold the two graphite frames in the two holes on the left. When the LDLPE graphite boat is assembled (shown in figure 4.10), slider #2 is on the top of slider #1. Slider #2 is able to move independently using the second push rod to move the position of the graphite frames (and hence the position of the Si plates) relative to the substrates.



Figure4.10 Assembled LDLPE slide boat

Figure 4.11 shows the positions of slider #1, slider#2, frames, source wafers, substrates, when they are assembled along arrows in the diagram before the LDLPE graphite boat is loaded into the furnace: source wafers and substrates are placed in the slider #1; two pairs of frame and plate are placed in slider #2. And slide #2 is on the top of slider #1; when sliders are assembled with the melt

container, the melt is on the top of source wafers. As the system is heated up, the indium melt will dissolve source wafers and get saturated.

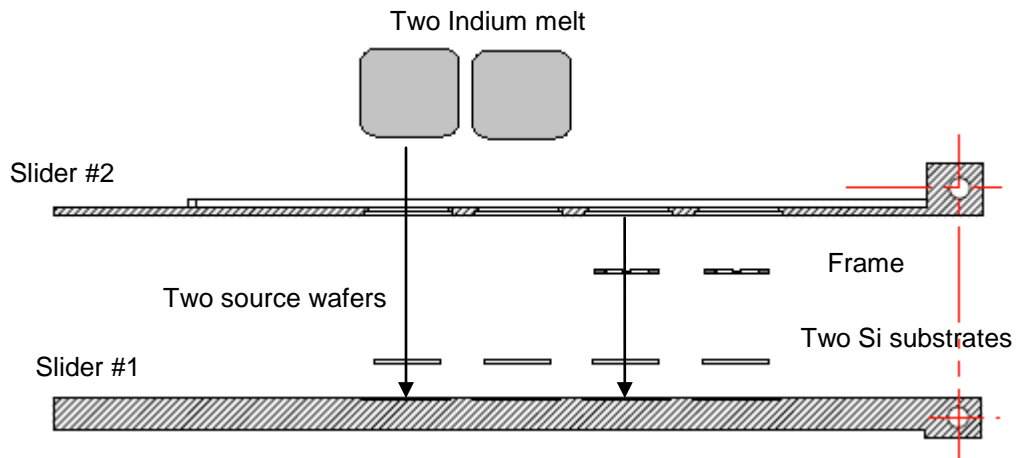


Figure4.11 Positions of sliders, frames, source wafers and substrates when assembled

4.3 Substrate Preparation

As introduced in chapter 3, the (111) substrate results in a flat surface epitaxial layer rather than a layer with a diamond or pyramid cross-section resulting from growth on a (100) substrate. For the purpose of growing single crystalline wafers directly by LDLPE, n-type (111) CZ single crystalline silicon substrates are adopted. Theoretically, silicon grown from indium melt is naturally p-doped. Thus, using the n-type substrate will result in a depletion region between the epitaxial layer and the substrate and promotes ease of electrical measurement of the p-type layer without taking off the epitaxial layer from the substrate.

4.3.1 Substrate Cutting

Rectangular substrates are cut from n-type (111) mono-crystalline Si wafer to a size of 20mm x 12mm by using a dicing saw. Then all corners of the substrate are chamfered by grinding on sand-paper with care. Scratches on the substrate surface should be avoided. Also, 12mm x3mm plates are cut from the same wafer.

Then, the substrates and plates are cleaned by the following procedure: 10 minutes ultrasonic clean in acetone and methanol to degrease; rinse in deionized wafer; 10 minutes gentle boil in a solution of $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2=2:1$ and rinse in deionized water; 10 minutes gentle boil in a solution of $\text{HCl}:\text{H}_2\text{O}_2=2:1$ and rinse in deionized water; 20 seconds dip in buffered HF solution to remove the native oxide and rinse in deionized water; finally, blowing the substrate and plate surfaces until dry by high purity nitrogen.

4.3.2 Silicon Dioxide Growth

After cleaning, substrates and plates are placed in a quartz boat and then put into an oxidation tube furnace. With a steady ultra-high purity oxygen flow, substrates and plates are sintered at 1200°C for 3 hours. Then a SiO_2 layer (~400nm) is formed on the surfaces of the substrate and plate.

4.3.3 Mask Fabrication by Photo-Lithography

The SiO_2 mask layer is fabricated on the substrate by the following steps: spin coating a photoresist (model:S1808) film of ~0.8 μm on the substrate at a

speed of 3000rpm for 30sec; baking substrate at 90°C for 1min 20sec to partially evaporate the organic solvent in the photoresist and harden the photoresist film; covering the substrate by the mask with the desired pattern followed by exposure under UV light (UV lamp: ENTELA B 100AP) for 40 sec; rinsing the substrate in developer (model:351) for 60sec; rinsing the substrate with deionized water and baking it at 120°C for 5mins; etching the substrate in buffered HF solution(40% NH₄F: 49% HF=10:1 in volume) for approximately 6mins 30sec; rinsing the substrate in deionized water and then repeating the cleaning procedures list in section 4.3.1 to remove the photoresist and organic/inorganic residues.

Substrates with different mask patterns are made, as shown in figure 4.12. The seedlines are orientated along the <211> direction, perpendicular to the primary flat, making each single seedline line up in the same direction. The width of the seedline is 100µm, and the width of the central bar, in figure 4.11(b), is 600µm. Before loading into the LPE furnace, the substrates with the SiO₂ mask are cleaned again by repeating the above cleaning procedures. The clean surface will minimize contamination and seedline oxidation which will improve the wettability by indium and therefore improve nucleation on the seedlines.

The source wafers, which are used to saturate the indium melt, are cut from slightly p-type doped Si wafers having the same size as the substrate. The source wafer is cleaned by following the same cleaning procedure as the substrate before the experiment.



Figure 4.12 (a) Single seedline substrate; (b) multiple seedlines substrate (seedlines in white and the oxide mask in grey)

4.4 Silicon LDLPE Growth Procedure

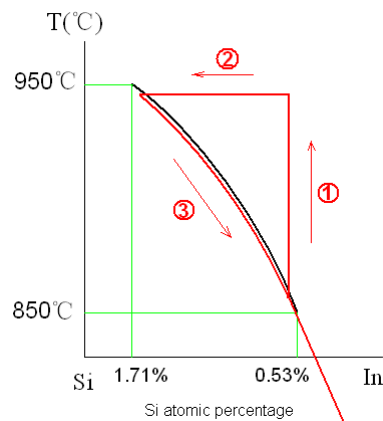


Figure 4.13 Illustration of one cycle of Si LDLPE growth: 1) temperature rises to 950 °C; 2) indium is saturated by Si source wafer, 3) growth starts at 950 °C and terminates at 850 °C, at the cooling rate of 0.25 °C/min

First, the LDLPE graphite boat is loaded with the indium (in the melt container), two graphite frames with plates (in slider #2), two substrates and two p-type source wafers (in slider #1). The slideboat is mounted inside the quartz tube. Then the tube is evacuated and filled with flowing palladium-purified (7N) hydrogen before heating.

Figure 4.13 shows the LDLPE Si strip growth cycle between 950 °C and 850 °C. The basic steps are: 1) The furnace is heated to 950 °C; 2) The graphite boat is baked overnight to remove oxide in the indium melt and to prevent the substrates from oxidizing during growth and the indium is saturated by p-type Si source wafer at 950 °C. The sliders remain their positions relative to the melt until this step, as shown in figure 4.11; 3) Slider #1 and Slider #2 are pushed forward together. The frames with plates and substrates are moved into saturated In/Si melt, as shown in figure 4.14. And the temperature decreases from 950 °C to 850 °C slowly at the cooling rate of 0.25 °C/min. The silicon dissolved in the indium melt precipitates on the seedline until the concentration of silicon in the melt decreases from 1.71% to 0.53% in atomic percentage[139]; 4) The growth is terminated by moving the substrate away from the silicon-rich indium melt.

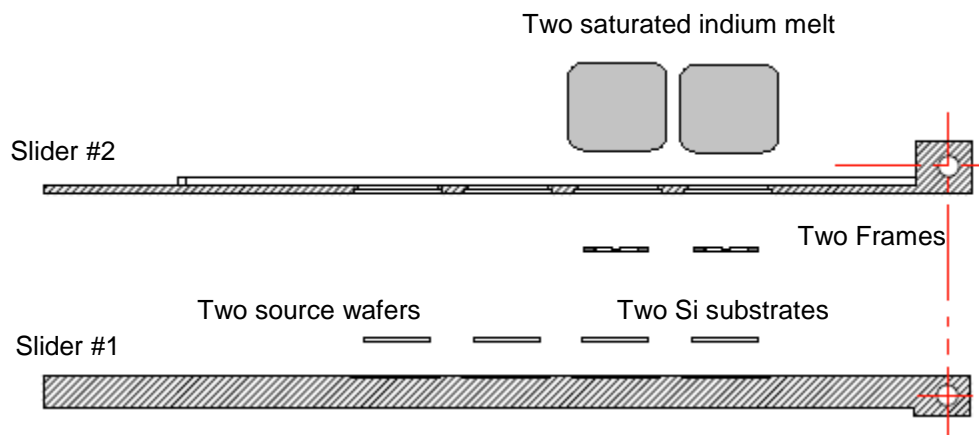


Figure 4.14 Positions of sliders, frames, source wafers when growth starts

Finally, after cooling down the system and purging the hydrogen in the quartz tube, the graphite boat and substrate can be taken out from the quartz tube. The residual indium on the substrate can be removed by hot HCl.

4.5 Pre-wetting Technique

Good wetting of substrate/seed line by indium/silicon alloy melt is an essential requirement for LDLPE. Non-wetting or partial wetting will cause growth failure. Figure 4.15 shows wetting properties of indium on silicon and SiO₂. The small contact angle θ indicates indium can wet pure silicon very well, and the large contact angle indicates the poor wetting properties of indium on SiO₂.

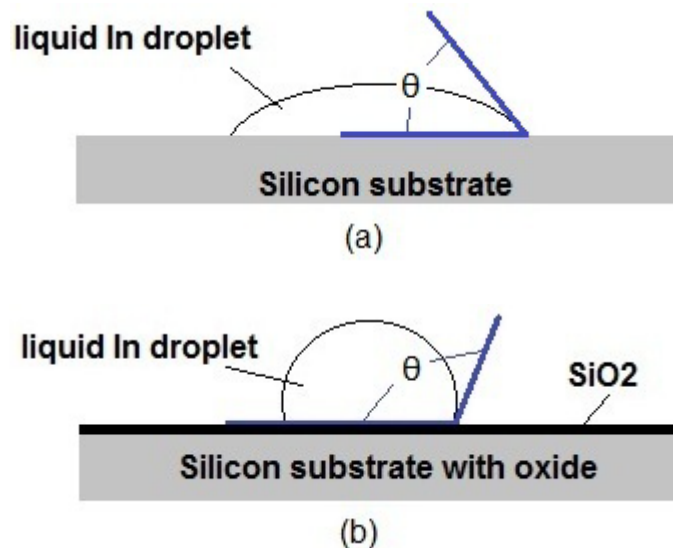


Figure 4.15 (a) Indium melt on pure silicon with an acute contact angle; (b) Indium melt on SiO₂ with an obtuse contact angle

For LPE growth on the substrate with a patterned SiO₂ mask, wetting is a not a problem. However, as shown in figure 4.16 for LDLPE, no matter the plate is push into indium melt with substrate or later than the substrate, because the plate and most areas of the substrate are covered by SiO₂ which cannot be wet well by indium, the plate will push the indium melt away and leave an H₂ bubble (in H₂ atmosphere) between the plate and the substrate. The existence of the H₂ bubble and poor wetting will cause growth failure.

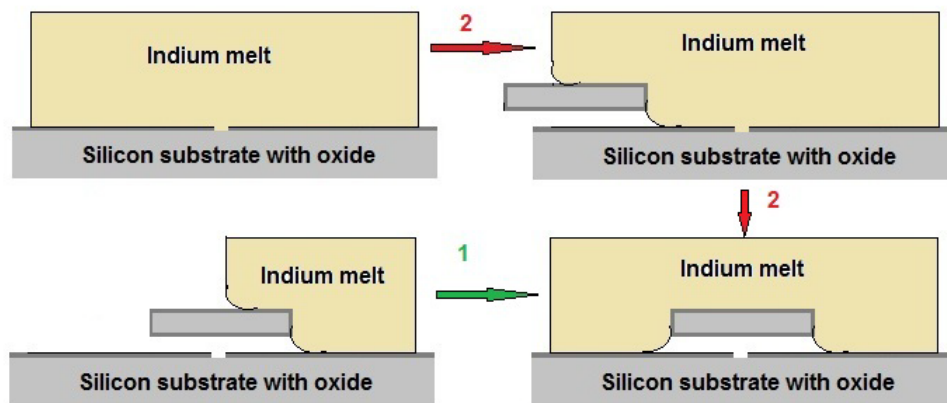


Figure4.16 Hydrogen bubble forms between plate and substrate. Method 1: plate is pushed into indium melt with substrate, method 2: plate is pushed into indium melt later than the substrate

The LDLPE wetting problem is solved by means of pre-wetting, shown in figure 4.17. The space between the plate and the substrate is filled with a droplet of indium before the graphite is mounted inside the quartz tube. Subsequently the indium melt gets saturated by the source wafer. The plates and substrates are pushed into the saturated indium melt together and the plate will now be surrounded by the indium melt, since the space between the plate and substrate

is filled by indium already. Some small H₂ bubbles may stay in this space, however, by moving the plate forward and backward a few times, we can eliminate these bubbles.

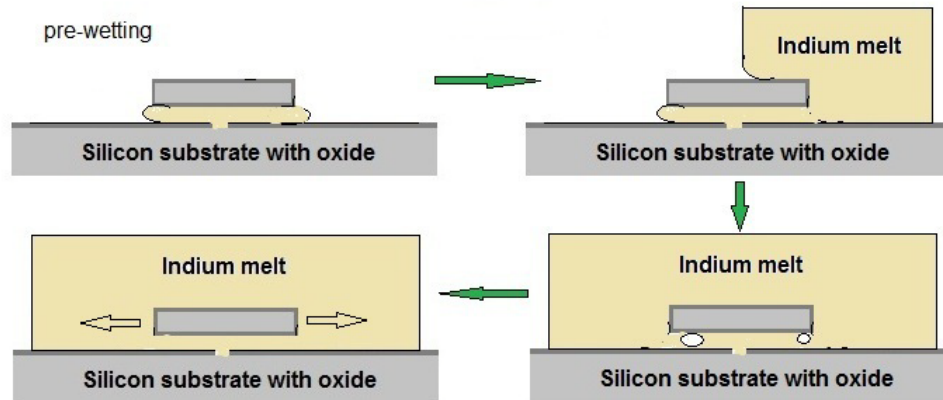


Figure4.17 Procedures of pre-wetting the substrate and eliminating the H₂ bubble by moving the plate backward and forward

4.6 Characterization Techniques

4.6.1 Scanning Electron Microscope (SEM)

SEM (JEOL 7000F) is used to characterize the silicon epitaxial layers grown by LPE and LDLPE from the indium melt. All images were collected using the secondary electron detector. Energy dispersive X-ray spectra (EDS) is not used to characterize the components of the silicon epitaxial layer, since the impurities concentration in the silicon epitaxial layer is much less than the resolution of EDS for material characterization.

4.6.2 X-Ray Diffraction

By comparing observed X-ray diffraction (XRD) patterns with those in the Joint Committee on Powder Diffraction (JCPD) Database, the crystal structure of the silicon ELO layer grown by LDLPE is determined. The diffraction patterns (rocking curve and 2-theta scan) were collected with a Nicolet diffractometer using a copper K_{α} radiation of 0.154nm (Bruker D8 Advance).

4.6.3 Photoconductive Decay

The minority carrier lifetime of the LDLPE silicon ELO layer is characterized by the photoconductive decay measurement. The apparatus mainly consists of a DC power supplier, a function generator (PHILIPS PM 5715), a pre-amplifier (Stanford Research System SR570) with a response time of 0.1 μ s and a digital oscilloscope (Tektronix TDS 1002B).

4.6.4. Hall Effect

The Hall Effect measurement is performed using Accent HL5500PC Hall Effect system with HL5580 amplifier at room temperature. It enables measurement of resistivity, carrier concentration and mobility on a wide range of semiconductors and with minimum effort in sample preparation. Thus carrier concentration in the LDLPE silicon ELO layer can be estimated by assuming all dopant atoms are ionized at room temperature.

Chapter 5. Experimental Results and Discussions

Epitaxy layer overgrowth of silicon is achieved by traditional LPE and LDLPE. By comparing their results, it is demonstrated that the configuration of LDLPE successfully improves the aspect ratio of the ELO layer. The measured electrical characteristics of the silicon ELO layer produced by LDLPE satisfy the electrical property requirements for solar grade silicon wafers. At the end of this chapter, parameters that affect the LDLPE results are discussed.

5.1 Single Crystalline Si Grown by Conventional LPE

5.1.1 Geometries of Si Strips

To grow epitaxial silicon ELO layer by LPE, the graphite boat shown in figure 4.8 is used. The substrates are cut from n-type (111) sc-Si wafers. A SiO₂ layer is formed on the substrate and is patterned as a multiple seedline mask, as shown in figure 4.12(b).

The growth starts at 950°C and is terminated at 850°C with a cooling rate of 0.5°C/min. To improve the wetting of indium on the seedline, an etching back process is adopted: when the substrate is moved into contact with the indium melt, the temperature is raised by 5°C for 5mins, and then the cooling down process begins.

Figure 5.1 shows a SEM image of the silicon grown on the substrate. On the central bar area, a layer of silicon is deposited, however there are large

grooves on the surface. On each seedline, two silicon strips are formed, with smooth top surfaces and side walls. The lengths of the silicon strips are up to 5mm, the length of the seedline on each side of the central bar. No silicon deposition is found on the area masked by SiO_2 .

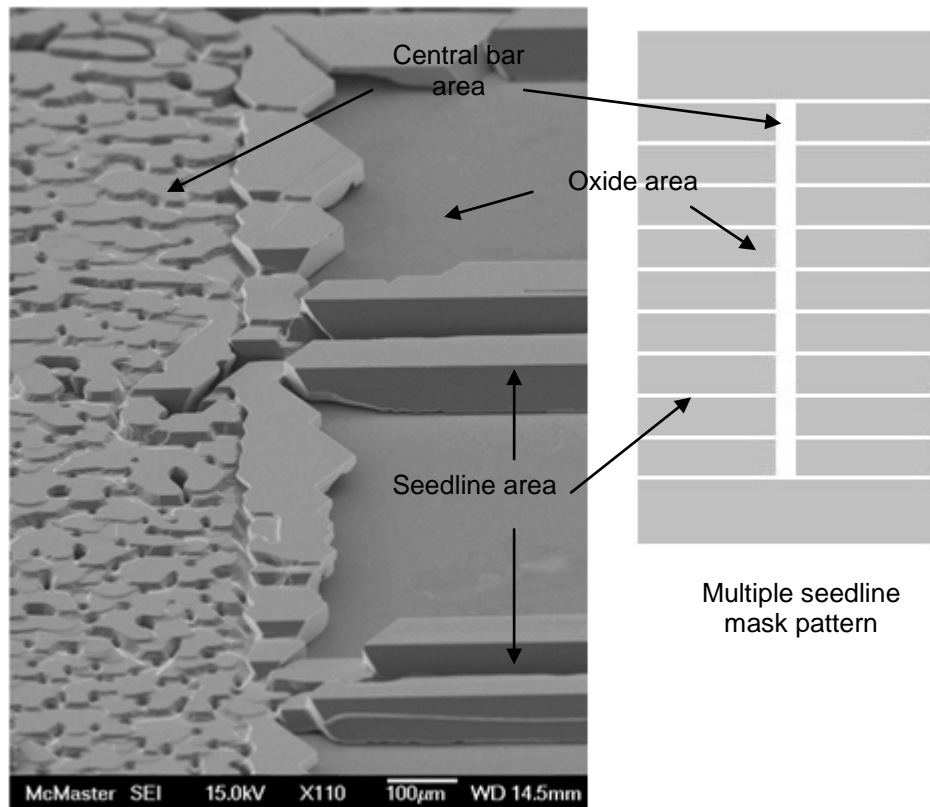


Figure5.1 SEM image of epitaxial silicon grown by LPE on the substrate with multiple seedline (top view with a 60 degree angle)

In order to see the cross-section of the silicon strips grown by LPE, the sample is embedded into epoxy. After the epoxy is cured, the plane of the epoxy block that is perpendicular to the silicon strips is ground using 600 Grit, 800 Grit, and then 1200 Grit sandpapers until the cross-sections of the middle of the silicon strips appear. Then the cross section is polished with $6\mu\text{m}$, and then $1\mu\text{m}$

diamond paste, and finally with colloidal silica. This process is illustrated in figure 5.2.

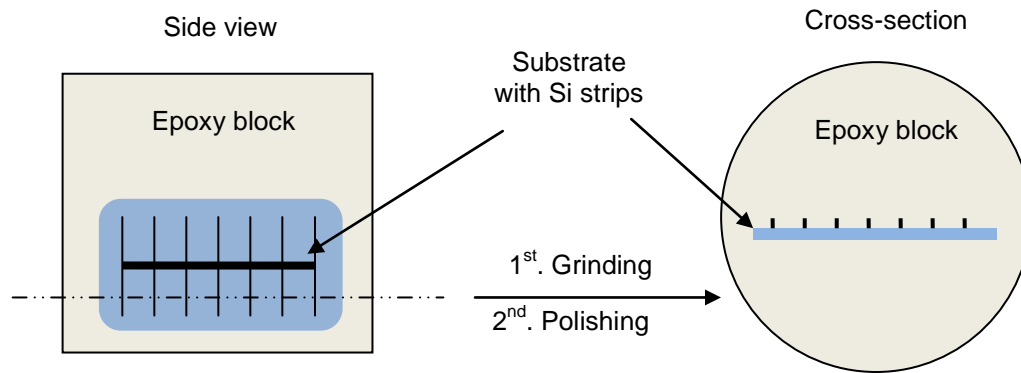


Figure 5.2 Illustration of grinding and polishing process for the cross-section preparation of the LPE silicon strips (the epoxy is ground until the plane indicated by the dash line is reached)

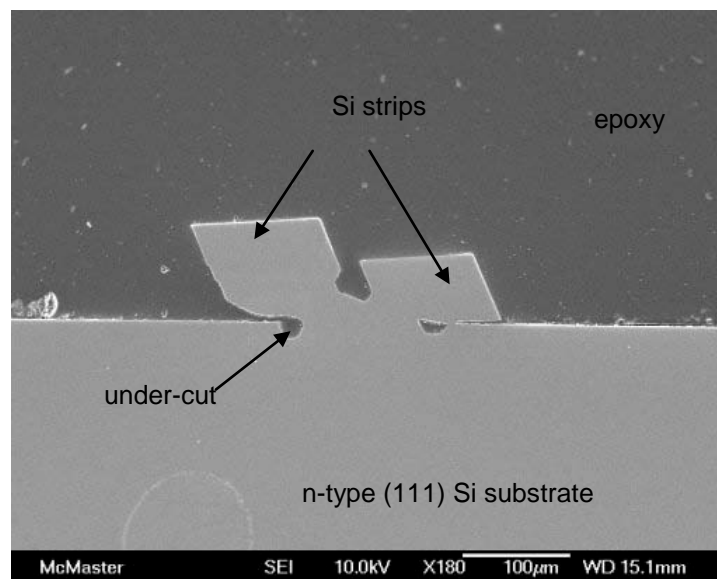


Figure 5.3 SEM image of the cross-section of silicon strips grown by LPE

The ELO layers grown by LPE (the strips) are shown in figure 5.3: the thicknesses of the strips are 70-90 μm ; the widths are around 90 μm and the aspect ratios are 1-1.28. The etching back process results in large under-cuts larger than 10 μm , suggesting a small temperature rise and/or etching back (due that occurred for a short time).

5.1.2 Formation of Under-cut during the Etching Back Process

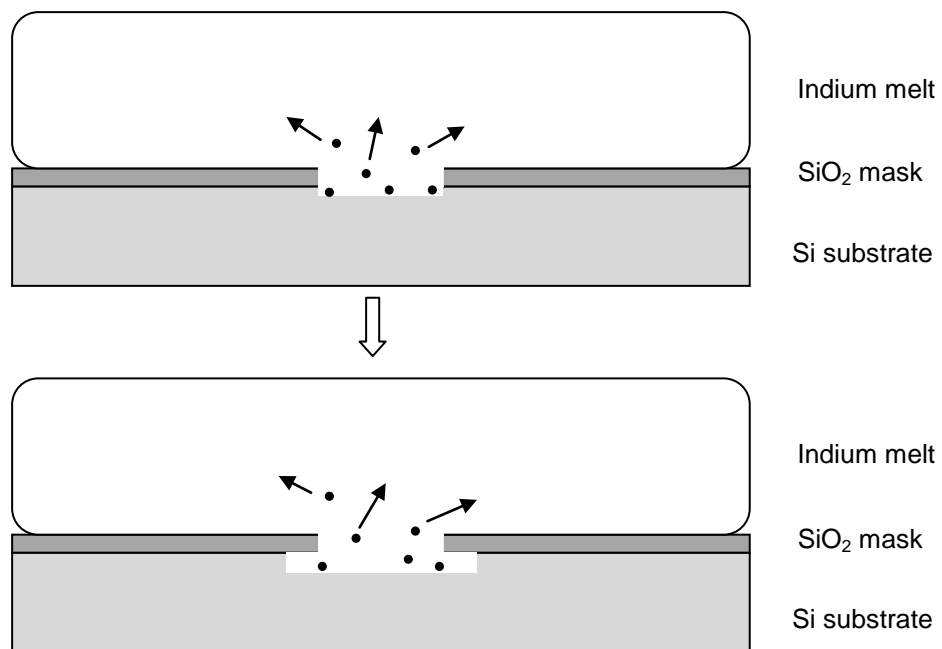


Figure5.4 Formation of the under-cut silicon during etching back

The formation of the under-cut is illustrated in figure 5.4. Due to the temperature rise of the melt, the silicon-saturated indium melt become un-saturated. Therefore the silicon is dissolved into the indium melt, and silicon atoms diffuse to build a new equilibrium condition, as indicated by the dots and

arrows in figure 5.4. At the beginning, only the silicon in the opening window area is dissolved. If equilibrium is not yet reached, the silicon is continuously dissolved isotropically, toward the underneath of the SiO₂ mask, forming the under-cuts.

5.1.3 Si Strip Grown on Single Seedline Substrate

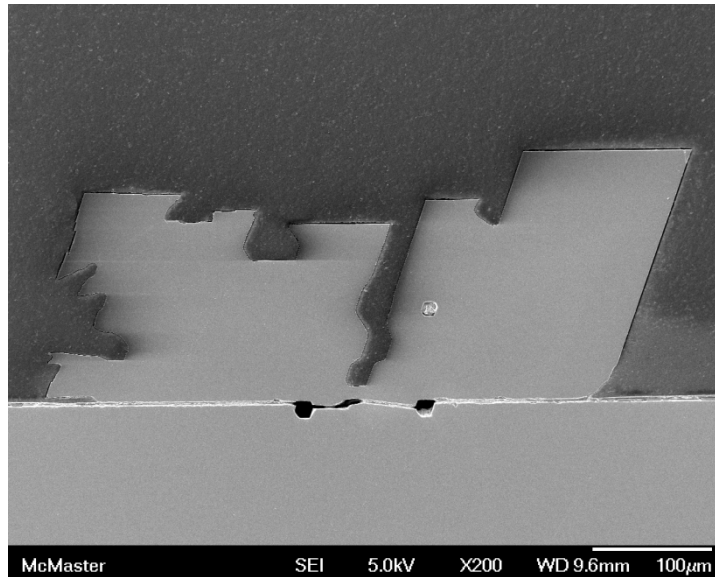


Figure 5.5 SEM image of Si strips grown on single seedline substrate (cross-section)

When a single seedline substrate (cut from (111) wafer with 0.5° misorientation) is used for LPE growth with the same processes as above, the deposition area is only a single seedline. If the cooling rate remains the same (0.5°C/min), the supersaturation will be much larger than that when the multiple seedline substrate is used. A very large supersaturation can cause a fast growth rate, but can also result in spontaneous nucleation in the melt and heterogeneous

nucleation on the SiO₂ mask. Therefore, a smaller cooling rate of 0.25°C/min is used, and the growth result is shown in figure 5.5.

The strips grown on the single seedline substrate are bigger than that shown in figure 5.4 as expected: the thicknesses are 173-207 μm; the widths are 206-262 μm and the aspect ratios are 1-1.5. Although a small cooling rate of 0.25°C/min is used, terraces and steps are formed on the silicon strips. The reason is likely fast but uneven growth due to the large supersaturation. The aspect ratios of the strips are not significantly different from those of strips grown on the multiple seedline substrates. This result indicates that the cooling rate has no obvious effect on the aspect ratio of the strips.

5.2 Single Crystalline Si Grown by LDLPE

5.2.1 Improvement of the Silicon Strip Aspect ratio

LDLPE silicon is grown on a single seedline substrate, with a configuration that the plate has a width of $W=2.7\text{mm}$ and is situated a height $H=0.5\text{mm}$ above the seedline, see figure 4.7. The pre-wetting process introduced in section 4.5 ensures a good wetting of indium on the seedline which has only a 0.5mm space between itself and the plate. Also, the indium used for the pre-wetting process removes native oxide on the seedline when the system temperature rises from room temperature to the growth start temperature. Hence, some etching back is caused by the pre-wetting process, and a separate etching back process before growth is not necessary.

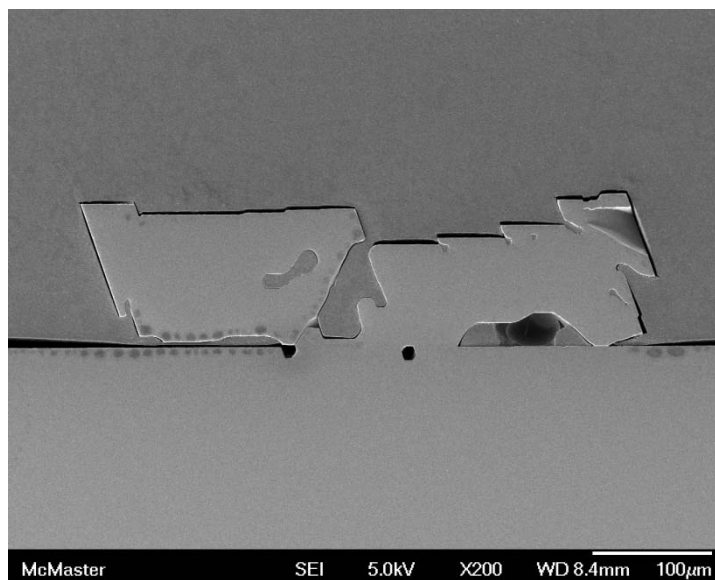


Figure5.6 SEM image of cross section of Si strips grown by LPE (aspect ratio: 1.75-2.82)

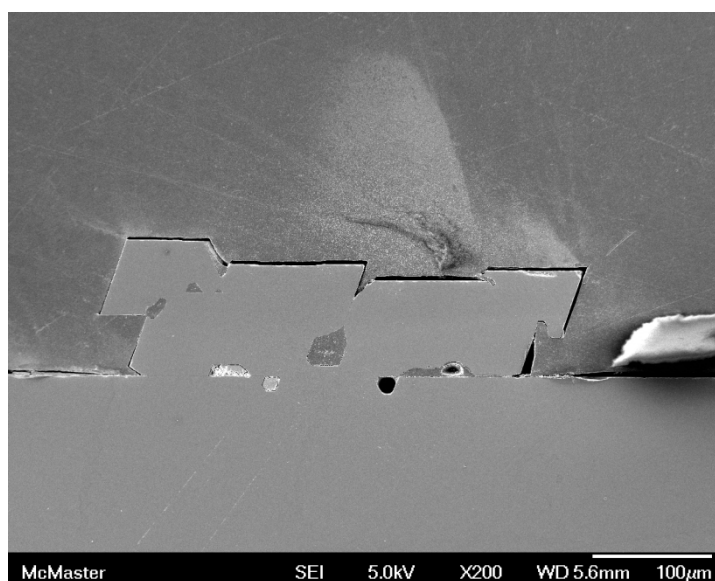


Figure5.7 SEM image of cross section of Si strips grown by LPE (aspect ratio: 1.5- 2.75)

The growth starts at the temperature 950°C and is terminated at 850°C at a cooling rate of 0.25°C/min. For strips in figure 5.6, the thickness is 83-126 μm, the width is 220-234 μm and the aspect ratio is 1.75-2.82. For strips in figure 5.7, the thickness is 80-120 μm, the width is 180-220 μm, and the aspect ratio is 1.5-2.75.

The average aspect ratio of LDLPE strips is bigger than 2, indicating the plate sitting over the seed line has a significant effect of increasing the aspect ratio and changes in cooling rate and substrate only have a minor contribution.

5.2.2 Formation of Terraces and Vacancies

Although (111) planes are favorable facets for both LDLPE and LPE strips, LDLPE strips have terraces on the surfaces and vacancies in the solid, as shown in figure 5.6 and figure 5.7. This is probably caused by the large supersaturation, since the precipitation of silicon on the single seedline may not be able to effectively release the supersaturation built up during the cooling process.

When the silicon precipitates on the seed line and the strip keeps growing, each facet of the strip tends to form a (111) plane, which has the highest atom density and smallest surface energy. After a facet becomes a (111) plane, it becomes a less favorable growth facet, because Si atoms prefer to precipitate on other non-(111) plane facets until they become smooth (111) planes and therefore reduce the surface energy. After all facets become (111) planes, the Si strip tends to grow slower and layer by layer. However, due to the large surface

area of the strip and the large supersaturation, the starting point of the layer growth is random, and the growth front may not propagate from one end to another on the strip facet. The growth front may stop somewhere and another layer may start to grow in a different direction and therefore terraces are formed. If a bridge is formed between two terraces, a vacancy will be formed in the silicon strip.

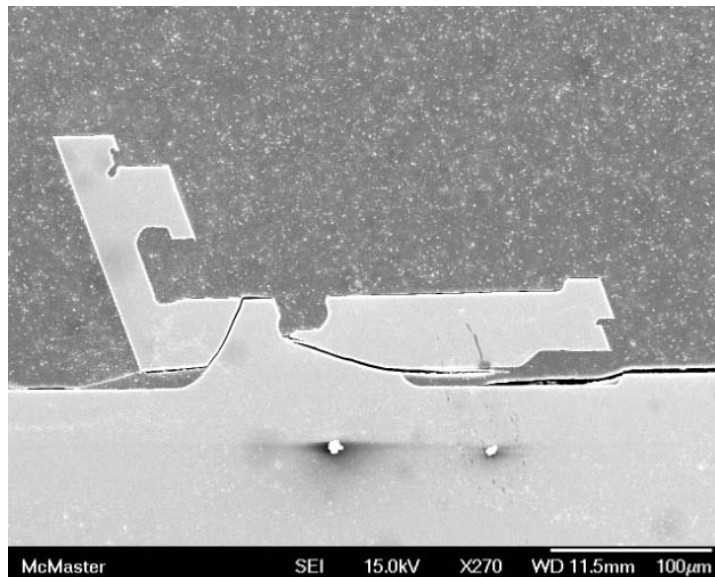


Figure 5.8 SEM image of cross-section of LDLPE Si strips with large terrace

Figure 5.8 shows a good example of the turning of growth direction. At the beginning, the two strips grow to the right and the left respectively. Half way through the growth, the left strip forms a perfect (111) plane on the left side facet. Therefore the strip stops growing to the left but grows upward. And then, again, it stops growing upward but grows to the right. At the same time, although ledges form on the right-most end of the right strip, the right strip keeps growing to the

right and achieves a large aspect ratio over 3, where the width is $\sim 180\mu\text{m}$ and the thickness is $\sim 50\mu\text{m}$.

5.3 X-Ray Crystallography

5.3.1 Silicon Strip Separation from Substrate

When a LDLPE Si strip is characterized by X-ray diffraction, it is best peeled off from the substrate, because the LDLPE Si strip is homogeneously epitaxially grown on the (111) Si substrate and the strip most likely has the same diffraction pattern as the substrate. A process is developed to separate the LDLPE strips and the substrate which is illustrated in figure 5.9 and figure 5.10:

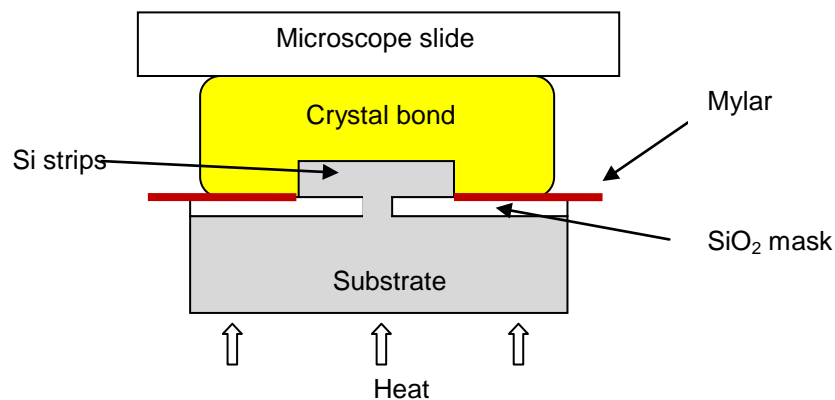


Figure 5.9 Bonding Si strips to glass carrier with crystal bond

1) Cover the masked area of the substrate with heat resistant plastic film such as Mylar™, a polyester film, leaving the silicon strips uncovered. The Mylar™ film has a thickness of $\sim 50\mu\text{m}$ and could withstand a high temperature up

to 200°C. 2) Heat the substrate to 90°C on a hot plate and apply crystal bond on the substrate. Due to the use of Mylar™ film, the molten crystal bond merges the silicon strips and covers the Mylar™ film, but does not contact the substrate. 3) When the silicon strips are fully emerged in the molten crystal bond, a microscope slide is put on the molten crystal bond as the glass carrier.

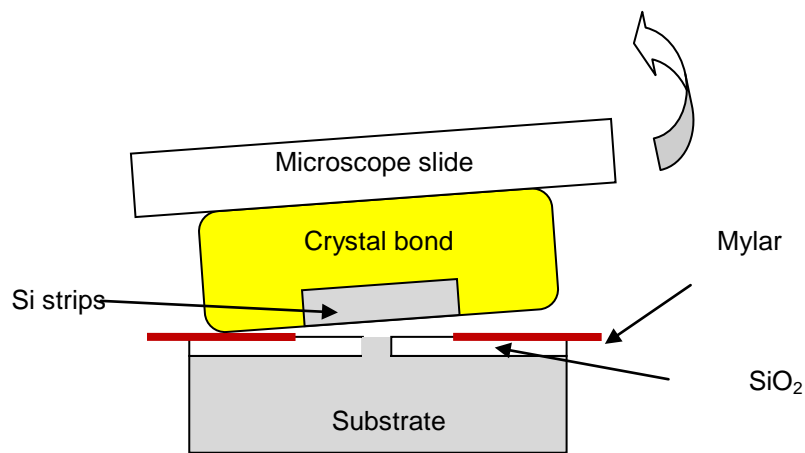


Figure 5.10 Separating silicon strips from the substrate

4) After cooling the sample down to the room temperature, the crystal bond solidifies and bonds the silicon strips and Mylar films to the microscope slide. A mechanical force applied to the microscope slide will break the silicon strips at the seedline and separate them from the substrate, as shown in figure 5.10. 5) When the crystal bond is dissolved in acetone, the silicon strips are separated from the Mylar films and microscope slide, and are ready for the X-ray diffraction characterization.

5.3.2 X-ray Diffraction of LDLPE Silicon Strip

The rocking curve and 2-theta scan are obtained using Bruker D8 Advance XRD system. Figure 5.11 shows the X-ray diffraction pattern of 2-theta scan from 25° to 70°. Only one single peak is observed at 28.45°. By comparing the results with the silicon XRD patterns in the Joint Committee on Powder Diffraction (JCPD) Database, the observed peak is identified as the diffraction pattern of (111) planes of crystalline silicon. The absence of other peaks indicates that the LDLPE silicon strips are (111) single crystals with diamond cubic crystal structure.

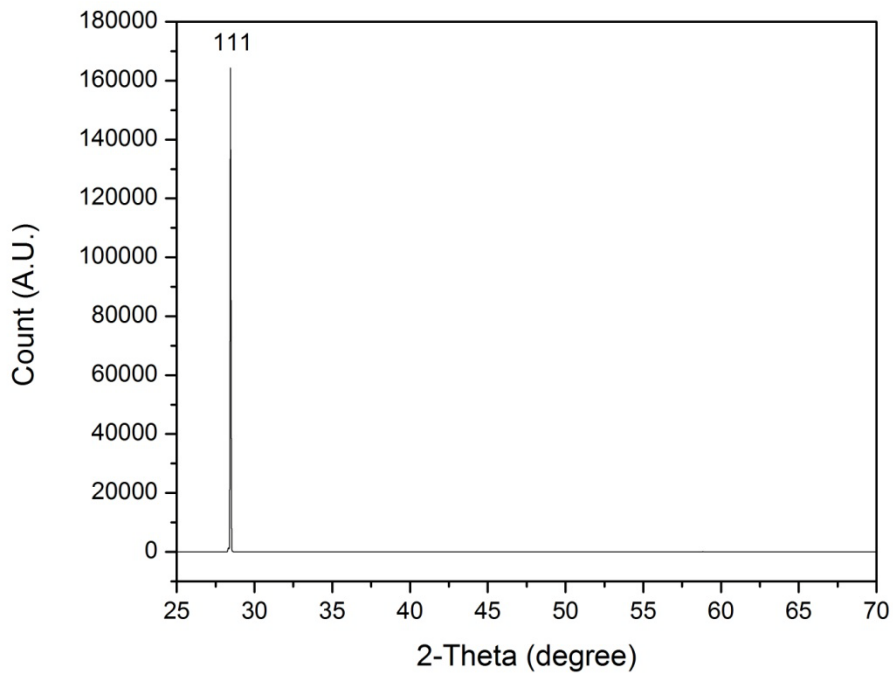


Figure 5.11 XRD pattern of 2-theta scan for LDLPE Si strip

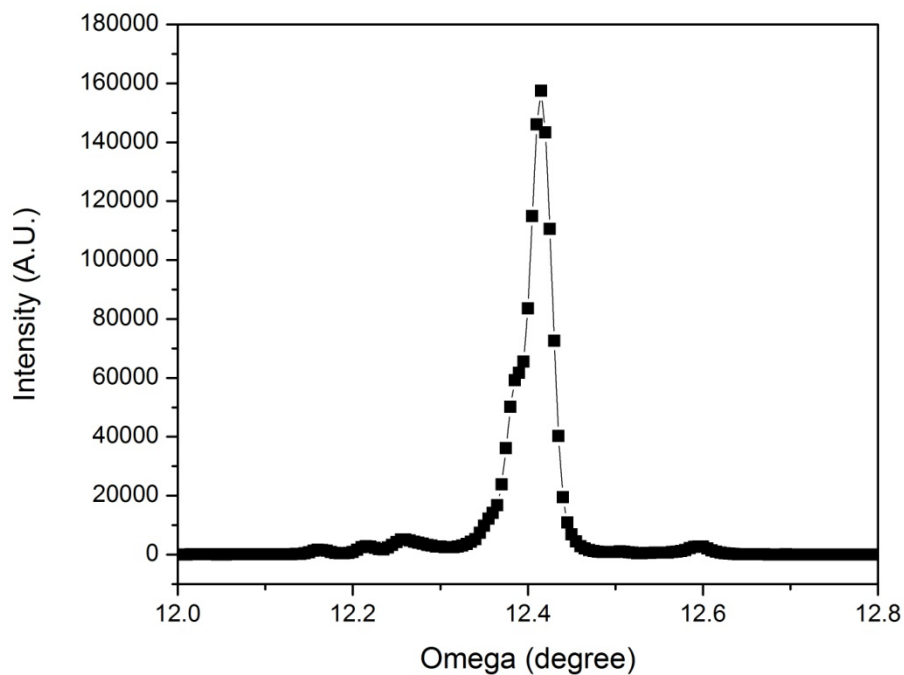


Figure 5.12 XRD pattern of (111) rocking curve for LDLPE Si strip

Figure 5.12 shows the XRD pattern of (111) rocking curve for a LDLPE Si strip peeled off from the (111) Si substrate. The peak is observed at 12.4° , having a full width at half maximum (FWHM) of 0.03° .

Theoretically, silicon strips grown at a near equilibrium condition should have near perfect crystal structure. However the FWHM of the rocking curve of the LDLPE silicon strip is much larger than that of an epitaxial thin film grown by LPE and MOCVD, which can grow. Two possible reasons may cause this result: 1) the silicon strip is very narrow relative to the width of the X-ray beam 2) The terraces on the strip surface and vacancies in the strip may also cause widening of the rocking curve peak.

5.4 Electrical Characterization

5.4.1 Hall Effect

Theoretically, the Si strip grown from the indium melt is naturally doped by indium, resulting a p-type doping. The concentrations according to a solubility limit of indium in solid silicon are temperature dependent, ranging from $10^{16}/\text{cm}^3$ to $1.6 \times 10^{18}/\text{cm}^3$, for growth temperatures from 920°C to 1250°C respectively [111, 120]. A high growth temperature results in a high growth rate, however, it also results in a high doping level. The doping level and the mobility of holes are significant to solar cells. The p-type crystalline silicon wafer for solar cells are typically required to have a relatively low doping levels on the order of $10^{16}/\text{cm}^3$ and resistivities ranging from 0.1 to $5\Omega\cdot\text{cm}$ [160, 161].

For Hall Effect measurement, two sample configurations are normally adopted: 1) Van der Pauw samples or 2) bar or bridge-type samples, illustrated in figure 5.13 and figure 5.14 respectively. The Van der Pauw configuration requires that the sample should be of uniform and small thickness and relatively large in area, and that the contacts are sufficiently small and located on the perimeter of the sample. The bar or bridge-type configurations require the sample to be symmetrical and suggests a sample length of $10\sim 15\text{mm}$, and a sample width $>2\text{mm}$ [162].

Although the LDLPE method improves the width: thickness aspect ratio, the typical size of strip obtained after one growth cycle is smaller than $0.2\text{mm} \times 0.1\text{mm} \times 5\text{mm}$ (width x thickness x length). This makes contact making on the

strip for Hall Effect measurement very difficult for either the Van der Pauw configuration or the bridge-type configuration.

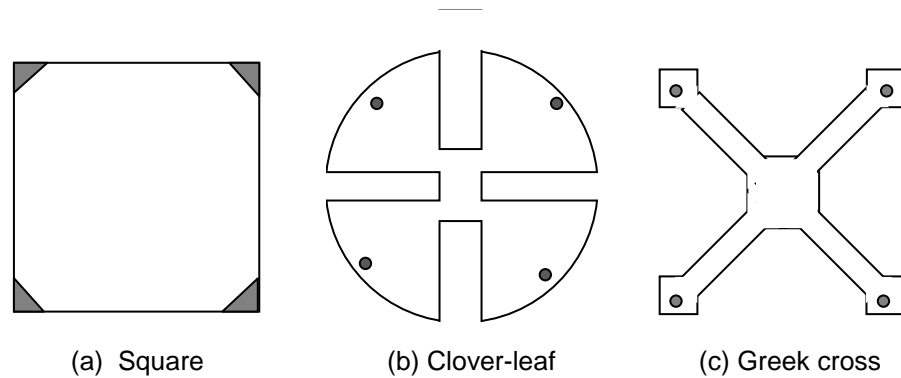


Figure 5.13 Typical Van der Pauw patterns and contacts positions [162]

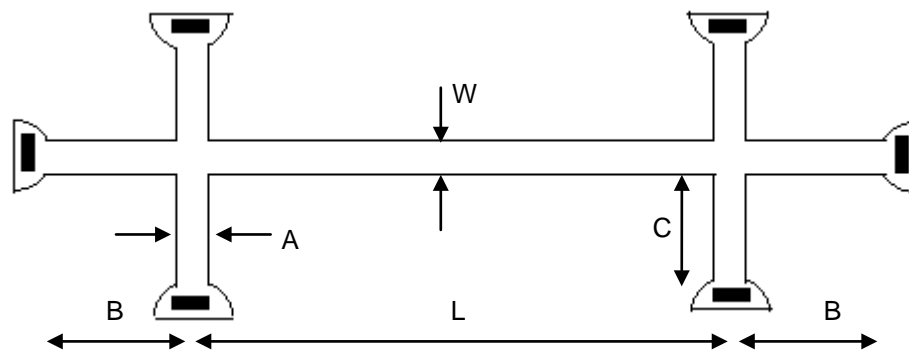


Figure 5.14 Typical bridge-shape samples and contact positions ($10\text{mm} \leq L \leq 15\text{mm}$, $W \leq 0.2L$, $A \leq W/3$, $B \geq 2W$ and $C \geq 1\text{mm}$) [162]

To obtain a sample which satisfies the requirements for Hall Effect measurement, a layer of Si is epitaxially grown on the antimony doped n-type substrate (cut from (111) wafer with 0.5° misorientation) with a round-shape opening window, using the same temperature profile as the LDLPE Si strip growth. The thin film is round, $40\mu\text{m}$ thick and has an area of 3.2mm^2 , as shown in figure 5.15. Four ohmic contacts are formed by painting gallium/indium eutectic

alloy on the circumference of the silicon film. Although the sample shape and contact positions do not resemble any of the three typical configurations shown in figure 5.13, they satisfy the Van der Pauw requirements for Hall Effect measurements.

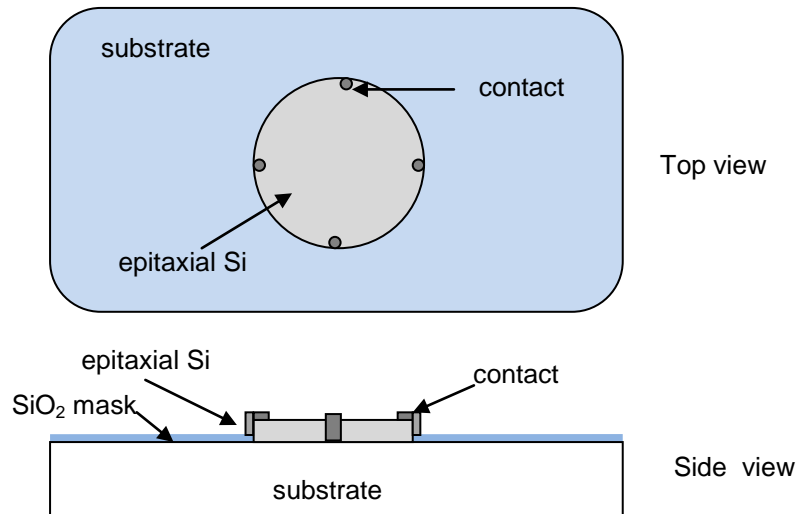


Figure 5.15 Epitaxial silicon film for Hall Effect measurement and contact positions

Because the same growth temperature and same cooling rate are used, the silicon film for Hall Effect measurement is supposed to have a similar composition, a similar doping level, and similar semiconductor properties to the LDLPE Si strips. Commercial p-type solar grade silicon is typically doped by boron at a level $\sim 2 \times 10^{16}/\text{cm}^3$ and the doping level can be varied according to the specific solar cell process. Correspondingly, p-type silicon with resistivity from 0.1 to $5\Omega\cdot\text{cm}$ is used for solar cells. [161]. In figure 5.16, it can be found that solar grade silicon has a hole mobility around $350 \text{ cm}^2/\text{V}\cdot\text{s}$, typically.

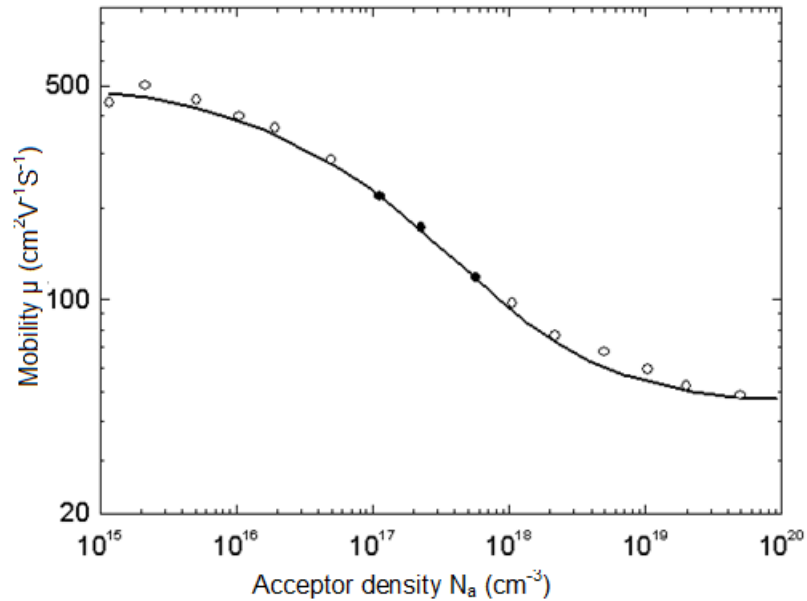


Figure 5.16 Hole drift mobility versus acceptor density at 300 K [163]

The Hall Effect measurement is performed using Accent HL5500PC Hall Effect system with HL5580 amplifier at room temperature. The substrate is antimony n-type doped, having a resistivity of 1-10 $\Omega\cdot\text{cm}$. If the epitaxial layer is p-type, a p-n junction will be formed between the epitaxial silicon film and the substrate. The Hall Effect system is able to correct for the effect of the depletion region and measure the junction-isolated layers.

According to references [126], the LPE silicon grown from indium is naturally p-type doped. However, the measured result shows that the epitaxial film is n-type, not p-type as we expected. Its resistivity is 0.41 ohm-cm, the carrier concentration is $3.9 \times 10^{16}/\text{cm}^3$, and the measured electron mobility is $391 \text{ cm}^2/\text{V}\cdot\text{s}$. There are some potential problems that may cause the observed conflict between measurement result and our expectation. One is the metal contacts on the

epitaxial layer are also on the side of the epitaxial layer and reach the oxide mask layer. The metal contact may penetrate the oxide or diffuse through the boundary between the oxide and the epitaxial layer, and reach the n-type substrate during the heat treatment. Therefore, in the future, Hall Effect measurement should be done on the detached LDLPE strip when we achieve bigger size, which is big enough for making a Hall Effect measurement sample.

To investigate the dopant concentration, a series of Hall Effect measurements should be carried out to find the carrier concentrations at different temperatures and hence determine activation energy for the dopant. Since at an intermediate temperature, the carrier concentration approximately equals the net doping, $|N_A - N_D|$, it decreases at low temperature due to incomplete ionization of the dopants and increases at high temperature because the intrinsic density approaches the net doping density.

At high temperature, for n-type silicon, the carrier density simply equals to the intrinsic carrier concentration,

$$n = n_i = \sqrt{N_C N_V} \exp\left(\frac{-E_g}{2kT}\right) \quad (\text{equ. 5.1})$$

$$\text{for } T \geq \frac{E_g}{k \ln N_C N_V - 2k \ln |N_D - N_A|}$$

where N_C and N_V are the density of state in conduction band and valence band respectively, N_D and N_A are the donor density and acceptor density respectively.

At low temperature, the carrier density is dominated by the ionization of dopants,

$$n = -\frac{(N^*+N_A)}{2} + \sqrt{\frac{(N^*+N_A)^2}{4} + N^*(N_D - N_A)} \quad (\text{equ. 5.2})$$

$$\text{for } T \leq \frac{E_g}{k \ln N_C N_V - 2k \ln |N_D - N_A|}$$

where E_C is the energy state of the conduction band and E_D is the energy of donor impurity state, so $E_C - E_D$ is the ionization energy.

$$N^* = \frac{N_C}{2} \exp\left(-\frac{E_C - E_D}{2}\right) \quad (\text{equ. 5.3})$$

The temperature dependence of carrier concentration is related to the activation energy by fitting the carrier density versus $1/T$ on a semi-logarithmic scale to a straight line of the form $n(T) = C \exp(-E_A/kT)$, where C is a constant. At high temperature, the activation energy equals to half the bandgap $E_A = E_g/2$. At low temperature, it equals to half the ionization energy $E_A = (E_C - E_D)/2$ when the electron density is lower than the donor density but higher than the acceptor density, or equals to ionization energy $E_A = E_C - E_D$, when electron density is lower than the acceptor density. The energy of the donor follows the Fermi-Dirac distribution, therefore the concentration of ionized donor is obtained by

$$N_D^+ = n = N_D [1 - f_F(E_D)] \quad (\text{equ. 5.4})$$

and then a quadratic equation for free carrier concentration can be obtained, where g is the ground state degeneracy and $E_d = E_C - E_D$

$$n^2 - \frac{1}{g} N_D N_C e^{-E_d/kT} + \frac{1}{g} n N_C e^{-E_d/kT} = 0 \quad (\text{equ. 5.5})$$

Therefore, when the free carrier concentration and activation energy are obtained from Hall Effect measurement, the dopant concentration can be obtained from equation 5.5[164]

5.4.2 Photoconductive Decay

The photoconductive decay time τ refers to the minority carrier lifetime at an ideal condition, where the sample is not modified and the surface recombination is negligible. However, most photoconductive decay measurement techniques produce the “effective lifetime” which is a conglomeration of bulk and surface recombination and device effects. To eliminate the device effects which are caused by forming contacts on the sample, contactless techniques are used, such as the microwave photoconductive decay technique[165]. Methods to distinguish the bulk and surface recombination are much more complicated: multiple measurements are required, and for most occasions, complicated surface preparation, dedicated equipment and/or sacrificial measurement samples are required.

Due to the small size of the LDLPE silicon strip sample, it is not practical to perform a contactless measurement, and very difficult to passivate the sample surface. The photoconductive decay time measured by using the experiment setup shown in figure 5.17 actually provides the “effective minority lifetime” of the sample. The following discussion and calculation is based on the assumption that the LDLPE strip is naturally doped with indium and is p-type silicon.

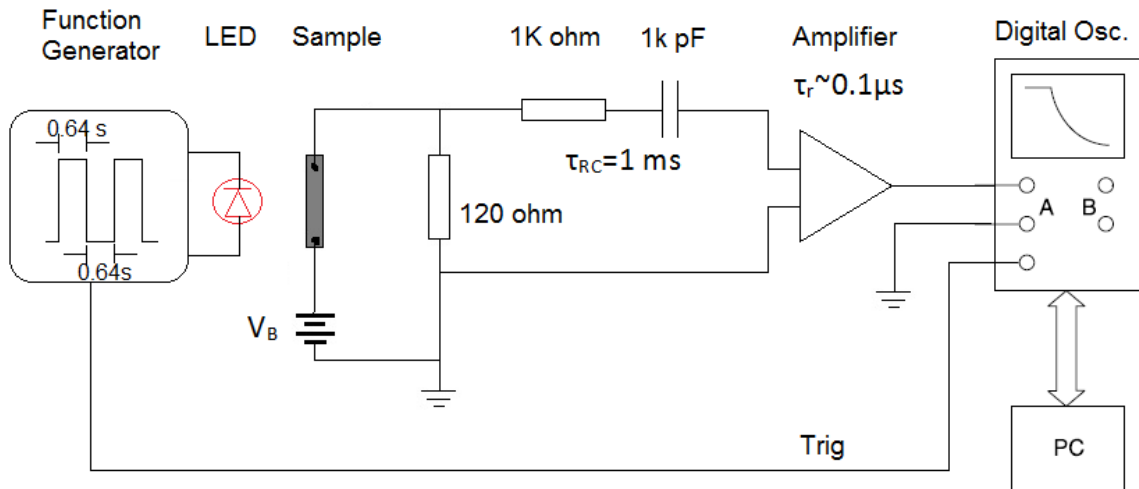


Figure 5.17 Experiment setup for photoconductive decay measurement

The silicon strip is first separated from the substrate and then ohmic contacts are formed on each end of the Si strip. The distance between the two contacts is 4mm. Bias across the sample is applied by a DC power supplier. The test strip is uniformly illuminated by super bright red ($\lambda=660\text{nm}$) light emitting diodes (LEDs) ($\lambda=660\text{nm}$, maker: Avago). The LEDs produce light pulses of 0.64s in width with a time delay of 0.64s between two pulses. The photo-generated pulses are amplified by SRS SR570 pre-amplifier with a response time of $0.1\mu\text{s}$ and they are recorded by a digital oscilloscope. Then the data is analyzed by a computer to determine the photoconductive decay time.

Figure 5.18 shows the measured photoconductance at room temperature when the bias voltage V_B across the sample is 1V. The photoconductance decays exponentially versus time and the time constant of the exponentially fitted curve is $24.4\mu\text{s}$.

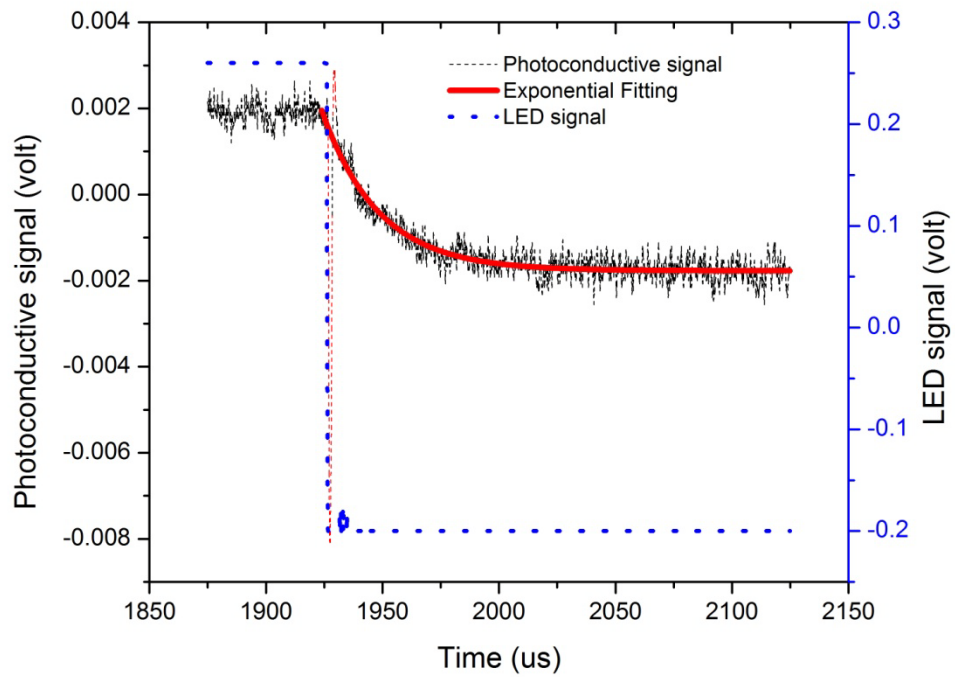


Figure 5.18 Photoconductive signal and the exponential fitting curve, bias = 1V

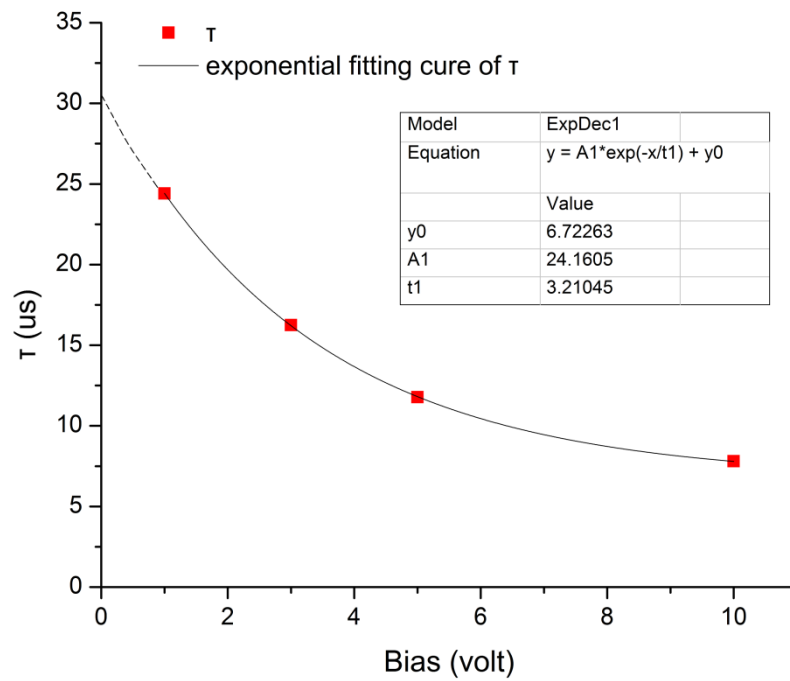


Figure 5.19 Photoconductive decay time measured with 1V, 3V, 5V and 10V bias at 300K

However, when a larger bias voltage is applied, a smaller photoconductive decay time is measured. Figure 5.19 shows the photoconductive decay time measured with 1V, 3V, 5V and 10V bias voltage, which are 24.4 μ s, 17.1 μ s, 12.0 μ s and 9.0 μ s respectively. These measured data points are fitted by an exponential function:

$$y = A_1 * \exp(-x/t_1) + y_0 \quad (\text{equ. 5.1})$$

where $A_1 = 24.16$, $t_1 = 3.21$ and $y_0 = 6.72$. This equation indicates an estimated photoconductive decay time $y = A_1 + y_0 \approx 30.9\mu s$, when bias voltage is zero ($x = 0$), obtained by extrapolating the curve as show in figure 5.19.

The effect of the bias voltage on the measured results is firstly complicated by the possibility of high-level injection. Under the high-level injection condition, the exponential decay is no longer valid. The excess minority carriers cannot decay exponentially, since there are not enough recombination sites, which are mostly occupied by injected electrons. Therefore, the recombination slows down and measured decay time should become longer under the high-level injection condition. Since we see a good fit of the decay with an exponential function, we will assume low level injection.

The “end effect” may explain why the photoconductive decay time decreases as the bias voltage increases. In an infinitely large sample, a light pulse generates excess carriers in a localized region. After the light is turned off, these excess carriers drift in the applied electric field until they recombine. When the sample is of a finite size, it is possible that excess carriers reach the metal

contact at the end of the sample before they recombine. In this condition, when excess carriers reach the metal contact, they are collected instantly, and the measured decay time appears shorter than the actual value.

Figure 5.20 shows the schematic of the sample with metal contacts on each end and the energy band diagram along the sample. Due to the heat treatment for making ohmic contacts, p^+ regions are formed in the contact regions of the sample. In these heavily doped p^+ regions, the minority lifetime τ_{end} is much shorter than τ_{bulk} , the minority lifetime in the bulk. However, the p^+ region has very small thickness, and therefore has negligible effect on the measured result.

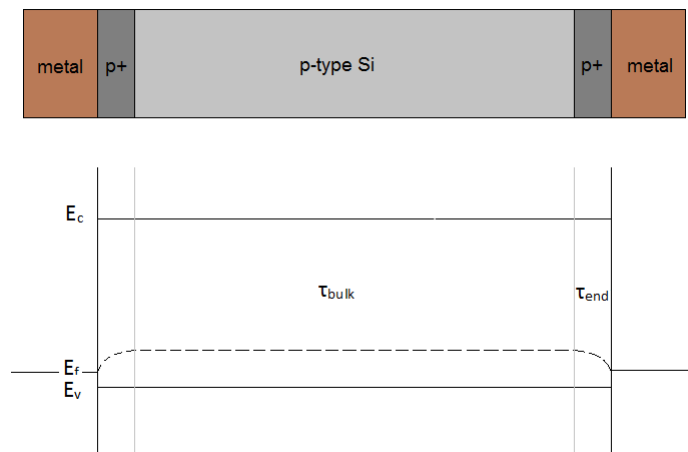


Figure5.20 Schematic of photoconductive measurement sample and the energy band diagram

In order to avoid the “end effect”, the transit time τ_t that defines the time for carriers to drift from the middle of the sample to the contact, should be much larger than the minority carrier lifetime τ_{bulk} . Now τ_{bulk} is equal to the measured

photoconductive decay time, and surface recombination can be ignored. Transit time can be evaluated as follows:

$$\tau_t = \frac{\text{distance}}{\text{velocity}} = \frac{L/2}{\mu E} = \frac{L/2}{\mu \cdot V_0/L} = \frac{L^2}{2\mu V_0} \quad (\text{equ. 5.2})$$

where V_0 is the applied bias voltage across the sample, L is the length of the sample, and μ is the carrier mobility.

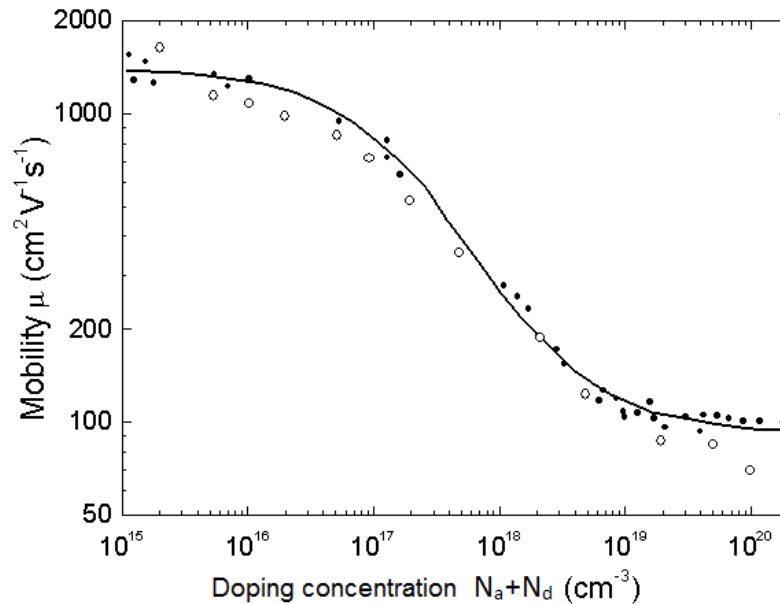


Figure 5.21 Electron drift mobility vs. total doping concentration for Si at 300K [163]

From the Hall Effect measurement, the carrier concentration of the silicon strip is around $3.9 \times 10^{16}/\text{cm}^3$. The electron drift mobility is approximately $1100 \text{ cm}^2/\text{V}\cdot\text{s}$, shown in figure 5.21. Therefore the transit time τ_t is $72.7\mu\text{s}$, $24.2\mu\text{s}$, $14.5\mu\text{s}$, and $7.3\mu\text{s}$ for 1V, 3V, 5V and 10V bias, respectively. Comparing with the measured photoconductive decay time, with 1V bias applied, the transit time τ_t is 2 times larger than the photoconductive decay time, indicating the “end effect” will

only have a small effect when the bias voltage is smaller than 1V for this sample. However, a small bias voltage will cause difficulties for measurement, since the noise signal becomes relatively big.

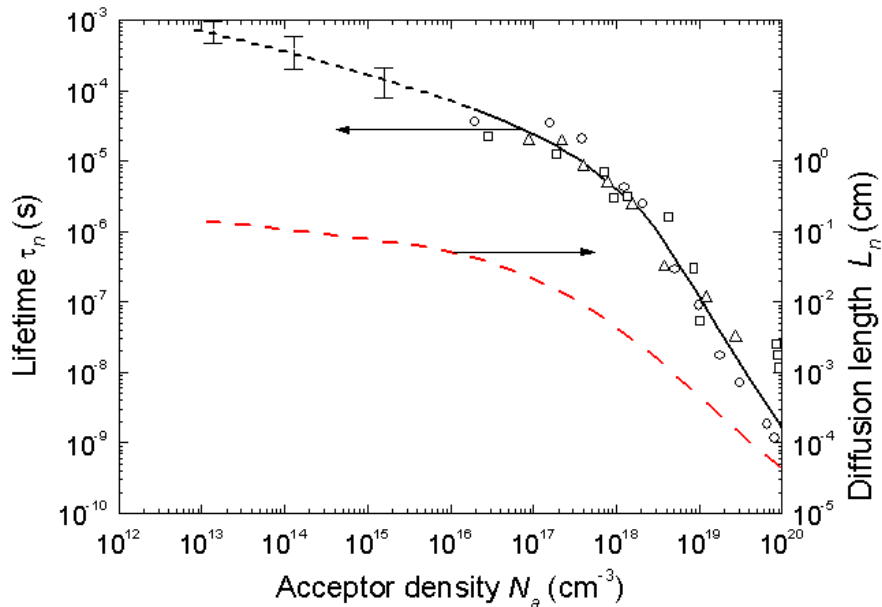


Figure 5.22 Electron lifetime vs. acceptor density at 300K[166]

When the bias voltage is assumed to be 0V, electrons, the minority carriers will not drift to the metal contact and the “end effect” can be negligible. Therefore the estimated photoconductive decay time $\tau = 30.9 \mu\text{s}$ which can approximately refer to the minority lifetime, is close to the $40 \mu\text{s}$ shown in figure 5.22 from the literature[166].

5.5 Random Walk Modeling and Monte Carlo Simulation

In order to understand the mechanism of LDLPE silicon strip growth, a 2-D Monte Carlo random walk model is used to simulate the effect of the plate on the aspect ratio of the silicon strip. Some assumptions are applied: 1) The indium/silicon melt is a dilute solution and silicon atoms are randomly distributed in the melt; 2) Silicon atoms move randomly and independently of other silicon atoms; 3) The silicon atom sticks when it reaches the solid silicon; it continues the random walk when it reaches the SiO₂ mask or/and the plate; 4) The site occupation probability depends on the surface condition: free silicon atoms favor sites that have more silicon atom neighbours over sites having fewer silicon atom neighbours; 5) the substrate and the epitaxial silicon have the simple crystal structure shown in figure 5.23; 6) indium doping is ignored.

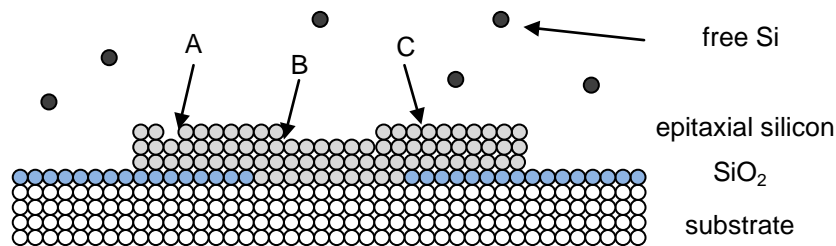


Figure 5.23 The simplified crystal structure and the site occupation probability $1 > A > B > C > 0$.

It is not practical to fully simulate 3-D bulk LDLPE Si growth by calculating each atom, since a huge amount of calculation is needed and it exceeds the computing capability of our desktop computers. To simplify the simulation, the

Monte Carlo random walk model was performed in a small 2-D space, presented by a 1000 x 1000 unit matrix. Each unit is occupied by a particle, formed by a group of atoms, either indium or silicon. Each silicon atom can move one unit during each time interval in one of the four directions randomly by exchanging its position with the neighboring indium melt atom, with equal probability. The seedline is 100 units wide and is located in the lower middle of the matrix. The plate is represented by a rectangle in the model which is 100 units above the seed line. The dimension of the rectangle is 200 x 50 unit, which is not to scale. Figure 5.24 shows both the LDLPE and LPE results for a comparison.

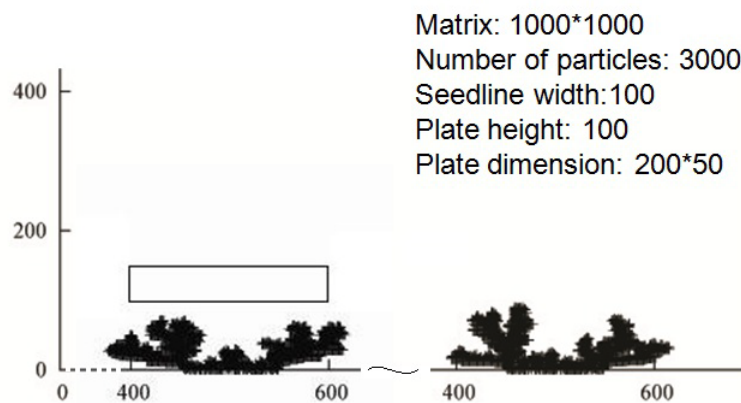


Figure5.24 Monte Carlo simulation of the effect of plate on Si strip aspect ratio

The width of the strip is defined from the middle of the seed line to the most right/left points, and the height is defined from the bottom to the highest point. Overall, the trend of mass transport is toward the seed line. The growth rate at the Si/SiO₂ interface is higher than that at the center of the seed line, because the large area of SiO₂ helps mass transport. The silicon starts to grow

laterally over the SiO₂ mask, and the gap at the center of the seed line starts to form, as shown in figure 5.24, which corresponds to the gap between two strips shown in the SEM image of the silicon strip cross-section. The average aspect ratio is 2.41 for LDLPE strips and 1.90 for LPE strips. Although the model is greatly simplified and the dimensions are not to scale, the simulation results demonstrate the contribution of the plate on the strip aspect ratio, which is supported by the experimental results.

5.6 Discussion

When multiple seedline substrates are used for silicon LPE growth, two strips are formed along each seedline, one strip on each Si/SiO₂ interface, as shown in figure 5.1. On the central bar area which is six times wider than the seedline, the epitaxial layer has a non-smooth surface, with large grooves on its surface. In contrast, the silicon strips have very smooth surfaces which are (111) planes. These results reveal that 1) the Si/SiO₂ interface is the preferred nucleation site; 2) the growth rate on the seedline is higher than that on the large area; this is probably caused by the mass transport on the SiO₂ surface; 3) the epitaxial lateral overgrowth can eliminate the defect caused by the large misorientation of the substrate.

5.6.1 Cooling Rate and Supersaturation

There are many parameters which can effectively affect the crystal quality and geometries of the silicon strips grown by LPE and LDLPE. For example, although a smaller cooling rate is adopted for LDLPE than that for LPE growth, the LDLPE strips is of less quality than LPE strips, since large terraces are formed on the surface and vacancies are formed in the strips. This is probably caused by the un-released large supersaturation which is a result of insufficient available nucleation area. When silicon is epitaxially grown using conventional LPE on an area which is much larger than the seedline, using a small cooling rate of 0.25°C, an epitaxial layer with smooth surface can be obtained, for example, the 3.2mm² round epitaxial layer grown by LPE for the Hall Effect measurement, shown in figure 5.15.

5.6.2 Growth Temperature

As introduced in section 3.2.3 and section 5.4.1, the growth temperature determines the indium concentration in the epitaxial silicon and thus the semiconductor properties, and a higher growth temperature normally results in a higher growth rate. Also, the growth temperature has a strong effect on surface morphology. It has been reported that for silicon epitaxial growth on (111) sc-Si substrate from the Au-Bi alloy solvent, when the substrate has a few degree misorientation, a growth temperature from 900°C to 800°C can result in an epitaxial layer with hollow structures in a size of ~20µm on its surface. In addition,

the lower growth temperature from 700°C to 600°C, can result in much larger structural defects on the epitaxial layer, for example, grooves with several hundred microns length and 20µm depth[167]. This suggests that a higher initial growth temperature results in less surface structure defects than a lower initial growth temperature.

For a certain initial growth temperature, we find that a higher terminating growth temperature also results in less surface structure defects than a lower terminating growth temperature.

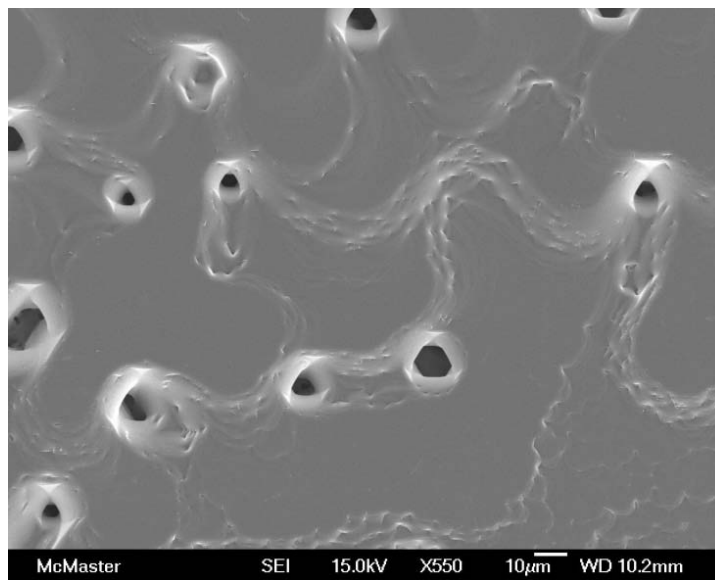


Figure 5.25 SEM image of epitaxial layer grown on the central bar area of the multiple seedline substrate (4° misorientation), growth temperature 950-910°C

As shown in figure 5.25, when the growth is started at 950°C and terminated at 910°C, hollow structures, like holes, are formed on the surface of the epitaxial layer, with diameters from 10 to 20µm. When the growth is started at

950°C and terminated at 850°C, grooves with several hundred microns length are formed on the surface of epitaxial layer, as shown in figure 5.26. The formation of these macroscopic steps can be referred to as a step-bunching growth mode, which is introduced by the large misorientation of the substrate (referring to section 3.3.3).

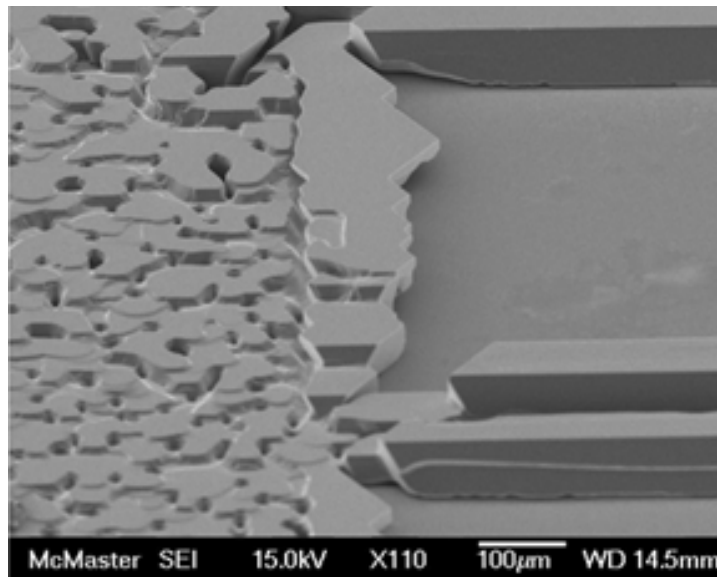


Figure 5.26 SEM image of epitaxial layer grown on the central bar area of the multiple seedline substrate (4° misorientation), growth temperature 950-850°C

Fortunately, the growth temperature dependent structure defects are not observed on silicon strips. The reason probably is that there is no misorientation along the direction of the seedline. Silicon strips are actually the ELO layers which only have small area attached to the substrate, and the growth of the ELO layer follows the Frank-Van Der Merwe growth mode (referring to section 3.3.3).

With the seedline setup shown in section 4.3.3, LDLPE strip growth is less affected by the misorientation of the substrate. Therefore, the growth rate and the temperature dependent doping level are most important considerations for choosing the growth temperature, and a compromise is needed for good electrical properties and reasonable growth rate.

5.6.3 Substrate Wetting Problems

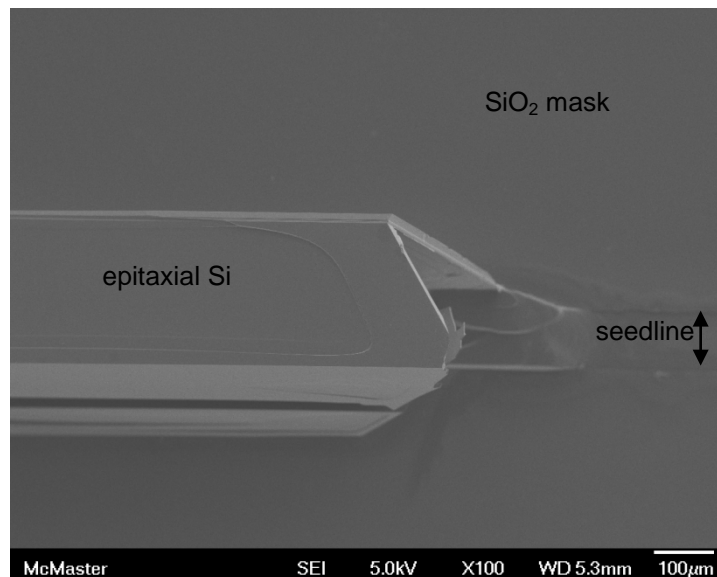


Figure 5.27 SEM image of LDLPE Si strip growth failure due to poor wetting

The wetting of indium melt to the seedline is essential for a successful LDLPE silicon strip growth. Poor wetting will lead to a failure of growth, as shown in figure 5.27. The space between the seedline and the plate is not fully filled by indium melt during the growth, and only a small part of the seedline is partially

wetted by the indium melt. Therefore, strips about 1mm long, with hollow structure, are grown and there is no epitaxial growth on most of the seedline.

5.6.4 Substrate Misorientation

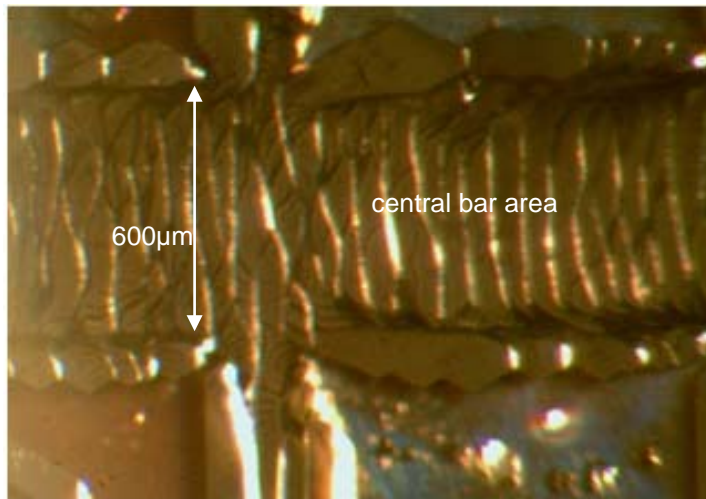


Figure 5.28 Optical microscope image of the epitaxial Si layer grown on (111) substrate with 4° misorientation

A small substrate misorientation can provide micro-steps which can enhance the nucleation as the nucleation sites. However, a large misorientation of the (111) substrate usually leads to an epitaxial layer with surface structure defects, like macro-steps. As shown in figure 5.28, the substrate has 4 degree misorientation about the direction of the seedline which is perpendicular to the central bar. The epitaxial layer grown on the 600 μm wide central bar area has a non-smooth surface with macro-steps, which can be observed by a 30x optical microscope.

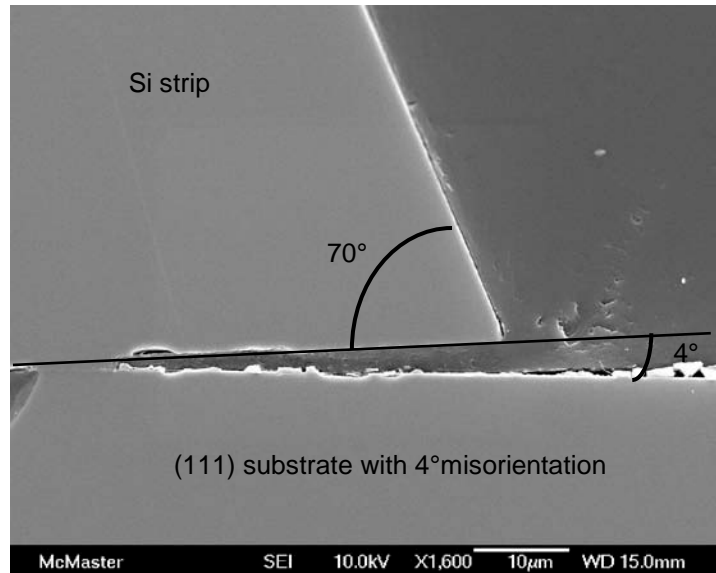


Figure 5.29 SEM image of cross-section of the bottom right corner of the silicon strip grown on (111) substrate with 4° misorientation

However, the surface morphology is not affected by the misorientation of the substrate. Each facet of the strip prefers to be the (111) plane with smooth surface. Figure 5.29 shows the cross-section of bottom right corner of the silicon strip grown on (111) substrate with 4 degree misorientation. The bottom facet has a 4 degree angle with the substrate surface, which is the same as the misorientation of the substrate, indicating that the bottom facet of the strip is the true (111) plane. The side facet of the strip has approximately a 70 degree angle with the bottom facet. For silicon crystal structure, the angles between (111) planes is $70^{\circ} 32'$ which is very close to the observed angle.

The surface of the strips naturally prefers to be a (111) plane, because the (111) plane has the largest density of atoms and the least surface energy. Therefore, the surface morphologies of the silicon strips grown by LPE and

LDLPE are not affected by the misorientation. Furthermore, the angle between the strip and the substrate with misorientation provide convenience for the strip separation process, since the (111) plane is the cleavage plane of crystalline silicon. When a mechanical force is applied to the strip, the silicon breaks along the (111) bottom facet into the substrate, keeping the integrity of the silicon strip.

5.6.5 Growth Failures

Poor substrate wetting is one of the most important reasons for LDLPE growth failures. However, when the seedline is well wetted by the indium melt, many other reasons could also cause growth failures.

Temperature fluctuation or large supersaturation can cause spontaneous nucleation of silicon in the melt and forming silicon flakes and needles. The large supersaturation causes a big free energy change ΔG . When the free energy change exceeds the critical value ΔG^* , stable nuclei which has a critical size r^* will form in the melt and then grows bigger. The spontaneous nucleation in the melt will consume and even deplete the silicon dissolved in the melt therefore cause a growth failure. Figure 5.30 shows the silicon flakes found in the melt after an LDLPE growth cycle.

Defects on the SiO_2 mask can cause silicon nucleation and deposition on the masked area, shown in figure 5.31. These defects on the SiO_2 surface such as scratches will provide nucleation sites, especially when the supersaturation is

large. This unexpected growth will consume the silicon which is available for the LDLPE growth and therefore causing a growth failure.

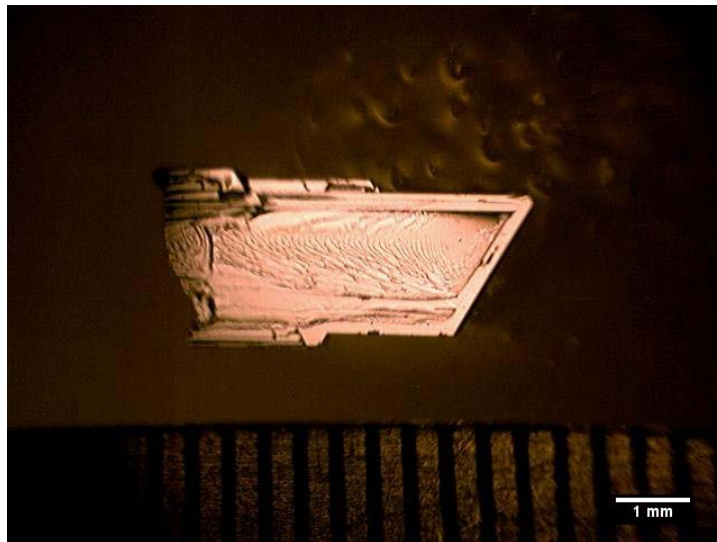


Figure5.30 Silicon flakes and needles in the melt

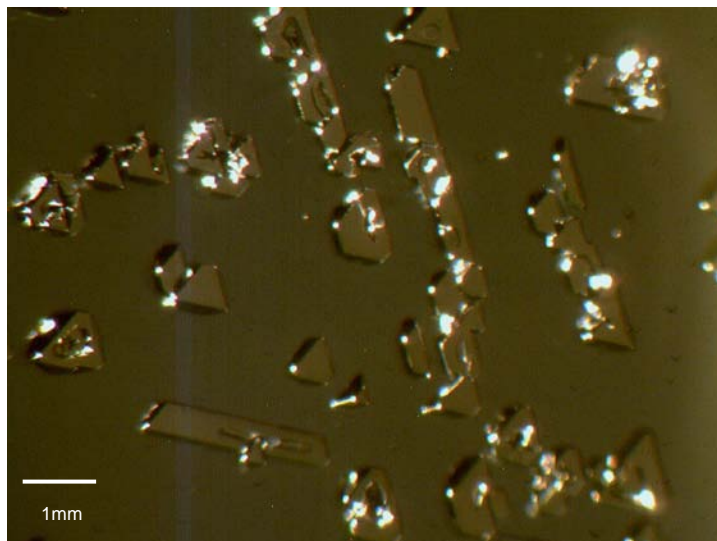


Figure5.31 Nucleation on the surface of SiO₂ mask

5.6.6 Half Growth Cycle Result

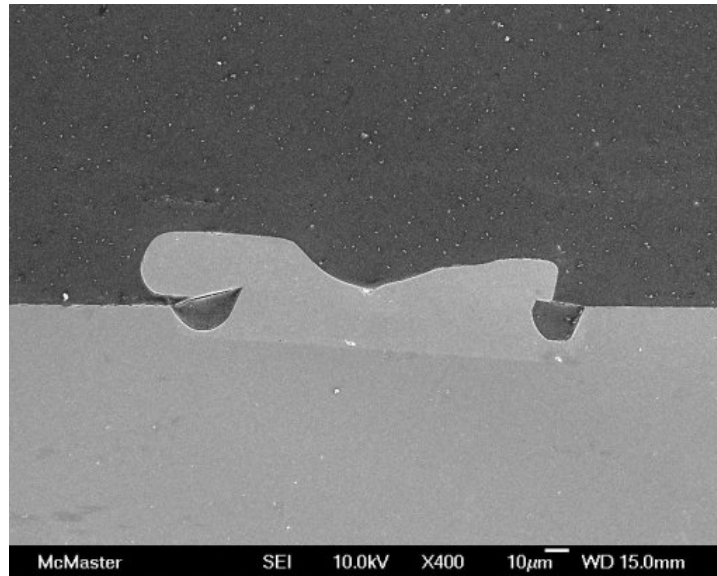


Figure 5.32 SEM image of cross section of half growth cycle LDLPE strips

A lack of in-situ and real-time monitoring and characterizing method is a disadvantage of LPE technology and makes it difficult to investigate the growth process of the LDLPE silicon strips. To look into the intermediate status of the silicon strip during an LDLPE growth cycle, the LDLPE growth was terminated at 910°C rather than 850°C. The cross-section of the LDLPE silicon strip is shown in the figure 5.32. Comparing with LDLPE silicon strips grown from 950°C - 850°C, the half growth cycle silicon strip has not only smaller width (~70µm) and thickness(~25µm), but also curved surface and round corners, indicating the (111) surface is not formed yet at 910°C. But the aspect ratio is about 2.8, similar to the maximum value of the aspect ratio of full growth cycle strips (1.7-2.8).

Chapter 6. Conclusion and Future Work

6.1 Conclusion

Lateral diffusion liquid phase epitaxy technology is invented for direct growth of single crystal substrate, eliminating the cutting, grinding and polishing processes which take a large part of the cost of traditional semiconductor wafers made by CZ or floating zone technology. Silicon, the most widely used semiconductor material, is used for pioneering LDLPE technology. A graphite boat with two sliders and graphite frames is designed to demonstrate the feasibility of growing single crystal substrate by using LDLPE technology. Although the single crystal grown by LDLPE is of small size that is not practical for industrial application, the mechanism of the LDLPE is proved potentially applicable.

The silicon strips grown by LPE and LDLPE technologies are different in their geometries. Both the experiments and simulation results demonstrate that the silicon strip aspect ratio is able to be increased by using a plate sitting over the seedline. The lateral overgrowth is promoted and the growth in thickness is limited. Therefore the silicon strip aspect ratio is increase from 1.2 for LPE to over 2 for LDLPE. The thickness of the LDLPE strip is around 100 μm , which should provide enough mechanical strength for separating the strip from the substrate and further device processing. Also, 100 μm is an ideal thickness for crystalline Si solar cells to absorb sunlight efficiently.

The silicon strip grown by LDLPE is proved an epitaxial layer which is (111) orientated as is the substrate by the XRD 2-theta scan. The quality of the single crystal is indicated by the XRD rocking curve which has a full width at half maximum (FWHM) of 0.03°.

Silicon grown from indium melt is naturally doped by indium, resulting in p-type doping. The doping level is mainly dependent on the growth temperature, because of the temperature-dependent indium solubility in solid silicon. At the growth temperature from 920°C to 1050°C, the concentration of indium in the silicon ranges from $10^{16}/\text{cm}^3$ to $1.6 \times 10^{18}/\text{cm}^3$ [111, 120]. The LDLPE silicon has a minority carrier lifetime of 24.4 μs measured by the photoconductive decay measurement. The measured electrical properties satisfy the requirement for photovoltaic application. The growth temperature is of the most important parameter for successful LDLPE growth. A compromise among the doping level, growth rate and nucleation quality is needed. Also, the growth is greatly affected by the cooling rate and the supersaturation. We believe that the single seedline substrate is not able to provide enough growth area for accommodating the large supersaturation and as a result we obtain non-uniform growth and non-smooth surfaces of the silicon strips. The substrate mis-orientation is not critical for the LDLPE silicon strip growth. A small misorientation could result in an angle between the silicon strip and substrate and provides convenience during the separation process.

Overall, at the current stage, single crystalline (111) orientated silicon strips can be grown by using the LDLPE technology. In spite of the fact that the silicon strips are too small for realistic application, the mechanism of the LDLPE is proved feasible for direct growth of single crystal substrate, and the silicon grown from indium melt is proved having good crystal quality and electrical properties for photovoltaic applications.

6.2 Future Work

Currently, LDLPE is an immature technology which is at the very early stage, compared to current industrial semiconductor wafer production and thin film growth technologies. This thesis has described the concept and mechanism of LDLPE and experiments have proved that LDLPE technology is feasible in principle. For practical applications, LDLPE should produce large wafers with consistent good quality and at a low cost for the single wafer.

First of all, important parameters, such growth temperature, cooling rate and substrate mis-orientation, should be optimized to achieve good nucleation and crystal morphology. Considering the electrical properties of the silicon grown from indium melt, the growth temperature should be not higher than 950°C. The large cooling rate leads to large growth rate, but it should be optimized to avoid an overly large supersaturation that may result in non-uniform growth and non-smooth crystal surface. Although the misorientation is less important, it should be

carefully chosen, so that the mis-orientated surface provides micro-steps as nucleation site and therefore increases the growth rate at beginning of the growth.

Secondly, the graphite boat set up should be optimized as the same time as the growth parameter optimization. The geometry of the plate on the top of the seedline determines the lateral diffusion distance for silicon atoms in the bulk indium melt to diffuse to the seedline, therefore determining the growth rate. The space between the plate and seedline limits the thickness of the silicon strips. A small space leads to a thin strip, but decreases the growth rate and may cause the failure of wetting.

Last but not least, an apparatus should be built up for continuous growth and scaling up. A plan is proposed in section 6.3. A large chamber will be needed for sophisticated graphite parts and movement control units. The temperature gradient and continuous growth set up make it possible to grow substrates in large size for practical device fabrication and the stack structure of the seed holder can increase the output of a single furnace.

In principle, LDLPE can grow a variety of semiconductors layer laterally and continuously, making wafers of large size. Examples of other semiconductors include GaAs or other group III-V semiconductors as well as the group IV semiconductor germanium. In some cases, larger compound semiconductor wafers (bigger than 4 inches) are very expensive or not available because it is difficult to make large single crystalline ingots for these semiconductors.

Therefore LDLPE may offer a means to increase wafer size as well as lowering cost for these expensive materials.

6.3 LDLPE Scale-up Concept

A LDLPE scaling up and continuous growth plan is proposed, so that the growth of silicon substrate with practical size at a practical growth rate might be achieved in a future production process. A stack LDLPE method in continuous growth mode for scaling up is proposed, shown in figure 6.1.

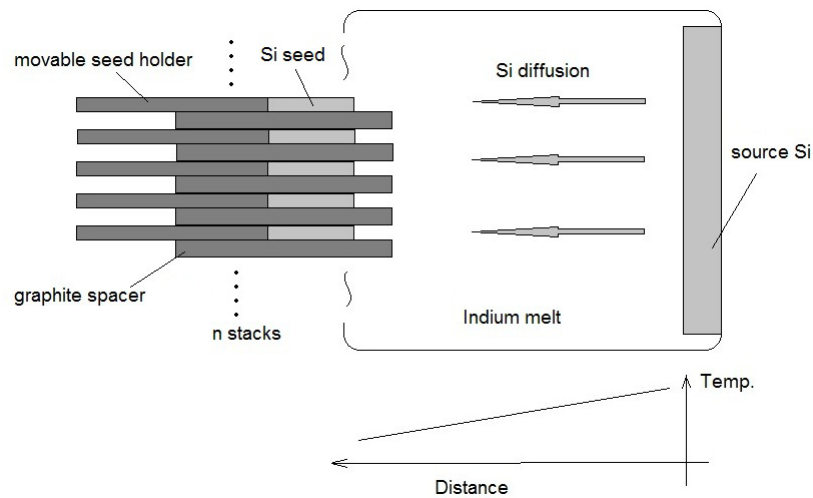


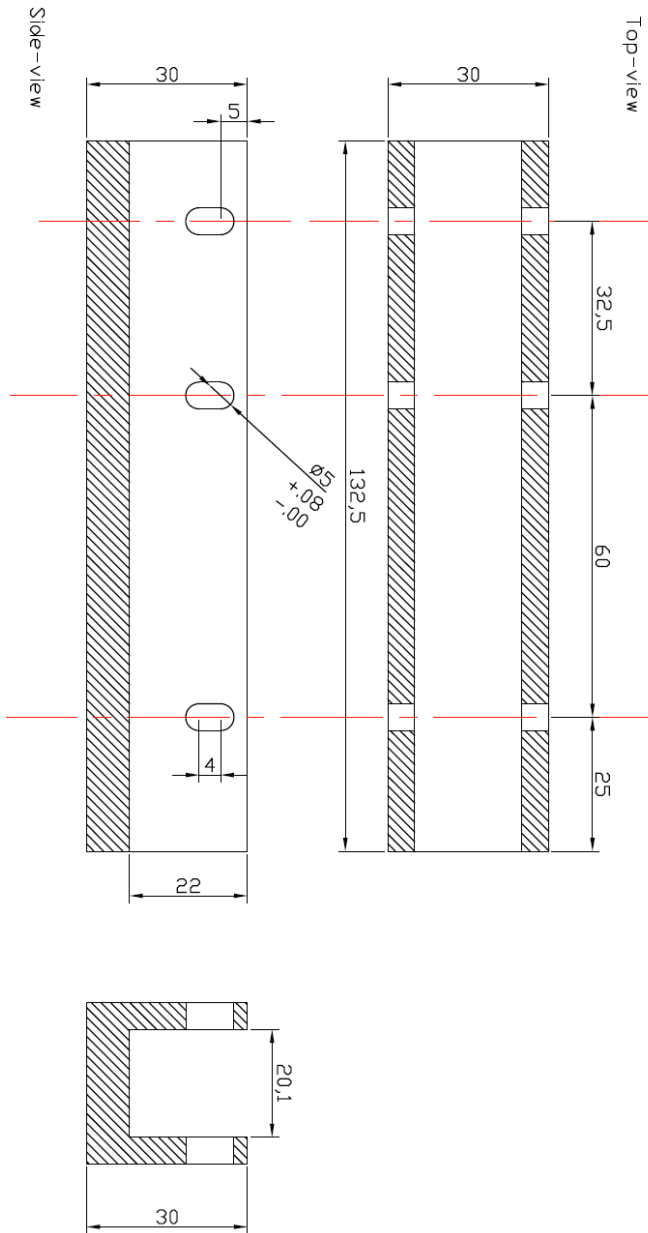
Figure6.1 Proposed LDLPE process for mass production

Single crystalline silicon seeds are held by movable seed holders and they are stacked up with graphite spacers between each other. These stacked silicon seeds are immersed into indium melt which has source silicon on another side. There is a temperature gradient between source Si and seeds. Source silicon is dissolved and silicon atoms diffuse from the source silicon side to the seeds side.

Therefore, silicon is epitaxially grown on the seeds laterally and continuously. Meanwhile, the seed holder could pull the seed at the same rate as the growth, until the LDLPE silicon grows to the desired size. A large growth area which is comparable to thin film deposition could be achieved by increasing the number of stacks. And thanks to the continuous growth mode, the pump-down, heating and stabilization time becomes a minor part of the total time of unit area Si wafer growth.

Appendix I: Drawing of LDLPE Graphite Boat

(Note: All dimensions in millimeter)

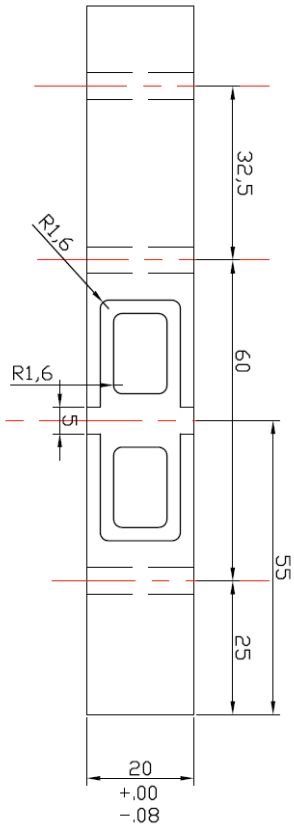


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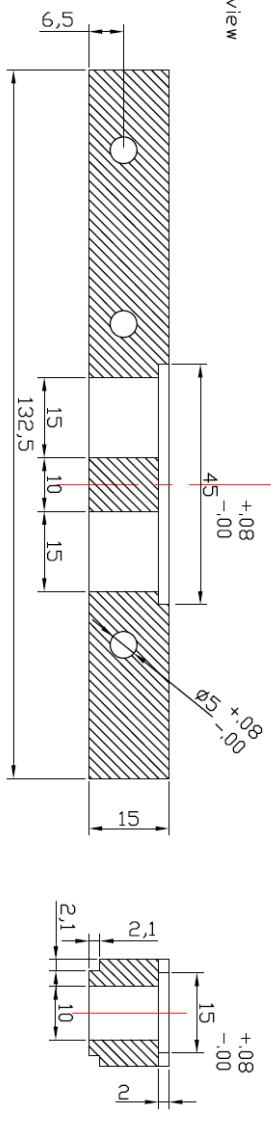
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McMaster

Top-view



Side-view

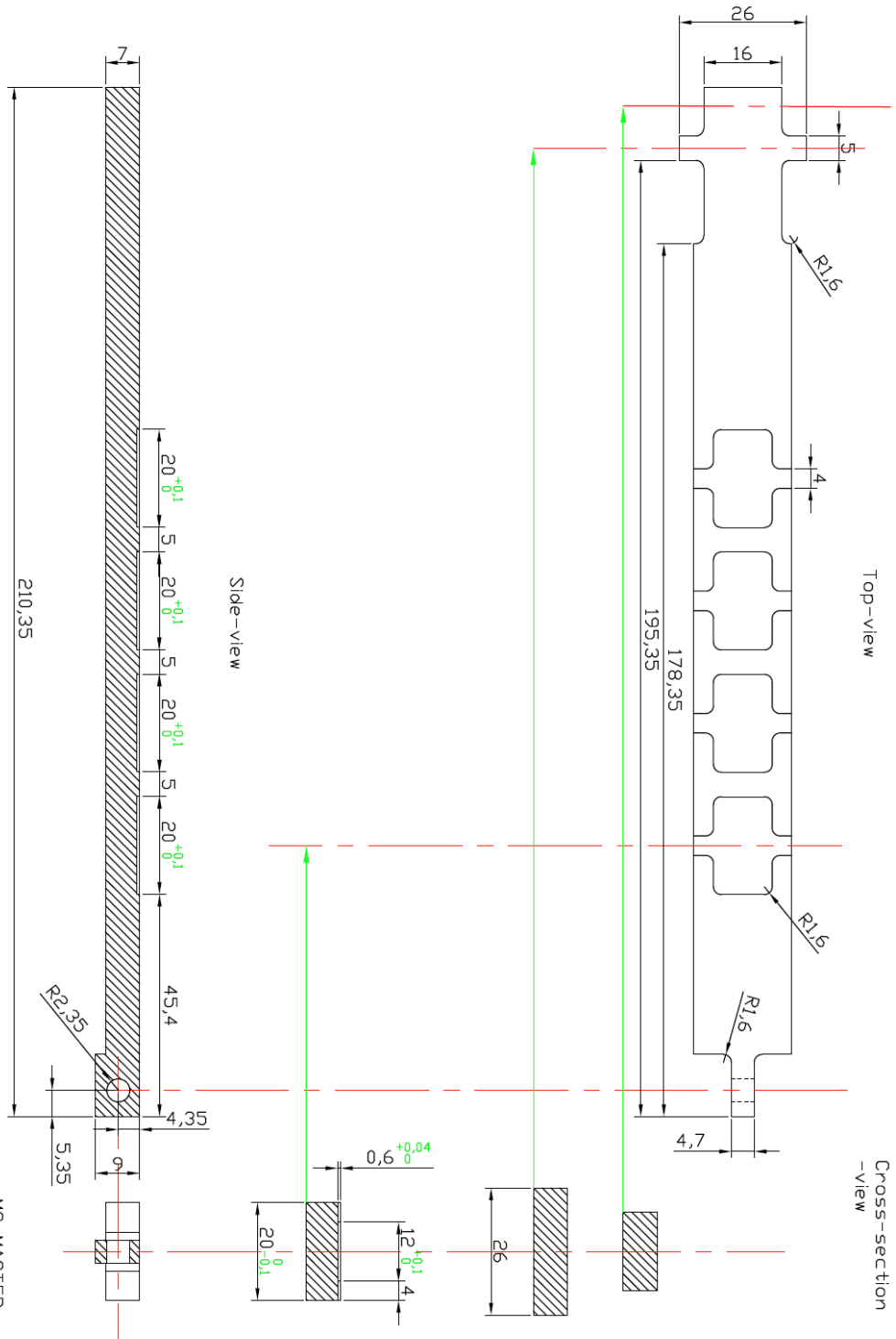


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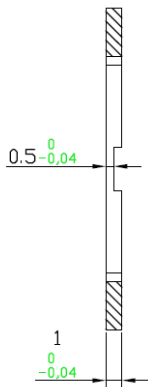
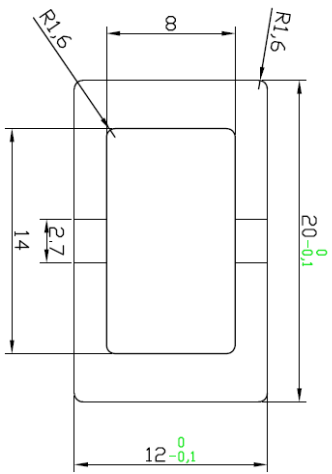
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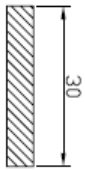
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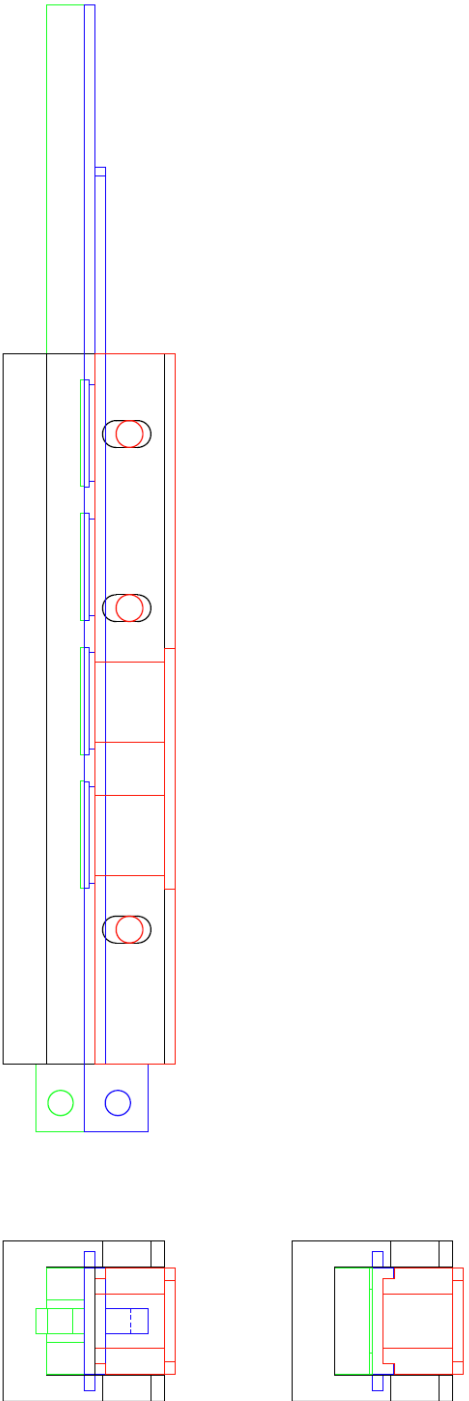


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TOLERANCES UNLESS SPECIFIED +/- .08	MATERIAL	CAP AND ROD
	DRAWN BY Bo Li	SK-08-11-08-1

MC MASTER

Graphite parts Assembling



MCMaster

TOLERANCES UNLESS SPECIFIED	MATERIAL	Assembling
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Appendix II: Code for Random Walk Modeling and Monte Carlo

Simulation

The following code is for simulating the random walk model. The code for printing out the result is also attached. All other code for functioning the code in PC is not attached.

```
/******  
  
FILE NAME: sim_engine.c  
  
PROJECT: silicon_sim  
  
ABSTRACT: Functions for creating and deleting the internal data structure  
          built by the parser.  
  
*****/  
  
#include "header.h"  
  
pthread_mutex_t mutex1 = PTHREAD_MUTEX_INITIALIZER;  
pthread_mutex_t mutex2 = PTHREAD_MUTEX_INITIALIZER;  
pthread_mutex_t mutex3 = PTHREAD_MUTEX_INITIALIZER;  
int result;  
  
int f_check_collision(int , int );  
void *f_simulate_thread(void *);  
int f_simulate_atom(int , int );
```

```
/******
```

FUNCTION: F_StartSimulation

ABSTRACT: Function for starting the simulation

RETURNS: None

```
*****/
```

```
void F_StartSimulation() {
    int cur_trial;
    time_t seed_time;
    int i;

    pthread_t tid[MAX_THREAD];

    F_Printf("Starting simulation...\n");

    if (Seed == -1) {
        time(&seed_time);
        srand(seed_time);
    } else {
        srand(Seed);
    }

    for (cur_trial = 0; cur_trial < NumTrials;) {
        result = 0;
        for (i = 0; i < NumThreads; i++) {
            #if SIMDEBUG == 1
                printf("Simulating atom # %d/%d at using
thread %d...\n", cur_trial+1, NumTrials, i);
            #endif
            if (pthread_create(&tid[i], NULL, f_simulate_thread, NULL)) {
                printf("Thread %d create failed!!\n", i);
            }
        }

        // Wait till all threads are done
        for (i = 0; i < NumThreads; i++) {
            pthread_join(tid[i], NULL);
        }

        #if SIMDEBUG == 0
            fprintf(stderr, "\r");
        #endif
    }
}
```

```

        fflush(stderr);
        printf("Simulating atoms # %d-%d/%d...", cur_trial+1,
cur_trial+NumThreads, NumTrials);
        fflush(stdout);
    #endif

    if (result > 1) printf("haha: %d\n", result);

    if (Disappear == 1) cur_trial += NumThreads;
    else
        cur_trial += result;
}

F_Printf("\n");
F_Printf("Done\n\n");
}

void *f_simulate_thread(void *msg) {
    int cur_x_pos, cur_y_pos;
    int thread_result;

    // random starting x position
    pthread_mutex_lock( &mutex3 );

    // cur_x_pos = rand()/(int)(((unsigned)RAND_MAX + 1) / SubstractWidth);
    // cur_y_pos = 0;

    // x is either the left or right side of object
    if ((rand()/((double)RAND_MAX + 1)) < 0.5) cur_x_pos = ObjectTopLeftX;
    else cur_x_pos = ObjectBottomRightX;

    // y is between bottom of object and boundary height
    cur_y_pos = ObjectBottomRightY + rand()/(int)(((unsigned)RAND_MAX +
1) / (BoundaryHeight - OxideThickness - ObjectBottomRightY));

    pthread_mutex_unlock( &mutex3 );

    #if SIMDEBUG == 2
        F_Printf("Simulating atom from (%d, %d) using thread %ld\n",
cur_x_pos, cur_y_pos, pthread_self());
    #endif

    thread_result = f_simulate_atom(cur_x_pos, cur_y_pos);
}

```

```

pthread_mutex_lock( &mutex2 );
if (thread_result == 1) result++;
pthread_mutex_unlock( &mutex2 );

    #if SIMDEBUG == 2
//        if (thread_result == 1)
            F_Printf("Thread %ld finished with return value %d (%d)\n",
pthread_self(), thread_result, result);
        #endif
    }

int f_simulate_atom(int cur_x_pos, int cur_y_pos) {
    int x_direction;
    int y_direction;
    int stick;
    int number_collide_surface;
    atom_struct *cur_atom;
    int result;
    float move_probability;
    float zeta;

    do {
        stick = 0;
        number_collide_surface = 0;

        // check how many atoms are in its neighboring position
        // right side is an atom
        if (f_check_collision(cur_x_pos+1, cur_y_pos) == 1)
number_collide_surface++;
        // left side is an atom
        if (f_check_collision(cur_x_pos-1, cur_y_pos) == 1)
number_collide_surface++;
        // bottom side is an atom
        if (f_check_collision(cur_x_pos, cur_y_pos+1) == 1)
number_collide_surface++;
        // bottom side is silicon
        if (f_check_collision(cur_x_pos, cur_y_pos+1) == 3)
number_collide_surface++;

        pthread_mutex_lock( &mutex3 );
        move_probability = rand()/((double)RAND_MAX + 1);
        pthread_mutex_unlock( &mutex3 );

        x_direction = 0;

```

```

y_direction = 0;

if (move_probability <= 0.25) {
    // move right
    x_direction = 1;

    if (cur_x_pos + 1 > SubstractWidth) {
        // out of right boundary

        #if SIMDEBUG == 1
            printf("Out of right boundary: %d\n", cur_x_pos);
        #endif

        return 0;
    }
} else {
    if (move_probability <= 0.5) {
        x_direction = -1;
        if (cur_x_pos - 1 < 0) {
            // out of left boundary
            #if SIMDEBUG == 1
                printf("Out of left boundary: %d\n",
cur_x_pos);
            #endif

            return 0;
        }
    } else {
        if (move_probability <= 0.75) {
            // moving down
            if (cur_y_pos < BoundaryHeight)
                y_direction = 1;
        } else {
            // moving up
            y_direction = -1;
            if (cur_y_pos - 1 < 0) {
                // out of top boundary
                #if SIMDEBUG == 1
                    printf("Out of top boundary: %d\n",
cur_y_pos);
                #endif

                return 0;
            }
        }
    }
}

```

```

    }
}

result = f_check_collision(cur_x_pos + x_direction, cur_y_pos +
y_direction);
if (result == 1 || result == 3) {
    // collision on movement, so see if it should stick
    #if SIMDEBUG == 1
        printf("Number of collide surface: %d\n",
number_collide_surface);
    #endif
    pthread_mutex_lock( &mutex3 );
    zeta = rand()/((double)RAND_MAX + 1);
    pthread_mutex_unlock( &mutex3 );

    switch(number_collide_surface) {
        case 1: if (zeta > Zeta1) stick = 1; break;
        case 2: if (zeta > Zeta2) stick = 1; break;
        case 3: stick = 1; break;
    }

    x_direction = 0;
    y_direction = 0;

    #if SIMDEBUG == 1
        printf("Collision result (%d, %d): type: %d, stick: %d\n",
cur_x_pos, cur_y_pos, result, stick);
    #endif
} else {
    if (result == 2) {
        #if SIMDEBUG == 1
            printf("Collision with oxide\n");
        #endif
        x_direction = 0;
        y_direction = 0;

        // for disappearing after contacting oxide
        // return 0;
    } else {
        if (result == 4) {
            #if SIMDEBUG == 1
                printf("Collision with object\n");
            #endif
            x_direction = 0;

```



```

        y_direction = 0;

        // for disappearing after contacting object
        // return 0;
    }
}

if (stick == 1) {
    #if SIMDEBUG == 1
        printf("Atom stick at (%d, %d)\n", cur_x_pos,
cur_y_pos);
    #endif
    cur_atom = F_NewAtom(cur_x_pos, cur_y_pos);

    pthread_mutex_lock( &mutex1 );
    l_append(AtomList, cur_atom);
    pthread_mutex_unlock( &mutex1 );
}

cur_x_pos += x_direction;
cur_y_pos += y_direction;

// #if SIMDEBUG == 1
//     printf("Atom move to (%d, %d)\n", cur_x_pos, cur_y_pos);
// #endif

} while(stick == 0);

return 1;
}

int f_check_collision(int cur_x_pos, int cur_y_pos) {
    atom_struct *cur_atom;

    // check if collision is with oxide
    if (cur_y_pos >= BoundaryHeight-OxideThickness) {
        if ((cur_x_pos <= (SubstractWidth/2 - SubstractGap/2)) // collide
with left oxide
            || (cur_x_pos >= (SubstractWidth/2 + SubstractGap/2)) //
collide with right oxide
        ) return 2;
    }
}

```

```

// check if collision with the object
if (cur_y_pos >= ObjectTopLeftY && cur_y_pos <= ObjectBottomRightY) {
    if (cur_x_pos >= ObjectTopLeftX && cur_x_pos <=
ObjectBottomRightX) {
        return 4;
    }
}

// check if collision is with silicon substract
if (cur_y_pos >= BoundaryHeight) return 3;

// check if collision is with other atoms
l_foreach(AtomList, cur_atom) {
    if ((cur_atom->x == cur_x_pos)
        && (cur_atom->y == cur_y_pos))
        return 1;
} l_endfor;

return 0;
}

```

List of Publications

Filed Patent Applications

- US provisional patent application: Lateral diffusion liquid phase epitaxy technology: a method to grow single crystalline semiconductor substrate/wafer, Ser. No. 61/487,005, filed May 17, 2011, A. H. Kitai, B. Li
- PCT patent application: Semiconductor formation by lateral diffusion liquid phase epitaxy, Application No. PCT/CA2012/050327, filed: May 17, 2012, A. H. Kitai, B. Li, H. L. Yu

Journal Papers and Proceedings

- B. Li, A. H. Kitai, Mono-crystalline Silicon Strips Grown by Liquid Phase Epitaxy for Photovoltaic Applications, Proc. SPIE 7750, 77502N (2010)
- B. Li, H. L. Yu, H. Shen and A. H. Kitai, Single Crystalline Si Substrate Growth by Lateral Diffusion Epitaxy, Journal of Crystal Growth (submitted, June 2012)
- H. L. Yu, B. Li, H. Shen and A. H. Kitai, Lateral Diffusion Epitaxy of Single Crystal Silicon Platelets from Silicon-indium Melt, Journal of Crystal Growth (for submission in July 2012)

Refereed Conference Presentations

- B. Li, and A.H. Kitai, Presentation: LDLPE Growth of Self Supported Single Crystalline Si Strips for Photovoltaic Applications, Photonics North 2011, Ottawa, June 2nd, 2011
- B. Li, H. Shen and A.H. Kitai, Presentation: Single Crystalline Si Substrate Growth by Lateral Diffusion LPE Technology for PV Applications, Electronic Materials Conference 2011, Santa Barbara; June 22nd, 2011
- H. L. Yu, B. Li, H. Shen and A. H. Kitai, Poster: Lateral Diffusion Epitaxial Growth of Single Crystal Silicon Platelets from Silicon-indium Melt, Photonics North 2012, Montreal, Canada, June 6-8, 2012,
- H. L. Yu, B. Li, H. Shen, and A. H. Kitai, Poster: Lateral Diffusion Epitaxial Growth of Single Crystal Silicon Platelets from Silicon-indium Melt, Electronic Materials Conference 2012, State College, PA, USA; June 20-22, 2012

Reference

1. Burgelman, M., *Cadmium Telluride Thin Film Solar Cells: Characterization, Fabrication and Modeling*, in *Thin Film Solar Cells: Fabrication, Characterization and Applications*, J. Poortmans and V. Arkhipov, Editors. 2006, John Wiley & Sons Ltd. p. 279/502.
2. Lincot, D., *Summary Report Environmental, Health, and Safety (EHS) Aspects of First Solar Cadmium Telluride (CdTe) Photovoltaic (PV) Systems*. 2009, French Ministry of Ecology, Energy, Sustainable Development. p. 3.
3. Meyers, P.V., *First Solar Polycrystalline CdTe Thin Film PV in 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion*. 2006: Waikoloa, HI. p. 2024-2027.
4. Hajimammadov, R., et al., *Effect of "CdCl₂ Treatment" on Properties of CdTe-Based Solar Cells Prepared by Physical Vapor Deposition and Close-Spaced Sublimation Methods* Japanese Journal of Applied Physics, 2011. **50**(5): p. 05FH01-05FH02.
5. Mahathongdy, Y., C.A. Wolden, and R.M. Baldwin. *Vapor CdCl₂ - Optimization and Screening Experiment for an All Dry Chloride Treatment of CdS-CdTe Solar Cells*. in *National Center for Photovoltaic 15th Program Review Meeting*. 1998. Denver, Colorado.
6. Moutinho, H.R., et al. *Studies of Recrystallization of CdTe Thin Films After CdCl₂ Treatment*. in *26th IEEE Photovoltaic Specialists conference*, . 1997. Anaheim, CA.
7. Antec Solar GmbH, G.; Available from: www.antec-solar.de.
8. Bonnet, D., *Manufacturing of CSS CdTe Solar Cells*. Thin Solid Films, 2000. **361-362**: p. 547-552.
9. Ferekides, C.S., et al., *High Efficiency CSS CdTe Solar Cells*. Thin Solid Films, 2000. **361-362**: p. 520-526.
10. First Solar Ltd., U.; Available from: www.firstsolar.com.
11. Kestner, J.M., S. McElvain, and C.A. Wolden, *Vapor Transport Deposition and Characterization of Polycrystalline CdTe Solar Absorbers*, in *MRS Proceedings*. 2003. p. B5.22.
12. Romeo, N., A. Bosio, and V. Canevari, *Recent progress on CdTe/CdS thin film solar cells*. Solar Energy, 2004. **77**(6): p. 795-801.
13. Hanket, G.M., et al., *Design of a Vapor Transport Deposition Process for Thin Film Materials*. Journal of Vacuum Science & Technology A: Vacuum, Surface and Films, 2006. **24**(5): p. 1695-1701.
14. Klenk, R. and M.C. Lux-Steiner, *Chalcopyrite Based Solar Cells*, in *Thin Film Solar Cells: Fabrication, Characterization and Applications*, J. Poortmans and V. Arkhipov, Editors. 2006, John Wiley & Sons Ltd. p. 240/502.
15. Jackson, P. and D. Hariskos, *New world record efficiency for Cu(In,Ga)Se₂ thin-film solar cells beyond 20%*. Progress in Photovoltaic Research and Applications, 2011. **19**(7): p. 894-897.

16. Copper Indium Gallium Selenide Solar Cells, W.; Available from: http://en.wikipedia.org/wiki/Copper_indium_gallium_selenide_solar_cells.
17. Shafarman, W.N. and L. Stolt, *Cu(InGa)Se₂ Solar Cells*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 569/1168.
18. Luck, I., et al., *Influence of Na on the properties of Cu-rich prepared CuInS₂ thin films and the performance of corresponding CuInS₂/CdS/ZnO solar cells*. *Solar Energy Materials and Solar Cells*, 2001. **67**(1-4): p. 151-158.
19. Ruckh, M., D. Schmid, and M. Kaiser, *Influence of substrates on the electrical properties of Cu(In,Ga)Se₂ thin films*. *Solar Energy Materials and Solar Cells*, 1996. **41-42**: p. 335-343.
20. Ascent Solar, U.; Available from: <http://www.ascentsolar.com/>.
21. Wurth Solar, G.; Available from: <http://www.wuerth-solar.com>.
22. Shafarman, W.N. and L. Stolt, *Cu(InGa)Se₂ Solar Cells*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 580/1168.
23. Kodigala, S.R., *Growth Process of I-III-VI₂ Thin Films*, in *Cu(In_{1-x}Ga_x)Se₂ Based Thin Film Solar Cells*. 2009, Academic Press.: London. p. 34/684.
24. Kapur, V.K., B.M. Basol, and E.S. Tseng, *Low cost method for the production of semiconductor films for CuInSe₂/CdS solar cells*. *Solar Cells*, 1987. **21**(1-4): p. 65-72.
25. Garcia, F.J. and M.S. Tomar, *A Screen Printed CdS/CuInSe₂ Solar Cell*. *Japanese Journal of Applied Physics*, 1983. **22 Supplement**: p. 535-538.
26. Basol, B. and V. Kapur, *Deposition of CuInSe₂ films by a two-stage process utilizing E-beam evaporation*. *IEEE Transactions on Electron Devices*, 1990. **37**(2): p. 418-421.
27. Solar Frontier Inc, J.; Available from: <http://www.solar-frontier.com>.
28. Avancis Inc, G.
29. Applied Materials, U. *Applied Materials Revolutionizes Solar Module Manufacturing with Breakthrough Thin Film Line*. 2007; Available from: www.appliedmaterials.com/newroom/new/applied-materials-revolutionizes-solar-manufacturing-breakthrough-sunfab-thin-f.
30. Deng, X. and E.A. Schiff, *Amorphous Silicon-based Solar Cells*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 521/1168.
31. Øvrelid, E.J., et al., *Introduction*, in *Crystal Growth of Si for Solar Cells*, K. Nakajima and N. Usami, Editors. 2009, Springer: Berlin Heidelberg. p. 4/255.
32. Ceccaroli, B. and O. Lohne, *Solar Grade Silicon Feedstock*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 168/1168.
33. Koch, W., et al., *Bulk Crystal Growth and Wafering for PV*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 208/1168.

34. Narayanan, M. and T. Ciszek, *Crystal Growth Technologies for Silicon Photovoltaics*, in *Handbook of Crystal Growth*, G. Dhanaraj, et al., Editors. 2010, Springer. p. 1705/1818.
35. Riemann, H. and A. Luedge, *Floating Zone Crystal Growth*, in *Crystal Growth of Si for Solar Cells*, K. Nakajima and N. Usami, Editors. 2009, Springer: Berlin Heidelberg. p. 54/255.
36. Green, M.A., *The path to 25% silicon solar cell efficiency: History of silicon cell evolution*. Progress in Photovoltaic Research and Applications, 2009. **17**(3): p. 183-189.
37. Koch, W., et al., *Ingot Fabrication*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 214/1168.
38. Koch, W., et al., *Ingot Fabrication*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 215/1168.
39. Kao, I., C. Chung, and R.M. Rodriguez, *Wafer Manufacturing and Slicing Using Wiresaw*, in *Handbook of Crystal Growth*, G. Dhanaraj, et al., Editors. 2010, Springer. p. 1728/1818.
40. Koch, W., et al., *Bulk Crystal Growth and Wafering for PV*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 224/1168.
41. Tobias, I., C.d. Canizo, and J. Alonso, *Crystalline Silicon Solar Cells and Modules*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 261/1168.
42. Koch, W., et al., *Bulk Crystal Growth and Wafering for PV*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 223/1168.
43. Hahn, G., A. Schonecker, and A. Gutjahr, *Description of Ribbon Growth Techniques*, in *Crystal Growth of Si for Solar Cells*, K. Nakajima and N. Usami, Editors. 2009, Springer: Berlin Heidelberg. p. 101/255.
44. W.Schmidt, B.woesten, and J.P. Kalejs, *Manufacturing Technology for Ribbon Silicon (EFG) Wafers and Solar Cells*. Progress in Photovoltaic Research and Applications, 2002. **10**(2): p. 129-140.
45. Kalejs, J.P., *Silicon riboons and foils - state of the art*. Solar Energy Materials and Solar Cells, 2002. **72**(1-4): p. 139-153.
46. I.Hanoka, J., *An overview of silicon ribbon growth technology*. Solar Energy Materials and Solar Cells, 2001. **65**(1-4): p. 231-237.
47. Bergmann, R.B., *Crystalline Si thin-film solar cells: a review*. Applied Physics A: Material Science & Processing, 1999. **69**(2): p. 187-194.
48. Catchpole, K.R., et al., *A review of thin-film crystalline silicon for solar cell applications. Part 2: Foreign substrates*. Solar Energy Materials and Solar Cells, 2001. **68**(2): p. 173-215.

49. McCann, M.J., et al., *A review of thin-film crystalline silicon for solar cell applications. Part I: Native substrates*. Solar Energy Materials and Solar Cells, 2001. **68**(2): p. 135-171.
50. Brendel, R., *Review of layer transfer processes for crystalline thin-film Si solar cells*. Japanese Journal of Applied Physics, 2001. **40**: p. 4431-4439.
51. Matsuyama, T., et al., *Improvement of n-type poly-Si film properties by solid phase crystallization*. Japanese Journal of Applied Physics, 1993. **32**(9R): p. 3720-2728.
52. Kluth, O., et al. *Texture etched Al-doped ZnO: a new material for enhanced light trapping in thin film solar cells*. in *26th IEEE Photovoltaic Specialists Conference*. 1997. New York.
53. Löffl, A., et al. *Al-doped ZnO films for thin-film solar cells with very low sheet resistance and controlled texture*. in *14th European Photovoltaic Solar Energy Conference*. 1997. Barcelona, Spain.
54. Wyrsh, N., et al. *Development of inverted micromorph solar cells*. in *2nd World Conference on Photovoltaic Solar Energy Conversion*. 1998. Vienna, Austria.
55. Baba, T., et al. *9.2% efficiency thin-film polycrystalline silicon solar cell by a novel solid phase crystallization method*. in *13th European Photovoltaic Solar Energy Conference*. 1995. Nice, France.
56. Matsuyama, T., et al., *Preparation of high-quality n-type poly-Si films by solid phase crystallization*. Japanese Journal of Applied Physics, 1990. **29**: p. 2327-2331.
57. Kroll, U., et al., *From amorphous to microcrystalline silicon films prepared by hydrogen dilution using VHF (70 MHz) GD technique*. Journal of Non-Crystalline Solids, 1998. **227-230, Part 1**: p. 68-72.
58. Schropp, R.E.I. and M. Zeman, *Amorphous and Microcrystalline Silicon Solar Cells: Modeling, Materials and Device Technology*. 1st ed. 1998, Boston. 232.
59. Tsai, C.C., et al., *Transition from Amorphous to Crystalline Si: Effect of Hydrogen on Film Growth*, in *MRS Proceedings*. 1988. p. 49-54.
60. Ray, S., et al., *Transition from Amorphous to Microcrystalline Si:H: Effecto of Substrate Temperature and Hydrogen Dilution*. Journal of Non-Crystalline Solids, 2002. **299-302, Part 2**: p. 761-766.
61. Matsuda, A., *Formation kinetics and control of microcrystallite in uc-Si:H from glow discharge plasma*,. Journal of Non-Crystalline Solids, 1983. **59-60, Part2**: p. 767-774.
62. Dutta, J., et al., *Dependence of intrinsic stress in hydrogenated amorphous silicon on excitation frequency in a plasma-enhanced chemical vapor deposition process*. Journal of Applied Physics, 1992. **72**(7): p. 3220-3222.
63. Wyrsh, N., et al., *Hydrogenated microcrystalline silicon for photovoltaic applications*. Solid State Phenomena, 1999. **67-68**: p. 89-100.
64. Yamamoto, K., et al., *Thin-film poly-Si solar cells on glass substrates fabricated at low temperature*. Applied Physics A: Material Science & Processing, 1999. **69**(2): p. 179-185.

65. Meier, J., et al. *Microcrystalline and micromorph thin-film silicon solar cells*. in *2nd World Conference on Photovoltaic Solar Energy Conversion*. 1998. Vienna, Austria.
66. Slaoui, A., et al., *Polycrystalline silicon solar cells on mullite substrate*. *Solar Energy Materials and Solar Cells*, 2002. **71**(2): p. 245-252.
67. Eyer, A., et al., *Crystalline silicon thin film (CSiTF) solar cells on SSP and on ceramic substrate*. *Journal of Crystal Growth*, 2001. **225**(2-4): p. 340-347.
68. Kunz, T., et al. *Crystalline silicon thin-film solar cells on graphite or SiC-ceramic substrate*. in *23rd European Photovoltaic Solar Energy Conference*. 2008. Valencia, Spain.
69. I.Gordon, S. Vallon, and A. Mayolet. *Thin-film monocrystalline-silicon solar cells on transparent high-temperature glass-ceramic substrate*. in *34th IEEE Photovoltaic Specialists Conference*. 2009. Philadelphia, PA.
70. Slaoui, A., et al. *Silicon films on ceramic substrates (SOCS): growth and solar cells*. in *3rd World Conference on Photovoltaic Energy Conversion*. 2003. Osaka, Japan.
71. Bourdais, S., et al. *Poly crystalline silicon thin films deposited onto mullite substrates: from material preparation to photovoltaic devices*. in *16th European Photovoltaic Solar Energy Conference*. 2000. Glasgow, UK.
72. Brendel, R., *Thin-Film Crystalline Silicon Solar Cells Physics and Technology*. 1st ed. 2003: Wiley-VCH GmbH. 306.
73. McClelland, R.W., C.O. Bolzer, and C.J.J. Fan, *A technique for producing epitaxial films on re-usable substrates*. *Applied Physics Letter*, 1980. **37**(6): p. 560-562.
74. Bozler, C.O., R.W. McClelland, and J.C.C. Fan, *Ultrathin high-efficiency solar cells made from GaAs films prepared by the CLEFT process*. *IEEE Electron Devices Letters*, 1981. **2**(8): p. 203-205.
75. Deguchi, M., et al. *Prospect of the high efficiency for the VEST (via hole etching for the separation of thin films) cell*. in *IEEE 1st World Conference on Photovoltaic Energy Conversion*. 1994. Waikoloa, HI.
76. Arimoto, S., et al., *High-efficiency operation of large-area (100 cm²) thin-film polycrystalline silicon solar cell based on SOI structure*. *Solar Energy Materials and Solar Cells*, 1994. **34**(1-4): p. 257-262.
77. Ishihara, T., et al., *Development of high efficiency thin film polycrystalline Si cells using the VEST process*, in *MRS Proceedings*. 1998. p. 3-11.
78. Weber, K.J., K. Catchpole, and A.W. Blakers, *Epitaxial lateral overgrowth of Si on (100) Si substrates by liquid-phase epitaxy*. *Journal of Crystal Growth*, 1998. **186**(3): p. 369-374.
79. Weber, K.J. and A.W. Blakers, *The Epilift technique for Si solar cells*. *Applied Physics A: Material Science & Processing*, 1999. **69**: p. 195-199.
80. Stocks, M.J., K.J. Weber, and etc. *Fabrication of solar cells using the epilift technique*. in *3rd World Conference on Photovoltaic Energy Conversion*. 2003. Osaka, Japan.

81. Stocks, M.J., K.J. Weber, and etc. *Silicon liquid phase epitaxy for epilift solar cells*. in *3rd World Conference on Photovoltaic Energy Conversion*. 2003. Osaka, Japan.
82. Gee, J.M., W.K. Schubert, and P. A. Basore. *Emitter wrap-through solar cell*. in *23rd IEEE Photovoltaic Specialists Conference*. 1993. Louisville, KY.
83. Yonehara, T., K. Sakaguchi, and etc, *Epitaxial layer transfer by bond and etch back of porous Si*. Applied Physics Letter, 1994. **64**: p. 2108.
84. Brendel, R. *A novel process for ultrathin monocrystalline silicon solar cells on glass*. in *14th European Photovoltaic Solar Energy conversion*. 1997. Barcelona, Spain.
85. Solanki, C.S., et al., *Porous silicon layer transfer processes for solar cells*. Solar Energy Materials and Solar Cells, 2004. **83**(1): p. 101-113.
86. Scheel, H.J., *Introduction to Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*, P. Capper and M. Mauk, Editors. 2007, John Wiley & Son Ltd. p. 1/464.
87. Tien, P.K., et al., *Optical waveguides of single-crystal garnet films*. Applied Physics Letter, 1972. **21**(5): p. 207-209.
88. Ferrand, B., B. Chambaz, and M. Couchaud, *Liquid phase epitaxy: A versatile technique for the development of miniature optical components in single crystal dielectric media*. Optical Materials, 1999. **11**(2-3): p. 101-114.
89. Baliga, B.J., *SILICON LIQUID-PHASE EPITAXY - A REVIEW*. Journal of the Electrochemical Society, 1986. **133**(1): p. C5-C14.
90. Kita, K., et al., *Study on the lateral growth of silicon films from metal solutions with temperature gradient*. Journal of Crystal Growth, 2002. **234**(1): p. 153-158.
91. Zytkiewicz, Z.R., P. Strak, and S. Krukowski, *Unlimited Growth of III-V Bulk Crystals by Liquid-Phase Electroepitaxy*. Crystal Growth & Design, 2011. **11**(10): p. 4684-4689.
92. Muller, M., et al., *Silicon LPE on substrates from metallurgical silicon feedstock for large scale production*. Proceedings of 3rd World Conference on Photovoltaic Energy Conversion, Vols a-C, ed. K. Kurokawa, et al. 2003. 1221-1224.
93. Arch, J.K., E. Bauser, and etc. *Characterization of liquid phase epitaxy silicon for thin film solar cells*. in *11th European Community Photovoltaics Solar Energy Conference*. 1993. Harwood, Switzerland.
94. Thompson, G.H.B. and P.A. Kirkby, *Liquid phase epitaxial growth of six-layer GaAs/(GaAl)As structures for injection lasers with 0.04 μm thick centre layer*. Journal of Crystal Growth, 1974. **27**: p. 70-85.
95. Shin-ichi Akai, et al., *Method and apparatus for production of liquid phase epitaxial layer of semiconductors*. 1976: U.S.A.
96. Chandvankar, S.S., A.P. Shah, and B.M. Arora, *Doping and surface morphology of Al_xGa_{1-x}As/GaAs grown at low temperature by liquid-phase epitaxy*. Journal of Crystal Growth, 1998. **186**(3): p. 329-337.
97. Mauk, M. and J. McNeely, *Equipment and Instrumentation for Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic*

- Materials*, P. Capper and M. Mauk, Editors. 2007, John Wiley & Son Ltd. p. 88/464.
98. *Liquid Phase Epitaxy*, in *Encyclopedia of Materials - Science and Technology*, K.H.J. Buschow, et al., Editors. 2001, Elsevier. p. 4588-4597.
 99. Hsieh, J.J., *Thickness and surface morphology of GaAs LPE layers grown by supercooling, step-cooling, equilibrium-cooling, and two-phase solution techniques*. Journal of Crystal Growth, 1974. **27**(0): p. 49-61.
 100. Bolkhovityanov, Y.B. and H.B. Zembatov, *Investigation of growth kinetics and mechanism of GaAs and (InGa)As thin films grown by a step-cooling technique of the liquid phase epitaxy*. Journal of Crystal Growth, 1977. **37**(2): p. 101-106.
 101. Wright, P.D., E.A. Rezek, and N. Holonyak Jr, *Lattice matching and dislocations in LPE in $1-x\text{Ga}x\text{P}1-z\text{As}z-\text{InP}$ heterojunctions*. Journal of Crystal Growth, 1977. **41**(2): p. 254-261.
 102. Kano, H., S. Miyazawa, and K. Sugiyama, *LIQUID-PHASE EPITAXY OF GAI-YINYASXSBI-X QUATERNARY ALLOYS ON GASB*. Japanese Journal of Applied Physics, 1979. **18**(11): p. 2183-2184.
 103. Feng, M., et al., *The influence of LPE growth techniques on the alloy composition of InGaAsP*. Applied Physics Letters, 1979. **34**(4): p. 292-295.
 104. Gorbachev, A., V. Mishurnyi, and F. de Anda, *Control of the critical supercooling in LPE*. Journal of Electronic Materials, 2000. **29**(12): p. 1402-1405.
 105. Arora, B., *Growth of III-V compounds by liquid phase epitaxy*. Bulletin of Materials Science, 1990. **13**(1): p. 11-26.
 106. Minden, H.T., *Constitutional supercooling in GaAs liquid phase epitaxy*. Journal of Crystal Growth, 1970. **6**(3): p. 228-236.
 107. Zheng, G.F., et al., *16.4% efficient, thin active layer silicon solar cell grown by liquid phase epitaxy*. Solar Energy Materials and Solar Cells, 1996. **40**(3): p. 231-238.
 108. Shi, Z., et al., *Solution growth of polycrystalline silicon on glass at low temperatures*, in *1994 Ieee First World Conference on Photovoltaic Energy Conversion/Conference Record of the Twenty Fourth Ieee Photovoltaic Specialists Conference-1994, Vols I and Ii*. 1994. p. 1579-1582.
 109. Shi, Z.R., et al., *INVESTIGATION OF POLYCRYSTALLINE SILICON DEPOSITION ON GLASS SUBSTRATES*. Solar Energy Materials and Solar Cells, 1993. **31**(1): p. 51-60.
 110. Mauk, M., *Silicon, Germanium and Silicon-Germanium Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*, P. Capper and M. Mauk, Editors. 2007, John Wiley & Son Ltd. p. 136/464.
 111. Kopecek, R., et al., *Structural and electrical properties of silicon epitaxial layers grown by LPE on highly resistive monocrystalline substrates*. Journal of Crystal Growth, 2000. **208**(1-4): p. 289-296.
 112. Wagner, B.F., et al., *15.9-PERCENT EFFICIENCY FOR SI THIN-FILM CONCENTRATOR SOLAR-CELL GROWN BY LPE*, in *Conference Record of the Twenty Third Ieee Photovoltaic Specialists Conference - 1993*. 1993. p. 356-359.

113. Ciszek, T.F., et al., *SI THIN-LAYER GROWTH FROM METAL SOLUTIONS ON SINGLE-CRYSTAL AND CAST METALLURGICAL-GRADE MULTICRYSTALLINE SI SUBSTRATES*, in *Conference Record of the Twenty Third Ieee Photovoltaic Specialists Conference - 1993*. 1993. p. 65-72.
114. Nitsche, R., D. Elwell. H. J. Scheel. *Crystal Growth from High-Temperature Solutions*. Academic Press 1975; XIV + 630 Seiten. Kristall und Technik, 1976. **11**(3): p. K28-K29.
115. Ito, K. and K. Kojima, *SOLUTION-GROWN SILICON SOLAR-CELLS*. Japanese Journal of Applied Physics, 1980. **19**: p. 37-41.
116. Ciszek, T.F., et al., *Growth of thin crystalline silicon layers for photovoltaic device use*. Journal of Crystal Growth, 1993. **128**(1-4): p. 314-318.
117. Ito, K., T. Nakazawa, and A. Masamura, *Silicon solar cells made by liquid phase epitaxy*. Japanese Journal of Applied Physics, 1982. **21S2**(Supplement 21-2): p. 125-129.
118. Satoh, Y., et al., *Influence of growth temperature on minority-carrier lifetime of Si layer grown by liquid phase epitaxy using Ga solvent*. Journal of Applied Physics, 2005. **98**(7): p. 073708-4.
119. Girault, B., et al., *LIQUID-PHASE EPITAXY OF SILICON AT VERY LOW-TEMPERATURES*. Journal of Crystal Growth, 1977. **37**(2): p. 169-177.
120. Scott, W. and R.J. Hager, *SOLUTION GROWTH OF INDIUM-DOPED SILICON*. Journal of Electronic Materials, 1979. **8**(5): p. 581-602.
121. Ujihara, T., et al., *High-quality crystalline silicon layer grown by liquid phase epitaxy method at low growth temperature*. Japanese Journal of Applied Physics Part 2-Letters, 2003. **42**(3A): p. L217-L219.
122. Ujihara, T., et al., *What is the most important growth parameter on crystal quality of the silicon layer by LPE method?* Proceedings of 3rd World Conference on Photovoltaic Energy Conversion, Vols a-C, ed. K. Kurokawa, et al. 2003. 1241-1244.
123. Werner, J.H., et al., *SILICON SOLAR-CELL OF 16.8 MU-M THICKNESS AND 14.7-PERCENT EFFICIENCY*. Applied Physics Letters, 1993. **62**(23): p. 2998-3000.
124. Kolodinski, S. and J.H. Werner. *Thin silicon solar cells from liquid phase epitaxy*. in *11th European Photovoltaic Solar Energy Conference*. 1993. Chur, Switzerland.
125. Wagner, G., et al., *Structural and electrical properties of silicon epitaxial layers grown by LPE and CVD on identical polycrystalline substrates*. Journal of Crystal Growth, 1997. **174**(1-4): p. 680-685.
126. Arch, J.K., J.H. Werner, and E. Bauser, *HALL-EFFECT ANALYSIS OF LIQUID-PHASE EPITAXY SILICON FOR THIN-FILM SOLAR-CELLS*. Solar Energy Materials and Solar Cells, 1993. **29**(4): p. 387-396.
127. Possin, G.E., *Solution growth of silicon from liquid tin for application to photovoltaic solar cells*. Solid-State Electronics, 1984. **27**(2): p. 167-176.
128. Peter, K. and G. Willeke. *Rapid growth of high quality crystalline silicon by a novel temperature gradient liquid phase epitaxy (LPE) technique*. in *13th European Photovoltaic Solar Energy Conf*. 1993. Nice, France.

129. Shi, Z., et al., *The effects of solvent and dopant impurities on the performance of LPE silicon solar cells*. Solar Energy Materials and Solar Cells, 1996. **41-2**: p. 53-60.
130. Konuma, M., et al., *Liquid phase epitaxy of Si from Pb solutions*. Journal of Crystal Growth, 1999. **198**: p. 1045-1048.
131. Blakers, A.W., K.J. Weber, and etc. *18% efficiency thin silicon solar cell by liquid phase epitaxy*. in *13th European Photovoltaic Solar Energy Conference*. 1995. Nice, France.
132. Blakers, A.W., et al., *17% Efficient thin-film silicon solar cell by liquid-phase epitaxy*. Progress in Photovoltaics: Research and Applications, 1995. **3**(3): p. 193-195.
133. Ballhorn, G., et al., *High-efficiency multicrystalline silicon solar cells by liquid phase-epitaxy*. Solar Energy Materials and Solar Cells, 1998. **52**(1-2): p. 61-68.
134. Peter, K., et al., *Thin film silicon solar cells on upgraded metallurgical silicon substrates prepared by liquid phase epitaxy*. Solar Energy Materials and Solar Cells, 2002. **74**(1-4): p. 219-223.
135. Lee, E., et al., *Optimization of P+ seeding layer for thin film silicon solar cell by liquid phase epitaxy*. Proceedings of 3rd World Conference on Photovoltaic Energy Conversion, Vols a-C, ed. K. Kurokawa, et al. 2003. 1214-1216.
136. Bergmann, R., *MODEL FOR DEFECT-FREE EPITAXIAL LATERAL OVERGROWTH OF SI OVER SiO₂ BY LIQUID-PHASE EPITAXY*. Journal of Crystal Growth, 1991. **110**(4): p. 823-834.
137. Kinoshita, S., Y. Suzuki, and T. Nishinaga, *Epitaxial lateral overgrowth of Si on non-planar substrate*. Journal of Crystal Growth, 1991. **115**(1-4): p. 561-566.
138. Mauk, M., *Silicon, Germanium and Silicon-Germanium Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*, P. Capper and M. Mauk, Editors. 2007, John Wiley & Son Ltd. p. 143/464.
139. Olesinski, R., N. Kanani, and G. Abbaschian, *The In-Si (Indium-Silicon) system*. Journal of Phase Equilibria, 1985. **6**(2): p. 128-130.
140. Mauk, M., *Silicon, Germanium and Silicon-Germanium Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*, P. Capper and M. Mauk, Editors. 2007, John Wiley & Son Ltd. p. 166/464.
141. Mauk, M., *Silicon, Germanium and Silicon-Germanium Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*, P. Capper and M. Mauk, Editors. 2007, John Wiley & Son Ltd. p. 117-119/464.
142. Stringfellow, G.B., *The calculation of regular solution interaction parameters between elements from groups III, IV and V of the periodic table*. Materials Research Bulletin, 1971. **6**(5): p. 371-379.
143. Wang, T.H. and T.F. Cizek, *Impurity segregation in LPE growth of silicon from Cu Al solutions*. Journal of Crystal Growth, 1997. **174**(1-4): p. 176-181.
144. Alonso, M.I. and E. Bauser, *Growth of Si_{1-x}Ge_x on silicon by liquid-phase epitaxy*. Journal of Applied Physics, 1987. **62**(11): p. 4445-4449.
145. Thurmond, C.D. and M. Kowalchik, *Germanium and Silicon Liquidus Curves*. Bell System Technical Journal, 1960. **39**(1): p. 169-204.

146. Smith, R., *The growth of crystals from the melt by J. C. Brice*. Acta Crystallographica, 1966. **21**(3): p. 454.
147. Kuhn, G., J. C. Brice. *The Growth of Crystals from Liquids (Series of Monographs on Selected Topics in Solid State Physics, Volume XII, Ed. E. P. Wohlfarth)*. North-Holland Publishing Company - Amsterdam, London and American Elsevier Publishing Company, Inc. - New York 1973 379 Seiten, zahlreiche Abbildungen und Tabellen, Preis: \$ 28, 10. Kristall und Technik, 1974. **9**(2): p. K27-K28.
148. Kühn, G., J. C. Brice. *Crystal growth processes*. Blackie & Son Ltd., Glasgow and London 1986 (distributed in the USA by Halsted Press, a Division of John Wiley and Sons Inc., New York), 298 Seiten, zahlreiche Abbildungen, Tabellen und Literaturzitate, Preis £ 29.00, ISBN 0-470-20268-8. Crystal Research and Technology, 1987. **22**(1): p. 8-8.
149. Garfinkel, M. and R.N. Hall., *Floating substrate process: Large-area silicon sheet task low-cost solar array project*. 1976, Jet Propulsion Laboratory, NASA Center.
150. Baliga, B.J., *Isothermal Silicon Liquid Phase Epitaxy from Supersaturated Tin*. Journal of the Electrochemical Society, 1978. **125**(4): p. 598-600.
151. Scheel, H.J., *Control of Epitaxial Growth Modes for High-performance Devices*, in *Crystal Growth Technology*, H.J. Scheel and T. Fukuda, Editors. 2003, Wiley & Sons, Ltd. p. 626/694.
152. Bauer, E., *Phänomenologische Theorie der Kristallabscheidung an Oberflächen. I*. Zeitschrift für Kristallographie, 1958. **110**(1-6): p. 372-394.
153. Frank, F.C. and J.H. van der Merwe, *One-Dimensional Dislocations. I. Static Theory*. Proceedings of the Royal Society of London. Series A. Mathematical and Physical Sciences, 1949. **198**(1053): p. 205-216.
154. Volmer, M. and A. Weber, *The Self Assembly of Superhydrophobic Copper Thiolate Films on Copper in Thiol Solutions*. Zeitschrift für Physikalische Chemie, 1926. **119**: p. 227.
155. Stranski, I.N. and L. Krastanow, *Abhandlungen der Mathematisch-Naturwissenschaftlichen Klasse IIB*. Akademie der Wissenschaften Wien, 1938. **146**: p. 797-810.
156. Bennett, B.R., et al., *Stranski-Krastanov growth of InSb, GaSb, and AlSb on GaAs: structure of the wetting layers*. Journal of Crystal Growth, 1997. **175–176**, Part **2**(0): p. 888-893.
157. *Stranski-Krastanov growth*. Available from: http://en.wikipedia.org/wiki/Stranski%E2%80%93Krastanov_growth#cite_note-stranski_krastanov-4.
158. Hawley, M., et al., *GROWTH-MECHANISM OF SPUTTERED FILMS OF YBA2CU3O7 STUDIED BY SCANNING TUNNELING MICROSCOPY*. Science, 1991. **251**(5001): p. 1587-1589.
159. Gerber, C., et al., *SCREW DISLOCATIONS IN HIGH-TC FILMS*. Nature, 1991. **350**(6316): p. 279-280.
160. Nelson, J., *The Physics of Solar Cells*, London, UK: Imperial College Press. 363.

161. Koch, W., et al., *Bulk Crystal Growth and Wafering for PV*, in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Editors. 2003, John Wiley & Sons Ltd. p. 216/1168.
162. *HL5500PC Hall Effect Measurement System with HL5580 Buffer Amplifier User Manual* A.O.T. Inc, Editor.
163. Jacoboni, C., et al., *A review of some charge transport properties of silicon*. Solid-State Electronics, 1977. **20**(2): p. 77-89.
164. E.F.Schubert, in *Quantum Mechanics Applied to Semiconductor Devices* 2004, Rensselaer Polytechnic Institute. p. 143.
165. Pisarkiewicz, T., *Photodecay method in investigation of materials and photovoltaic structures*. Opto-Electronics Review, 2004. **12**(1): p. 33-40.
166. del Alamo, J.A. and R.M. Swanson, *Modelling of minority-carrier transport in heavily doped silicon emitters*. Solid-State Electronics, 1987. **30**(11): p. 1127-1136.
167. Ujihara, T., et al., *Effects of growth temperature on the surface morphology of silicon thin films on (111) silicon monocrystalline substrate by liquid phase epitaxy*. Journal of Crystal Growth, 2004. **266**(4): p. 467-474.