DEVELOPMENT OF A SEM MICROLITHOGRAPHY SYSTEM: APPLICATION TO GHz SURFACE ACOUSTIC WAVE DEVICES

By

DIETER G. SEILER, B.ENG., M.ENG.

A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfilment of the Requirements

for the Degree

Doctor of Philosophy

McMaster University

1979

© DIETER G. SEILER 1979

DEVELOPMENT OF A SEM
MICROLITHOGRAPHY SYSTEM

DOCTOR OF PHILOSOPHY (1979)
(Electrical Engineering)

McMASTER UNIVERSITY
Hamilton, Ontario

TITLE: Development of a SEM Microlithography System: Application to GHz Surface Acoustic Wave Devices

AUTHOR: Dieter G. Seiler, B.Eng. (McMaster University)
M.Eng. (McMaster University)

SUPERVISOR: Professor C.K. Campbell

NUMBER OF PAGES: xii, 179

ABSTRACT

This thesis concerns itself with the design and implementation of an electron beam lithography system. A novel microcomputer-controlled vector-scan pattern generator was constructed and interfaced to a commercially available scanning electron microscope (SEM). A software monitor program was incorporated into the 8-bit microcomputer, which allows pattern data entry in decimal coordinates via a keyboard/display interface, and subsequent storage of the coded data on cassette tape.

The usable scan field size for accurate pattern exposure in the Stereoscan Mark II A SEM has been determined to be 1mm x 1mm. The electron beam lithography system was used to scan a 1 GHz surface acoustic wave (SAW) delay line pattern, which featured a total of 480 fingers, each 7,680 Å in width. Polymethylmethacrylate (PMMA) electron-sensitive resist was used for the pattern exposures, and a linear charge density of 1×10^{-8} C/cm was used. The lift-off fabrication process was used to obtain the final device circuit features. The resulting delay line exhibited an untuned insertion loss of 24.3 dB, and was subsequently incorporated into the feedback loop of an amplifier with excess gain to form a SAW oscillator.

Several other circuit patterns were scanned, including a 2 GHz SAW delay line with 3000 Å linewidths, and sub-micron bubble memory T-I bar circuits. Details of all the scanning parameters are given, along with the pattern exposure results.

ACKNOWLEDGEMENTS

The author would like to express his thanks and appreciation to his supervisor, professor C.K. Campbell, for his support and interest in this work. Thanks is also given to the National Research Council, which made this research work possible through their funding and scholarship programs.

The author would also like to thank Dr. V.M. Ristic from the University of Toronto; whose initial interest in electron lithography prompted the research carried out in this thesis.

The author also thanks Fred Pearson and Fred Smith for their support and help with the Cambridge Stereoscan electron microscope. The members of the research lab, namely Jim Reilly, Mark Suthers, Pala Nanayakkara, and Peter Edmonson are thanked for providing a stimulating and helpful work environment.

Finally, the author wishes to express sincere thanks to his fiancee, Renate Reichert, for her expert typing of this thesis, her meticulous proof-reading, and her loving consideration and understanding during the course of this thesis research and writing.

TABLE OF CONTENTS

		Page
CHAPTER 1:	INTRODUCTION	1
1.1	Background	1
1.2	Scope of this Thesis	4
CHAPTER 2:	HIGH RESOLUTION LITHOGRAPHY: A REVIEW	6
2.1	Introduction	6
2.2	Lithography Schemes	6
2.3	Basics of Scanning Electron Microscope (SEM) Operation	14
2.4	State of the Art Systems	31
2.5	Conclusions	41
CHAPTER 3:	DESIGN AND IMPLEMENTATION OF LITHOGRAPHY SYSTEM	44
3.1	Introduction	44
3.2	Design Objectives and Considerations	44
3.3	Pattern Generator Hardware	51
3.4	Software: The Monitor Program	59
3.5	The Complete Lithography System	65
3.6	Conclusions	67
CHAPTER 4:	DEVICE FABRICATION: PROCEDURE AND SYSTEM VERIFICATION	69
4.1	Introduction	69
4.2	Resist Considerations	70
4.3	Substrate Preparation	82
4.3.1	Substrate Cleaning	82
4.3.2	Resist Application	85
4.3.3	Post Baking and Mounting	86
4.3.4	Conductive Layer Application	87
4.4	Pattern Exposure	88
4.4.1	SEM Parameter Settings	88

TABLE OF CONTENTS (continued)

		Page
4.4.2	Alignment Procedure	93
4.4.3	Scanning the Pattern	97
4.5	Pattern Development	99
4.6	Post Development Processing	101
4.7	Identification of Fabrication Problems	104
4.7.1	Pattern Generation Errors	104
4.7.2	Device Processing Problems	106
4.8	Conclusions	115
CHAPTER 5:	APPLICATION: FABRICATION OF A 1 GHz SURFACE ACOUSTIC WAVE OSCILLATOR	117
5.1	Introduction	117
5.2	Fundamentals of SAW Oscillators	117
5.3	Design Parameters for 1 GHz Delay Line	127
5.4	Fabrication Summary	129
5.5	Test Results	136
5.6	Conclusions	143
CHAPTER 6:	FURTHER EXPERIMENTAL STUDIES	144
6.1	Introduction	144
6.2	2 GHz SAW Delay Line	144
6.3	General Format Scanning	147
6.4	Bubble Memory Fabrication	150
6.5	Discussion and Conclusions	152
CHAPTER 7:	CONCLUSIONS	155
APPENDIX A:	THE MONITOR PROGRAM	159
APPENDIX B:	ALIGNMENT MARK FABRICATION	172
REFERENCES		176

LIST OF FIGURES

Figure		Page
2.1	Basic lithographic process using a mask.	9
2.2	Simplified schematic of a SEM illustrating principles of operation.	15
2.3	Schematic of self-biased electron gun system.	16
2.4	(a) Relationship of beam current and brightness to applied bias voltage.	19
	(b) Emission characteristic of self-biased electron gun.	19
2.5	(a) Schematic of axially symmetric electromagnetic lens.	21
	(b) Components of magnetic field intensity vs. axial distance.	21
2.6	Ray trace representation of final spot formation.	23
2.7	Final electron beam current to beam diameter relationship.	27
2.8	Electron beam interactions with the sample in a SEM.	28
2.9	Detection schemes for backscattered (B), secondary (Se) and absorbed electrons.	29
2.10	Block diagram of simplified pattern generator.	32
2.11	Block diagram of analog/digital pattern generator.	34
2.12	Rotational alignment procedure.	37
2.13	IBM computer-controlled E-beam microfabrication system.	38
2.14	Schematic of IBM hardwired pattern generator.	40
2.15	Shape menu, with dotted lines indicating beam traverse with beam blanked.	42
3.1	Schematic of Stereoscan Mark II A electron column.	46
3.2	Spot exposure results for Stereoscan Mark II A by DeVore.	49
3.3	Schematic of simplified vector scan generator.	52

LIST OF FIGURES (continued)

Figure		Page
3.4	Photograph illustrating scan generator board (top) and amplifier and beam blanking board (below).	55
3.5	Front and rear views of completed pattern generator.	57
3.6	(a) Pattern generator keyboard/display unit.	58
	(b) Cassette data storage system.	58
3.7	General monitor output coding format for two consecutive 8-bit data bytes.	60
3.8	Monitor program flowchart. (a) Data input, conversion, and storage routine.	61
	(b) General format scan program.	62
	(c) Cassette loader program.	63
3.9	Microfabrication system using Stereoscan Mark II A SEM.	66
4.1	Positive resist profiles for three levels of exposure (a) high charge density (b) medium charge density, and (c) low charge density.	74
4.2	(a) Developed resist slope angle vs. charge density for PMMA.	76
	(b) Family of profiles for various accelerating potentials, with PMMA thickness of 4000 Å on silicon substrate, and q_l is the linear charge density = 1×10^{-8} C/cm.	76
4.3	Definition of variables x, y, z, and r in relation to an E-beam line scan with velocity $\bar{V}$.	78
4.4	$E(y,z)\|_{ARRAY}$ for an array of lines exposed in a 4000 Å PMMA layer at 20 keV beam energy, with interline spacings of (a) 2μm, (b) 1μm, (c) 0.5μm, and (d) 0.3μm.	80
4.5	(a) Back-scattering coefficient shown as a function of substrate atomic number Z.	81
	(b) Back-scattering coefficient shown as a function of accelerating potential for various elements.	81

LIST OF FIGURES (continued)

Figure		Page
4.6	(a) Glass vapour-cleaning apparatus.	84
	(b) Resist application set-up.	84
4.7	Mounted quartz substrate, ready for pattern exposure.	89
4.8	Relation of final aperture to probe diameter and working distance.	91
4.9	Relation between spot size and lens currents for first two condenser lenses C1 and C2, at various working distances.	92
4.10	(a) x42 photograph of gold alignment marks on substrate surface.	94
	(b) x48 SEM photograph of alignment marks as they appear to the operator on the SEM CRT display.	94
4.11	Alignment mark placement on 1cm x 1cm ST-X quartz substrate.	95
4.12	Sub-micron circuit fabrication techniques. (a) Etch process.	102
	(b) Lift-off process.	102
4.13	D/A converter zero-crossover defect in test circuit.	105
4.14	10μm grid scan in PMMA. (a) x44 optical photo of entire field.	107
	(b) x90 optical photo of upper left corner.	107
4.15	Two optical photographs (x390) illustrating beam-lagging effects. (a) On both finger and pad.	109
	(b) End finger.	109
4.16	(a) Connection pad overexposure effects.	110
	(b) The 'Spaghetti' effect.	110
4.17	(a) Incomplete lift-off.	113
	(b) Close-up of above.	113

LIST OF FIGURES (continued)

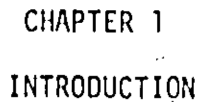
Figure		Page
4.18	Internal view of vacuum chamber showing filament arrangement.	114
5.1	Schematic of basic generation and detection scheme for SAWs.	118
5.2	Schematic of basic SAW delay line oscillator.	122
5.3	Normalized response of SAW delay line showing mode suppression principle.	126
5.4	(a) Developed pattern of 1 GHz SAW delay line (x45).	132
	(b) x980 SEM photo of finger and pad area.	132
5.5	SEM photos illustrating exposed finger areas near pad. (a) x10,600	133
	(b) x21,200	133
5.6	(a) Chromium mask of extension pads, with exposure jig.	137
	(b) SAW delay line mounted in 3cm x 3cm test package.	137
5.7	Frequency response of SAW delay line. Log reference = 0 dB Vertical = 10 dB/div. Bandwidth = 300 kHz Horizontal = (a) 20 MHz/div.	138
	(b) 5 MHz/div.	138
5.8	Test set-up for measuring SAW oscillator spectrum.	141
5.9	Output power spectrum of 1 GHz SAW oscillator. (a) Log reference = +10 dBm Vertical = 10 dB/div. Horizontal = 100 MHz/div. Bandwidth = 300 kHz	142
	(b) Log reference = +10 dBm Vertical = 10 dB/div. Horizontal = 2 kHz/div. Bandwidth = 0.3 kHz	142

LIST OF FIGURES (continued)

Figure		Page
6.1	(a) x900 photograph of 2 GHz SAW delay line pattern in 4000 Å PMMA.	146
	(b) x9,800 SEM photo of 3000 Å finger structure of (a).	146
6.2	Several 480 finger 2GHz SAW delay lines scanned on a substrate.	148
6.3	(a) Alphabetical pattern scanned in PMMA using general format scan program.	149
	(b) 60μm x 60μm array of T-I bubble memory structures.	149
6.4	Close-up SEM photos of 4,600 Å linewidth T-I bar circuit features.	
	(a) x4,900	151
	(b) x19,500	151

LIST OF TABLES

		Page
TABLE 1.1	Electron Lithography Facilities	3
TABLE 2.1	High Resolution Lithographic Techniques	10
TABLE 4.1	Characteristics of Several Electron Resist Materials	71
TABLE 5.1	Several SAW Substrates and Their Related Properties	121
TABLE 5.2	Summary of SAW Delay Line Design Parameters	130



CHAPTER 1

INTRODUCTION

1.1 Background

In the past two decades, the electronics industry has experienced a phenomenal growth, both in volume and technological innovations. The reasons for this surge can be narrowed down to two important factors, one being the invention of the transistor, and the other being the miniaturization of electronic devices and circuits. The recent trend in micro-miniaturization has been to use electron beam (E-beam) or X-ray techniques to define the circuit patterns, thus overcoming the inherent limitations of light optics due to the wavelength of visible light. Since the effective wavelength of electrons (<1 Å) is many times smaller than that of light, an electron beam can readily be used to define sub-micron geometries with high resolution and accuracy, given the proper exposure conditions and control electronics.

The current minimum feature size for integrated circuits in mass-production is in the 2-4μm range. Optical techniques are presently still being used, however, electron beam exposure systems are anticipated for mass production techniques by the early 1980's. There are several driving forces behind this trend: an ever-increasing demand to shrink circuit dimensions, and the inevitable limitation on optical resolution of 1μm over small areas, (a few mm^2). To the manufacturer, these smaller circuit dimensions translate into a chip with increased density, thereby featuring less external connections, higher reliability, increased func-

tions per area, and an eventual decrease in cost. At the single device level, the decreased dimensions of the circuit usually translate into an increase in operating frequency, with surface acoustic wave (SAW) and field effect transistor (FET) devices being primary examples.

There are a limited number of E-beam microfabrication facilities in the world today, and several are listed in Table 1.1 [1], [2]. The majority of these systems were custom built as research tools, to study the problems associated with the entire lithographic process. In each case, the eventual goal was to produce a machine which could resolve 2μm and below pattern features at mass-production rates. At the present time, this goal has not yet been reached. Although electron lithography has been developed rather extensively in the past ten years, the throughput demanded by the manufacturing industry to make E-beam systems economically viable is still not possible. The few commercial lithography systems which have recently appeared on the market are primarily intended for the production of master masks, for use in subsequent ultraviolet exposure systems. The high cost of these systems rules out their use as a pure research tool for most institutions. As a result, the research effort in electron lithography is concentrated at the facilities listed in Table 1.1.

The large expense associated with the E-beam systems is due to several factors, the chief one being the amount of research money poured into the projects to develop the relatively new technology. Teams of specialized engineers, physicists, and technicians were required to tackle the problems, and as a result, totally new E-beam columns were designed from the ground up, supported by sophisticated new electronic

TABLE 1.1

Electron Lithography Facilities

Firm	System Name	Resolution	Comments
Toshiba, Japan	EBM-105	1μm ± .1μm	commercial, raster scan (1979)
NTT/Hitachi, Japan	—	1μm over 2mm x 2mm	vector scan, commercial
VEB Carl Zeiss of Jena, East Germany	ZBA-10	1μm ± .1μm	mask production
Cooperative Laboratory, JEOL, Japan	JBX-6A	—	direct-on-wafer high throughput
Texas Inst., USA	EBMII	1μm	research
Bell Labs, USA	EBES	.25μm address	
IBM, USA	EL1 VS1	2.5μm ±..5μm .5μm,over 3mm x 3mm	direct-on-wafer vector scan
Hughs Research, USA	—	<1μm	vector scan
Etec Corp., USA	MEBES	.25μm address	licensed from Bell Labs
Varian Associates, USA	EBMG-20	.25μm address	licensed from Bell Labs
Bell Northern Research, Canada	—	2μm	fast turn around vector scan
Cambridge Scientific Inst., England	EBMF-2	1μm	commercial
Philips, Netherlands	ENPG-3	.1μm	commercial, vector scan

systems. Powerful, fully-supported minicomputer systems are used to control all the relevant functions, usually with megabyte disc storage and the use of high level languages such as Fortran.

1.2 Scope of this thesis

This thesis concerns itself with the design and testing of an E-beam lithographic system, which utilizes an existing scanning electron microscope (SEM) facility. The primary contribution of this work is the design of a SEM pattern generation system which is inexpensive, extremely flexible, simple to use, and easily adaptable to a commercially-available SEM.

The reasons for the high costs of electron lithographic equipment were studied in detail by the author, and an analysis was then made of the individual system components to determine their function and relevance to the basic operation of the machine. The final design of the author's pattern generator was based on the results of this analysis, and also with the consideration that the end user will be affiliated with a research institution (university or small firm) which already has access to a commercially-made SEM. In some cases, only minor modifications are necessary to the SEM in order for it to be used as an experimental electron lithography system. The availability of a facility such as this to most research institutions would be a great asset, primarily in the area of device research as well as electron beam studies. This would allow the theoretical designs of sub-micron devices to be put to practice, thus providing a necessary link between theoretical predictions and experimental results. One further advantage of this system is that it can equally

well be used to fabricate small-area master masks, which would offset the time and expense of using the E-beam system for each device individually.

The available literature too often masks out the important detailed fabrication steps, usually for proprietary reasons. Therefore, a further contribution of the thesis is the step-by-step procedure necessary for the successful fabrication of a sub-micron linewidth device. The completed pattern generator was put to the test by fabricating a 1 GHz SAW delay line, which involved scanning 480 sub-micron-sized lines in a scan field of less than 1 mm square. The delay line was subsequently placed in the feedback loop of an amplifier with excess gain to form a stable UHF oscillator. Further experimentation was carried out to demonstrate both the high resolution potential of the system, and also the flexibility of the pattern definition/generation process by scanning 2 GHz SAW delay lines and bubble memory structures. All test results and procedures are documented, and further suggestions as to system improvement in design and use are summarized in the final chapter of this thesis.

CHAPTER 2

HIGH RESOLUTION LITHOGRAPHY: A REVIEW

2.1 Introduction

A brief review will be given in this chapter of the various high resolution lithography techniques which are currently in use or available to the microelectronics industry. The relevance of E-beam lithography compared to the other techniques will then be discussed, primarily in the context of replacing existing lithographic schemes in the near future. The necessity and importance of the goals of sub-micron lithography will be stressed in order to justify the concentration on E-beam systems. The basic principles of a SEM will be presented, since this thesis concerns itself with the application of a SEM to E-beam lithography. The difference between custom-designed systems and one centering around a commercially available SEM will also be clarified. Finally, state of the art E-beam lithography systems will be presented, so that appreciation can be gained for the relevance of the author's system in the field of microelectronics research and production.

2.2 Lithography Schemes

All microelectronic circuits, whether of the integrated type, or the single device type, require some form of pattern transfer to define the basic structure on a substrate. Regardless of the technology being incorporated into the device (eg. CMOS, SOS, CCD, SAW, or Bubble Domain),

certain planar shapes must at some point be designed and fabricated, such that the resulting technology/shape combination yields the desired response. These shapes may range from simple line gratings right up to complex arrangements of lines and rectangles at various angles, and lithography is the general term which is used to describe the process whereby these shapes are defined on a substrate surface.

In the majority of microelectronic applications, the substrate is flat, and hence the lithographic steps and subsequent processing are referred to as a planar technology. The role of the substrate is to provide a base for the patterned circuit, which may or may not depend on the material properties of the substrate itself. The simplest substrate configuration (eg. glass) merely provides a smooth, flat support for the planar circuit structure, while most other configurations rely on an intimate relationship between the substrate and the corresponding circuit features. This relationship is dependent on several factors, such as proximity, regions or area of overlap, orientation, substrate and circuit material properties, and type of interface (eg. surface or implantation). Once the appropriate pattern has been designed, either manually or with computer-aided techniques, one has a list of numbers which represent the two dimensional coordinates of the various circuit features (external boundaries). At this stage, there are several possible techniques available to the designer for transferring the required circuit pattern onto the substrate surface. The simplest and most common technique used to achieve this transfer involves the coating of the substrate with a photosensitive material called photoresist, followed by the optical imaging of the original pattern or "mask" (usually made larger than the final

required size) onto the substrate. Following this exposure, the photosensitized substrate is developed and the positive or negative of the original pattern now exists on its surface, defined in photoresist. This completes the lithographic aspect of the device fabrication, and the substrate is then ready for further processing, such as metal evaporation or plasma etching.

The basic principles of the lithographic process are illustrated in Figure 2.1 for a line grating exposure, although the process is valid for any arbitrary shapes and configurations. The key feature to note is that a mask is being used, which means that at some stage the pattern data points had to be transformed into a two dimensional picture of the pattern, usually enlarged on rubylith (a material with a thin, removable opaque layer based on a transparent plastic sheet). The various methods of using a mask for exposure differ mainly in the areas of mask proximity to the resist-coated substrate, the type of exposure radiation used, and the use (or absence) of optics in the process.

A list of the major types of lithography for high resolution applications is given in Table 2.1 [3]. Projection printing requires high-precision lenses for focussing the mask pattern onto the substrate. This results in a very expensive system in order to achieve 1μm resolution, and for smaller linewidths, the area of coverage is inherently very small due to optical lens limitations (eg. .5mm x .5mm). The mask pattern is usually defined on rubylith or thick glass plates and back-lit, with the lens demagnifying the original pattern by some integer factor to yield the final desired linewidth.

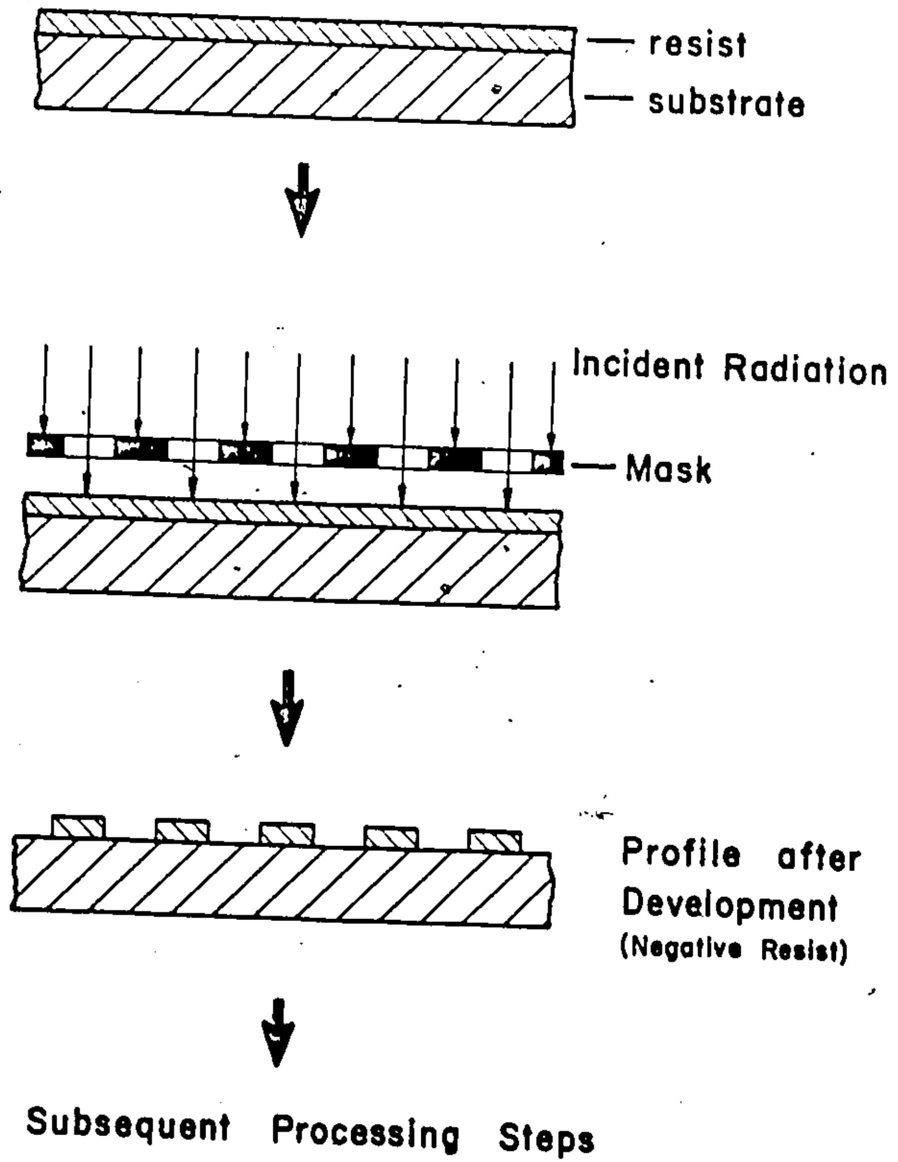


Figure 2.1 Basic lithographic process using a mask.

TABLE 2.1

High Resolution Lithographic Techniques

Technique	Resolution	Comments
Projection Printing	.9μm over 8mm dia.	non-contact optical imaging
Shadow Printing	.4μm over 10cmx10cm	intimate contact required, conformable mask -
	1μm large area	close contact, hard mask
Holographic Recording	~800 Å over several centimeters	gratings only
Electron Lithography	80 Å over 1mmx1mm	software mask
	4000 Å over 10cmx10cm	registration and accurate table control
X-Ray Lithography	3000 Å over standard wafers	requires E-beam generated masks

Shadow printing eliminates the need for optics between the mask and substrate since a 1:1 exposure is made with the mask in close contact with the resist-covered substrate. There are generally two versions of shadow printing in use: close contact and conformable photomask. The close contact technique utilizes thick (~1.5mm) glass masks placed directly onto the photoresist surface, and accuracy and resolution are limited by factors such as proximity, substrate surface flatness, resist film irregularities, and incident radiation collimation. Damage to both the mask and the substrate is very prevalent with this method, due to surface irregularities. An offshoot of this method which overcomes these problems is the conformable mask technique. By incorporating a thin, flexible glass mask, it is possible to achieve intimate contact over the entire surface area and even around surface irregularities. The contact is achieved by use of a vacuum in a special jig which forces the mask tightly over the substrate surface, while the flexibility of the mask automatically accounts for any non-flatness or obstacles on the surface. The lithographic techniques mentioned up to this point all require an original, usually enlarged mask from which the resulting pattern is developed. These masks are prepared by cutting the feature perimeters into rubylith on a machine, either by hand or under computer control, which could take hours, depending on pattern complexity. The appropriate 'cut' areas must then be lifted off by hand, a very long and tedious task as well. Once a rubylith mask is finished, any desired alteration (involving accuracy) can only be made by generating an entirely new mask.

Holographic recording [3] is a technique which makes use of the fact that any two coherent light sources, which meet at a known angle to

each other, will produce interference fringes with spacing given by

$$d = \lambda/2 \sin(\alpha/2) \quad Å \tag{2.1}$$

where λ = wavelength of source in Å

α = angle between two beams in radians

Short-wavelength laser light is used as the source, and extremely stable mounts are needed for the reflecting optics in order for this technique to produce usable results in exposing the photoresist. The prime disadvantage of this lithography system is that it is suitable only for line grating exposures.

Electron beam lithography digresses from conventional photolithographic techniques in several advantageous ways. With the exception of flying spot scanner systems, electron beam masks are software-oriented, rather than physical objects. Hence the numbers representing the pattern coordinates can be used directly to generate a required pattern, via a computer-controlled scan of an electron beam. The focussed electron beam is used to expose the resist layer on the substrate surface, with the beam diameter directly determining the ultimate resolution and minimum linewidth attainable. The path of the beam, and whether it is on or off, can be controlled by a computer, and hence a pattern is written directly onto the substrate, eliminating any intermediate steps. Resolution and accuracy is excellent for a small, fixed field of view (eg. 1mm x 1mm), and positional registration accuracies of ±1000 Å have been quoted [2] for the more complex step and repeat systems. At present the throughput

rate for E-beam systems is still behind that of conventional photolithography, but further research into new electron-sensitive resists and scanning systems will close the gap. Pattern changes can be effected quickly, simply by changing the software program or data, and similarily the resulting changes in device performance can be measured sooner, since many intermediate processing steps have been eliminated. Several variations exist in E-beam systems as to how the pattern data is exposed to the substrate. An earlier method, which makes use of a physical mask, is called a flying spot scanner system. Essentially, the mask is attached to the face of a large high-resolution cathode ray tube (CRT) and the focussed CRT beam is rastered across the pattern in synchronism with the electron beam in the SEM column. Whenever the CRT beam is blanked by an opaque feature on the mask, the electron beam is correspondingly blanked to replicate the features onto the substrate surface. This raster scan approach is also used without the flying spot scanner system, and beam on/off points are controlled by computer software. The most popular and efficient technique is the vector scan system, where only those lines which need to be exposed are actually scanned.

X-ray lithography relies on the straightness of an emitted X-ray beam and its corresponding low diffraction. The method consists of flooding a mask with X-rays such that the transmitted rays expose the desired pattern onto the substrate, which is not in close contact with the mask. The small wavelength and low diffraction of X-rays allow high resolution replication of sub-micron features from a special mask, despite the relatively large distance between the mask and substrate. This technique is well suited for mass production because of its parallel processing feature,

however, it should be noted that an E-beam system is required initially for the fabrication of the mask. The X-ray process is still plagued with problems, such as long exposure times and initial alignment errors between the mask and the substrate.

2.3 Basics of Scanning Electron Microscope (SEM) Operation

The basic structure and operation of a SEM will be discussed in this section, along with relevant points concerning its application in an E-beam lithography system. Figure 2.2 illustrates the basic SEM features. An analysis will be made starting at the top of the SEM column with the electron gun.

The electron gun provides the source for the electron beam, and this is achieved in a number of ways. The most common method is that of thermionic emission, where electrons escape from a material when it is elevated to sufficiently high temperatures. A typical self-biased electron gun [4] is shown schematically in Figure 2.3. The filament is usually made of tungsten, and is shaped into a hairpin formation to allow electrons to escape from the tip. Electrons are emitted from the filament when the tungsten is heated to approximately 2700°K, and the resulting current density J_c coming from the cathode can be expressed by Richardson's Law as

$$J_c = AT^2 \exp(-E_W/kT) \quad A/cm^2 \tag{2.2}$$

where A = a material-dependent constant in $A/cm^2{}^\circ K^2$

T = the emission temperature in °K

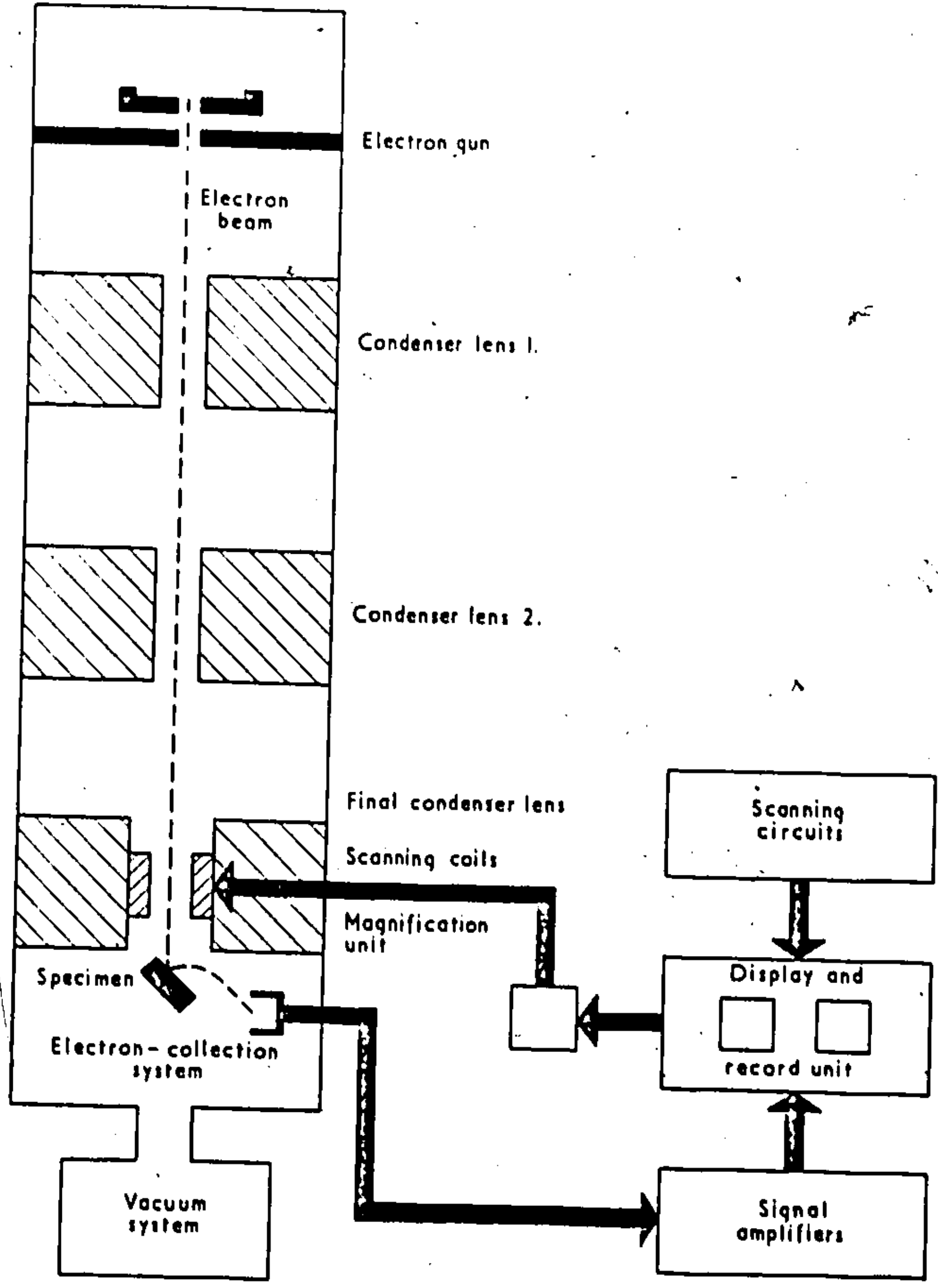


Figure 2.2 Simplified schematic of a SEM illustrating principles of operation. [6]

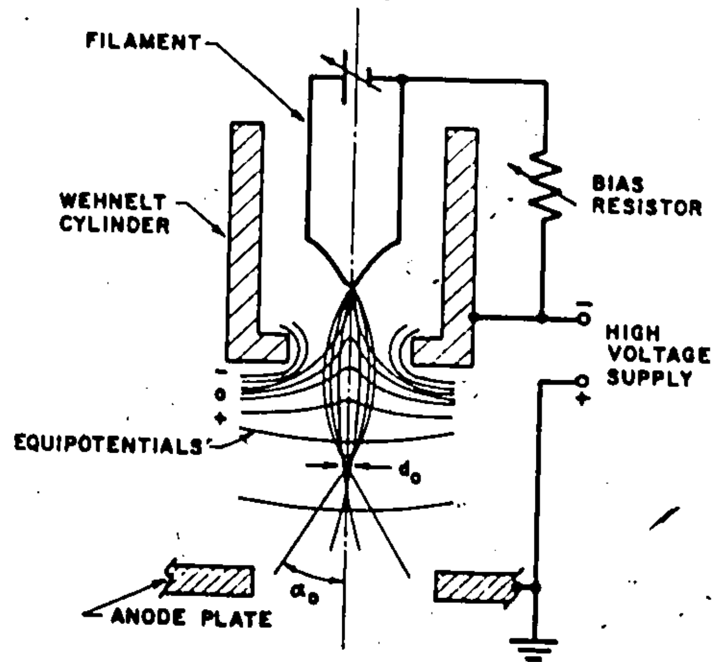


Figure 2.3 Schematic of self-biased electron gun system. [4]

k = Boltzmann constant (8.62×10^{-5} eV/°K)

E_w = the work function for the material in eV

For tungsten, at a temperature of 2700°K, A = 60A/cm^2°K^2 and E_w = 4.5eV, yielding a current density at the tip of 1.75A/cm^2. The emitted electrons are then accelerated toward the anode since a large accelerating potential exists between the filament and the anode,* usually from 1 to 50 kV. A grid cap, called the Wehnelt cylinder, is negatively biased by several hundred volts with respect to the filament. This grid is positioned and biased in such a way that the accelerated electrons are forced to converge to a crossover point with width d_o and divergence angle α_o, at some point below the grid. The maximum current density at this crossover point is given by

$$J_b = 4i_b/\pi d_o^2 \tag{2.3}$$

where i_b is the beam current measured from the filament

The most useful parameter which indicates the efficiency of an electron gun is its brightness, β, which is defined in terms of a solid angle through which the maximum beam current flows, and can be expressed as

$$\beta = 4i_b/(\pi d_o \alpha_o)^2 \tag{2.4}$$

and $\beta_m = J_c e E_o/\pi kT$ A/cm^2 steradian (2.5)

where J_c = current density at cathode (2.2)

E_o = accelerating voltage in volts

e = electronic charge, 1.602×10^{-19} C

β_m = maximum attainable brightness

The relationship between beam current and brightness [4] is illustrated in Figure 2.4 (a) as a function of bias voltage applied to the Wehnelt. Too high a bias has the effect of inhibiting the electron flow, while a low bias causes appreciable defocussing. The peak of the brightness curve is the optimum operating point. Once a beam current is chosen, it is desired to have a stable gun such that fluctuations in the beam current do not occur. The self-bias arrangement satisfies this requirement by saturating the filament, as shown in Figure 2.4 (b). Typical values of these parameters for a conventional SEM are

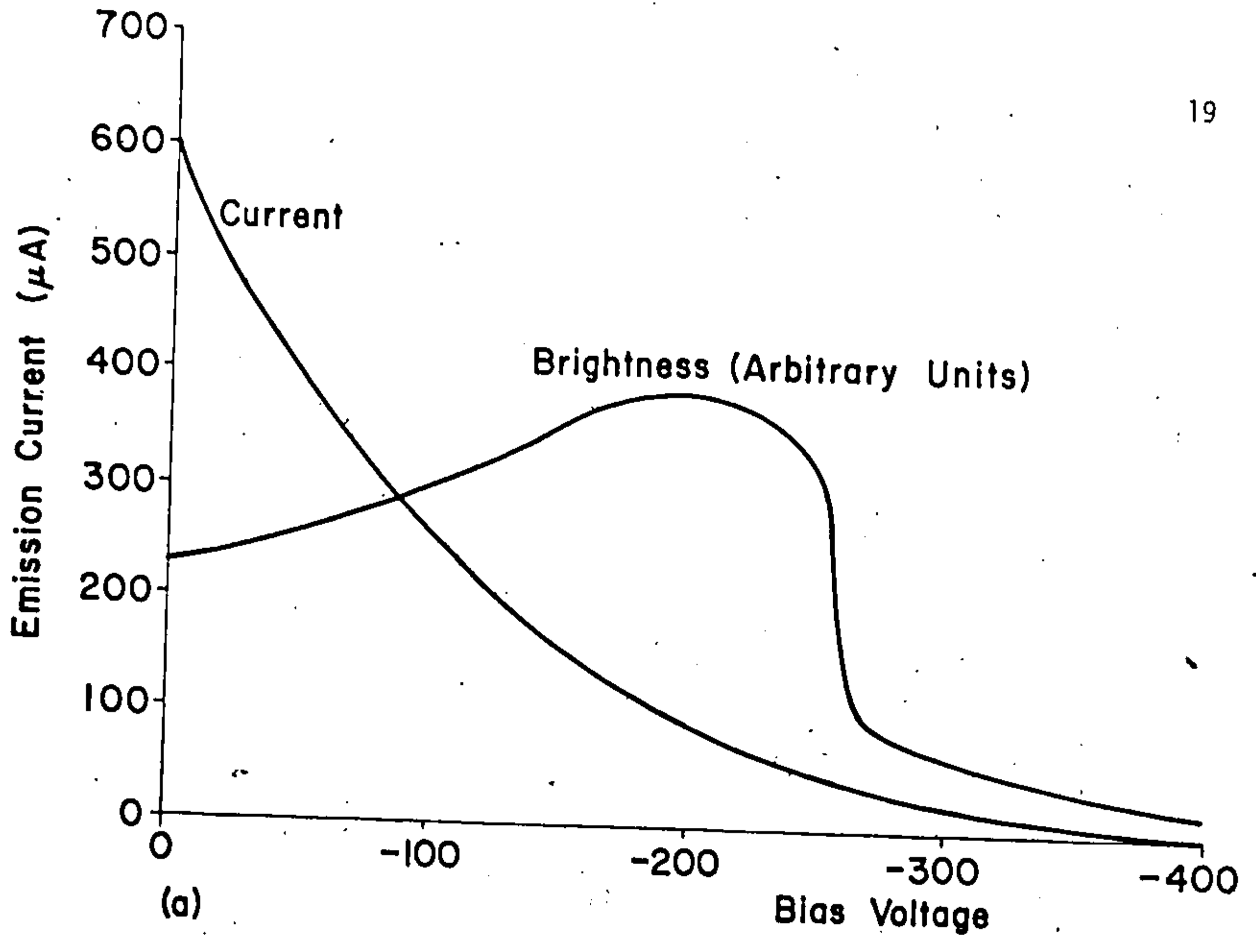
$d_o \sim 25$ to $100\mu m$

$\alpha_o \sim 3 \times 10^{-3}$ to 8×10^{-3} radians

$\beta = 60{,}000$ A/cm^2 steradian (for $E_o = 25$ kV and $J_c = 1.75$ A/cm^2)

$i_b \sim 100$ to $200\mu A$

Another type of electron gun is based on a LaB_6 (lanthanum hexaboride) rod which has a much smaller work function ($E_w = 2.4$eV) and consequently produces a source up to ten times brighter than that of tungsten. Several problems hinder its full acceptance, including high vacuum requirements and evaporation of the rod, but these problems are slowly being solved. The rod is usually 1mm square and has one end milled to a 10μm



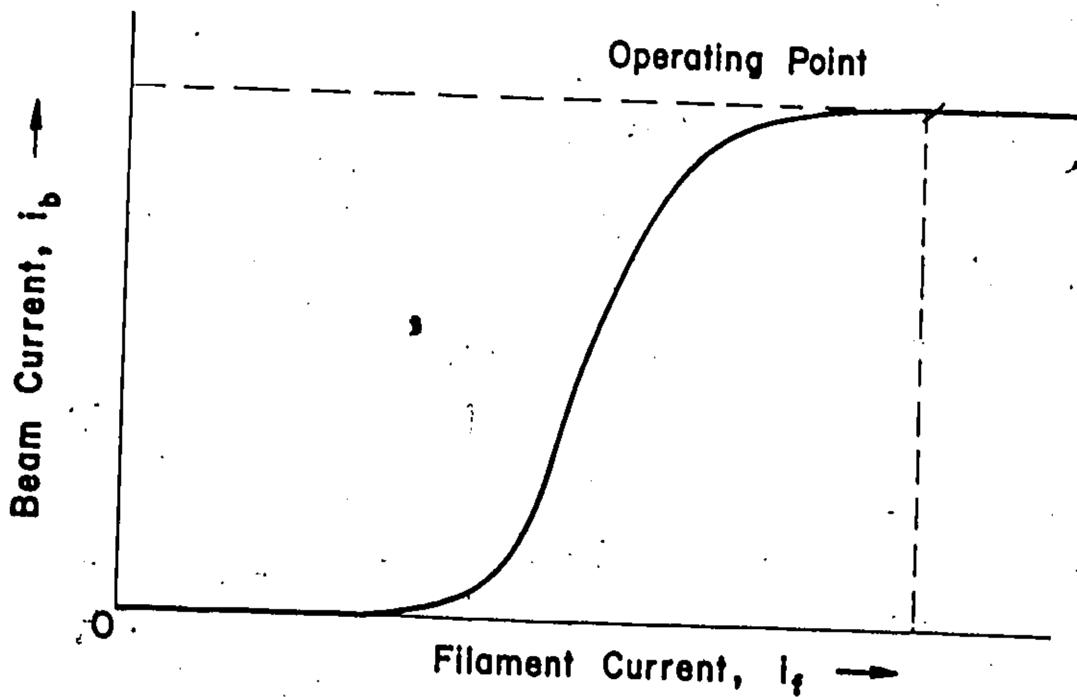


Figure 2.4 (a) Relationship of beam current and brightness to applied bias voltage. [4]
(b) Emission characteristic of self-biased electron gun.

point for emission purposes. Since LaB_6 cannot support high currents as tungsten can, the rod must be indirectly heated with a tungsten heater-coil wrapped around it. A long operating life, several orders of magnitude greater than that of tungsten, is another advantageous feature of the LaB_6 source, along with high brightness, making it attractive for lithographic applications.

A third electron source is based on the field emission gun, which uses a high electric field to force the electrons from a small (200 to 2000 Å) tungsten tip. A dual anode configuration is used to obtain and focus the electrons. This source is very attractive for beam sizes under 300 Å, but otherwise it has many problems which rule out its use in replacing conventional thermionic sources. Extremely high vacuums of 10^{-10} torr are required, and the fragile cathode tips are relatively unstable under normal operating conditions, making this type of source unsuitable for E-beam lithography applications.

One or two condenser lenses usually follow the electron gun which serve to demagnify the 25 to 100μm source, and also determine the beam current reaching the sample. The final or objective lens is used to determine the final beam size and hence the focus. The schematic of an axially symmetric electromagnetic lens is shown in Figure 2.5 (a), and part (b) illustrates the relationship of the components of magnetic field intensity to the axial distance through the lens. A focussing action occurs on an electron moving through the lens due to its interaction with the magnetic field set up by the coil. The force exerted on the moving electron is given by the vector relationship [4]

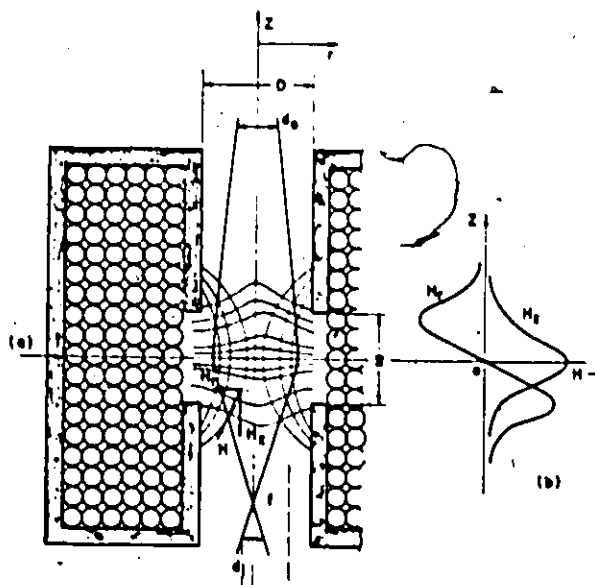


Figure 2.5 (a) Schematic of axially symmetric electromagnetic lens. [4]

(b) Components of magnetic field intensity vs. axial distance. [4]

$$\overline{F} = -e(\overline{v} \times \overline{B}) \qquad N \tag{2.6}$$

where e = electronic charge, 1.602×10^{-19} C

$\overline{v}$ = velocity of electrons (vector) in m/sec.

$\overline{H}$ = magnetic field intensity vector in A/m

X denotes the vector cross product

The lens is constructed with a gap S which separates the north and south pole pieces of the lens, and a bore diameter D which allows entry of the diverging beam from the previous crossover point. The magnetic field lines are shown in Figure 2.5 (a) along with the corresponding equipotential lines, and the demagnification from d_o to d_i is illustrated and can be verified by applying (2.6) to each electron trajectory. The intensity of the magnetic field is directly proportional to NI, where N is the number of turns in the solenoid and I is the current flowing through the lens. Therefore the focus point can be changed by varying the lens current, since the focus is inversely proportional to the magnetic field intensity.

Figure 2.6 illustrates schematically the inter-relationship of the objective lens with the preceding condenser lens. The demagnification factor M for the condenser lens is defined as S_o/S_i, where S_o is the distance from the previous crossover point to the lens gap, and S_i is the variable distance out to the focus point. The image size is given by $d_i = d_o/M$, and the resulting divergence angle is given by $\alpha_i = M\alpha_o$. A similar demagnification occurs for the objective lens with $M = S/S'$.

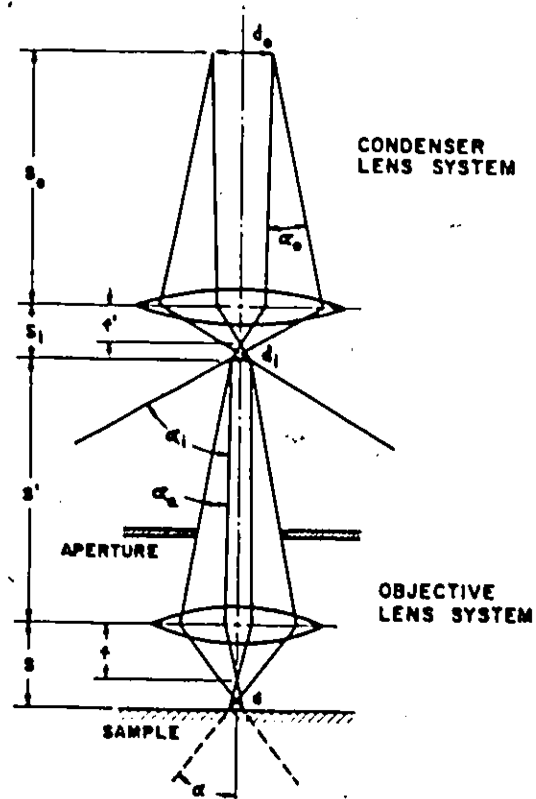


Figure 2.6 Ray trace representation of final spot formation. [4]

By increasing the current to the condenser lens, the focal point distance f' shortens, resulting in a broadening of the divergence angle α_i. Since the beam limiting aperture size is fixed, the effect of decreasing the condenser lens focal length is to decrease the beam current. Any change in current to the objective lens results in a direct control of the beam spot size and focus. The distance from the bottom pole piece of the objective lens to the sample surface (under focussed conditions) is termed the working distance, and usually varies from 5 to 25mm to allow samples to be scanned outside the magnetic field range of the lens.

The bore of the objective lens is usually made large enough for a pair of scanning coils to fit inside, which are used to deflect the electron beam over the sample in a predetermined fashion. Post-lens deflection coils also exist for specialized purposes, and in general, there exist a great variety of deflection configurations and techniques. The final scanned spot size is directly related to the beam current, which can be expressed as [5]

$$i_o = \left[\frac{\pi d^2}{4}\right] \frac{eE_o}{kT} J_c \alpha^2 \qquad (2.7)$$

where d = Gaussian spot size

e = electronic charge

E_o = accelerating potential in V

k = Boltzmann constant

T = cathode temperature in °K

J_c = cathode emission density in A/cm^2

α = semi-angular aperture

As with all lens systems, the electron column has certain aberrations associated with it, along with diffraction effects. These aberrations have the effect of increasing the final minimum spot size from its theoretical value, and also introduce distortion when scanning over a sample. The resulting final beam diameter can be expressed as [5]

$$d_f = \sqrt{\left[d^2 + d_s^2 + d_d^2 + d_c^2\right]} \quad \mathring{A} \tag{2.8}$$

where $d_s = \frac{1}{2} C_s \alpha^3$

$d_d = 1.22\lambda/\alpha$ diffraction disk of confusion

$d_c = C_c \alpha$

α = divergence angle at image plane in radians

λ = electron wavelength = $\frac{12.26}{E_o^{1/2}}$ $\mathring{A}$

The terms C_s and C_c respectively represent the spherical and chromatic aberration coefficients of the magnetic lens, and are usually expressed in cm. The lower these coefficient values are, the better the quality of the lens. In order to obtain the maximum beam current for a given beam diameter, (2.7) and (2.8) can be combined to yield the optimum aperture for obtaining this condition, which can be expressed as

$$\alpha_{opt} = \left(\frac{d_f}{C_s}\right)^{1/3} \text{ radians} \tag{2.9}$$

with d_s (optimum) = $d_f/2$

The relationship of final beam diameter to current under optimum aperture conditions is illustrated in Figure 2.7 [4] for both tungsten and LaB_6. Since the value of α is much smaller for an electron optical lens than for any light microscope lens, the resulting depth of field is improved by a factor of up to 100x for the SEM. This factor becomes important in E-beam lithography systems when dealing with non-flat substrate surfaces.

When an electron beam impinges on a sample surface, a number of electron/material interactions can take place, some of which are illustrated in Figure 2.8 [6]. For the purposes of E-beam lithography, only the back-scattered and absorbed electron interactions will be considered in this thesis. For standard SEM imaging, the back-scattered electrons are detected and the resulting signal is processed to yield an image of the sample. The most popular type of detector used to collect the back-scattered and secondary electrons is the scintillator-photomultiplier type, commonly referred to as an Everhart - Thornley detector. This type of detector relies on a scintillation material which emits light when struck with high-energy electrons. The light is then guided by a light pipe to a photomultiplier which greatly amplifies the incident energy and produces an output signal proportional to the number of collected electrons. The scintillator is usually biased with a high positive voltage as depicted in Figure 2.9, to allow efficient collection of the low-energy secondary electrons. A Faraday cage, with a low bias applied to it, is incorporated around the scintillator to prevent interaction between the incident electron beam and the high scintillator bias potential.

The output of the photomultiplier is processed with a video amplifier which in turn drives a high resolution CRT. The scan generaton

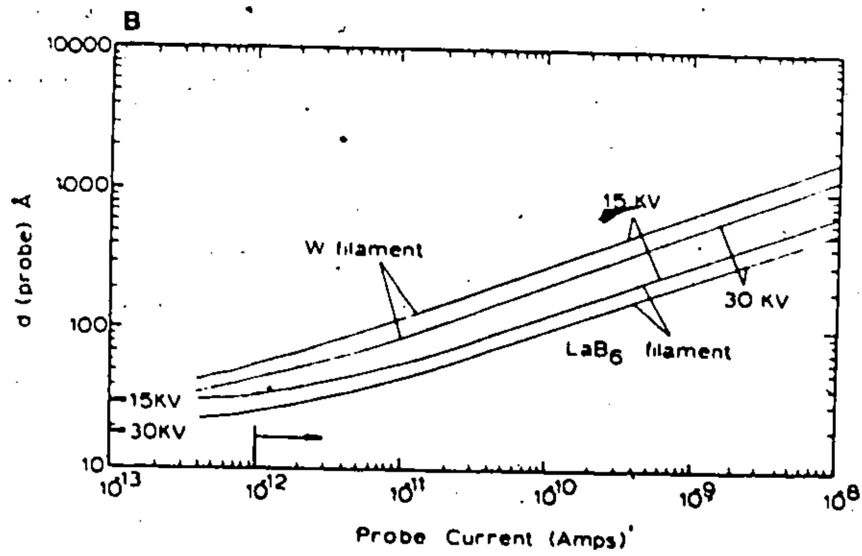


Figure 2.7 Final electron beam current to beam diameter relationship. [4]

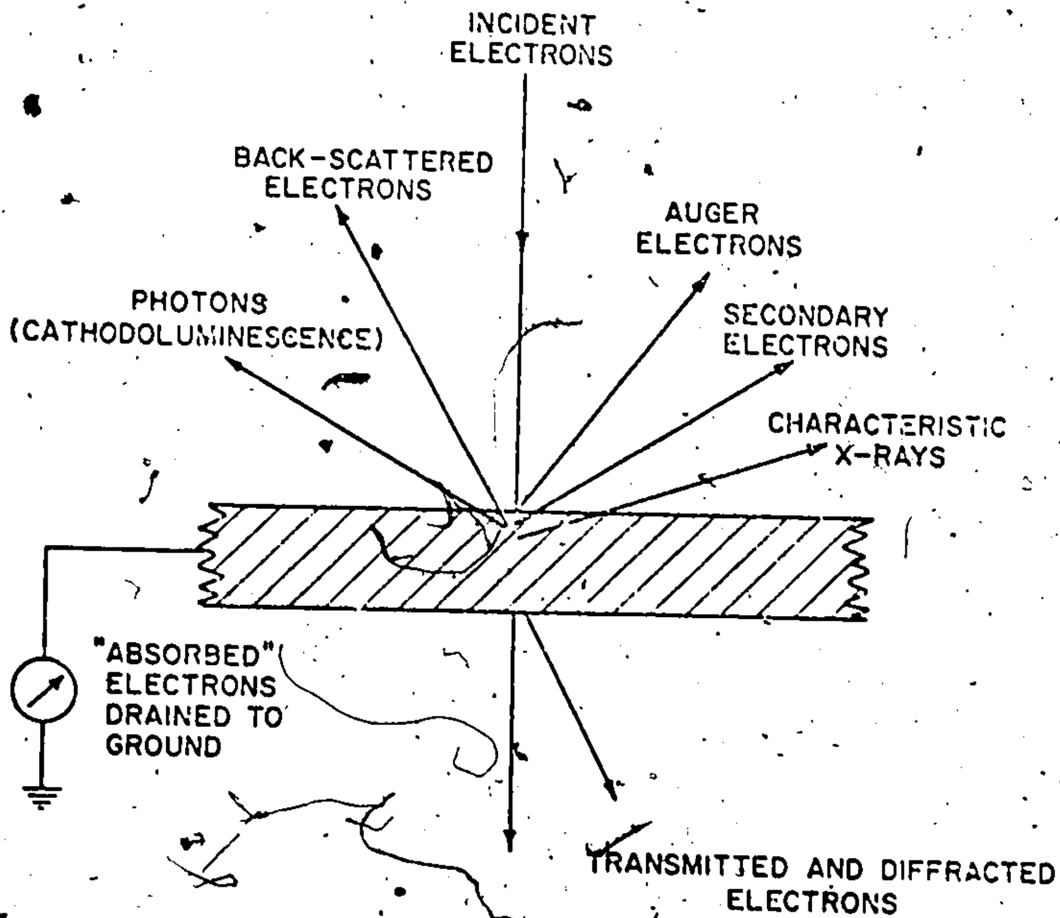


Figure 2.8 Electron beam interactions with the sample in a SEM. [6]

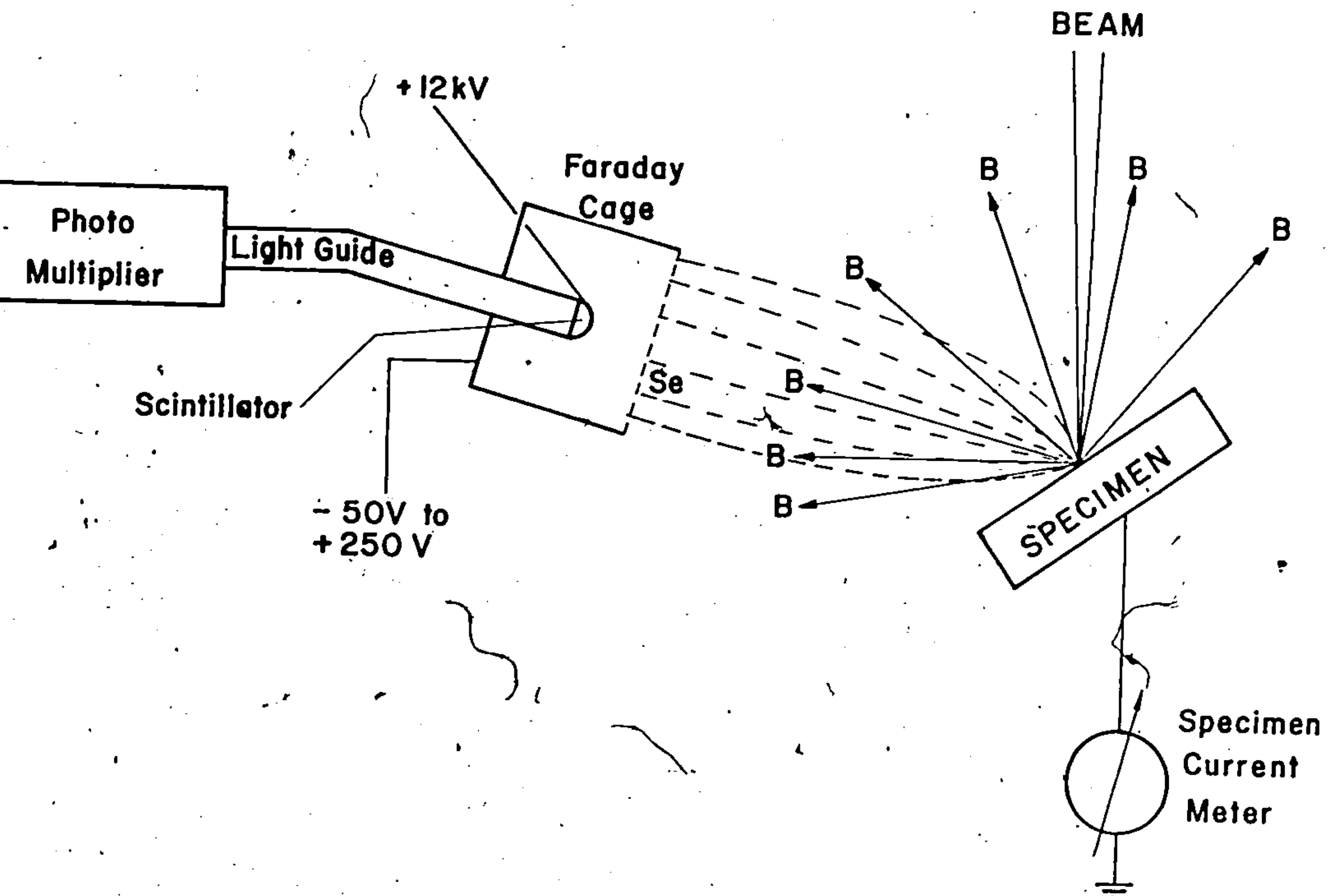


Figure 2.9 Detection schemes for backscattered (B), secondary (Se) and absorbed electrons. [6]

drives both the E-beam deflection coils and the CRT spot synchronously, while the output of the Everhart - Thornley detector is used to modulate the intensity of the CRT display, thus creating an image of the scanned area on the sample surface. Also shown in Figure 2.9 is a specimen current meter which monitors the level of absorbed electrons in the sample. This can also be used to modulate the CRT display for certain applications, however, for E-beam lithography the specimen current reading is used primarily to give an indication of the electron beam current magnitude.

The SEM mode of operation in an E-beam system is important for lithography applications since the substrate must be aligned to the scan field for proper orientation and dimensional correspondence. The backscattered electron signal is used in the alignment procedure, and aside from the resultant CRT display, a Y-modulated oscilloscope trace is useful in displaying the position-dependent intensity of the detected signal for each line scan. The signal displayed on the oscilloscope is useful for implementation in computerized or automated alignment systems for lithography machines. Normally the electron beam is scanned in raster fashion over the required square area on the sample in the SEM mode. Since most lithography systems incorporate computer control of a digital scan generator, the electron beam no longer has to adhere to a raster scan format. This allows total flexibility in the method of alignment in the SEM mode, and also for the method of pattern generation in the lithography mode. One basic addition to the standard SEM for lithographic purposes is a beam blanking mechanism, to allow the beam to be turned on and off without upsetting the electron gun stability. Most lithography systems employ either an electromagnetic coil or electrostatic plates, somewhere

between the electron gun and the first or second condenser lens, which, when energized, will force the beam quickly off its axis.

The basic purpose of a SEM is to produce an undistorted magnified image of a sample's surface, with ultimate attainable resolutions well below the 1μm level. The basic purpose of an E-beam lithography system is to produce undistorted circuit features onto a resist-covered sample, with ultimate resolution also well below the 1μm level. It is evident that the two afore-mentioned systems have similar goals, which makes the SEM application to lithography a feasible venture, as long as certain design differences are appreciated and accounted for [17].

2.4 State of the Art Systems

Many E-beam lithographic systems have been built to date, as illustrated by the examples given in Table 1.1. Some of these systems have been developed around a commercially available SEM, with minor modifications made, [7]-[9], while others have been designed from the ground up as specialized lithography machines only [10], [11], [15].

The simplest configuration for a pattern generator, which the author has come across in the literature, consists of a paper tape reader/translator developed by Dix [12]. A schematic of the pattern generator is given in Figure 2.10. A paper tape reader is the main source of pattern data input to the controller, which is hardwired to detect and execute instructions according to a fixed coding scheme. The generator is basically set up to scan rectangles of various sizes, oriented with sides parallel to the X and Y axes only, and defined by four coordinates.

X, Y - centre of rectangle, 10 bits each

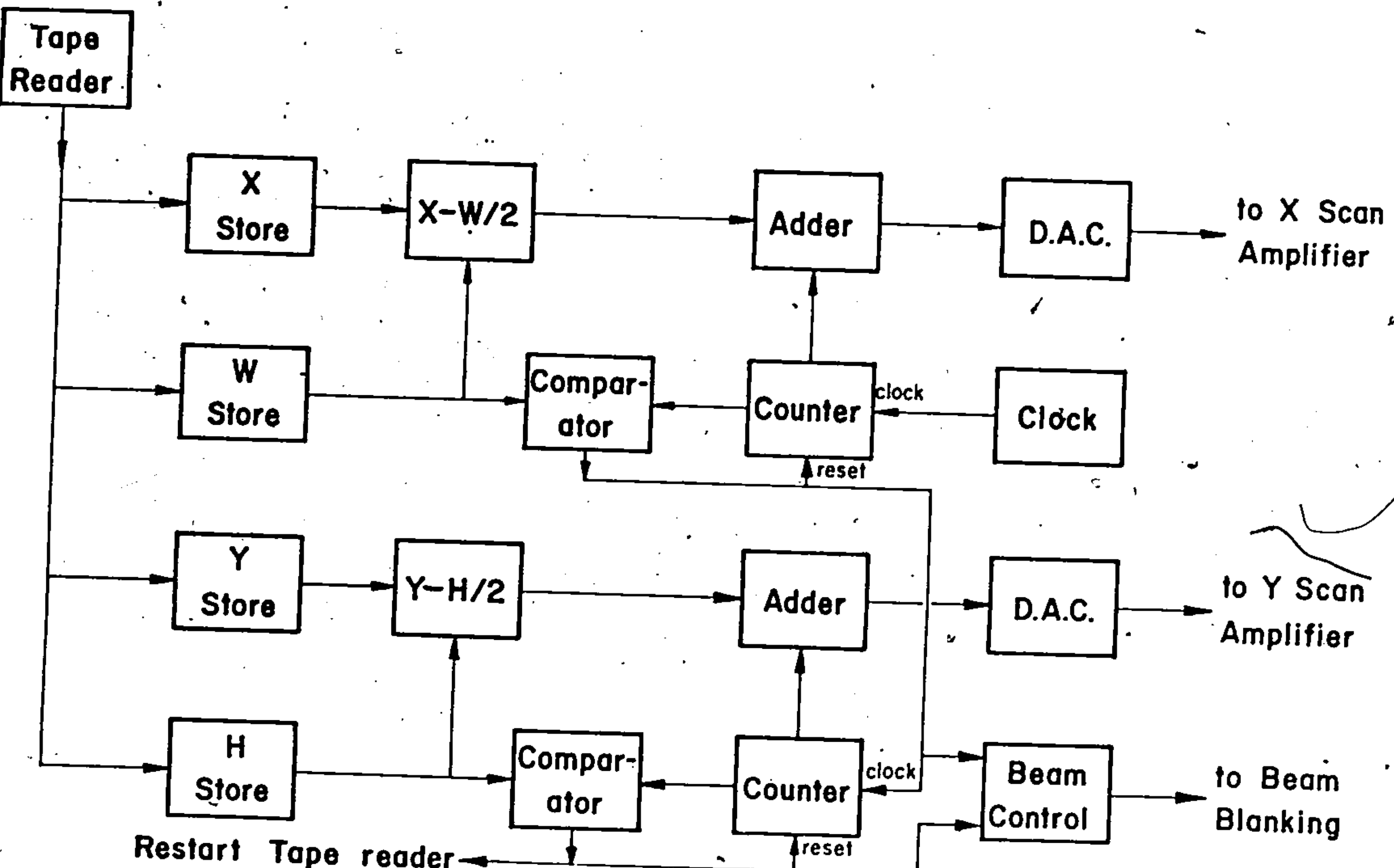


Figure 2.10 Block diagram of simplified pattern generator. [12]

W, H - width and height of rectangle, 8 bits each

The data format on the paper tape is similar to a numerical control format, and eight bytes (8 bits long) of punched data are needed to define each rectangle, which are read by the reader in 16ms. This slow rate of data input limits the ultimate writing speed of the pattern generator. The best resolution obtained with the system's 10 bit digital-to-analog (D/A) converters was 0.5μm, over a 100μm x 100μm field of view. No reference is given as to how the source data is generated, since the pattern generator only reads-in prepared tapes and has no memory or software control of any kind. Facilities for the variable control of the D/A clock rate, while scanning, as well as alignment procedures, are not available.

Wolf et al. [12] have implemented a unique pattern generator design which incorporates both digital and analog drive circuitry, as illustrated in Figure 2.11. The digital point-by-point exposures are reserved for all high resolution sections of a pattern, while the analog ramp generators are used for the low resolution or fill-in sections. This technique is designed to minimize the performance required of the individual pattern generator components for a given overall level of system performance. It was also designed to maximize the throughput rate, an important consideration for mass production applications only. The system incorporates facilities for varying the scanning speed, and also for making small adjustments to the X and Y gains, as well as a rotation control for alignment purposes. The digital scanning section handles linewidths in the 0.1 - 0.4μm range while the analog section covers the 0.4 - 1.0μm range. Although large area rectangles are scanned by the analog section,

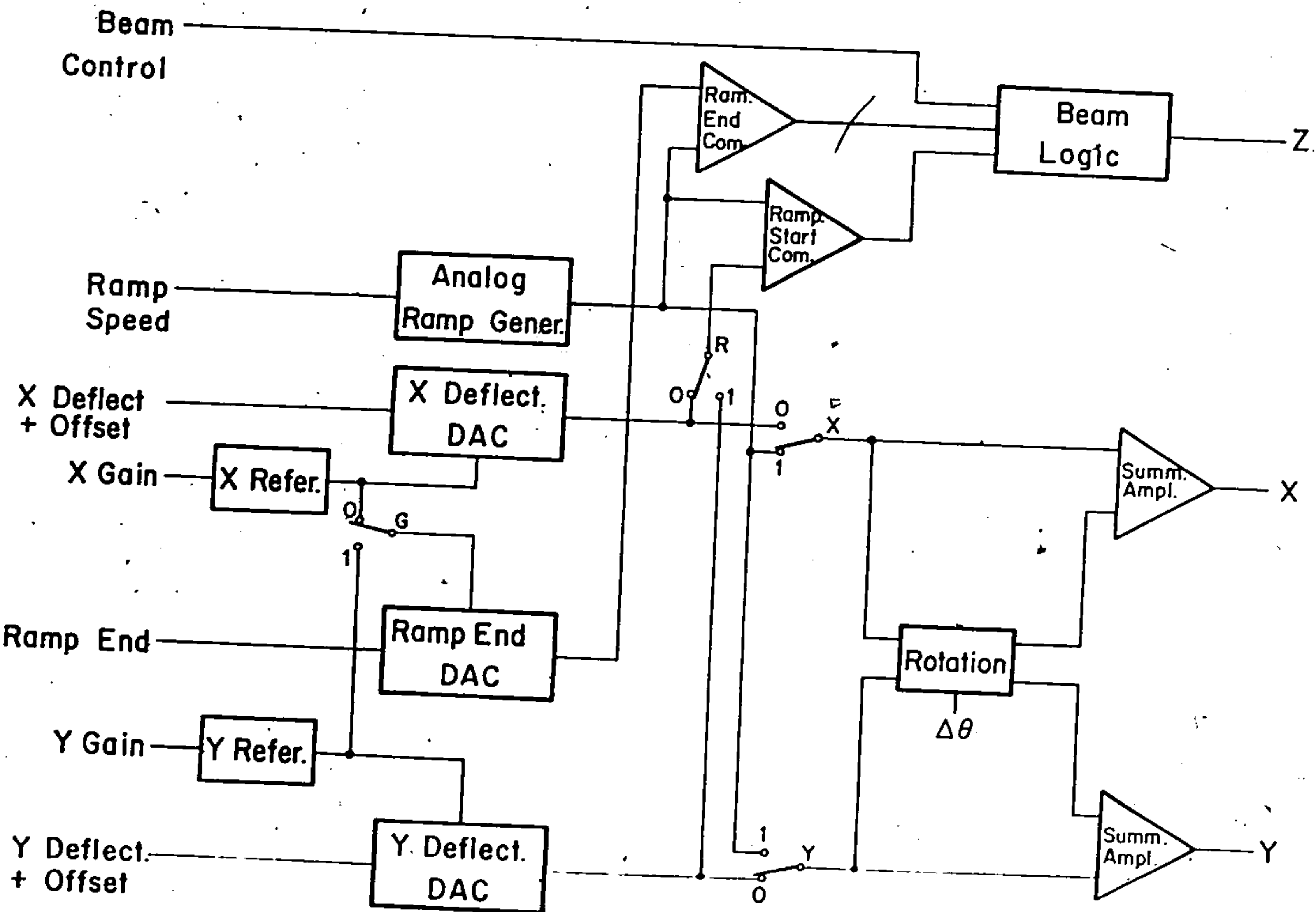


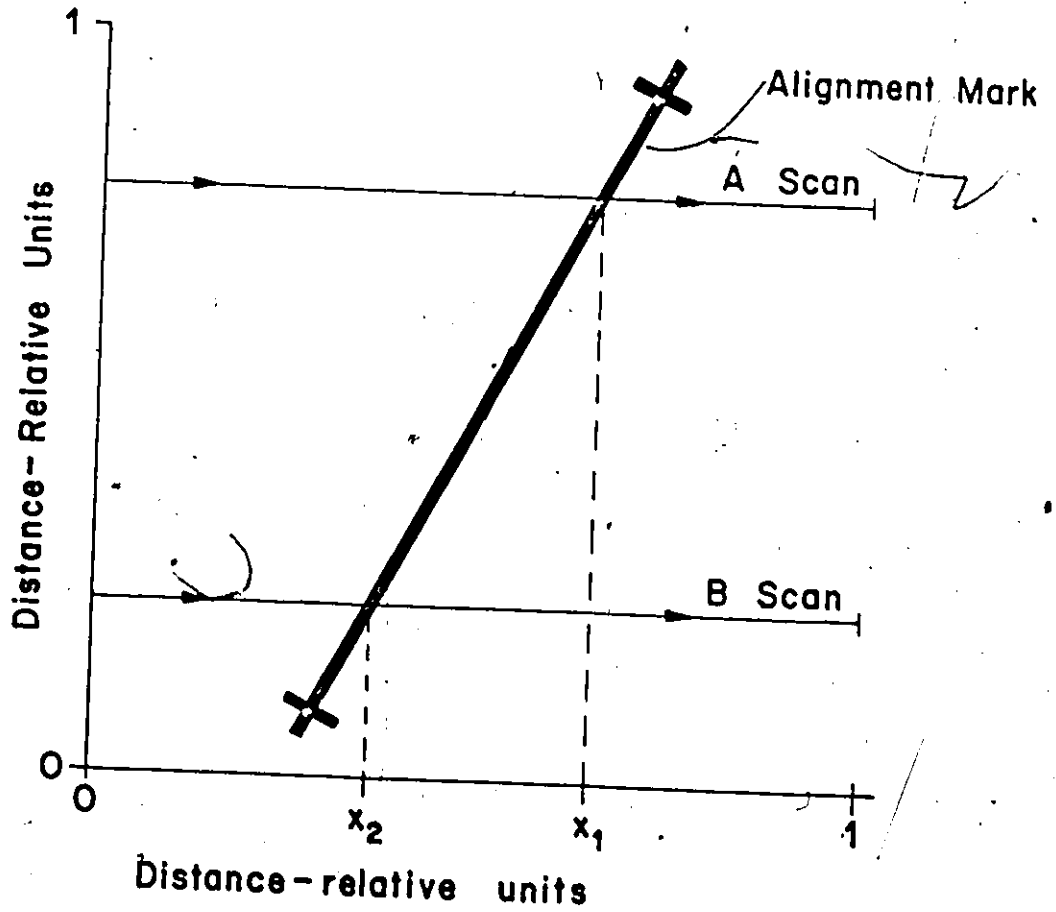
Figure 2.11 Block diagram of analog/digital pattern generator. [12]

the perimeters are defined by the D/A converters to retain pattern accuracy. A writing speed of 1cm^2/100 seconds is claimed, working with a 1μm (i.e. all analog scan) linewidth. The form of the data input to the pattern generator is not mentioned, and neither is the extent of software support needed to generate and sort out pattern data to the appropriate section in the pattern generator.

Extensive software control is used by Wolf [13] and others, [9], [14], [15], to automatically align the substrate to the scan field of the E-beam system. In most cases, the scan field is defined on the substrate surface with previously-fabricated registration marks, usually consisting of some form of cross-hairs marking the four corners of the desired field. The registration mark is made from a high molecular weight material (higher than the substrate), such that more backscattered electrons are generated when the electron beam impinges on the mark. In the SEM mode, the system can easily detect the location of these registration marks due to the high signal levels caused on the Y-modulated oscilloscope line-scan trace. The computer systematically controls the electron beam such that it scans back and forth across these registration marks only, with short scans, and each time the detected analog signal is converted to digital (A/D conversion). At this point a comparison is made with a pre-determined value and a corresponding decision and action results. The action may consist of increasing the pattern generator gain, moving the scan field a small X or Y distance, or rotating the scan field slightly, depending on the purpose of the particular alignment scan. In order for the computer to execute these corrections, many control functions must be specially interfaced to allow digital control, (eg. stepping motors on the

stage controls). An illustration of a rotational correction procedure is given in Figure 2.12 by Wolf [7]. Two consecutive line scans are made across the top and bottom of a rotationally-misaligned benchmark. When the A scan reaches the benchmark, the resulting high backscatter signal is recognized by some hardware and is used to indicate the distance x_1 to the computer. A similar process occurs for the B scan and the two distances are compared, and a correction signal is sent to the rotation control, until further test scans yield equal distances.

To date, one of the most sophisticated E-beam lithography systems is the IBM vector scan machine, [10]. The overall system is depicted in Figure 2.13. The field size can range up to 4mm square with a deflection resolution of 14 bits per axis. A LaB_6 gun is used, along with a minimum spot size of 500 Å for microfabrication. A powerful minicomputer with substantial peripheral support is used to control the various system functions, including the initial pattern data preparation. Among the various computerized functions are control of the pattern generator, the scan rate clock, the field offset positon, the rotation and orthogonality of the field, the automatic registration circuitry, the video processing of the detector, and finally, the worktable monitor and control. For accurate monitoring and control of the worktable, laser interferometers are utilized because of their high accuracy. Quality stepping motors and drive systems are used to move the worktable for initial positioning and subsequent changing of scan fields on the substrate. Fine shift or rotation adjustments are made electronically, and the typical combined monitor/control registration accuracy is 1000 Å. Equally as complex and sophisticated as the hardware control system, is the computer software, which is



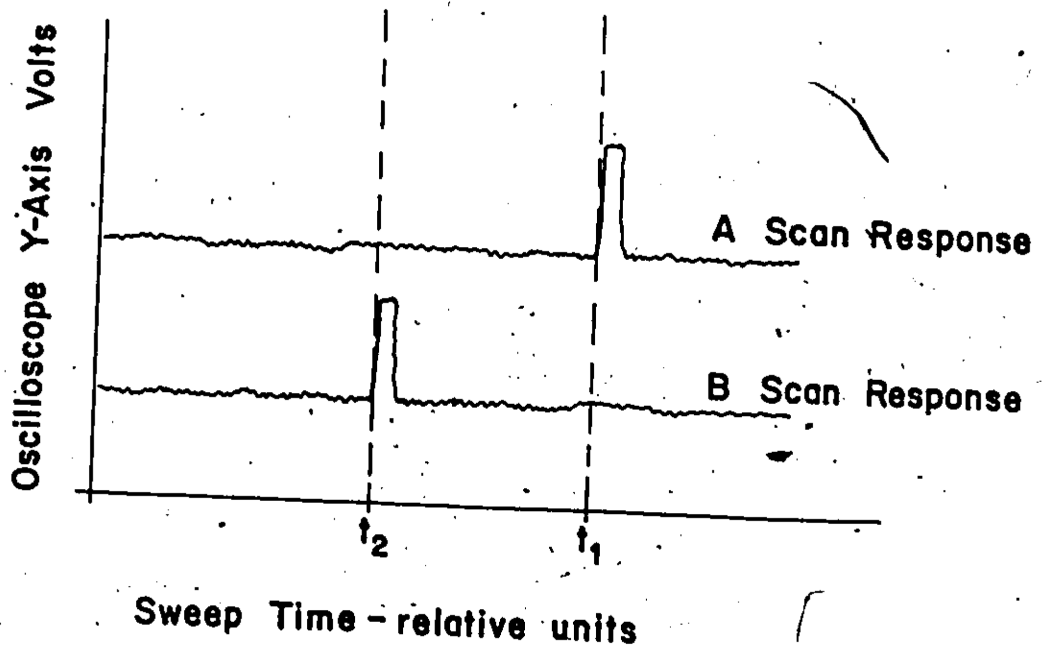


Figure 2.12 Rotational alignment procedure.

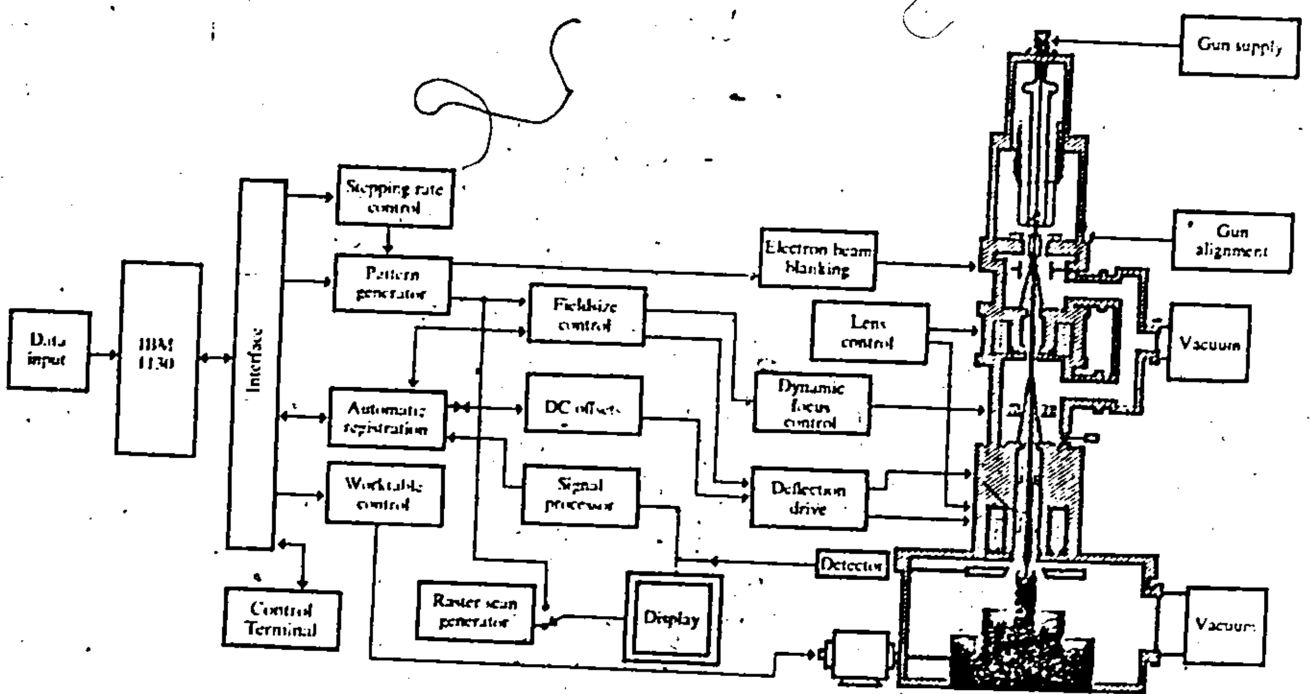


Figure 2.13 IBM computer-controlled E-beam microfabrication system: [10]

needed to effectively control and combine the various operations into a workable and successful technique.

The latest additon to this IBM lithography system is a new pattern generator by Patlach et al. [16]. The impetus for designing this new version was to achieve data compaction, since enormous amounts of memory space were being used previously to define complex masks in the 16K x 16K scan field. It was also desired to minimize the update time of the pattern generator, since this process interfered with the computer's monitoring and control functions. The resulting system is illustrated in Figure 2.14. The data compaction has been achieved by appropriate coding of the data words sent to the pattern generator, and by incorporating the various shape routines into hardware as part of the generator electronics. This technique saves computation time and storage requirements only while the pattern is being generated. Substantial computation is needed when the original data points are being analyzed, coded, and stored for future re-call by the E-beam writing program. Data transfer time to the pattern generator is minimized by incorporation of a cache memory, which is periodically updated with data from core storage by means of a direct memory access channel, making the transfer transparent to the monitor and control routine. A word sorter takes care of decoding the various control and data words, and directs them to the appropriate sections of the pattern generator. A special control word is used to specify the 'shape' store and scan sections. Once a specific shape has been stored and scanned, only the differences of the next shape need be entered if the shapes are similar. For example, if the counting and shape registers have been previously initialized to scan a rectangle, and the next required shape is

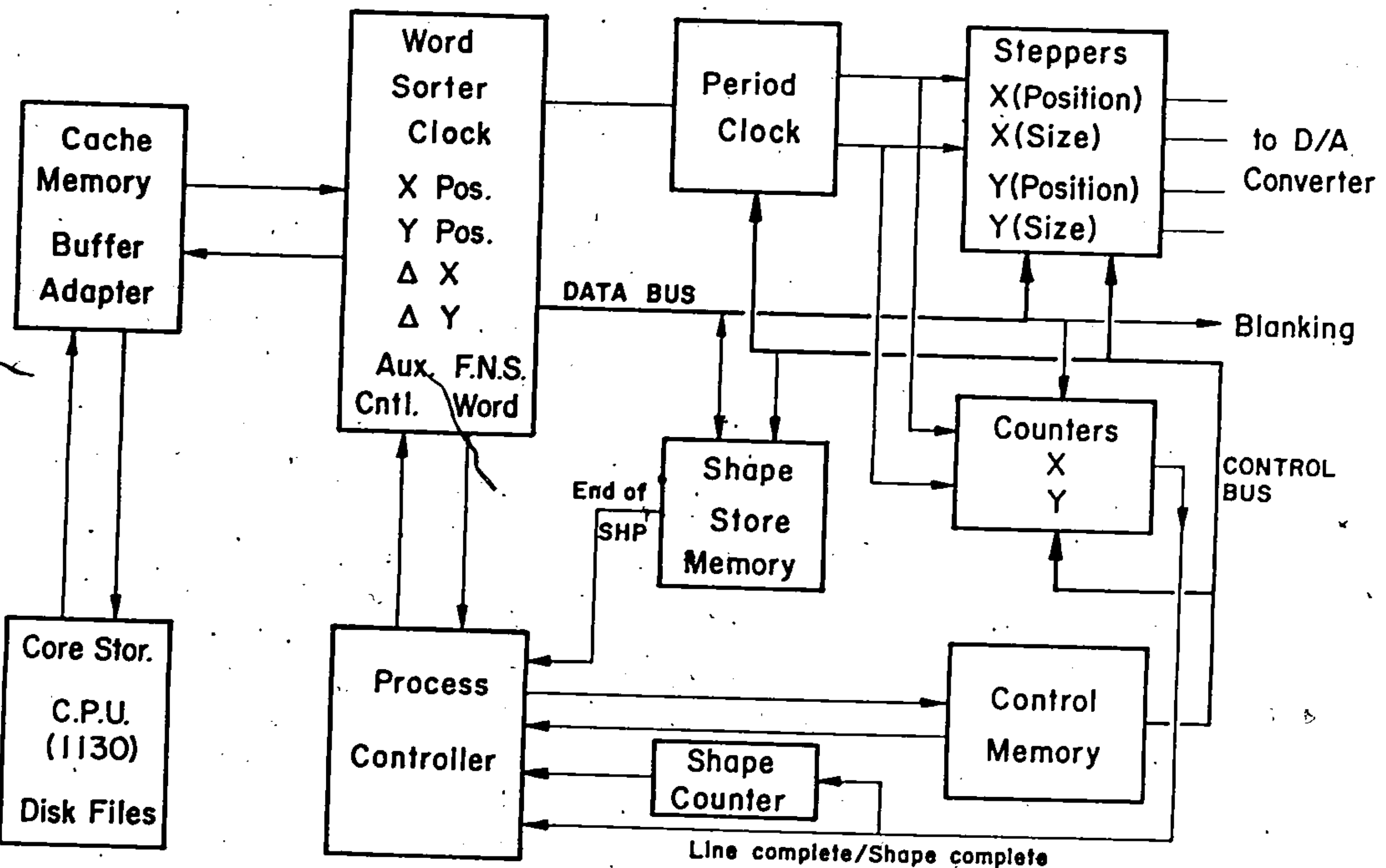


Figure 2.14 Schematic of IBM hardwired pattern generator. [16]

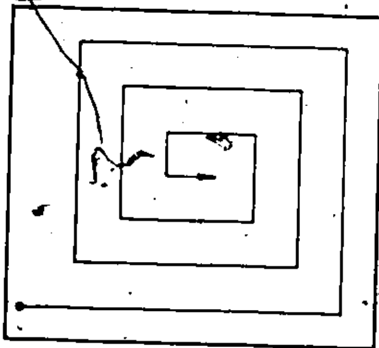
also a rectangle with a larger width, then the only data which need be transmitted to the pattern generator are the new X and Y reference coordinates and the new rectangle width.

The variety of shapes and scan techniques which have been incorporated into the pattern generator are depicted in Figure 2.15. The number of microcode steps needed to initialize and scan these figures ranges from 17 instructions for the flyback raster to 39 for the triangle scan. Aside from the usual repertoire of regular-sided shapes, the pattern generator features a shape memory which can store pattern data for odd shapes, one shape at a time.

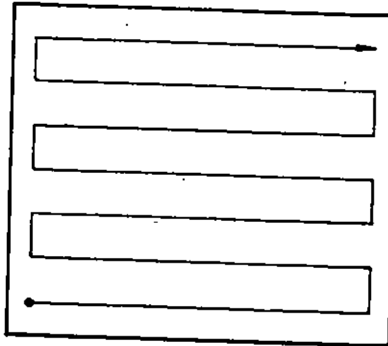
There is no doubt that the system just discussed is extremely sophisticated, and has been designed with the goal to maximize throughput in the most efficient manner. However, the author feels that it is important to point out several drawbacks to the afore-mentioned system. The pattern generator is hardwired, which implies that the code formats, shape menus, and scan techniques must remain fixed, and cannot be easily modified without physical wiring changes being made to the generator electronics. Furthermore, the small improvement in throughput is offset by the expense and complexity of the pattern generator design, which consists of over 800 integrated circuit dual in-line packages on fourteen wire-wrapped circuit cards.

2.5 Conclusions

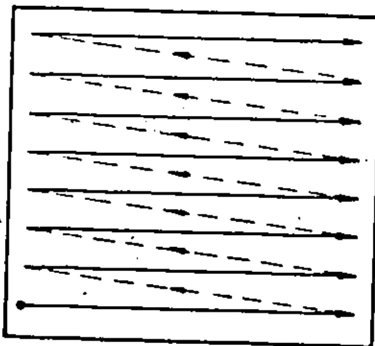
The basic process of lithography has been described, illustrating its purpose and subsequent processing steps. Various methods of high resolution ($\leq 2\mu m$) lithography were reviewed, and the results of this



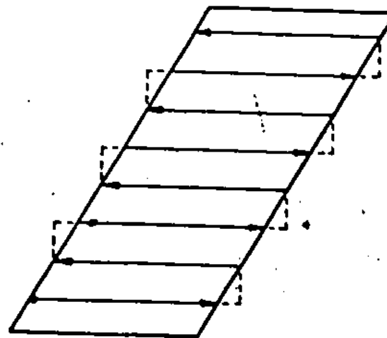
Spiralled Rectangle



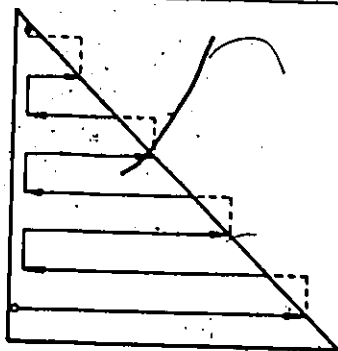
Right/Left Rastered Rectangle



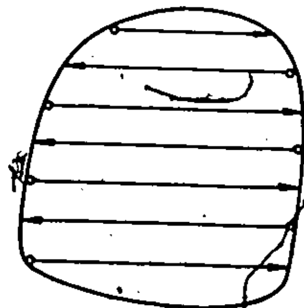
Flyback Rastered Rectangle



Parallelograms



Triangles



Shape Store

Figure 2.15 Shape menu, with dotted lines indicating beam traverse with beam blanked. [16]

particular study make it evident that E-beam lithography is the only practical contender for flexible sub-micron pattern definition in the near future. X-ray techniques will most likely dominate the mass production aspect of sub-micron circuits, however, the required X-ray masks will still have to be E-beam generated.

The basic operating principles of a SEM were covered, in order that appreciation could be gained for the interdependence of certain SEM components and operating procedures with the ultimate pattern size, resolution, and accuracy attainable. Finally, various electron lithographic systems were discussed, including the simple designs as well as the state of the art systems. The striving for more sophistication in pattern generation schemes is primarily motivated by the demand for higher system throughput. It is generally agreed by the semiconductor industry, that in order for the large investment in an E-beam lithographic facility to be economically feasible, a four inch wafer must be processed in 6 minutes (one level mask). This speed has not yet been attained, and the author feels that the intensive research being carried out to meet this specification is overshadowing the needs and desires of the single-device, one of a kind, research and production facilities.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF LITHOGRAPHY SYSTEM

3.1 Introduction

This chapter deals with the design and construction of an E-beam lithography system, based primarily on a microprocessor-controlled pattern generator. The design objectives are discussed, along with the results of a feasibility study to determine the accuracy and applicability of the available SEM to electron lithography. After careful analysis of the desired objectives, the details of the pattern generator hardware and software are covered. This chapter concludes with a discussion of the integration of the pattern generator with the SEM, to form a complete functional system.

3.2 Design Objectives and Considerations

The first and most important consideration in designing a SEM lithography system is the characterization of the SEM's distortion, which will ultimately determine whether a particular SEM is suited for E-beam lithography or not. Features on the SEM such as beam blanking and external scan inputs are also necessary for lithographic applications; however, these features can be controlled or corrected more easily than a severely distorted scan field.

The SEM used for this work is a Cambridge Stereoscan Mark II A, which is owned and operated by the Materials Research facility at McMaster University. A simplified diagram of the column assembly is shown in

Figure 3.1. A tungsten filament is used in the electron gun, which features a continously variable high voltage potential range from 1-30 kV. Three pre-aligned condenser lenses are used, which have a combined worst-case stability of 65 ppm/5 minutes. The available working distance range in the specimen chamber is from 0 to 40 mm. The theoretical magnification range is from x10 to x200,000, with a maximum resolution of 200 Å. An Everhart - Thornley type detector is incorporated for the collection of both back-scattered and secondary electrons. The instrument is also equipped with an external input facility for the X and Y scan amplifiers, which drive a double deflection coil system, housed inside the bore of the final lens. A beam-blanking unit is also supplied, which utilizes an electromagnetic deflecting coil, situated between the electron gun and the first condenser lens. A specimen current meter is also available, which indicates the current through the specimen and stub to ground, due to the absorbed electrons from the incident beam.

There are several alternatives which a designer has when trying to characterize the distortion of a particular SEM without the aid of an accurate digital pattern generator to fabricate test patterns with. Smith [18] has applied moiré fringe techniques to the analysis of scan distortions in SEMs. This method requires the use of a high-accuracy linear grating as the specimen, which when viewed in the SEM with a periodic raster scan, produces a moiré fringe pattern on the display. The effectiveness of this technique is very dependent on how the resulting fringe patterns are interpreted, and also the absolute accuracy of the grating used. Chang [19] also uses a reference grating to characterize SEM distortion, but uses a 'stripe scan' method to display any static or

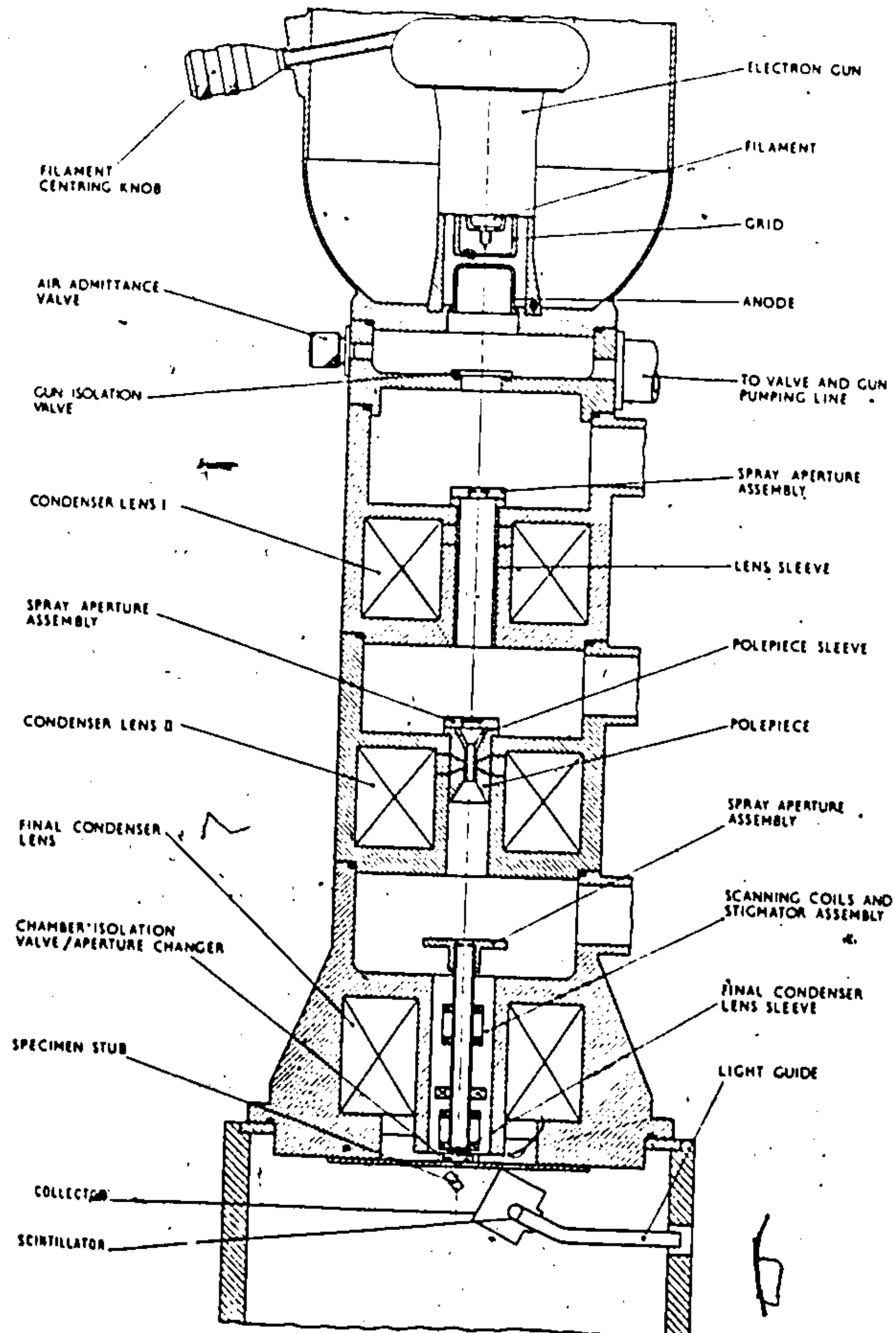


Figure 3.1 Schematic of Stereoscan Mark II A electron column. [5]

dynamic distortions directly on the CRT display. Each line of the grid is scanned its full length, but the width of each scan is only several microns on the surface of the grid. Any deviation of the long scan over a single grid line will readily appear on the display, available for recording, measurement, and subsequent analysis.

The previously discussed techniques are important when the source of the distortion must be characterized, and they also give a real-time measurement, as opposed to a method which involves post development of generated grid patterns, and subsequent optical microscope evaluation on interferometer-monitored workstages. For the application required in the author's work, it was not desired to find the cause of the distortion, but rather the amount of distortion present, since changes could not be made to the SEM's optical system. Considerable information is available on the distortion characteristics of the Mark II A column [3], [7], [20], [21]. Most of the techniques which were used in these studies involved sophisticated equipment and samples which were not available to the author. Hence, the results published in the literature were relied on and used in the design of the pattern generator and lithography system as a whole. An earlier feasibility study by the author [22] indicated good results over a small field of view of 100μm on the same SEM. Wolf et al. [7] have measured the errors in the Mark II A system, and have found an error of ~5 parts in 10^4 for a 1mm x 1mm scan field, along with a nonorthogonality error of 0.1°. DeVore [21] has devised a simple technique for studying deflection aberrations in SEMs, based on observing spot profiles exposed into an acrylic substrate at various distances away from the undeflected beam axis. Results based on this method are illus-

trated in Figure 3.2 for the Mark II A column, with an accelerating potential of 20.7 kV, 200μm final aperture size, working distance equal to 14mm, and a field size of 1.7mm x 1.7mm.

Based on the above collective results, it was decided by the author to aim for a 1mm x 1mm scan field in the design of the lithography system. Another important consideration in the system design is the throughput rate. Since the system will be used in a research environment, throughput is no longer an important factor, and many system component specifications can be relaxed as a result. Since only single or one of a kind devices are going to be scanned within a small area, there is no longer a need to monitor table movement, allowing the workstage to remain fixed during the scanning of a pattern. This latter constraint is perhaps the biggest factor responsible for the simplification and resultant low cost of the author's lithography system. The resultant accuracy of scanned patterns will be functions only of the initial registration accuracy and the SEM scan system.

Automatic registration is no longer necessary since only one or two registrations have to be made per device, and these can be easily implemented by the SEM operator, in less than a minute, for a well-designed system. Other operations which are normally under computer control such as beam current, focus, deflection centering, and electron gun centering, may all be operator-controlled quite effectively, avoiding system complexity and reducing the otherwise high cost. This operator-centered mode of operation is quite feasible for the proposed lithography system because scan times for devices will be relatively short (several minutes) which negates any effects due to long-term drift in the electronics.

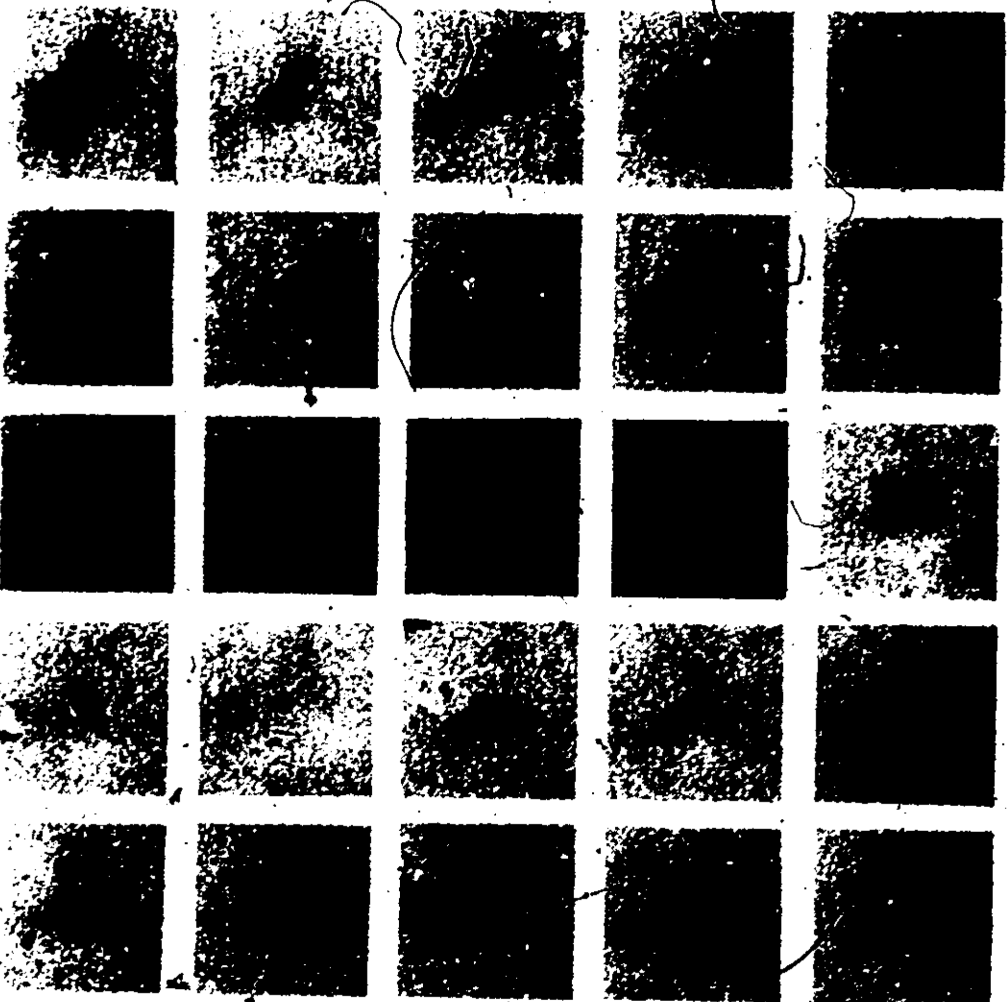


Figure 3.2 Spot Exposure Results for Stereoscan Mark II A by DeVore.

causing defocussing and changes in beam current and scan orientation.

The basic considerations for the pattern generator are accuracy, flexibility, and low cost. The accuracy of the pattern generator is strictly a function of the specifications of the D/A converters used, along with specifications of any post-amplification or attenuation circuitry for the analog output signals, including the often-overlooked power supplies. Synonymous with accuracy is the required resolution of the pattern generator, which is directly determined by the number of bits that the D/A converter resolves. The final positioning resolution in the scan field on the sample is also determined by the number of D/A bits, but in conjunction with the maximum linear dimension of the field size, which corresponds to the full-scale or reference value used for the D/A converters.

Pattern generator flexibility was achieved by incorporation of a microcomputer and a simple hardwired scanner design. The 'vector scan' approach was chosen because of its efficiency in scanning only those areas which need to be scanned, which total less than 50% of the entire scan field for the majority of devices. By keeping the scanner design simple and general, a variety of special purpose scan routines may be implemented at will, simply by changing the software program in the microcomputer. A further contribution to system flexibility and efficiency is the incorporation of an interactive keyboard and display, which can be used to enter pattern data in decimal coordinates, and thus generate an entire pattern program on-line.

The low cost consideration has been met by the use of a microcomputer with low memory requirements, as opposed to a fully-supported mini-

computer system. Pattern data storage is achieved by the use of cassette tapes, which offer an inexpensive and portable alternative to computer memory or bulky paper tape.

3.3 Pattern Generator Hardware

The pattern generator hardware consists of four basic system blocks:

(a) hardwired scanner
(b) microcomputer
(c) keyboard/display
(d) cassette storage

The hardwired scanner will be discussed first, since it performs the primary function of the pattern generator. The simplest configuration for a vector scan generator consists of specifying the start and stop coordinates of a line, and having the scanner draw a straight line between the two points with the beam on. The system becomes even more simplified if the line scans are restricted to the orthogonal X and Y directions, since no corrections have to be made for the linear scan speed, which must remain constant for all scans. The resulting scanner system is illustrated in block diagram form in Figure 3.3. Two binary counters are used to control the D/A converters, one each for the X and Y axes. Each channel (X and Y) has an input holding register, which serves to store the end or destination coordinate of a line scan, while the counter registers always contain the present or start coordinate of a scan. Control of the line scan is governed by a comparator for each channel, which compares the start coordinate in the counter register to

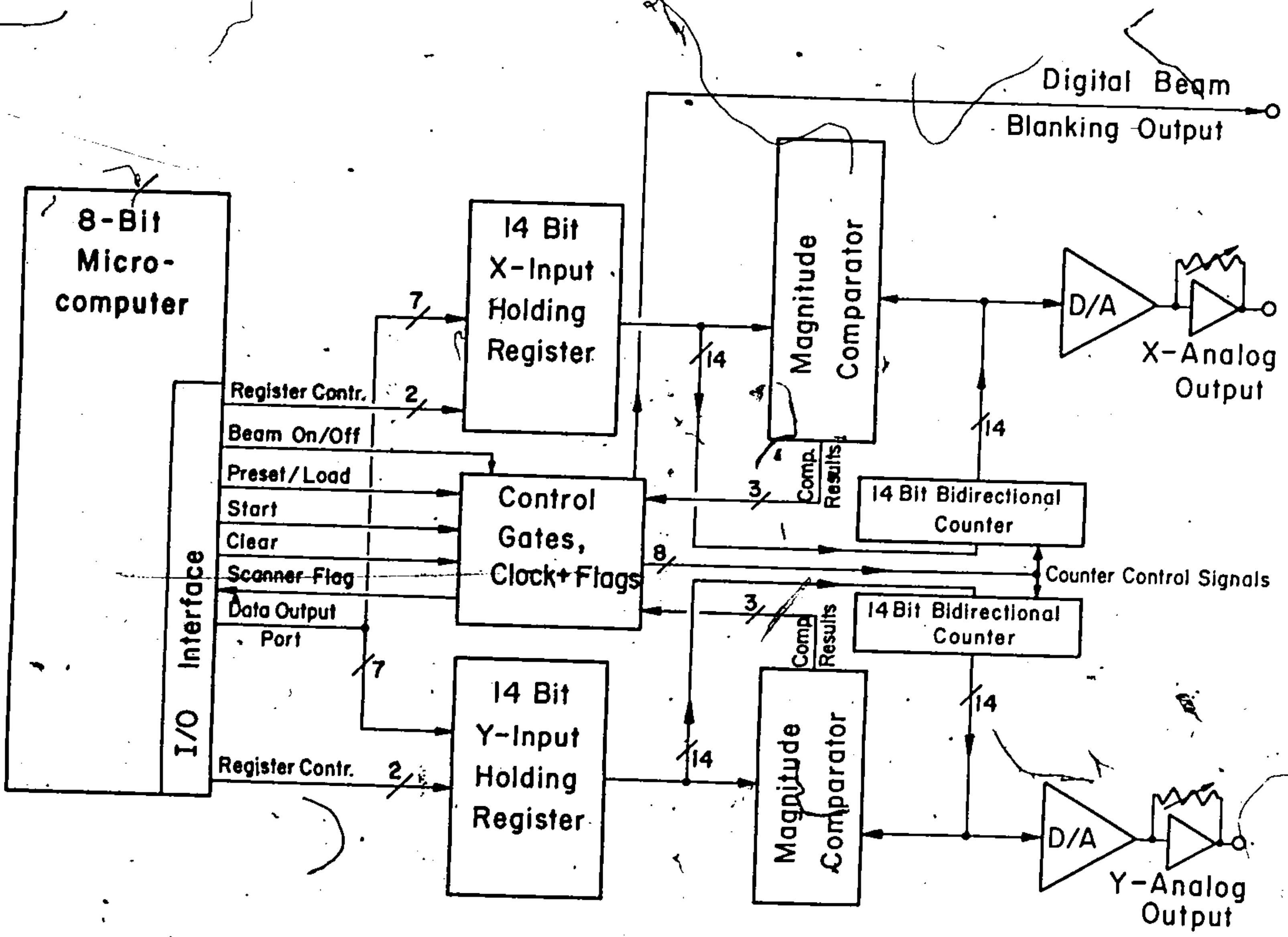


Figure 3.3 Schematic of simplified vector scan generator.

the destination coordinate in the holding register. If both values are equal, the clock circuitry is inhibited and the scanner is disabled; this occurs at the end of each line scan. If the values are not equal, the comparator determines which value is higher, and appropriately controls the counting direction (up or down) of the counter to ensure that the line scan is made in the proper direction. The extent of computer interfacing consists of the 8-bit output port and four control lines for loading the X and Y input registers, a master clear/reset line for initialization, a preset/load line, start scan signal, beam on/off control, and finally, a scanner flag status input to the microcomputer.

The preset/load line allows the scanner to be preset immediately to the destination coordinate without scanning. This feature is useful when long moves have to be made with the beam off. The beam on/off control merely sets a flag on the scanner board, whose status is used to control the beam-blanking circuitry upon receipt of a start signal. The start signal enables the clock to the counters, turns the beam on (dependent on beam status flag), and clears the scanner status flag to indicate to the microcomputer that the pattern generator is in the scan mode. Upon detection of a completed scan by the comparators, the clock is disabled, the beam is turned off, the beam flag is cleared, and the scanner flag is set to indicate that the scanner is ready for more data input. The various control features discussed above allow bidirectional scanning to take place in either the X or Y direction (one at a time) with the beam either on or off. Scanning to a coordinate point with the beam off is also possible, as well as 45° angle scans, if the clock rate is adjusted accordingly by a $1/\sqrt{2}$ factor to yield the required constant

scan speed.

The D/A converters are 14-bit R/2R resistance ladder discrete types, which can resolve one part in 16,384. Having chosen a 1mm x 1mm scan field, the resulting positional resolution is 625 Å/bit, such that 16 bits represent 1μm. This accuracy is on the order of one electron beam diameter during scanning of sub-micron linewidths, which is more than sufficient. Settling time of the converters was fast enough for the relatively slow clock rates which are used in the scanning process. Provision for scale alignment was made by incorporating variable gain amplifiers at the D/A converter outputs. Operational amplifiers with excellent temperature stability and low offset voltage specifications were used in conjunction with precision 10-turn potentiometers to implement the variable-gain amplifier. The X and Y analog outputs are then directed with a switch located on the front panel of the pattern generator, to either a set of connectors on the rear chassis for monitor purposes, or to the SEM via a shielded cable.

Figure 3.4 illustrates the completed scanner and amplifier circuitry on two 6x9 inch circuit cards. The scanner board (top) contains all the digital circuitry, including an internal clock, although provisions have been made for external clock sources as well. The amplifier board (bottom) contains the precision operational amplifier circuits for the X and Y analog outputs, and also an opto-isolator circuit for transforming the digital beam on/off signal into the required analog ±15 volt levels.

The microcomputer used in the pattern generator is a Digital MPS system, based on the 8-bit Intel 8008 central processing unit (CPU).

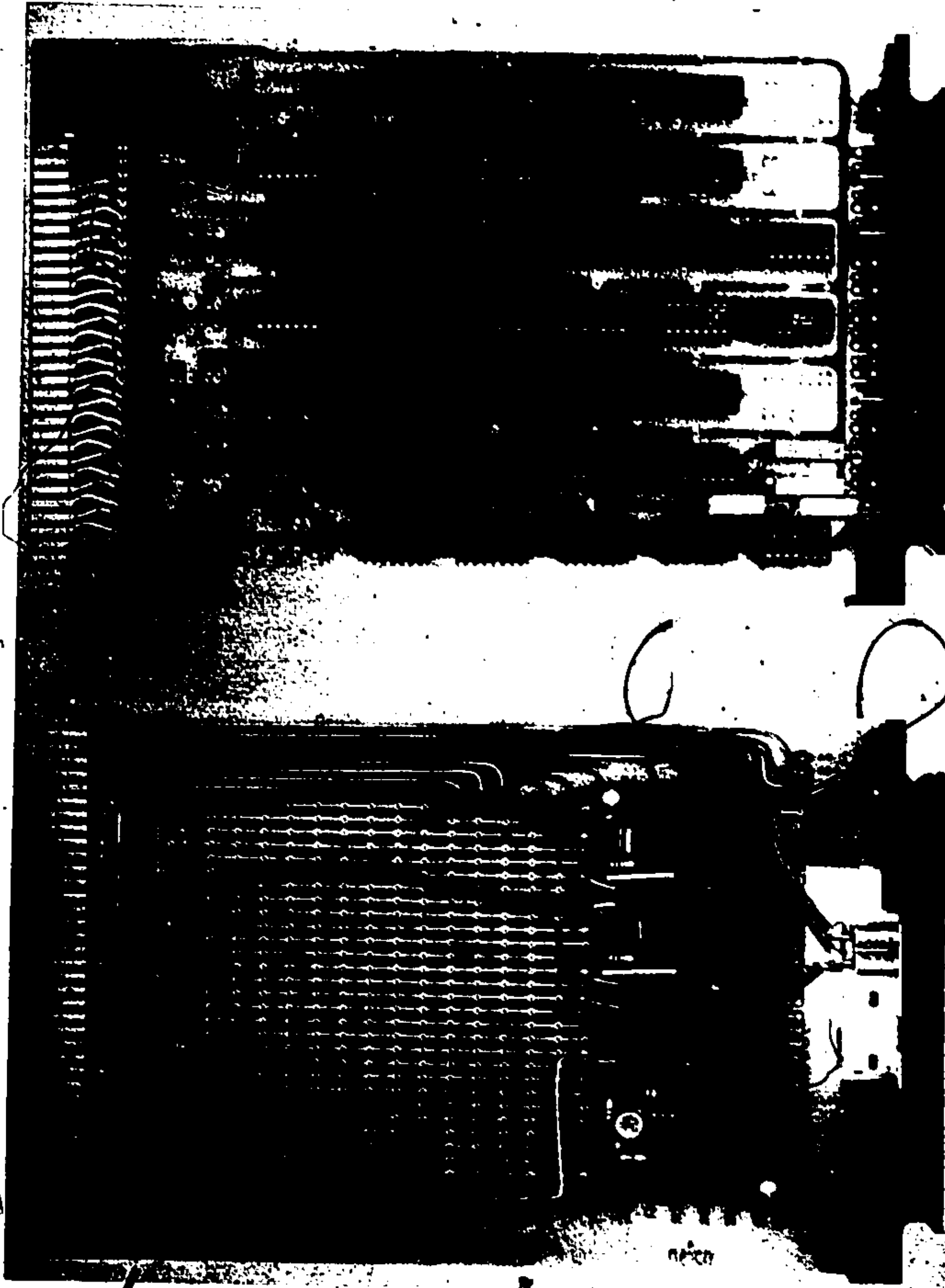
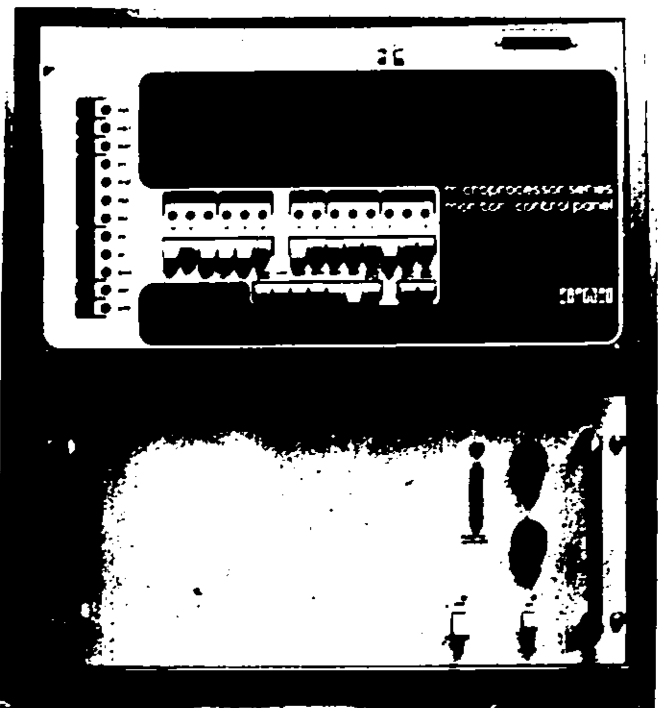


Figure 3.4 Photograph illustrating scan generator board (top) and amplifier and beam blanking board (below).

The microcomputer features 48 basic instructions with instruction times ranging from 12 to 44μsec, and includes 8 input and 24 output ports. The microcomputer system employed 2K (2048 bytes) random access memory (RAM) and 256 bytes of read only memory. The completed pattern generator is illustrated in Figure 3.5, showing both front and rear views, complete with all power supplies. The circuitry layout was designed taking into consideration such problems as ground loops, electrical interference, calibration, and ease of accessibility.

An interactive keyboard and display was designed in order to allow pattern data to be entered directly in the form of decimal coordinates. Seven-segment light-emitting diode (LED) displays are used to echo the keyboard data inputs, while single LED displays are used to indicate an X, Y, or beam on command. The completed keyboard/display unit is shown in Figure 3.6 (a), which simply connects to the pattern generator main chassis by means of a flat cable, and can be disconnected whenever it is not in use. Further description of the keyboard and its use is given in Section 3.4 of this chapter, in relation to the monitor program.

Cassette tape was chosen as the medium for data storage because of its low cost, portability, and effectiveness. A cassette storage system was designed using the variable speed Triple I Phi-Deck cassette transport. The playback and record electronics were designed by the author, and incorporate a frequency-shift-keying (FSK) scheme for recording the digital serial data stream. Basically, a digital bit assignment of logical '1' is represented on the tape by one frequency f_1, while a logical '0' is represented by a second frequency f_2. By ensuring that each bit is represented by at least four cycles of its corresponding frequency,



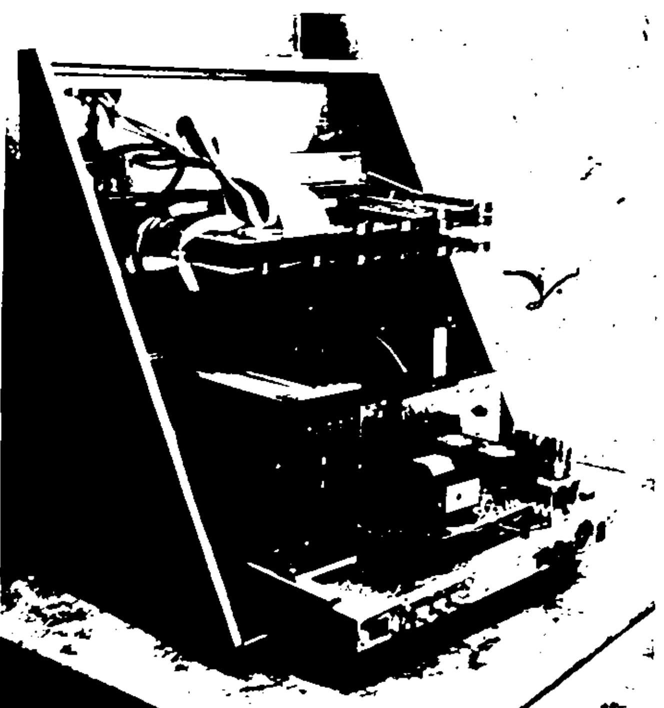
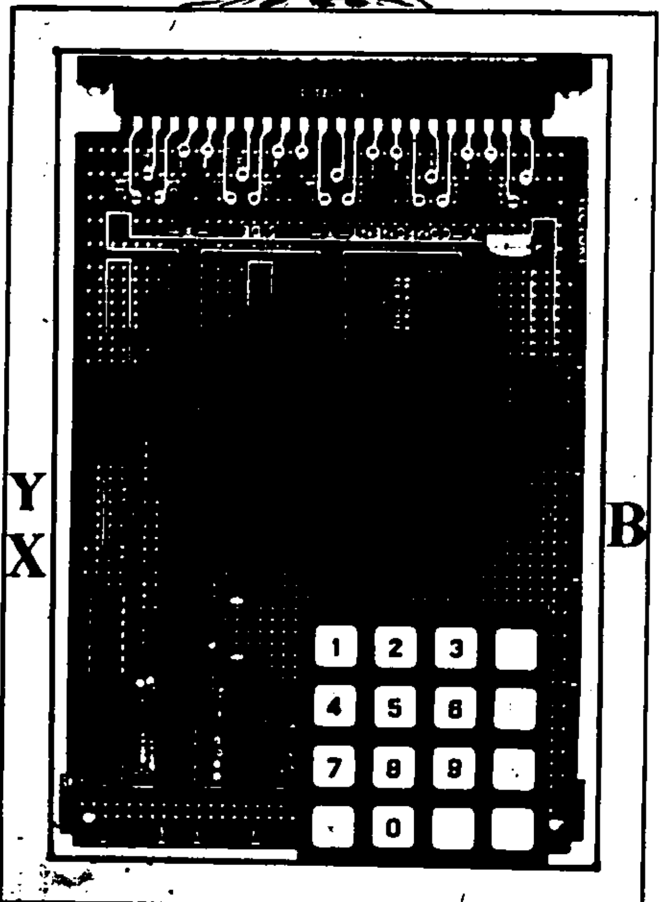
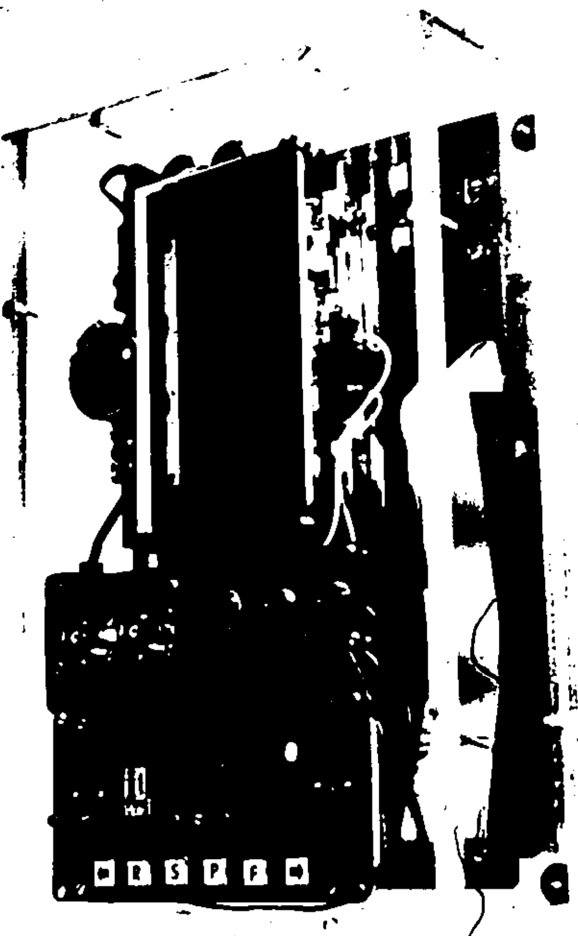


Figure 3.5 Front and rear views of completed pattern generator.



(a)



(b)

Figure 3.6 (a) Pattern generator keyboard/display unit.
(b) Cassette data storage system.

the error rate is kept low, and a reliable storage system is obtained. Further details on this recording and playback method may be found in [23]. Data was recorded and played back at $3^3/_4$ ips. with a data transfer rate of 110 baud. The cassette system is shown in Figure 3.6 (b).

3.4 Software: The Monitor Program

A monitor program was designed which would interact with the keyboard/display unit to accept the input data and process it accordingly. The decimal input coordinate, along with X or Y coding and beam on/off information, are converted into two 8-bit binary numbers which are coded as shown in Figure 3.7. The coding scheme offers the ultimate in compactness, while still being flexible. Given that the E-beam is allowed to move only in one of the X or Y directions at a time, then the only information needed, aside from the 14-bit data to the D/A converter circuitry, is the direction of travel (X or Y) and the beam status (on or off). Each of these latter specifications have only two possibilities, and can therefore be represented by one bit each, yielding a total coded word length of 16 bits to completely specify one scan. This data compaction technique greatly reduces memory requirements, compared to systems which utilize ASCII coding or multiple code words.

A flowchart outlining the monitor program functions is illustrated in Figure 3.8. A detailed program listing of the monitor along with procedures on its use are given in Appendix A. Upon monitor initialization, data is entered on the keyboard, specifying the coordinate type first (X or Y), the decimal data next (in decimal up to 16,000), the beam status (press B key if beam on), followed by the 'Next' key. The display

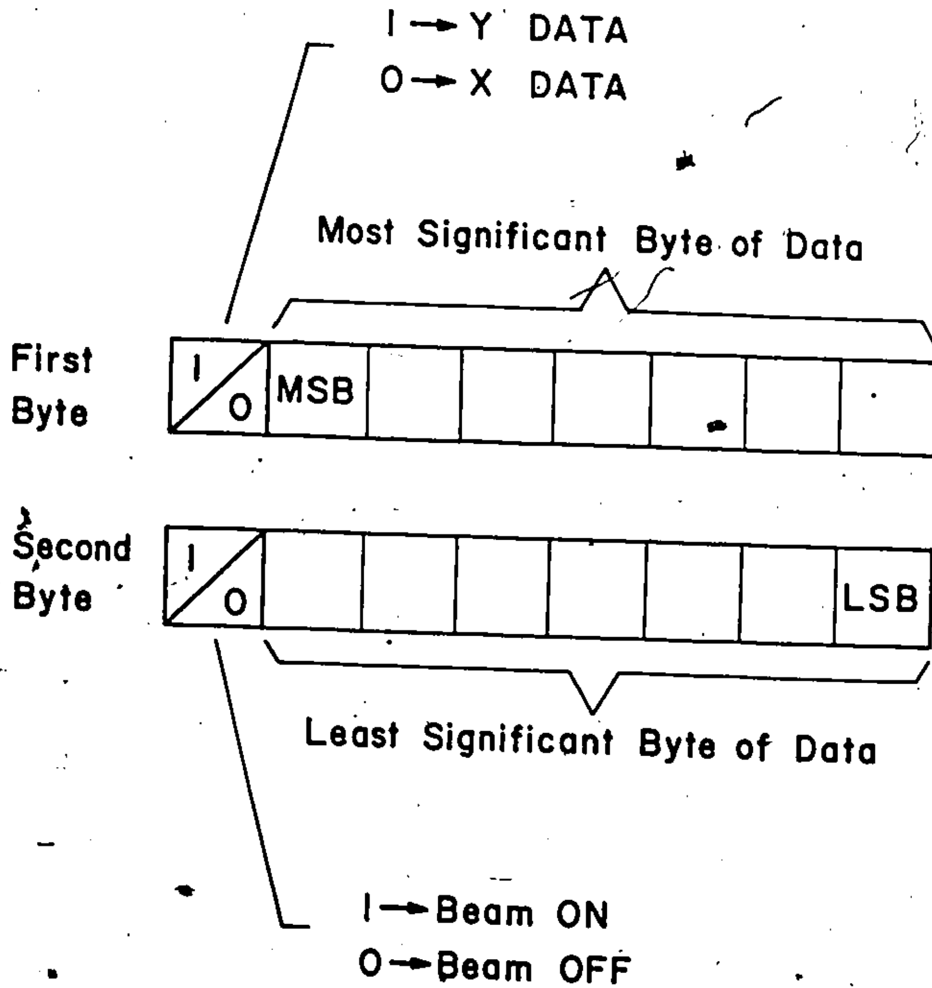


Figure 3.7 General monitor output coding format for two consecutive 8-bit data bytes.

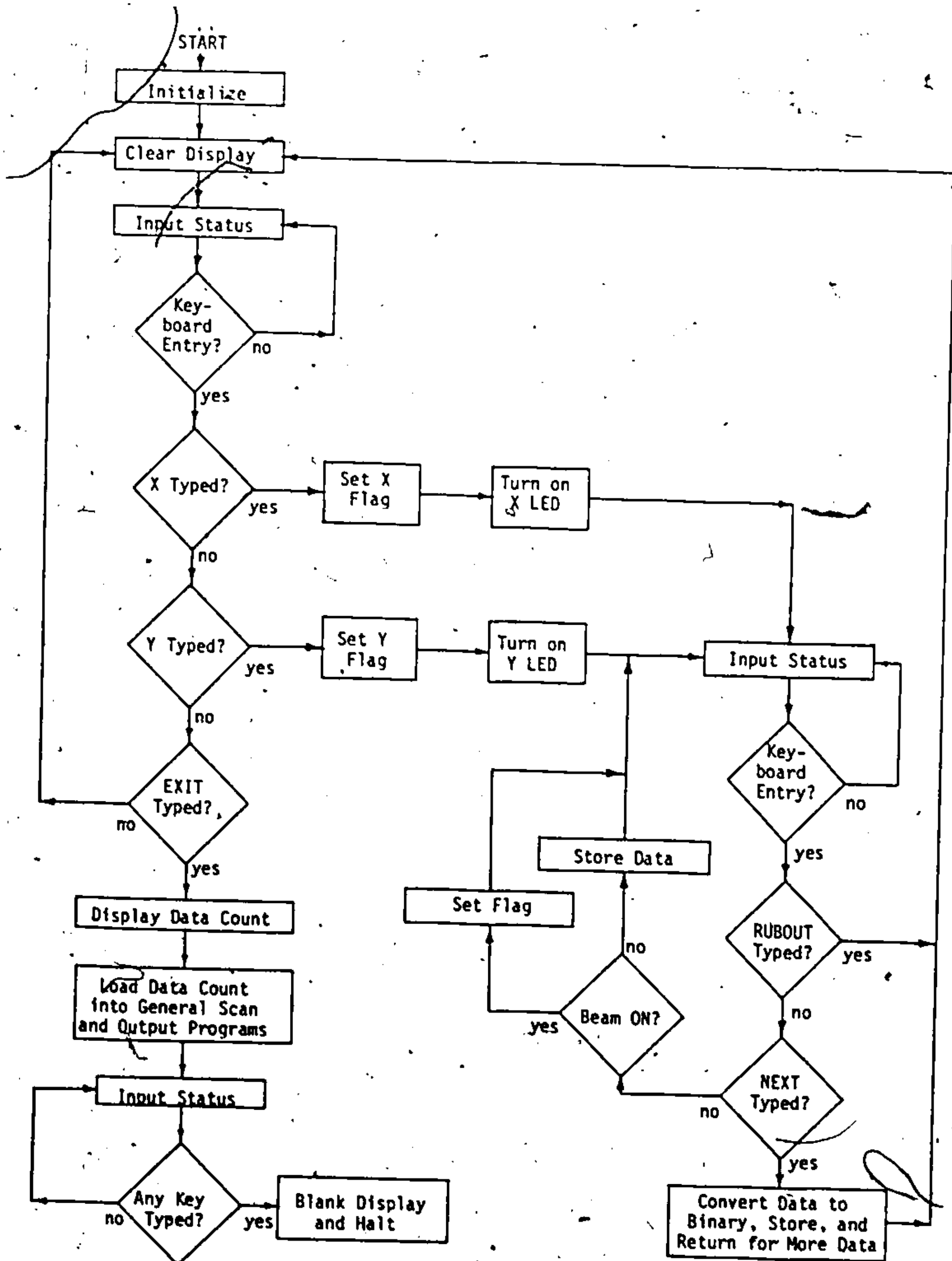


Figure 3.8 (a) Data input, conversion, and storing routine.

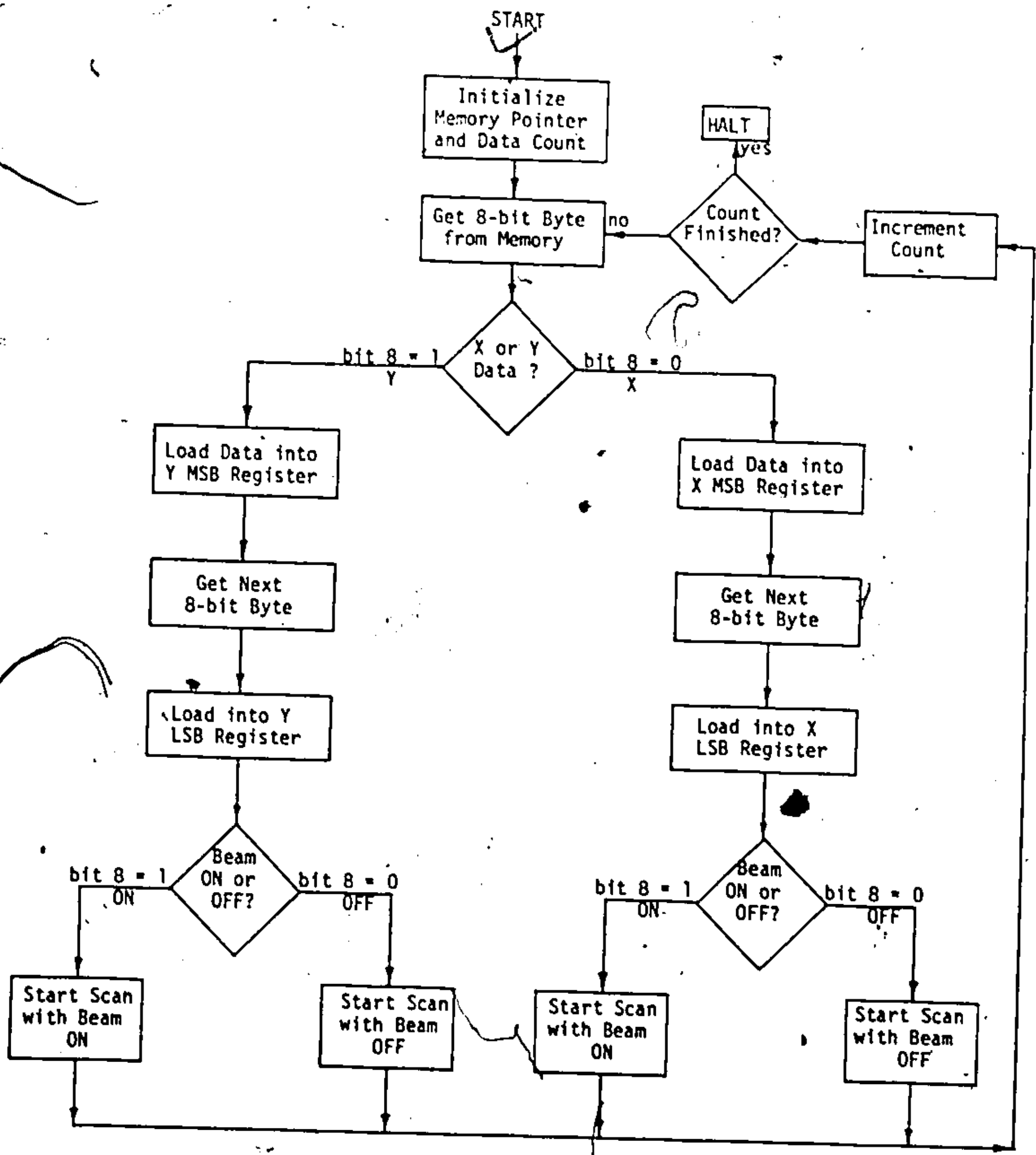


Figure 3.8 (b) General format scan program.

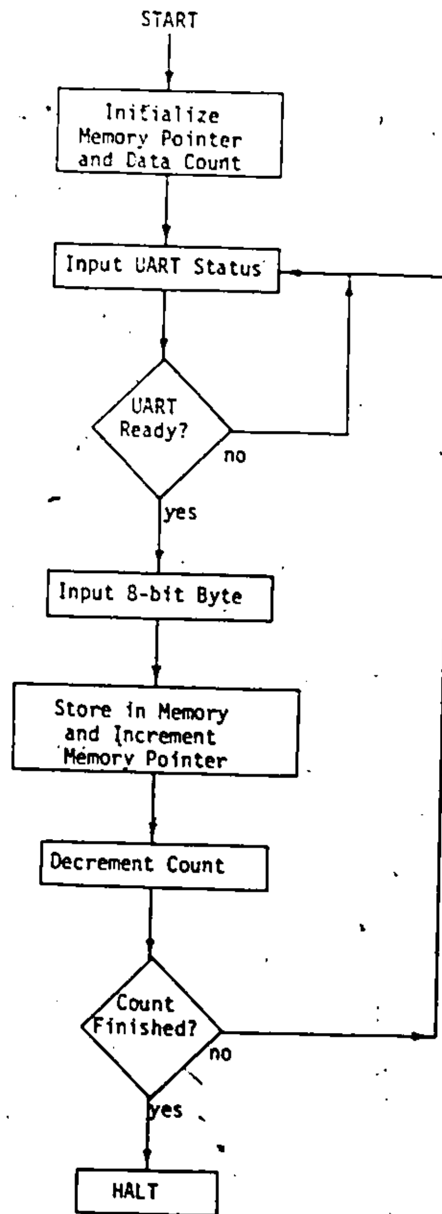


Figure 3.8 (c) Cassette loader program.

echoes the input to allow checking and subsequent corrections, since the data is not processed until the 'Next' key is depressed. If the proper input sequence is not adhered to, the present entry is automatically aborted. The converted data is sequentially stored in memory, and upon completion of the data input, typing the 'Exit' key displays the octal data count, which is also loaded into the cassette loader and general scan programs. In order to preview a pattern for error detection or other tests, an oscilloscope with blanking or intensity modulation capabilities may be connected to the pattern generator monitor jacks, and the general scan routine in the monitor will scan the newly entered data. When the pattern data is complete and error free, the cassette loader routine in the monitor loads the data automatically onto a cassette tape for permanent storage. Available memory space, set aside for data storage using the monitor routine, is 1K of RAM. Should the expected data count exceed this limitation, the data may then be formatted into blocks on the cassette tape.

One advantage of the monitor is that it does not require operator knowledge of both the microcomputer language, and the details of the interfacing between the scanner electronics and the microcomputer. However, the system does not have to adhere to the monitor format. As an example, in many cases it is required to scan a pattern which has many repetitive elements in it. Rather than representing each repetitive element with its own unique set of data coordinates, the basic features of the element may be incorporated in the form of relative coordinates into a software subroutine. Each time the repetitive element is required to be scanned, only the coordinate points of a key reference point need be given. This

technique has the potential of reducing memory or storage requirements by extremely large factors. A third technique, which works well for simple repetitive structures such as gratings, consists of writing a customized program specifically for the application, using repetitive loops in the programming structure.

3.5 The Complete Lithography System

The SEM pattern generator was designed to be portable, enabling the generation and testing of data programs to be carried out in a conducive environment, remote from the SEM facility. When the programs and samples have been prepared, the pattern generator may be interfaced to the SEM within several minutes. The entire lithography system is illustrated in Figure 3.9, showing the pattern generator interfaced to the Stereoscan Mark II A SEM. A shielded four-conductor cable is used to connect the analog X and Y outputs from the pattern generator to the 'external scan input' connector on the rear of the SEM scan generator. The external scan mode is enabled by means of switches, located on the front panel of the scan generator. The beam blanking signal is fed to the SEM via a separate coaxial cable, which connects to one of three possible input jacks, located at the rear of the beam-blanking unit of the SEM. The appropriate input jack is selected by a front panel pushbutton, the entire unit being situated just above and to the right of the operator's display CRT. A second CRT on the right side of the SEM panel is used for recording purposes when in the SEM mode of operation. The specimen current meter is situated just above and to the left of the display CRT. Details on how this microlithography system is used to produce

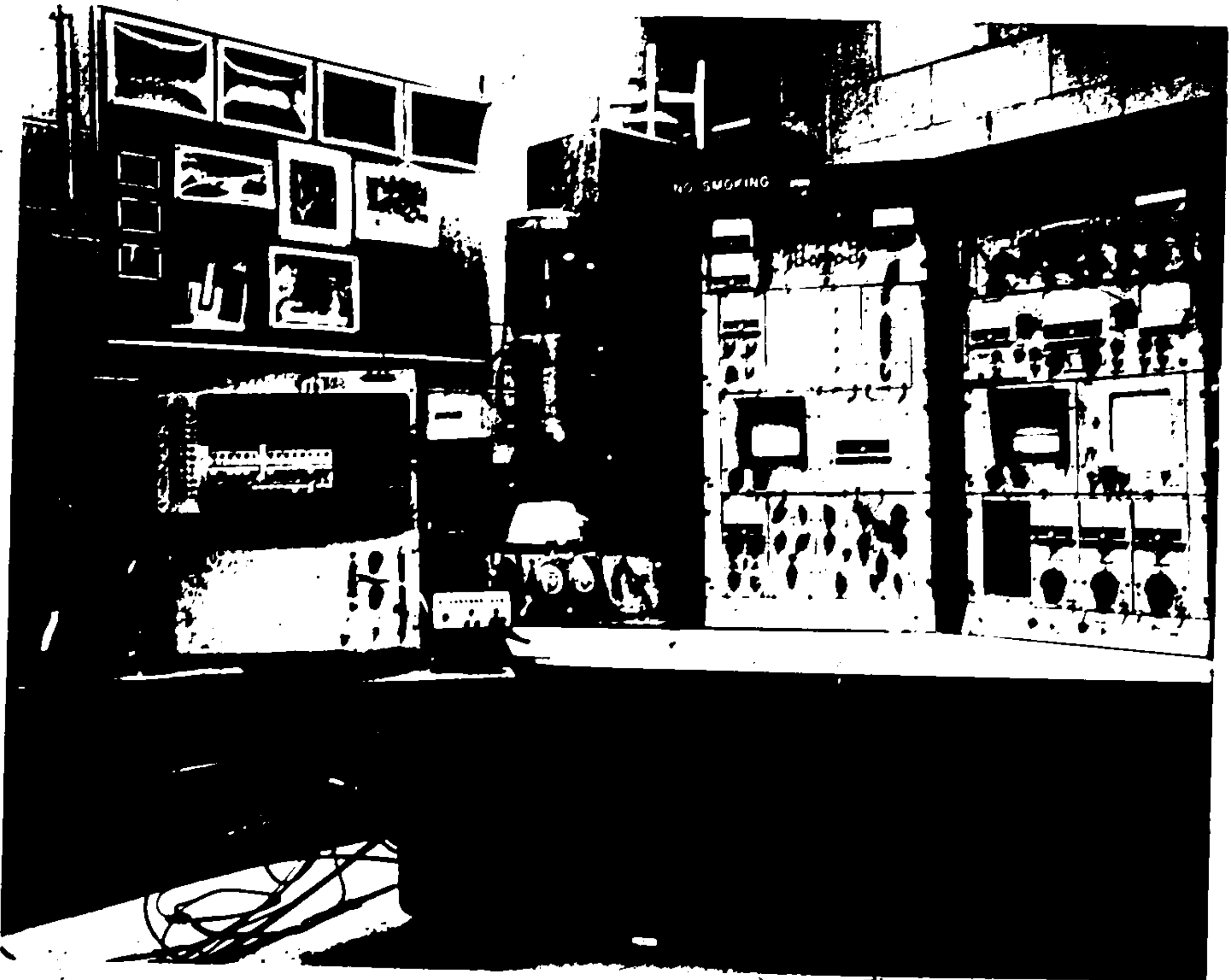


Figure 3.9 Microfabrication system using Stereoscan Mark II A SEM.

devices are covered in the next chapter.

3.6 Conclusions

The initial considerations and objectives of the E-beam lithography system design have been discussed, with particular emphasis on the application of a standard SEM to microlithography. The primary features required of a commercial SEM for E-beam lithographic purposes can be summarized as follows:

(a) reasonably low distortion over the required scan field

(b) an external input facility to the scan amplifiers, effectively bypassing the internal raster scan generator

(c) a beam-blanking facility, consisting of either an electromagnetic deflecting coil or electrostatic deflection plates, along with appropriate driving circuitry

(d) a specimen current meter, or means by which the absorbed electron current in the specimen can be externally measured and monitored

The basic methods of scan field distortion analysis for SEM instruments have been reviewed, and several results have been presented which relate specifically to the SEM used in this work. The details of the hardware design and implementation have been covered, as well as descriptions of the software monitor program function and operation. Finally,

the pattern generator and SEM are presented as a system where both facilities are used in a combined effort to produce sub-micron sized patterns.

CHAPTER 4

DEVICE FABRICATION: PROCEDURE AND SYSTEM VERIFICATION

4.1 Introduction

This chapter deals with the various aspects of device fabrication, pertaining especially to pattern formation by means of the E-beam lithography system discussed in the previous chapter. Various considerations regarding the electron resist used for lithography will be covered, particularily the basic types of resist, their sensitivity, beam profiles, and development characteristics. The complete and detailed steps involved in substrate preparation are included, since these steps differ from the standard photolithographic techniques in several areas. The entire pattern exposure process is explained, and includes data for choosing the SEM parameter values for proper exposure. The alignment procedure, along with scanning techniques, is also discussed. The pattern development steps are covered, and include such factors as developer concentrations, development times, and other secondary effects. Post development processing is discussed in general terms, but for the purposes of this thesis, the concentration is on single-level planar fabrication, using evaporation techniques for realizing circuit structures. The identification of certain fabrication problems, which the author has experienced, are discussed such that a greater understanding of the overall process and its problems can be gained.

4.2 Resist Considerations

The existence and properties of resists form the basis for the entire field of lithography. Resists, as the name implies, consist of a variety of chemicals which are usually applied to surfaces in the form of thin films, and which tend to 'resist' certain chemical or radiation effects, thus protecting the substrate area underneath. Many common resists are polymers, and are sensitive to a particular spectrum or wavelength of incident energy. For positive-acting resists, the incident energy causes scission of the long chain-like molecules of the polymer when applied with the proper dosage levels. Subsequent immersion in an appropriate developer will dissolve away the scissioned molecules only, leaving the unexposed regions intact, thereby defining a pattern on the substrate surface. Negative-acting resists behave in the opposite manner, with the exposed regions remaining after development, due to cross-linking of the polymer molecules upon exposure. Resists which are sensitive to incident light energy (usually in the ultraviolet region) are termed 'photoresists', while those sensitive primarily to electron radiation are termed 'electron resist'.

The important qualities of a resist are its sensitivity to incident radiation, high-resolution capability, contrast, ability to resist etchants, and ease of application and development. Table 4.1 lists several of the popular resists used for microfabrication [1]. An important consideration, which is not usually quoted as a resist specification, is the latitude in exposure, or sensitivity range of a resist. This latter factor becomes important when areas of double or multiple exposure occur during the scanning of a pattern. As an example, a positive resist with a very

TABLE 4.1

Characteristics of Several Electron Resist Materials

Material	Type	Typical sensitivity (C/cm^2)	Resolution (minimum line width reported)(μm)	Compatibility with semiconductor fabrication processes
KTRF-KMER-KPR (Kodak)	negative	5×10^{-6} **	1	good
Silicones	negative	10^{-5}	0.5	fair
Epoxidized polybutadiene	negative	5×10^{-8} **	?	fair
Shipley AZ-1350	positive	5×10^{-5} *	1	good
Poly (a-methyl-styrene)	positive	10^{-4} *	?	poor
Poly (methyl methacrylate)	positive	5×10^{-5} * 5×10^{-6} **	<1,000 Å	good
Poly (butene-1 sulfone)	positive	10^{-6}	0.5	good
Polydiallylorthophthalate	negative	10^{-6} **	2	good
Poly glycidylmethacrylate ethyl acrylate	negative	5×10^{-7} **	0.5	good

*No thickness loss after development **Significant thickness loss

narrow sensitivity range could not tolerate double exposures, since cross-linking would dominate the scission process in these areas. In general, the positive resists offer greater resolution and contrast compared to the negative resists, although they suffer from a lower sensitivity. Sensitivity to the incident radiation becomes important when a high pattern-writing speed is desired, which relates again to the demand for a higher throughput rate.

As illustrated in Table 4.1, the positive resist polymethylmethacrylate ($C_5H_8O_2$, abbreviated PMMA) has the highest resolution capability. This positive-acting resist has several other advantages, which make it the best choice for E-beam lithography whenever throughput is not the primary concern. The exposure latitude of PMMA extends over an order of magnitude from 5×10^{-5} to 5×10^{-4} C/cm^2, allowing considerable tolerance for overlapping regions of exposure. The resist is not sensitive to light in comparison to the commercial photoresists, and this avoids the need to work under safe-light conditions. A further advantage of PMMA is that it is readily available and inexpensive, existing in its most common form as plexi-glass.

The PMMA is applied to substrate surfaces by means of spin coating to yield layers varying from 1000 Å to several microns. The polymer is dissolved in a solvent with a specific concentration, which determines the final thickness of the spin-coated layer. Electron irradiation of the thin film within the required sensitivity range causes scission of the long polymer chains, which effectively reduces the molecular weight of the exposed resist. The reduction in molecular weight is always quite pronounced [24], dropping from the usual molecular weight value for PMMA

of several hundred thousand to below 20,000. The development process is achieved by immersing the film-covered substrate into a poor solvent, which primarily dissolves molecules of low molecular weight and leaves the high molecular weight molecules unaffected. The poor solvent is obtained from the mixing together of a good solvent for the entire molecular weight range, with one that will not even dissolve the lowest molecular weights. Harris [24] has determined that the ideal molecular weight distribution for PMMA consists of a very narrow range, with very few molecules below the weight of 50,000, and few being above several hundred thousand. This results in a compromise between two opposing properties. High molecular weights are desired to prevent pinhole formation in the development process, but an increased difficulty in dissolving the polymer for resist application purposes results, yielding poor films. Low molecular weight range PMMA yields good solubility characteristics and excellent films, however, it is more prone to pinhole formation since it is within the soluable range of the developer.

The contrast provided by PMMA is excellent, and this is due in part to the negative slope profiles which can be obtained under proper exposure conditions. Figure 4.1 illustrates the three main types of exposure profiles which result from varying the incident charge density of the electron beam [25]. For high charge densities, a negatively-sloped profile results in the developed resist layer, and the resulting contour is dominated by the teardrop-shaped electron penetration profile. Medium charge densities result in vertical-walled profiles, which are due partly to the electron penetration profile, and partly to the development process. Low charge density profiles demonstrate positively-sloped

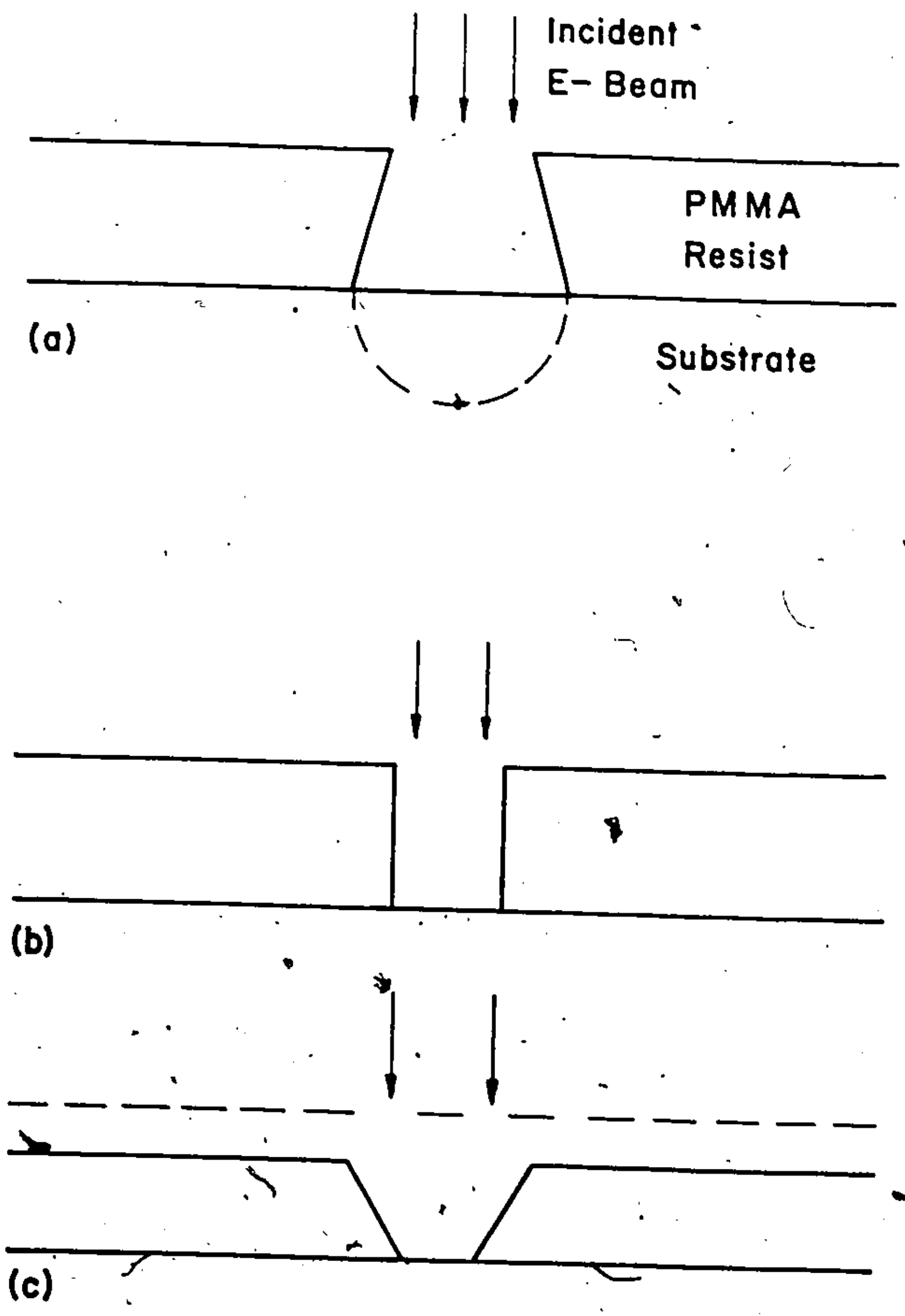


Figure 4.1 Positive resist profiles for three levels of exposure (a) high charge density (b) medium charge density, and (c) low charge density.

walls and appreciable resist thickness loss, since the resulting contours are dominated almost completely by the development process. Figure 4.2(a) summarizes these results for a one micron thick layer of PMMA, exposed at 20 kV. The surface normal line at 0° corresponds to vertical walls, which is considered to be the optimum exposure point, since this condition yields the minimum line-to-line spacing possible. The effect of accelerating potential on the developed line profiles is illustrated in Figure 4.2 (b) from the experimental work of Wolf [26]. These results show that the linewidth increases with increased linear charge density due to electron backscattering from the resist/substrate interface, and also from scattering off the polymer atoms of the resist itself. The developed linewidth tends to decrease with increased accelerating potential since more higher-energy electrons are entering the substrate, rather than scattering back to expose more resist. The slightly undercut profiles which result from the proper combination of accelerating voltage and linear charge density are very desirable for the lift-off technique, to be discussed later in this chapter.

The previously-discussed results are valid for E-beam line exposures which occur no closer than 2μm from each other. Line exposures below about 2μm spacing experience what is termed the 'proximity effect' [3], [27], [28], which involves cooperative exposure of lines in an array due to lateral electron scattering from the point of entry into the resist. From [29], the exposure of a single line can be characterized by:

$$E(y,z)b = D \quad \text{ergs/cm}^3 \tag{4.1}$$

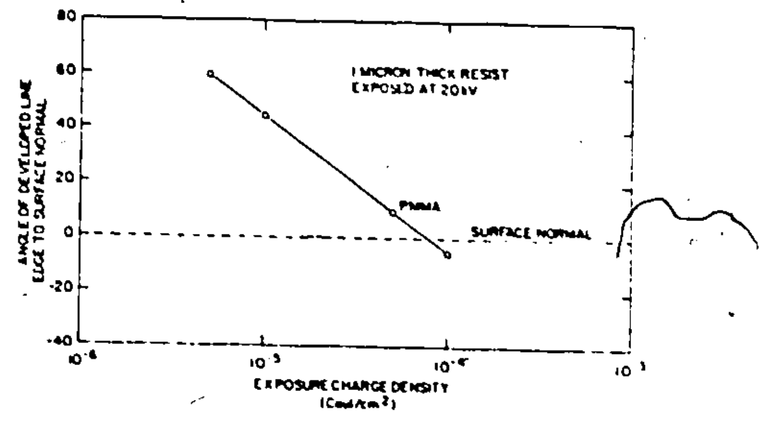


Figure 4.2 (a) Developed resist slope angle vs. charge density for PMMA. [25]

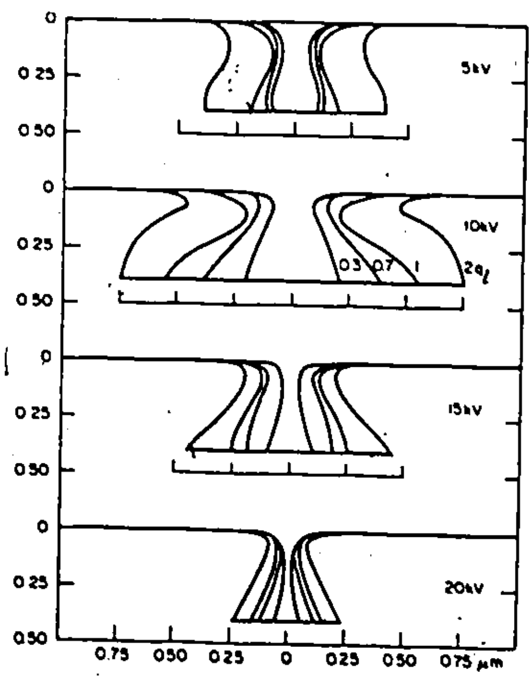


Figure 4.2 (b) Family of profiles for various accelerating potentials, with PMMA thickness of 4000 Å on silicon substrate, and q_l is the linear charge density = 1×10^{-8} C/cm. [26]

$$E(y,z) = \int_{-\infty}^{\infty} qI(r,z)dx \quad ergs/cm^2.C \qquad (4.2)$$

where D is the energy dissipated per unit volume for adequate exposure results

b is the linear charge density in C/cm

q is the number of electrons per coulomb

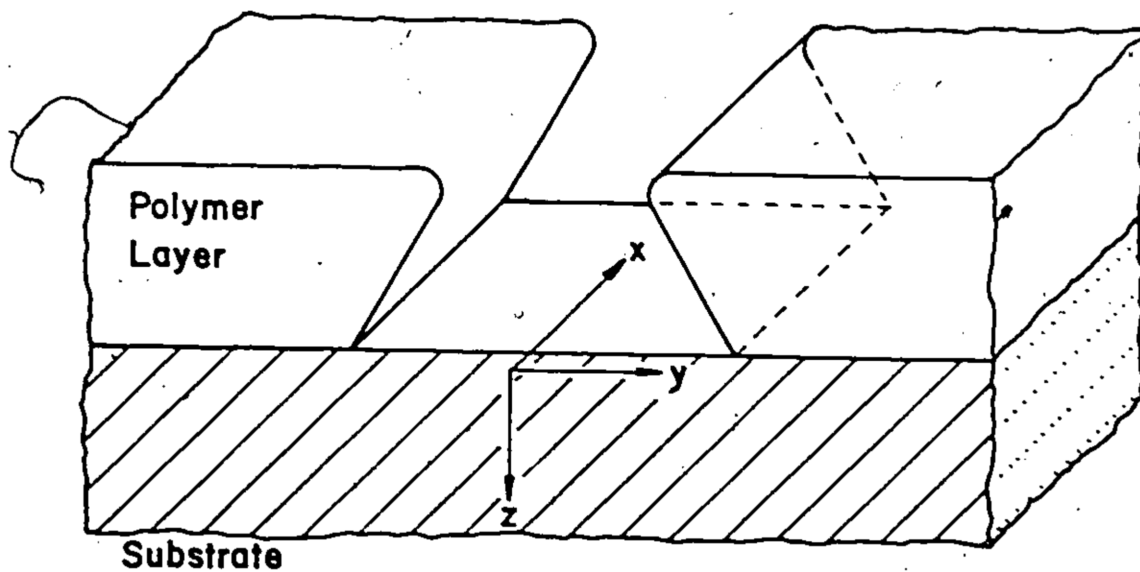
E(y,z) is the energy dissipated per unit volume per coulomb per centimeter

I(r,z) is the radially symmetric function representing the energy dissipated per unit volume per electron ($ergs/cm^3$ electron)

The variables in (4.1) and (4.2) are defined in Figure 4.3 with respect to a line scan at velocity $\overline{V}$ and beam current 'i' amperes. The resultant linear charge density 'b' is given by the beam current divided by the beam velocity. The function I(r,z) has been theoretically calculated by Hawryluk et al. [29] using the Monte Carlo technique of calculating electron trajectories in solids. The exposure due to lines separated by an interline spacing of 'ℓ'μm is:

$$E(y,z)\Big|_{ARRAY} = E(y,z) + \sum_{n=1}^{N}\left[E(n\ell-y,z) + E(n\ell+y,z)\right] \qquad (4.3)$$

where n = the number of adjacent lines



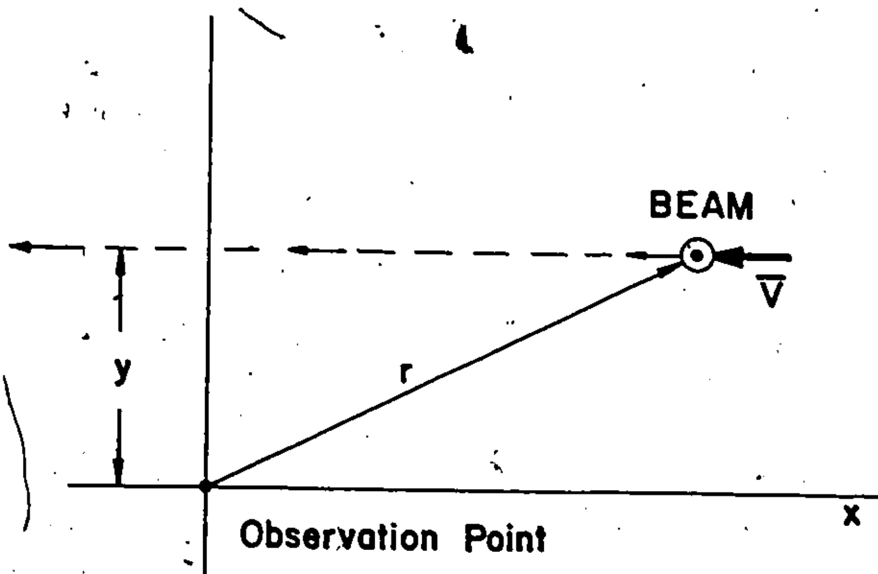


Figure 4.3 Definition of variables x, y, z, and r in relation to an E-beam line scan with velocity $\overline{V}$.

The first term in (4.3) is the response due to a single line exposure as given by (4.2). The second term accounts for the cooperative exposure effects of the neighbouring line exposures, and becomes insignificant when $N\Delta y > 7.55\mu m$ for PMMA at a 20keV beam energy. A plot of (4.3) for various interline spacings is given in Figure 4.4 [27]. The important feature to note from the plot of $E(y,z)_{ARRAY}$ is the rise in background energy dissipation as the interline spacing becomes smaller. Hence, if the linear charge density is not decreased correspondingly with the interline spacing, the pattern development will fail, due to exposure of all the resist between the line scans.

Another factor which affects the exposure parameters and final resolution is the type of material used as a substrate. Materials of differing atomic numbers will have different amounts of backscattered electrons when irradiated with an electron beam. This property is made use of later in the fabrication and detection of alignment marks. Substrates made of gold or copper would require a smaller dosage than silicon, for example, when generating sub-micron linewidth patterns in PMMA. The gold and copper substrates generate more backscattered electrons than silicon, which contribute to the exposure of the resist as well as the incident beam. In general, the higher the atomic number of the substrate, the less exposure is needed to generate sub-micron linewidths. This relationship is illustrated in Figure 4.5 (a) which shows how the number of backscattered electrons increases with increasing atomic number [6]. Figure 4.5 (b) illustrates how the number of backscattered electrons does not vary appreciably with the accelerating potential.

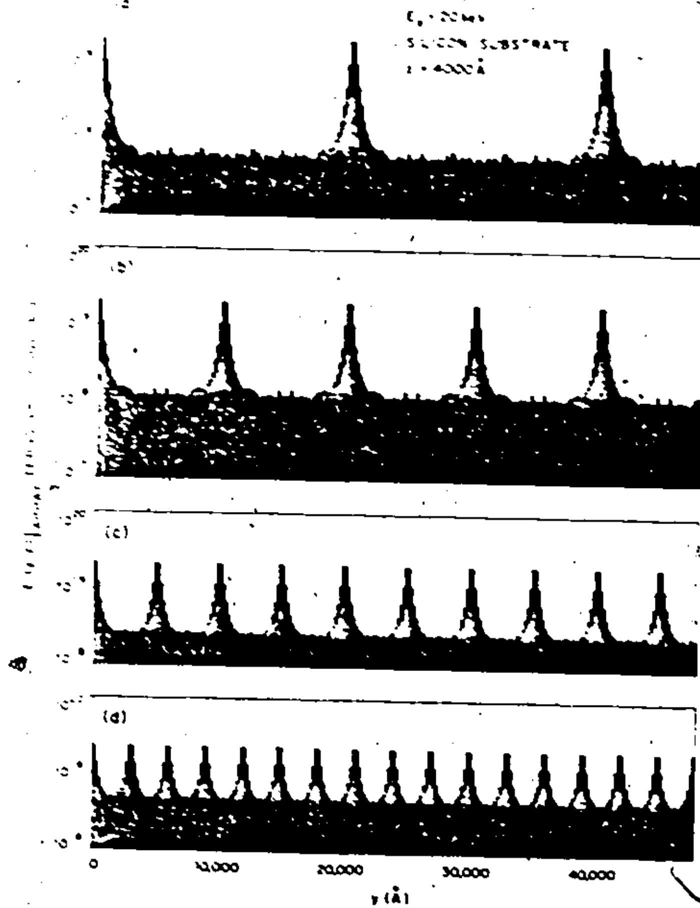
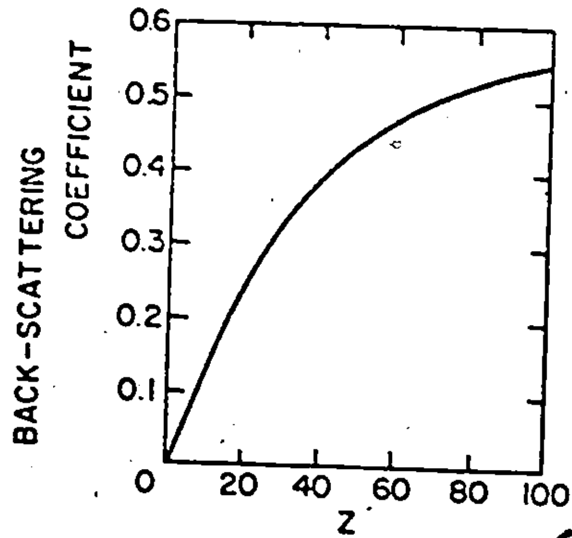


Figure 4.4 $E(y,z)\Big|_{ARRAY}$ for an array of lines exposed in a 4000 Å PMMA layer at 20 keV beam energy, with interline spacings of (a) 2μm, (b) 1μm, (c) 0.5μm, and (d) 0.3μm. [27]



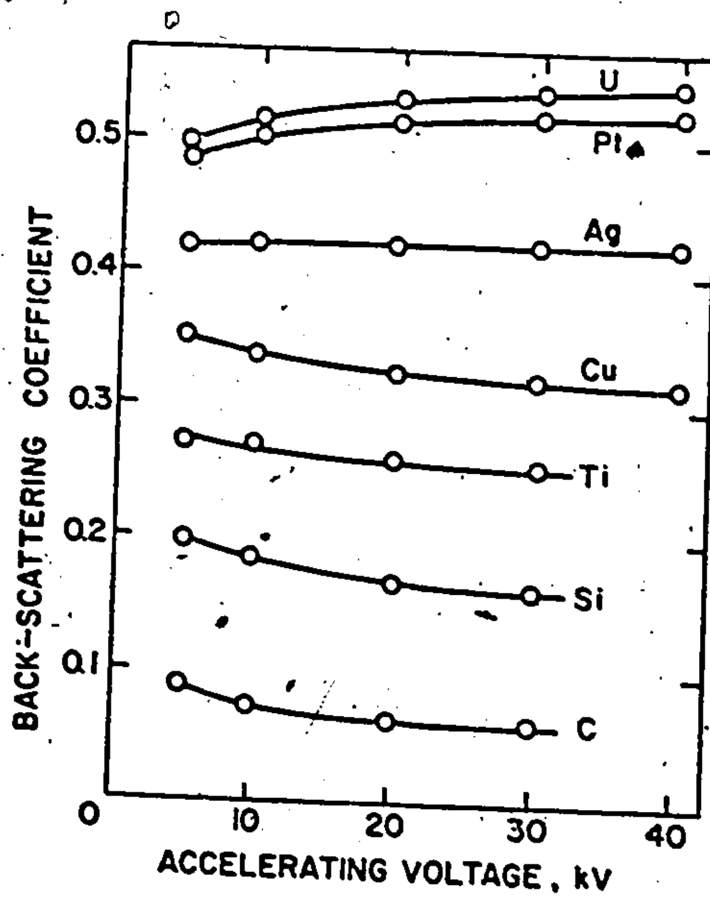


Figure 4.5 (a) Back-scattering coefficient shown as a function of substrate atomic number Z. [6]

(b) Back-scattering coefficient shown as a function of accelerating potential for various elements. [6]

4.3 Substrate Preparation

4.3.1 Substrate Cleaning

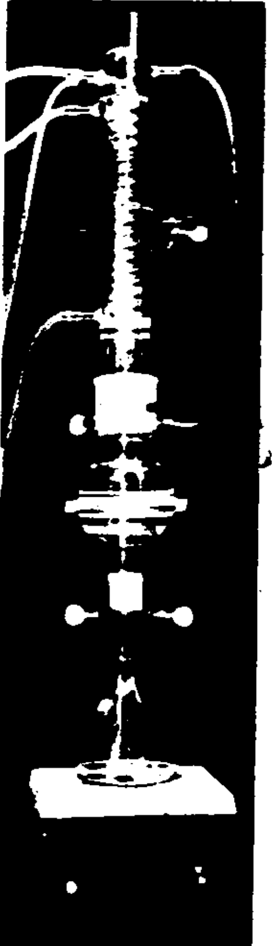
It is imperative that substrate surfaces be extremely clean for use in E-beam lithography work. The initial cleanliness of the substrate surface determines the success of subsequent processing steps, such as resist adhesion and uniformity. In the lift-off process, the resist layer remains on the clean surface right up to the final device processing step, which is the stripping of the resist. Cleanliness of the resist layer surface must also be maintained in the intermediate processing steps for successful device fabrication.

Various substrate cleaning procedures may work more effectively on some substrates than others, due to substrate properties such as density, molecular structure, degree of surface flatness and polishing. The substrates used exclusively for this thesis work were ST-X quartz, which have a highly-polished flat surface on one side. The following procedure describes how these substrates were cleaned, in readiness for the electron resist application. The procedure assumes that the substrates are not contaminated initially with residual metal films or baked-on oxide layers.

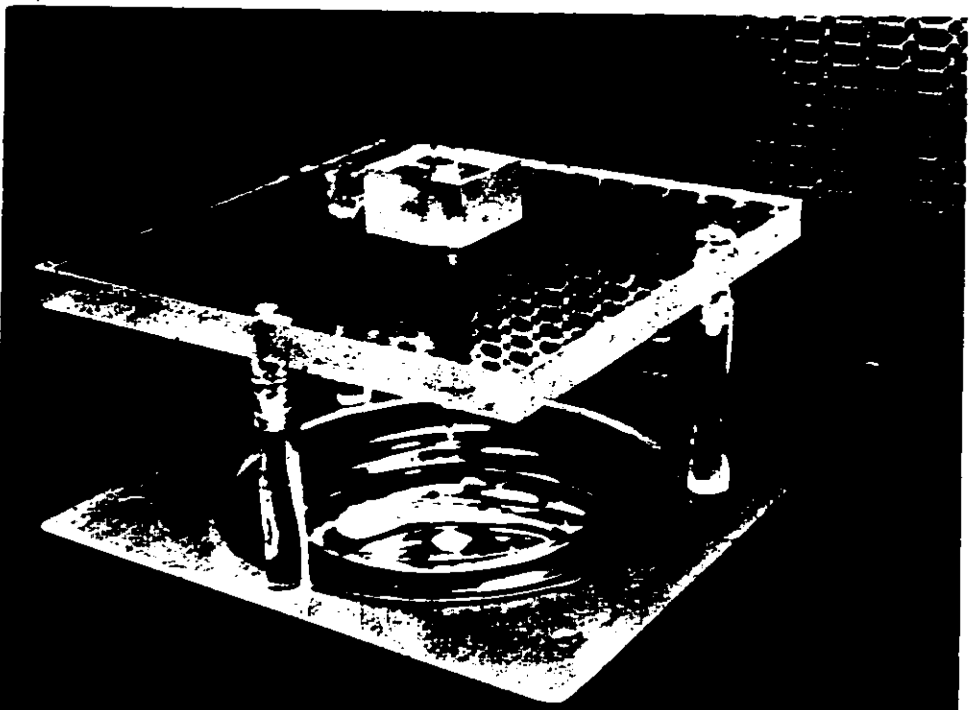
A Headway Research Inc. Model EC101 spinner was used for the initial cleaning steps. The substrate (1cm x 1cm) was placed on the vacuum chuck of the spinner, polished surface facing up (this is the working surface of the quartz substrate), and flooded with acetone. While continually pouring a steady stream of acetone onto the surface, the spinner was accelerated to the working speed of approximately 6000 RPM. A 20 second spray of acetone was followed by 20 seconds of methanol spray,

and finally with a 45 second rinse of distilled water. It is important that when changing from one spray to the next, the applications should always overlap so that the substrate surface never has a chance to dry. After the water spray, the substrate was allowed to spin dry for approximately 30 seconds. This completed the first phase of substrate cleaning, and visual inspection of the surface at this stage should show no visible traces of smears or waterspots. Visible inspection of the highly-polished quartz surface is quite effective since any surface impurities show up readily when the surface is used as a mirror to reflect a light source.

The final phase of substrate cleaning was accomplished with the use of a distilling apparatus which is illustrated in Figure 4.6 (a). Methyl alcohol (high purity) was placed in the flask situated on top of the electric heater. The substrates (up to eight at once) were supported on a fine stainless steel wire mesh, situated in the bulging glass section immediately above the flask. A double-walled condenser is positioned directly above the substrates, with a cooling coil running up the centre of the condenser, as well as having the outer jacket cooled. This construction results in the condensation of the evaporated methyl alcohol in such a manner that a steady stream of condensed droplets fall onto the substrate surfaces from a 10 cm height. This cleansing action, combined with the surrounding hot vapour atmosphere, produces an ultra-clean substrate surface. The substrates were left inside the apparatus anywhere from 20 minutes to several hours, after which time they were baked in an 80°C oven for at least one hour, to remove any moisture content from the surfaces.



(a)



(b)

Figure 4.6 (a) Glass vapour-cleaning apparatus.
(b) Resist application set up.

4.3.2 Resist Application

The PMMA electron resist which was used throughout this thesis work was obtained from Esschem Co., and has a molecular weight of 950,000. Various concentrations of the polymer in the solvents methyl isobutyl ketone (MIBK) and methyl ethyl ketone (MEK) were experimented with in relation to final film quality on the substrate surface. It was found that the PMMA dissolved more readily in the MEK, a process which took about one hour at 40°C for a 5% concentration. The solubility of high molecular weight PMMA is poor, and the preparation of a high dissolved-polymer concentration can take up to 12 hours. A maximum concentration of 5% was chosen, since the consistency of higher concentration resist solutions approaches that of glue, and the resulting films become unacceptable. The final thickness of the resist layer is a function of the polymer concentration in the resist, and the RPM of the spinner at the time of application. It is highly desirable to achieve thin, uniform resist coatings with no wave-like structures present or dust particles imbedded on the surface. The best results are obtained when the resist is applied while the substrate is spinning at the desired speed. In order to obtain repeatable and uniform coatings, a jig was constructed to allow precise application of the resist, as illustrated in Figure 4.6 (b). It was found that both the height and the centering of the resist applicator affected the quality of the resulting films, and the special jig served to keep these factors constant.

The consistency of the 5% resist solution ruled out pre-application filtering, as is usually done with standard photoresists. Therefore extreme care must be exercised in preparing the solution, to ensure clean

glassware and associated utensils in handling the resist. All preparatory work and resist coating should be done on a clean air bench facility, at the very least, and preferably in an ultra clean air room. A standard eyedropper is used to apply the resist, and is positioned in the jig approximately 5 cm above the substrate surface. A resist thickness of 4000 Å was desired, and this was achieved by applying 3 drops of resist at 10 second intervals onto the substrate, which was spinning at 4000 RPM. This procedure was arrived at by a series of tests in which the final baked resist thickness was measured and calibrated. Corning 1"x1" No. 2 glass slides were used for the test, and the resist thickness was measured with a Taylor-Hobson Talysurf 4 unit by scanning across an abrupt resist edge. During application of the PMMA resist, a vacuum cleaner attachment to the Headway spinner provided a downward suction around the periphery of the spinning substrate. The purpose of this suction was to prevent any resist strands, or fine webs characteristic of spun PMMA, from falling back on the surface of the substrate, thus ruining the film. After resist application, the substrate was allowed to spin for an extra 30 seconds to let the excess solvent evaporate off.

4.3.3 Post Baking and Mounting

Immediately after resist coating, the substrates were baked in a filtered air-circulating oven at 170°C for 20 minutes. Heating the polymer film to above 160°C allows all the remaining solvent to be released, and results in better film adhesion to the substrate surface. Above the glass transition temperature of PMMA (100°C to 110°C), the polymer becomes rubber-like and elastic, allowing molecules to slide over each other and

thus releasing any strains which were generated during the coating process. Temperatures in excess of 190°C cause thermal degradation of the polymer, and should be avoided [24]. Baking the films for longer than 30 minutes at 170°C results in a harder and more brittle film, which becomes increasingly more difficult to dissolve in PMMA developer, or stubborn to remove in the lift-off process. After baking, the substrates were set aside in a covered glass dish to air cool.

After cooling, the substrates were mounted to standard 12 mm specimen stubs. GC Electronics conductive silver paint (Cat. No. 21-2) was used to mount the substrates onto the stubs. The paint was used very sparingly at the centre of each side of the substrate, since previous experience by the author has shown that the silver paint particles can interfere drastically with the subsequent device processing steps. Care must be exercised when mounting the substrates to ensure that they are lying flat on the specimen holder, since the silver paint can easily permeate beneath the substrate. A level mounting is desired to avoid loss of focus with the E-beam system when scanning over appreciably sized areas, in which case the depth of focus range is exceeded. The silver paint connections were cured by baking in an 80°C oven for 15 minutes.

4.3.4 Conductive Layer Application

In both microscopy and lithographic applications of the SEM, a low resistance path to ground must be provided from the sample, in order to prevent charging of the sample. Since ST-X quartz is an insulating substrate, it must be coated with a thin (~400 Å) layer of aluminum to provide a path for the excess electrons to the aluminum specimen stub,

and hence to ground. This task was achieved by placing the mounted substrates inside an Edwards Model 12-E vacuum coating unit, and evaporating the 400 Å layer of aluminum onto the resist-covered substrate surfaces at a pressure of 10^{-} torr. The substrates were left inside the evaporator in a partial vacuum until they were ready to be scanned by the SEM. The mounted substrate, ready for exposure by the lithography system, is illustrated in Figure 4.7. This particular sample has a visible horizontal line across the centre of the substrate surface, which is due to a spun PMMA strand which has fallen back across the surface.

4.4 Pattern Exposure

4.4.1 SEM Parameter Settings

Several parameters or constraints have already been chosen up to this point which are:

(a) the resist: PMMA

(b) scan field size of 1mm x 1mm

(c) D/A converter resolution of 625 Å

(d) linewidth capability of less than 1μm in 4000 Å thick resist layer

For the scanning of lines in PMMA resist, it is generally agreed that the beam diameter should be on the order of five to ten times smaller than the smallest required linewidth [3]. This criterion will ensure good resolution and contrast whenever it can be met. An accelerating potential of 20 kV was chosen for the pattern exposures, since this potential yields sub-micron linewidths over a large range of linear charge densities as

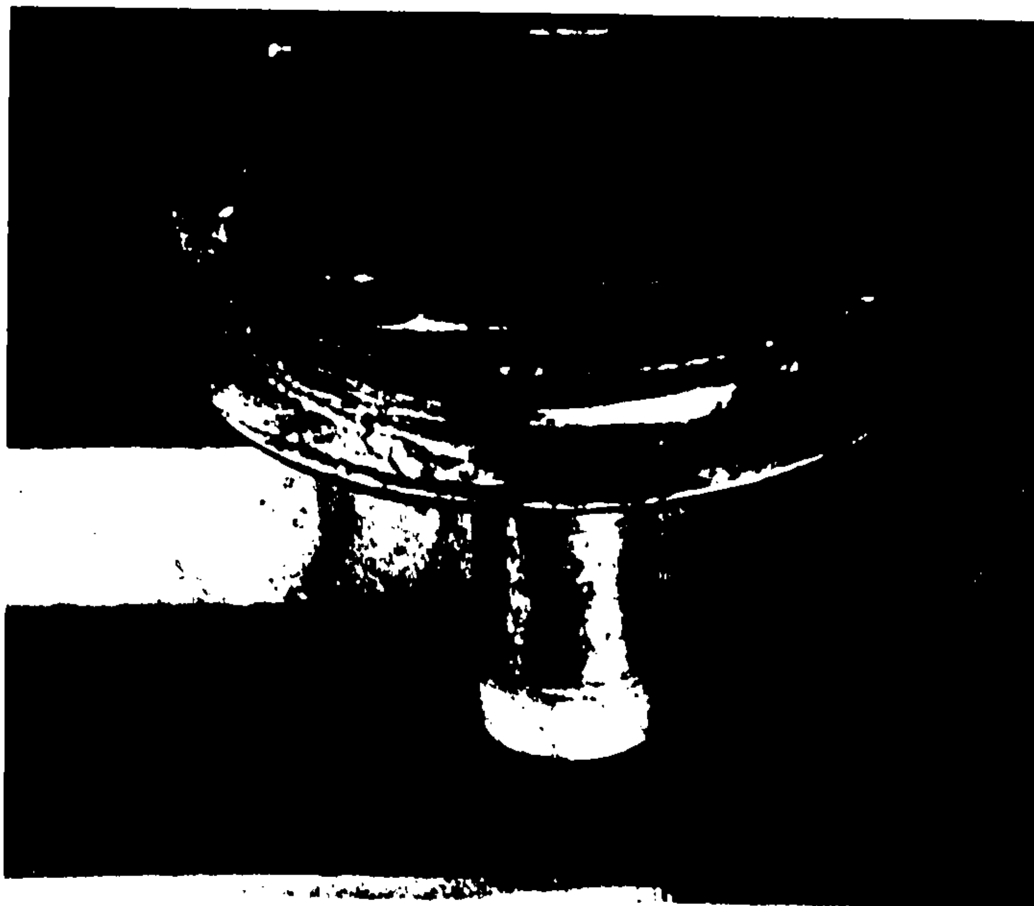


Figure 4.7 Mounted quartz substrate, ready for pattern exposure.

illustrated in Figure 4.2 (b). The final aperture size must be chosen so that the proper relationship between beam diameter and working distance is obtained, to minimize the opposing constraints. A plot of the optimum aperture for a maximum given beam current (2.9) is given in Figure 4.8 [5]. A working distance of 12 mm was chosen to give a reasonable trade-off between deflection distortion and desired beam diameter. A 200μm aperture was used to obtain the minimum possible beam diameter for the chosen working distance.

Having fixed the working distance, the lens current supply to the third condenser lens was varied until the required working distance was indicated on the SEM magnification meter. For a working distance of 12 mm, this lens current value is 0.62 A on the Mark II A column. Figure 4.9 illustrates the relationship between the beam diameter and the lens supply currents for the first two condenser lenses of the electron column [5]. To keep the beam diameter below 1000 Å, a value of 5×10^{-10} A was chosen (see Figure 2.7) for the beam current, which is determined primarily by the first condenser lens. The resulting values of lens currents were 0.50 A for the first lens, and 0.54 A for the second condenser lens.

The filament was always set up for saturation, which takes place at a filament current of 2.4 A. A bias setting on the electron gun of position #4 was needed to bring the beam current in the gun into the 100μA to 140μA range. Details on the operation of the Stereoscan SEM in regard to specimen loading, pumpdown operation, and working procedure are given in [6]. Various other combinations of SEM parameters for pattern generation were initially tested by the author, but the aforementioned settings were found to yield the best overall results, although an exhaus-

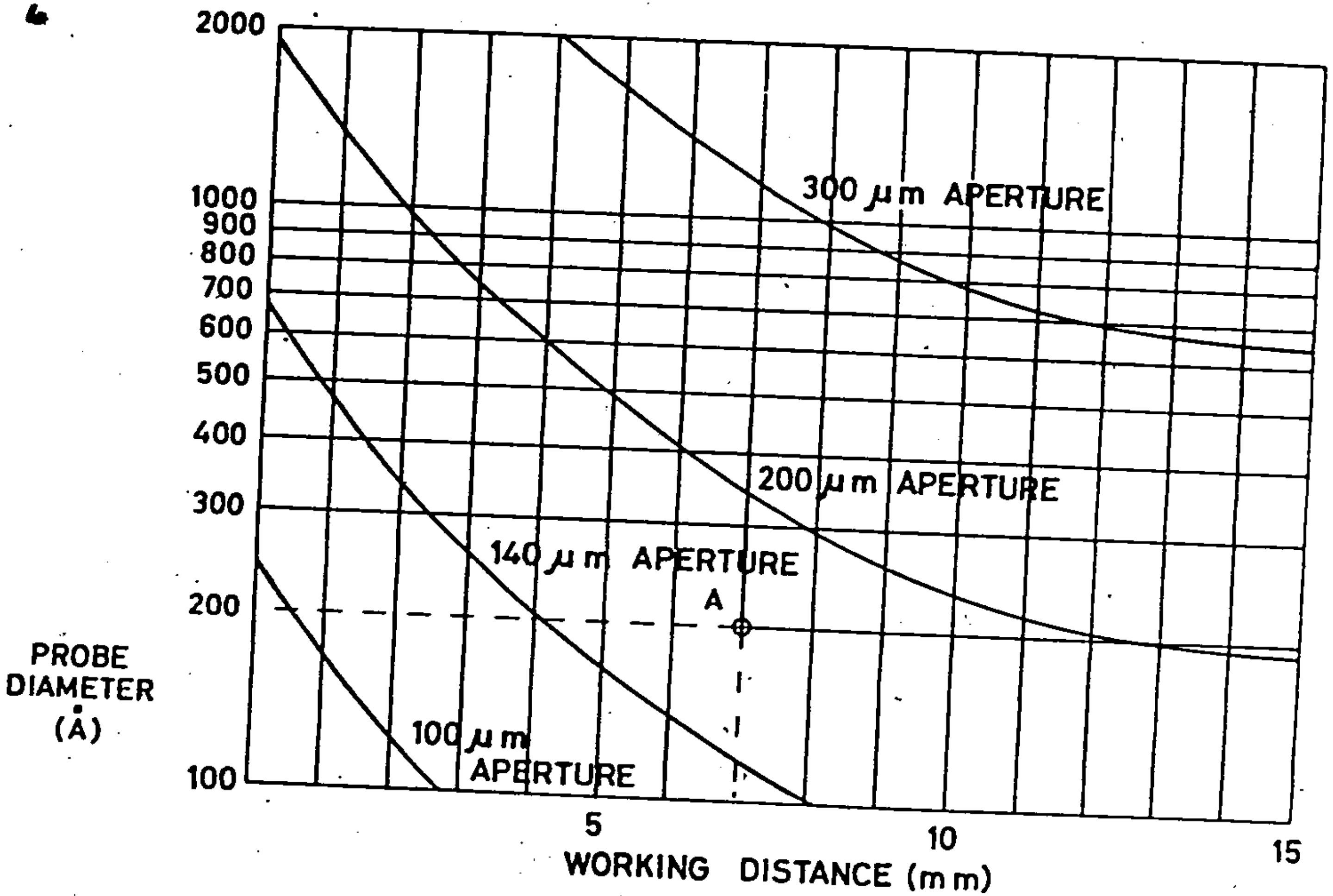


Figure 4.8 Relation of final aperture to probe diameter and working distance. [6]

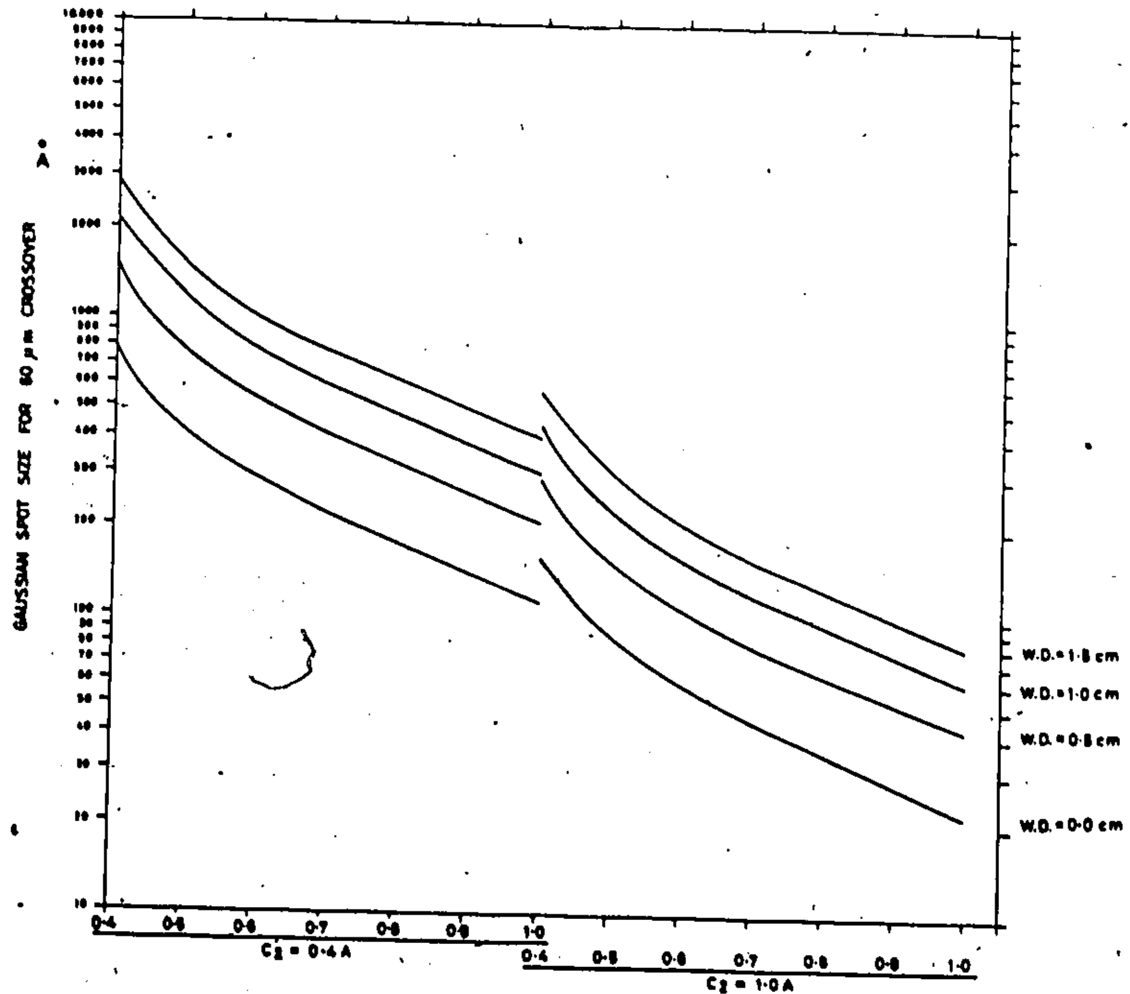


Figure 4.9 Relation between spot size and lens currents for first two condenser lenses C1 and C2, at various working distances. [6]

tive test was not carried out because of the large number of possibilities.

4.4.2 Alignment Procedure

Alignment marks must be used on the substrate surface to allow dimensional calibration of the pattern generator to the surface, and for proper alignment to the scan field (rotational, as well as X and Y directions). These alignment marks consist of a high atomic number material (gold), such that they may readily be detected in the SEM using the back-scattered electrons. The alignment mark pattern, which was fabricated for this work, consists of 4 cross hairs, defining the corners of a .035 inch square (889μm x 889μm), as depicted in Figure 4.10 (a). Each line of a cross hair is 114.3μm long and 12.7μm wide, and the gold is approximately 1000 Å thick on a 200 Å chromium base. Complete details on how these alignment marks were fabricated are given in Appendix B. It is important to note that the alignment marks already existed on the substrate surface for the cleaning and resist application procedures described in the previous sections. Figure 4.10 (b) illustrates how the alignment marks are displayed on the SEM CRT display. The dimensions of the alignment pattern were chosen so that the cross hairs appear well within the outer edges of the CRT display, therefore reducing the possibility of alignment distortion. This also had the effect of easing the alignment process, since all four cross hairs could be kept in view when moving the specimen stage.

The alignment marks were placed 1mm to the left of the required circuit positions, as illustrated in Figure 4.11, using optical alignment techniques. The bevels on the left corners of the substrate serve to

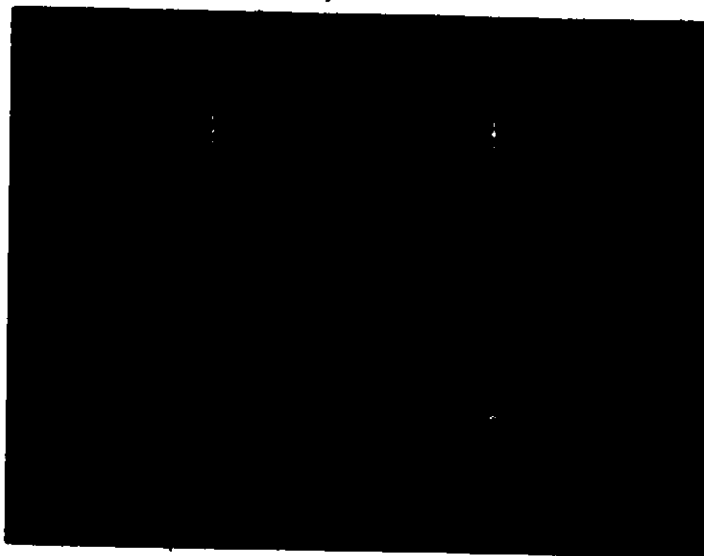


Figure 4.10 (a) X42 Photograph of gold alignment marks on substrate surface.

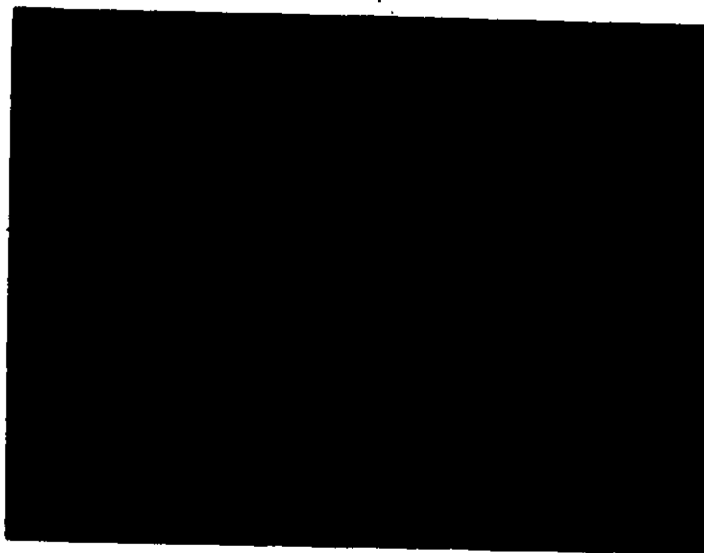


Figure 4.10 (b) X48 SEM photograph of alignment marks as they appear on SEM CRT display.

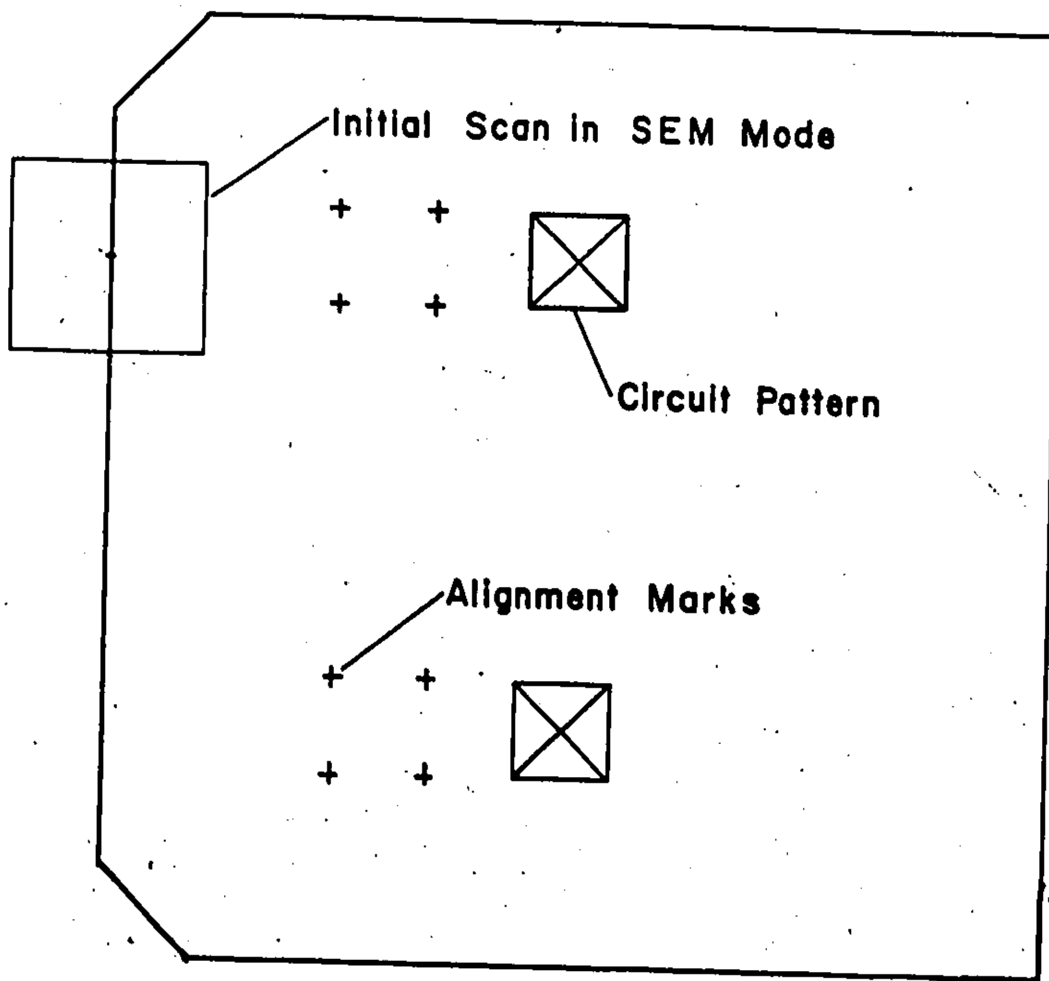


Figure 4.11 Alignment mark placement on 1cm x 1cm ST-X quartz substrate.

define the X-axis of propagation for ST-X quartz. When initially loading the substrate into the specimen chamber, a simple alignment gauge was used to sight the target area of the electron scan onto the upper left-hand edge of the substrate as depicted in Figure 4.11. With an initial magnification factor of x50, coarse focussing and alignment of the vertical edge were carried out. If the required working distance for lithography was set, and the image on the CRT display was grossly out of focus, then the z-axis micrometer adjustment on the specimen stage was used to bring the substrate surface into focus. Fine focussing was achieved by viewing a particle on the surface at x2000 magnification, usually the edge of the silver paint area, and adjusting the current to the third condenser lens. The stage was then moved to the left to bring the alignment marks into view, and centered on the CRT display. The SEM was then switched to the working magnification for lithography, which is x100 for a 1mm x 1mm field of view. At this point the pattern generator was readied for use by setting the external clock frequency to 200 kHz, and starting the alignment scan program which is resident in the monitor at location *022#000. This program produces a square perimeter line scan, whose dimensions correspond to the square defined by the alignment marks (889μm x 889μm). By switching manually from the SEM mode to the external scan mode several times, the alignment marks and square line scan appear simultaneously on the CRT display due to its long persistence. The alignment process consists simply of adjusting the pattern generator X and Y gain controls until the square perimeter-scan corners line up exactly with the alignment mark centres.

The alignment scan exposes the PMMA resist, and one method of

checking the alignment accuracy is to view the developed line scan in relation to the alignment marks under a microscope. With the alignment procedure finished, the SEM was left in the external scan mode and the alignment program was halted, which blanks the electron beam. The specimen stage was then moved 2mm to the left to position the beam axis over the centre of the circuit scan field.

4.4.3 Scanning the Pattern

The exposure current needed to fully expose a given area of PMMA coated substrate surface is given by:

$$i = \frac{A\ S}{t} \quad A \tag{4.4}$$

where A = the area covered by the beam in cm^2

S = the resist sensitivity in C/cm^2

t = time for scan to be completed in seconds

For the PMMA used in this work, $S = 10^{-4}$ C/cm, and the resulting time needed to expose the entire 1mm x 1mm scan field with the given beam current is

$$t = \frac{A\ S}{i}$$

$$= \frac{(10^{-2})(10^{-4})}{5 \times 10^{-10}}$$

$$= 33.3 \text{ minutes}$$

This is a very long time, and demonstrates the slow speed of PMMA resist. Most devices, however, require only a 10 to 15% coverage of the entire scan field area, which brings the scan time down considerably. Patterns requiring close spacing of lines can be scanned at even faster rates (or less beam current) due to the cooperative exposure effect.

In order to determine the scan speed (clock rate) that should be used to properly expose the PMMA, the information in Figure 4.2 (b) can be used as a starting point. Smith [3] and Wolf [26] have empirically determined the linear beam dosage for linewidths ranging from 1.2μm to several thousand angstroms. The resulting value of linear beam dosage is $b = 5 \times 10^{-9}$ C/cm for linewidths around 0.75μm wide, based on a silicon substrate. ST-X quartz is 13% more dense than silicon, and will therefore require slightly less beam current for proper exposure. Using the fact that the linear charge density is equal to the beam current divided by the beam velocity, one obtains

$$
\begin{aligned}
V &= i/b \qquad (4.5) \\
&= \frac{5 \times 10^{-10}}{5 \times 10^{-9}} \\
&= 1\text{mm/sec.}
\end{aligned}
$$

The resulting clock rate for the D/A converters is calculated by replacing the length unit in the velocity by the equivalent number of D/A steps or cycles. In this case, 16,000 steps represent 1mm, and hence the resulting clock rate is 16 kHz. The theoretical calculations for scan speed are only meant to give approximate indications, and it is

accepted standard procedure to make test scans covering an appreciable range of beam dosage about the theoretical value. Having set the external clock rate for the pattern generator, the pattern program was started and the circuit pattern was scanned and monitored at the same time on the SEM CRT display. Upon completion, the stage was moved to another site on the substrate for further scanning, after having first refocussed and re-aligned the beam if necessary.

4.5 Pattern Development

The first step in developing the exposed circuit pattern consists of removing the 400 Å conductive aluminum layer. This must be done quickly and with great care to avoid resist adhesion problems. A 10% solution of sodium hydroxide was used to etch away the aluminum layer, and this process was usually achieved in 10 to 15 seconds. The substrate was then rinsed with distilled water for one minute to remove all traces of the etch, followed by low pressure dry nitrogen drying. The substrates were supported with stainless steel triceps at all times to avoid surface damage and to ease their handling.

The PMMA developer used in this thesis work is referred to as 'standard developer' by Hatzakis [30], and consists of a 3:1 mixture ratio of isopropyl alcohol (IPA) to MIBK. Development times range from 45 seconds to 2 minutes, depending on the exposure conditions and minimum linewidth present in the pattern. Test batches must also be made at this stage in order to completely characterize the development process because of the unique factors associated with each device and procedure. The substrates were immersed into the developer, with no agitation taking

place, and were rinsed gently with IPA immediately upon completion of the development process. After the IPA rinse (about 10 sec.), the substrate was rinsed with distilled water for 30 seconds, and subsequently blown dry with dry nitrogen. The developed pattern was then checked with a high quality optical microscope (Zeiss Amplival pol. u) used in the reflection mode.

A 30 second spray of developer is commonly recommended [24] to succeed the initial resist pattern development by immersion. The function of this technique is to develop and rinse away stubborn scissioned molecules, expecially the ones at the exposed/unexposed interfaces. The spray technique was implemented by the author, but met with consistent poor results. The spray always caused complete over-development, and in most cases, complete removal of the entire resist film. The reason for this behaviour is that the type of spray required to perform the function is not specified in the literature, in regard to spray pressure, droplet size, nozzle to substrate distance, angle of application, and pulsed or continuous operation. Consequently, the spray pressure and droplet size were perhaps the reasons for failure of the technique when tried by the author. It is evident that a fixed and repeatable set-up is required for post development spraying, and since satisfactory results were obtained by the author without spraying, this particular area of investigation was not elaborated on. If a resist pattern is underdeveloped upon inspection, the substrate may be immersed in developer again, in order to completely develop the pattern.

4.6 Post Development Processing

The processing techniques used after pattern development are highly device dependent, and therefore a simple universal process cannot be generally applied. The definition of circuit or device patterns in a positive resist does, however, lend itself well to the lift-off technique. Sub-micron linewidth structures can be fabricated in one of two common ways; the etch process, or the lift-off process. A comparison of these two techniques is shown in Figure 4.12, for the particular case where the required circuit or device feature consists of a metallized array of lines. The key initial difference between the two techniques is that the etch process starts off with the required metal type and thickness already applied to the substrate surface before resist application. The resist coating, E-beam exposure, and development processes are identical for both techniques. The numbered arrows for the E-beam exposure indicate the order in which the lines were vector-scanned, in a direction perpendicular to the plane of the page. In the etching process, after development, the corresponding 'spaces' between the required array of lines are etched away into the metal layer. The etching technique may be dry or wet, but dry etching is usually preferred for sub-micron geometries, since it yields better results with less undercutting [31]. The resist on the surface of the substrate protects the metal underneath it from the etch process, and this metal then forms the desired circuit pattern after resist removal.

The lift-off technique relies on the slightly undercut profile of the resist after development for its successful operation. When evaporating the required metal onto the patterned surface, a discontinuity

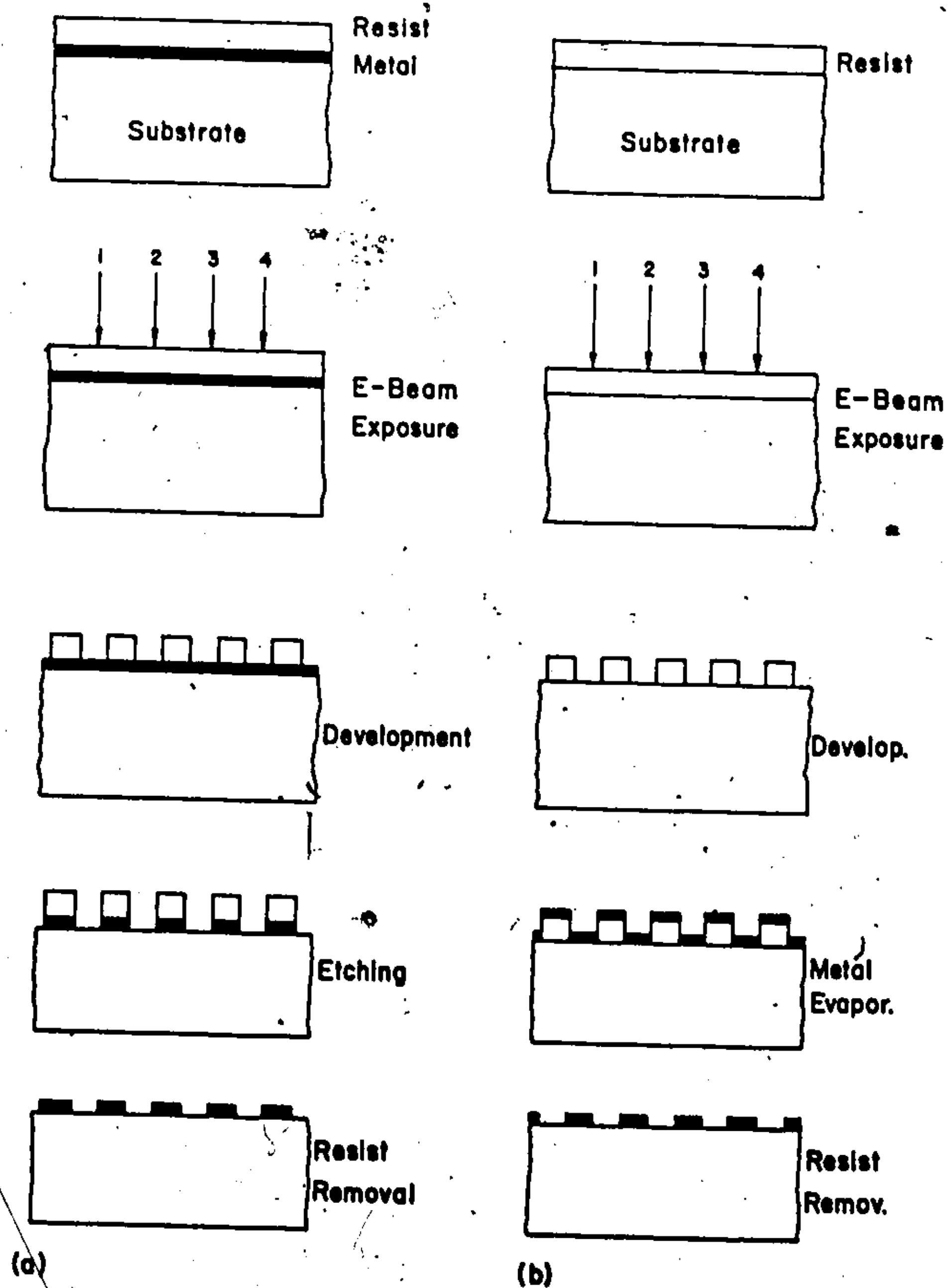


Figure 4.12 Sub-micron circuit fabrication techniques.
(a) Etch process.

(b) Lift-off process.

in the metal layer occurs wherever a line is exposed down to the substrate surface. When the resist layor is removed, only the metal which adhered to the substrate surface remains, thus realizing the required circuit features. This technique is successful only when the following criteria are satisfied [3]:

(a) the resist wall profile is either vertical or slightly undercut
(b) the metal thickness does not exceed 60% of the resist thickness
(c) the evaporated metal strikes the substrate surface at right angles

Lift-off with PMMA is accomplished by soaking the substrate in hot trichloroethylene. With mild agitation, the process takes about 5 minutes for complete resist removal. Some resist layers need up to several hours of soaking, and extremely stubborn layers may be ultrasonically agitated for very short periods (1 to 5 seconds). Extended ultrasonic agitation will eventually lead to device failure since the metal circuit features themselves will start to lift off from the surface.

The properties of PMMA satisfy the requirements of both the etch and lift-off fabrication techniques. Once the basic pattern is defined in the PMMA resist, a number of various processing techniques are available to the device designer, including substrate etching, thin film etching, selective ion implantation, and material evaporation. A combination of these techniques may also be applied, in the case of transistor fabrication, for example. However, this requires multiple patterning and consequent re-registration to the same alignment marks (covered with resist layers from previous exposures) in order to maintain pattern overlay accuracy. This latter technique has its own unique set of problems

associated with it, and will not be dealt with in this thesis.

4.7 Identification of Fabrication Problems

4.7.1 Pattern Generation Errors

A total of more than 200 circuits were scanned by the author in the process of characterizing the entire E-beam lithographic system. The equipment, as well as the processing techniques, had to be verified and characterized. Aside from the usual problems which plague electronic circuits and computer systems, one key error was discovered with the operation of the E-beam pattern generator from early tests. The cross-over point for the D/A converters was not a smooth transition, with more than the usual step value of one least significant bit occuring. The D/A crossover point occurs when enabling of the most significant bit from a previous condition of all ones (except the MSB) causes switching from the negative reference power supply to the positive one. The effect of this problem on a test circuit is illustrated in Figure 4.13. The test circuit consists of 200 fingers, each 7,500 Å wide, scanned with a 1.5μm periodicity in 4000 Å of PMMA. A distinct vertical line is noticed close to the centre of the array, which corresponds to a gap caused by the D/A cross-over. The problem was rectified by incorporating 10-turn trim potentiometers into the D/A converter electronics.

A persistent problem of pattern overexposure which lasted for several weeks was also traced to the pattern generator. The problem was found to be so obscure, that the author deems it important to mention its circumstances in this thesis. Although the pattern generator visually

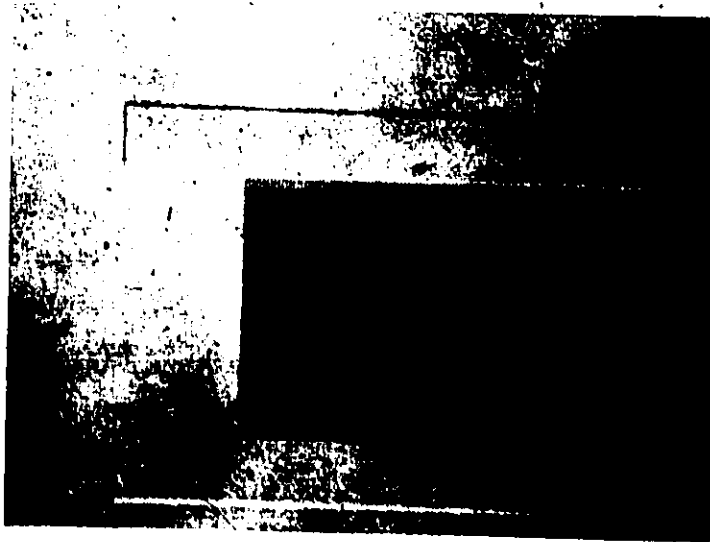


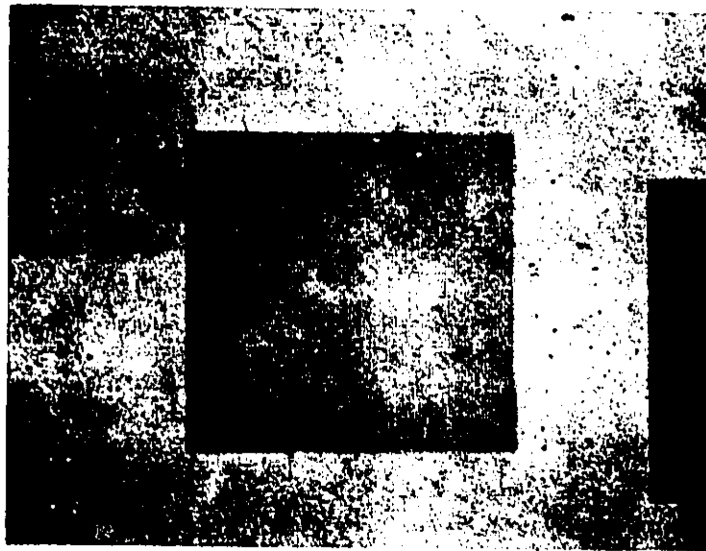
Figure 4.13 D/A converter zero-crossover defect in test circuit.

appeared to be scanning the circuit patterns properly, the least significant bit of the Y axis D/A converter was inactive. This caused the E-beam to sit at one particular scan point for twice the intended time, which of course overexposed that region, and undercut the resist profile right to the adjacent line scan. Upon development, all of the resist was consequently always removed. The problem was originally masked because of the low resolution monitoring equipment and the 'apparent' proper functioning of the pattern generator.

An initial grid scan was made to check for any scan field distortion which would limit the accuracy of circuits made with the system. The grid scan was programmed into the pattern generator, and consisted of a 100 x 100 array of 10μm squares, covering the entire 1mm x 1mm scan field. Figure 4.14 illustrates the grid scanned into a 4000 Å PMMA layer. The grid was observed with a high quality Zeiss Amplival pol. u microscope, and no appreciable pincushion or scanning distortion was noticed. Only a very slight widening of the scanned lines at the scan field perimeter was noticed.

4.7.2 Device Processing Problems

The test pattern used in characterizing the E-beam lithography system consisted of a 1 GHz SAW delay line, with finger width and spacings equal to approximately 7,500 Å. The pattern generator was initially programmed such that the electron beam was preset from one finished scan feature to the next. An example of this may be when the beam has just finished scanning the fingers on the input transducer, and is then preset



(a)

(b)

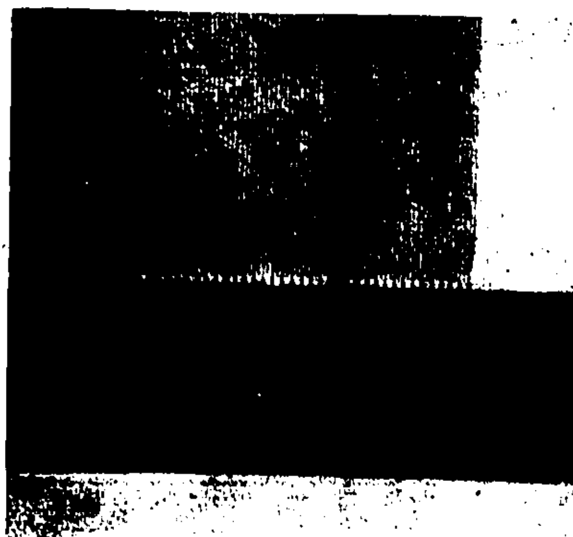
Figure 4.14 10μm grid scan in PMMA.
(a) X44 optical photo of entire field.
(b) X90 optical photo of upper left corner.

to the output transducer area for further scanning. Presetting of the beam over a distance of more than about 100μm caused beam lagging effects, as depicted in Figure 4.15. This lagging effect is caused by the limited speed of the electron deflection system and its associated support electronics. Figure 4.15 (a) shows the resulting effect on both the connection pad and the end finger of a metallized transducer. The problem can be alleviated by incorporating a software generated delay to match the deflection system response. An easier approach simply involves scanning the beam to the next location with the beam blanked, which was the approach used in this work.

Cooperative exposure effects became evident when scanning a large filled-in area adjacent to a sub-micron linewidth array. Figure 4.16 (a) illustrates this effect, and the overdose is seen to affect finger definition as far as 20μm from the connection pads. The finger scan was made at a 14 kHz clock rate, with a specimen current reading of 5×10^{-10} A. The pad scan was completed at a 12 kHz clock rate, with a specimen current reading of 7×10^{-10} A. The fingers were exposed first, and both exposures were made at an accelerating potential of 20 kV. The pads must be exposed with a lower dosage in order to avoid this problem.

A problem which plagued the device development process quite often was the lifting of the unexposed resist lines from the substrate surface. Figure 4.16 (b) illustrates the problem, which has been dubbed 'the spaghetti effect' by the author, due to its appearance. The resist lines in this case correspond to the spaces between the fingers of the final device. There are several factors which may singly or collectively cause the spaghetti effect:

(a)



(b)

Figure 4.15 X390 optical photographs illustrating beam-lagging effects (a) on both finger and pad, and (b) on end finger.

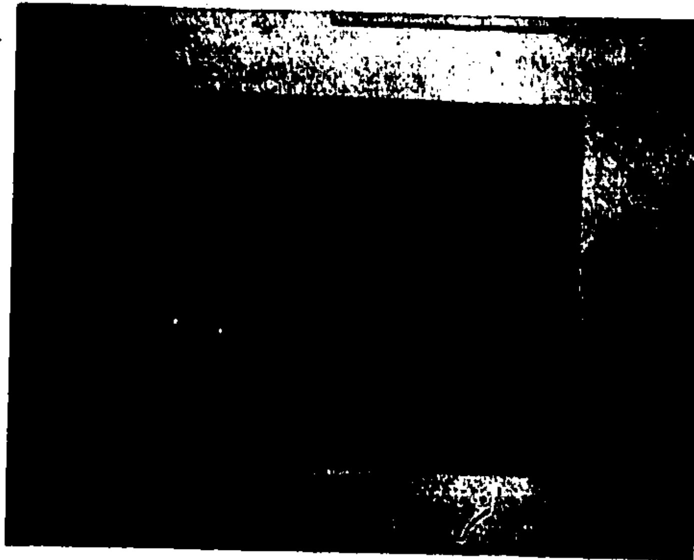


Figure 4.16 (a) Connection pad over exposure effects.

Figure 4.16 (b) The "Spaghetti" effect.

(a) overexposure of the fingers, where the negative slope profile undermines the resist line from both sides

(b) overdevelopment of the exposed pattern

(c) excess agitation or surface pressures encountered in the development process

(d) poor resist adhesion, due to a dirty substrate, poor substrate/resist adhesion properties, residual solvents or water in the resist layer, or improper baking procedures

Incomplete removal of the 400 Å conductive aluminum layer can cause severe problems with the development process. If a thin 50 Å layer of aluminum were to remain on the resist-covered surface, this would hinder the development of the pattern, resulting in longer development times, and usually ending with unsatisfactory results. Since these thin aluminum residues are difficult to detect visually, it is important to make sure that the sodium hydroxide (NaOH) etch has had sufficient time to remove the entire aluminum layer. Etch times in excess of 20 seconds should be avoided since this may adversely affect the resist adhesion to the substrate. A fresh filtered etch was made for each processing day, to avoid contamination of the resist surface before development.

The lift-off technique was used for the fabrication of the various circuit structures in this thesis. Lift-off is the last process step in completing the device fabrication, other than lead connection and packaging. Incomplete lift-off at this stage results in device failure, since short circuits are usually created between circuit structures as a result.

Examples of this problem are illustrated in Figure 4.17. Several possible causes for incomplete lift-off are:

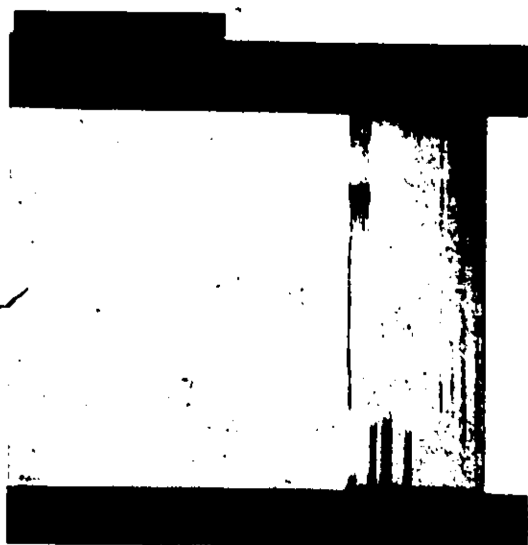
(a) deposited metal thickness is too great

(b) insufficient or no undercut in resist edge profile

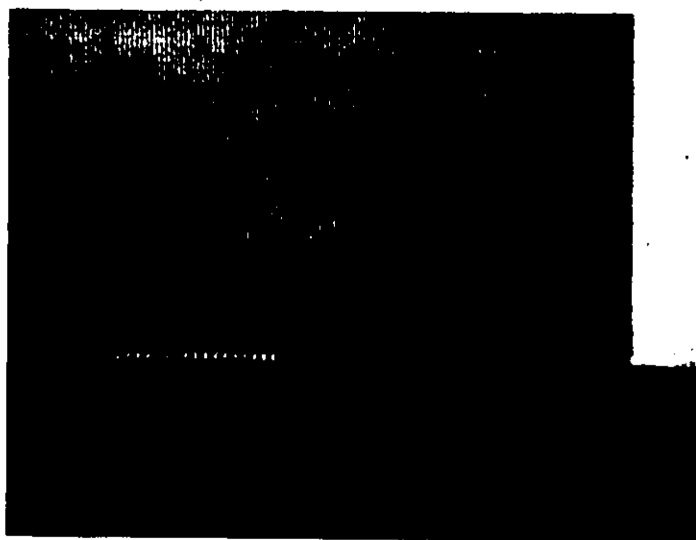
(c) metal is deposited onto surface at various angles other than perpendicular to the resist plane

(d) resist is baked too long after spin coating, causing excessive adhesion to the substrate surface

The lack of an undercut or straight resist profile is usually due to improper exposure conditions, but can also be caused by intense or prolonged heating during the metal evaporation process [30]. For this reason, the evaporation of the circuit metal(s) must be made as quickly as possible. In order to approximate perpendicular incidence of the evaporated metal onto the patterned resist layer, the distance between the evaporation source and the substrate surface should be relatively large (>30cm) if possible. A further problem occurs when two metals must be evaporated, since the source should ideally approximate a point source. To solve this problem, a special filament holder jig was implemented by the author, which is illustrated in Figure 4.18. Basket-type tungsten filaments were used to evaporate the various metals (gold, chromium, aluminum), and the holder allowed close positioning of the two filaments, with a metal shield separating them to prevent interaction and mutual contamination.



(a)



(b)

Figure 4.17 (a) Incomplete lift-off.

(b) Close-up of circuit in (a)

Figure 4.18 Internal view of vacuum chamber showing filament arrangement.

4.8 Conclusions

This chapter has dealt with the various aspects of electron resists, and in particular with PMMA. When PMMA is exposed by an electron beam, the resulting linewidth depends on:

(a) nature of the polymer

(b) linear charge density

(c) polymer film thickness

(d) substrate atomic number

(e) accelerating potential

(f) proximity of other exposed regions

The details of substrate preparation were presented, and can be summarized as follows:

(a) spin and vapour-clean substrate

(b) bake at 80°C for 1 hour

(c) apply PMMA resist by spin-coating at 4000 RPM

(d) post-bake substrates at 170°C for 20 minutes

(e) mount on specimen stubs with silver paint and cure

(f) evaporate 400 Å aluminum conductive layer onto resist

The details of the pattern exposure were also presented. The SEM parameter settings, used for the proper exposure of 7,500 Å lines in a 4000 Å PMMA layer over a 1mm x 1mm field, were as follows:

(a) 20 kV accelerating potential

(b) 5×10^{-10} A specimen current

(c) 12mm working distance

(d) 200μm final aperture

(e) condenser lens currents of 0.5, 0.54, and 0.62 A for first, second and third lenses respectively

(f) filament current of 2.4 A to saturate gun

(g) 100-140μA beam current for #4 bias setting

(h) beam diameter between 600-1000 Å

Procedures for alignment and pattern scanning were given, along with pattern development, which basically involved the following steps:

(a) remove substrate from specimen holder

(b) etch away Al layer in 10% NaOH

(c) develop in 3:1 IPA to MIBK for 45 seconds to 2 minutes, dependent on pattern and exposure conditions

(d) rinse with IPA for 10 seconds

(e) rinse with distilled water for 30 seconds

(f) blow dry with low pressure dry nitrogen

Several types of post development processing techniques were mentioned, with particular emphasis given to the lift-off technique. Finally, the problems which were encountered in the various stages of device fabrication were discussed, as well as the solutions which were applied by the author.

CHAPTER 5

APPLICATION: FABRICATION OF A 1 GHz SURFACE ACOUSTIC WAVE OSCILLATOR

5.1 Introduction

This chapter will begin with a brief introduction to the surface acoustic wave phenomena, and how this phenomena can be utilized to build delay lines, filters, and other structures. The fundamentals of delay-line type SAW oscillators will then be covered, leading up to the design implemented in this thesis. The design parameters for a 1 GHz delay line will be developed, along with considerations for testing and packaging. A complete and detailed fabrication summary will be given, including substrate preparation, SEM parameter settings, exposure conditions, and subsequent development procedures. Finally, test results of both the delay line and the oscillator will be illustrated and discussed.

5.2 Fundamentals of SAW Oscillators

The basic principles of surface acoustic wave devices can best be illustrated by referring to Figure 5.1. Two metallic interdigital transducers (IDTs) are positioned on the surface of a highly polished substrate, which have an aperture width W, and finger width d, and a periodicity of 2L, where L is the finger to finger centre spacing. These transducers usually consist of several thousand angstroms of aluminum, and connection pads are provided for interfacing to either a radio frequency (r.f.) source or an electrical load. The substrates used for SAW devices are piezo-

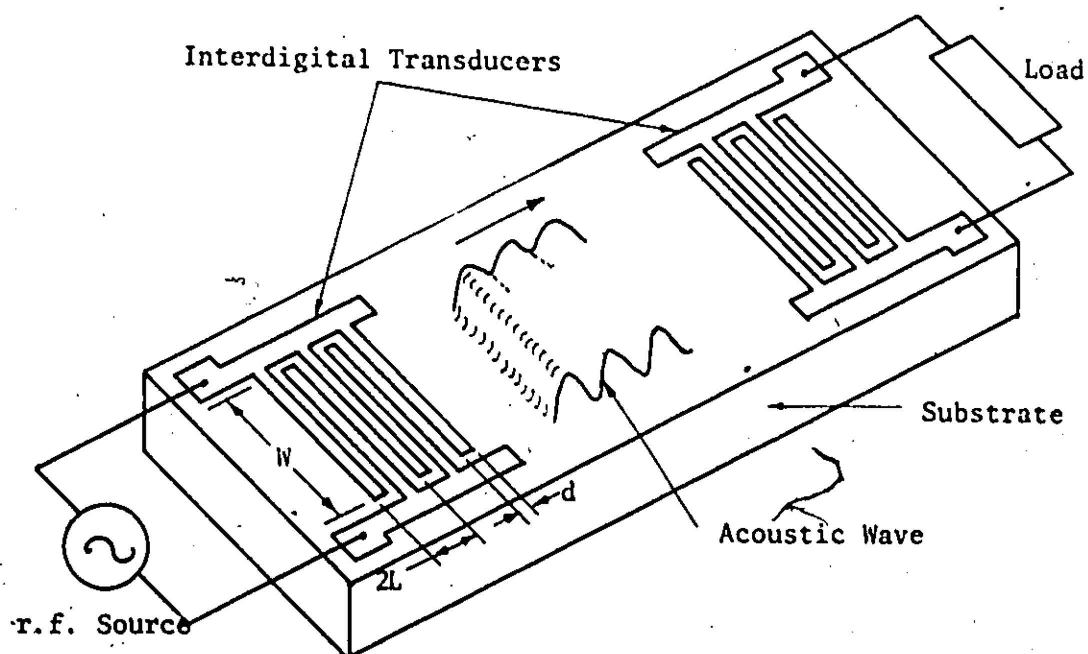


Figure 5.1 Schematic of basic generation and detection scheme for SAWs.

electric, and therefore electric field variations on or close to the surface induce corresponding mechanical or acoustic variations in the material. A device which allows or makes possible the controlled transfer of electrical energy into acoustic energy (and vice versa) is called a transducer. The IDT happens to be one specific kind of transducer which is best suited for the generation of acoustic waves on a piezoelectric substrate. If an alternating voltage source is applied to an IDT, the corresponding adjacent fingers will alternate in potential along with the driving source, and the resulting electric fields interact with the piezoelectric material to generate acoustic waves. The acoustic waves leave the transducer in a bidirectional fashion, and their period or wavelength understandably correspond to the period of the transducer fingers. Since the majority of the energy contained in the acoustic wave lies within several microns of the surface, the waves are referred to as surface acoustic waves. With the input IDT generating acoustic waves, an output IDT some distance away can be used to detect and reconvert the acoustic waves back to electrical signals. These signals can then be fed to a load for further processing and amplification.

The principle advantage of SAW devices is the relatively slow speed of the surface waves, a factor of 10^5 times slower than electromagnetic wave propagation. This means that relatively long delays can be realized in very short distances, which makes SAW delay lines quite attractive. Numerous other configuarations can be realized, including tapped delay lines, filters, convolvers and other specialized circuits [32], [33], [34]. The frequency range of operation for SAW devices extends from the low megahertz region to several gigahertz, and is

directly determined for a particular device by the period of the IDT, which corresponds to an acoustic wavelength. This fundamental relationship is given by:

$$f_o = v_a/\lambda_A \qquad (5.1)$$

where f_o = centre or synchronous frequency of operation in Hz

v_a = surface wave velocity in m/sec.

λ_A = acoustic wavelength (=2L) in metres

Table 5.1 illustrates several popular SAW substrates and their corresponding properties [32]. The piezoelectric coupling constant k^2 gives an indication of the transduction or coupling efficiency for a particular substrate. The long delay and zero (1st order) temperature coefficient of ST-X quartz make this substrate a suitable choice for oscillator applications. Various configurations exist for SAW oscillators [35] which utilize both delay line and resonator structures.

This thesis application concerns itself with the delay line type of SAW oscillator. Basically, a SAW delay line exhibiting a fixed and stable delay is put in the feedback loop of an amplifier with excess gain, and oscillation at the delay line centre frequency results. This configuration is illustrated in Figure 5.2. The loop is able to support a comb of frequencies for which the total phase shift around the loop is equal to an integer number of cycles or 2π radians, therefore:

$$\frac{2\pi f_A \ell}{v_a} + \phi_E = 2p\pi \qquad (5.2)$$

TABLE 5.1

Several SAW Substrates and Their Related Properties

Material	Crystal Cut and Orientation	Piezo-electric Coupling Constant k^2(%)	Acoustic Velocity v_a(m/s)	Delay Per Unit length (μs/cm)	Delay Time Temper-ature Coefficient (ppm/°C)
$LiNbO_3$	YZ	4.5	3488	2.87	91
$Bi_{12}GeO_{20}$	(111),(011)	1.7	1680	5.95	128
ZnO	basal	1.0	2700	3.70	40
$LiTaO_3$	YZ	0.74	3200	3.12	37
Quartz	YX	0.23	3170	3.15	-22
Quartz	ST,X	0.16	3150	3.17	0

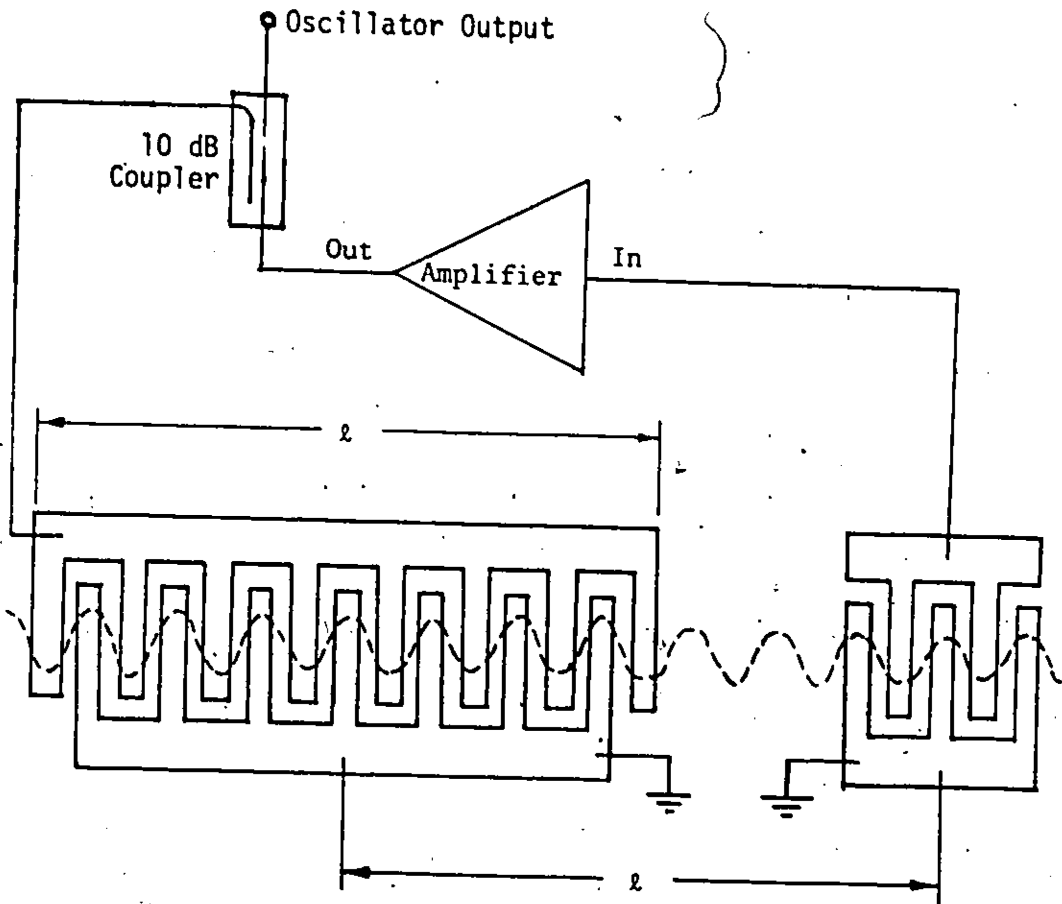


Figure 5.2 Schematic of basic SAW delay line oscillator.

where f_A = allowed frequencies of oscillation due to loop delay

ℓ = distance between phase centers of the two IDTs in acoustic wavelengths (metres)

ϕ_E = electronic phase shift due to amplifier in radians

p = positive integer $\neq 0$

The first term in (5.2) represents the total phase shift in the SAW delay line, and this value is usually quite large (several hundred 2π radians) in comparison to the amplifier phase shift ($<2\pi$). Hence, the total loop delay is determined primarily by the SAW device, and neglecting ϕ_E, the allowable oscillation frequencies are:

$$f_A \simeq \frac{pv_a}{\ell} \quad \text{Hz} \tag{5.3}$$

If the delay line had all-pass filter characteristics, then the loop would oscillate at all the frequencies which satisfy (5.3), given the appropriate wideband amplifier. However, a uniform, constant aperture, non-apodized IDT pair exhibit a limited bandwidth frequency response, which has the form [36]:

$$E(x)^2 = \left[\frac{n \sin x}{x}\right]^2 \tag{5.4}$$

where $E(x)^2$ = amplitude response of delay line

n = number of fingers in IDT

$$\text{and } x = \frac{n\pi}{2}\left[1 - \frac{f}{f_o}\right] \text{ radians} \tag{5.5}$$

Therefore, the simple SAW delay line exhibits a sinc-function type frequency response. This inherent bandpass characteristic can be used to select a single frequency operating mode for the delay loop. To choose the operating frequency, the delay line response is simply centred on f_o (the desired frequency), yielding an acoustic wavelength from (5.1) of v_a/f_o. To ensure that the neighbouring loop modes are sufficiently suppressed, the delay line is designed such that the nodes of the sinc frequency response fall exactly in the positions of the adjacent allowable frequencies, when viewed in the frequency spectrum. In order to achieve this condition, the nodes of the response must first be determined from (5.4). The nodes of (5.4) occur when $x = m\pi$, where m is an integer $\neq 0$. Using this relation in (5.5), the result is:

$$m\pi = \frac{n\pi}{2}\left[1 - \frac{f_n}{f_o}\right]$$

$$f_n = f_o\left[1 - \frac{2m}{n}\right] \tag{5.6}$$

where f_n = frequencies where nodes occur in sinc response

Letting $N = n/2$ represent the number of finger pairs in the transducer, or alternatively, the length of the transducer in acoustic wavelengths, then (5.6) becomes:

$$f_n = f_\circ\left[1 - \frac{m}{N}\right], \quad m \neq 0 \tag{5.7}$$

The above equation demonstrates that the distance between adjacent nodes for the sidelobes of the frequency response is $f_\circ/N$. In order to position these nodes at the adjacent allowable frequency positions, the interval between allowable loop frequencies must be made equal to the node interval. The loop frequency interval is obtained from (5.3) as v_a/ℓ, and equating to the node interval:

$$v_a/\ell = f_\circ/N$$

$$\ell = N\lambda_\circ \tag{5.8}$$

Equation (5.8) describes the principle criterion for suppression of mode ambiguity in the delay line oscillator, which is to make the delay pathlength between the transducers equal to the length of the input transducer. Figure 5.3 shows the typical normalized response of the SAW delay line, and also illustrates the mode suppression principle.

The output transducer is usually a wideband design incorporating fewer fingers, since the input transducer response is used to determine the frequency selectivity. Also, the mode suppression constraint dictates a shorter output transducer to prevent second order effects due to close proximity of input and output IDTs. The amplifier used in the feedback loop should demonstrate high power and low noise capabilities, in order to obtain a strong, clean output spectrum. A directional coupler can be used on the output of the amplifier to increase the power output capabi-

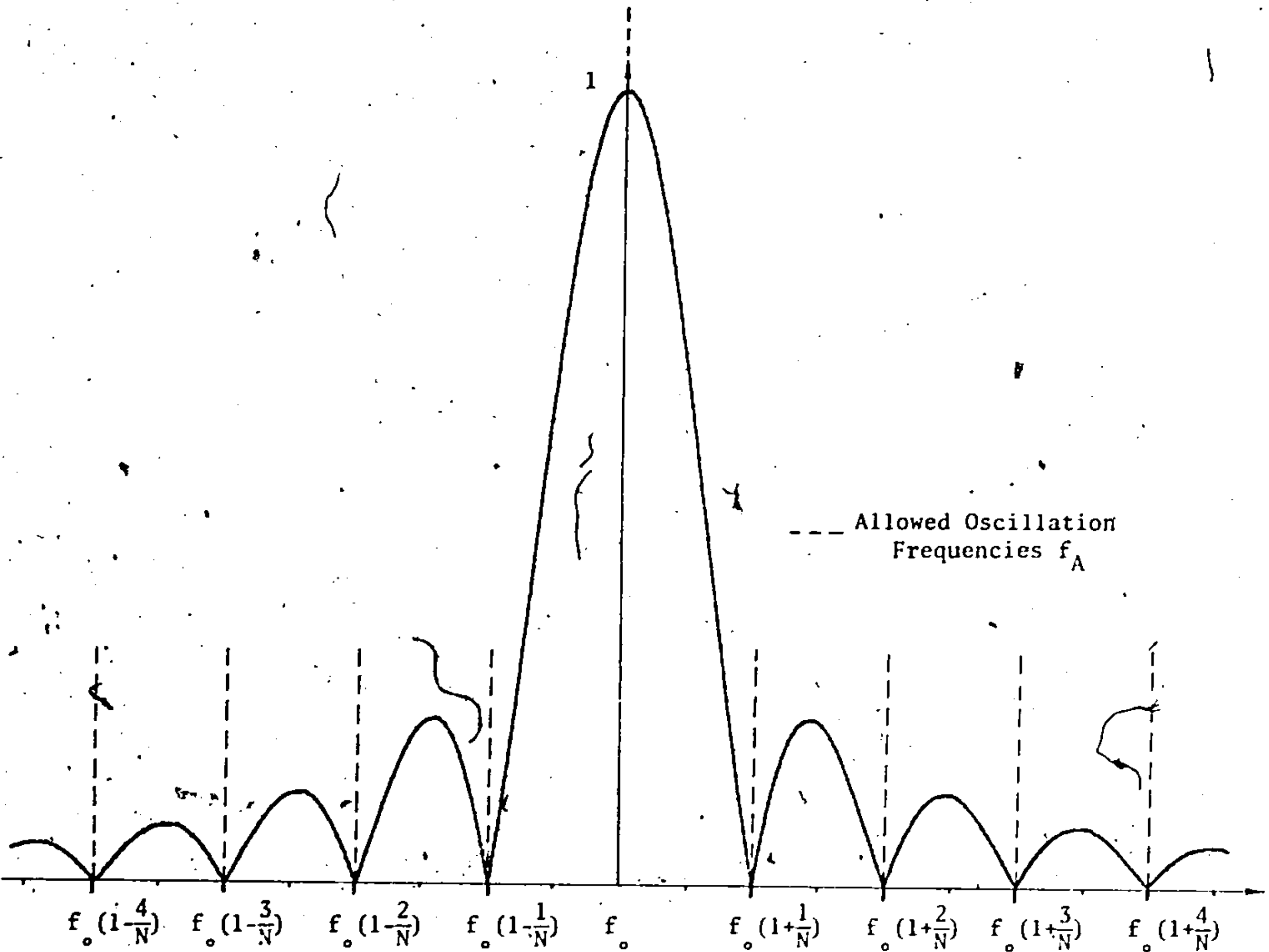


Figure 5:3 Normalized response of SAW delay line showing mode suppression principle.

lity of the oscillator, and to provide some isolation. Further details on the SAW delay line oscillator regarding substrate specifications, amplifier considerations, stability criteria, matching, and second order effects may be found in [36].

5.3 Design Parameters for 1 GHz Delay Line

Delay line SAW oscillators offer distinct advantages over resonator type structures at frequencies in the gigahertz range, and this accounts for their popular use in this region [37]. The advantages of much higher Q's for resonator structures in the lower megahertz region are offset at 1 GHz due to the increased losses for resonator structures. The fine tuning and modulation capabilities of the delay line oscillator also influence its choice for this frequency range.

It was decided to implement a $200\lambda_A$ delay line, with a $40\lambda_A$ length output transducer. These design parameters led to a 75% coverage of the scan field length, which was considered adequate in determining the lithography system's accuracy. Rather than centre the design exactly at 1 GHz, a more convenient acoustic wavelength was initially chosen, such that subsequent measurements could be made more easily. A wavelength of 3μm was chosen, which from (5.1) yields

$$f_\circ = \frac{3,150}{3 \times 10^{-6}} = 1.05 \text{ GHz} \qquad (5.9)$$

The 3μm wavelength implies 7,500 Å space and finger widths for a unity mark/space ratio. The parameter N has already been chosen equal to 200, which leaves only the aperture width W to be determined. The aperture of

the input transducer was chosen to yield a reactive impedance equal to 50Ω at the synchronous frequency, which resulted in the minimum untuned insertion loss [38]. Hence, from the work of Slobodnik [39]:

$$\frac{1}{j\omega_o C_T} = 50$$

$$C_T = 1/100\pi f_o \tag{5.10}$$

$$W = \frac{C_T}{C_{FF} N \lambda_o} \tag{5.11}$$

where C_T = static capacitance of transducer in pF

C_{FF} = capacitance per unit length of a single period for unity mark/space ratio, in pF/m

= 50.8 pF/m for quartz

λ_o = acoustic wavelength of synchronous frequency

W = aperture width in wavelengths

Substituting (5.10) into (5.11), and using the given parameters, the aperture width becomes:

$$W = 1/100\pi C_{FF} N v_a \tag{5.12}$$

$$= 100 \text{ wavelengths}$$

where N = 200 finger pairs or acoustic wavelengths

This concludes the theoretical design of the SAW delay line, and considerations for connection pads and packaging will be covered in the next section on device fabrication. A summary of the designed parameters for the delay line is given in Table 5.2.

5.4 Fabrication Summary

The 1cm x 1cm ST-X quartz substrates were cleaned and coated with PMMA using the same procedure outlined in Chapter 4, section 4.3. A resist thickness of 4000 Å was chosen to ensure a successful lift-off technique, with metal thicknesses of no more than 1200 Å being applied.

The SEM parameter settings which were used for the successful exposure of the 1 GHz SAW delay line are as follows:

Accelerating voltage:	20 kV
Filament current:	2.4 A (saturated)
Beam current:	135μA @ bias #4
Lens currents:	Condenser #1 → 0.51 A Condenser #2 → 0.54 A Condenser #3 → 0.62 A
Working distance:	11.8mm
Magnification:	x 96.5 (for x100 setting)
Final aperture:	200μm
Specimen current:	5×10^{-10} A
Finger scan rate:	16.5 kHz
Pad scan rate:	13.0 kHz

A specialized computer program was written to scan the required SAW delay line pattern, rather than utilizing the general-scan format program resident in the monitor. This decision was prompted by the

TABLE 5.2

Summary of SAW Delay Line Design Parameters

Parameter	Value
Centre Frequency:	1.05 GHz
Acoustic Wavelength:	3.0μm
Delay Pathlength:	$200\lambda_o$
Delay Line Aperture:	$100\lambda_o$
Finger Width:	7,500 Å
Mark/Space Ratio:	1
Input Transducer	
Length:	$200\lambda_o$
No. of Fingers:	400
Output Transducer	
Length:	$40\lambda_o$
No. of Fingers:	80

simplicity and repetition inherent in the required pattern, and program loops were used extensively in the software. The resulting length of the program was shorter than the equivalent size of memory which would have been needed to store all the individual pattern data points. Total scan time for the entire circuit was 3.5 minutes, and a halt was incorporated at the end of the finger scan to allow changing of the scan speed (clock rate) for the connection pads. The delay line connection pads were scanned in a raster fashion, with a 1μm incrementing distance between adjacent line scans, and at a slower scan rate to ensure complete resist removal. The scanned substrates were subsequently immersed in a 10% NaOH solution for 12 seconds, and then developed in the standard PMMA developer for 95 seconds. The development procedure which was used is outlined in Chapter 4, section 4.5.

The developed pattern in PMMA resist is shown in Figure 5.4. The horizontal finger connection pads for the larger input transducer measure 642μm x 60μm, while both sets of the protruding pads measure 162μm x 162μm. Figure 5.4 (b) is a SEM photograph showing the exposed line structure at the connection pad interface. The light-coloured areas in the photograph correspond to the PMMA resist, while the darker areas correspond to the substrate surface from which the exposed resist has been developed away. The angled line in the top right corner of the picture is the end of the 60μm connection pad. Figure 5.5 illustrates the excellent definition which can be obtained using E-beam lithography. These SEM photographs are close-ups of the finger structure near the connection pad, taken from the device illustrated in Figure 5.4 (a). It can be noted that there is no discernable waviness or irregularity associated with the

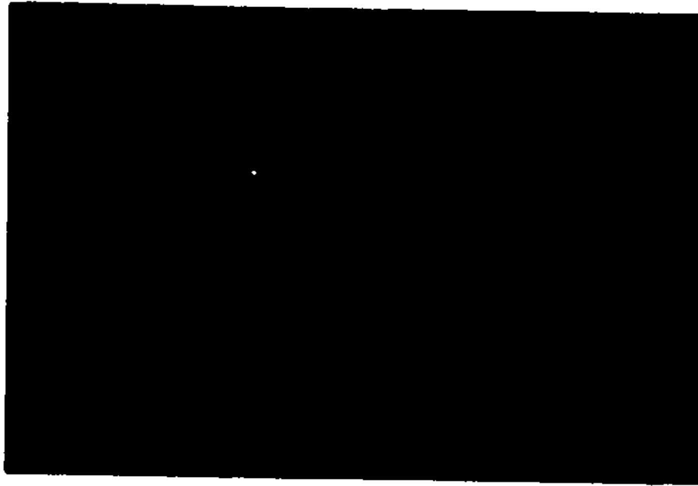


Figure 5.4 (a) Developed pattern of 1 GHz SAW delay line (x 45)

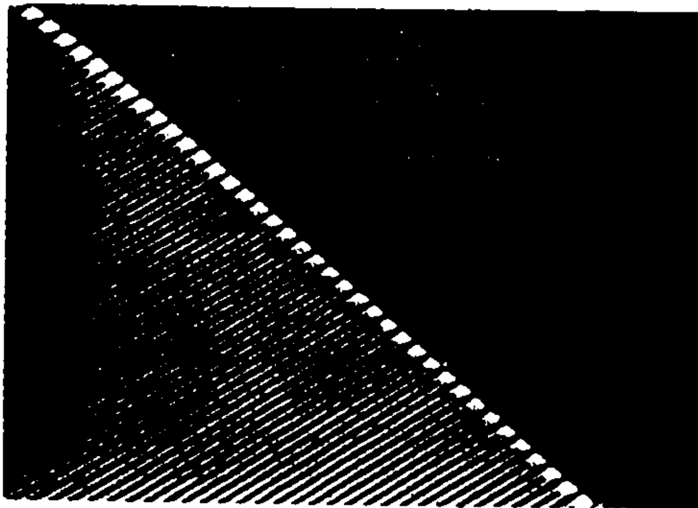
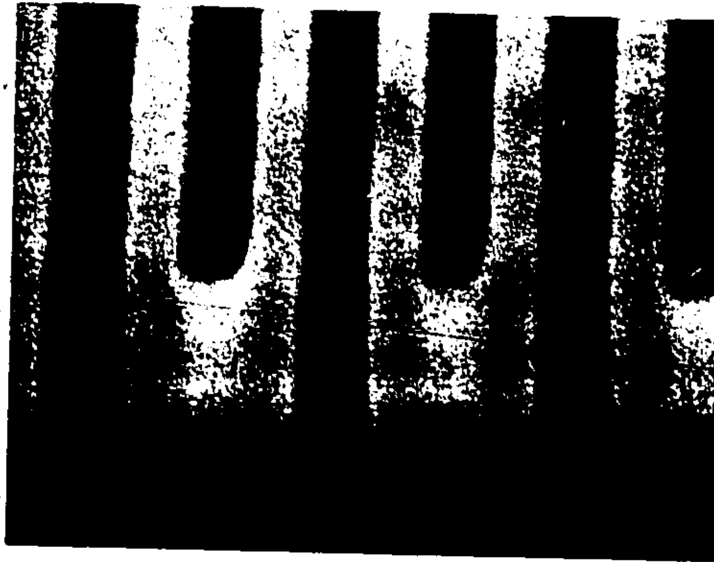


Figure 5.4 (b) x 980 SEM photo of finger and pad area.



(a)

(b)

Figure 5.5 SEM photos illustrating exposed finger areas near pad. (a) x 10,600 (b) x 21,200

walls of each line scan, qualities which usually plague photolithographic exposures.

Measurements were performed on each completed exposure to determine the accuracy of the alignment process. In all cases, the Y-axis alignment was excellent, as observed by the intersection of the horizontal alignment scans (now visible after development) with the centres of the alignment cross hairs. This observation was made with a microscope which has facilities for measuring observed dimensions (eg. calibrated graticule). Smith [3] has determined that alignment accuracies of 0.1% can be obtained using the visual alignment procedure outlined in section 4.4.2 of Chapter 4, for a 1mm x 1mm scan field. Measurements made on the delay-line period and linewidths indicated a deviation from the design dimensions. The observed linewidth was 7,680 Å instead of the predicted 7,500 Å. Measurement of the X-axis alignment scan indicated that the X-axis was aligned to 910μm instead of the required 889μm, corresponding to a 2.4% error. This behaviour was noticed for four separate scans and alignment procedures, even though the SEM CRT display indicated exact alignment each time. It was concluded that there was a calibration error in the X channel of the SEM electronics, which was never corrected for any of the work presented in this thesis.

Aside from the aforementioned problem, the resulting patterns met all specifications. The mark/space ratio is unity for all practical purposes, as evidenced by Figure 5.5 (b). As soon as possible after development, the substrates were put in a vacuum coating unit (Edwards Model 12 E), preceded first by a 15 minute bake cycle at 80°C to remove any residual moisture. At a pressure of 5 x 10^{-6} torr, chromium was first

evaporated, using a filament current of 30 A for approximately 5 minutes. A 200 Å layer of chromium was deposited to improve the adhesion characteristics of the aluminum to the substrate [40]. The evaporation of the chromium was followed immediately by evaporation of a 700 Å layer of aluminum. Thickness determination of the evaporated layers was made by incorporating a bulk wave resonating crystal inside the chamber, and monitoring the change in oscillator frequency as the metal is evaporated [41]. The evaporation must be done quickly and efficiently in order to avoid excess heat build-up inside the chamber, which could result in degradation of the resist profile, causing subsequent device failure at the lift-off stage. The substrates were always carefully centred exactly above the evaporation sources, and at a height of 26cm, which was limited due to the bell jar dimensions.

Upon removal from the vacuum coating unit, the substrates were placed in hot trichloroethylene (~80°C), and the lift-off process was usually completed within 5 minutes. Stubborn resist lines were removed with 1 or 2 second intervals of ultrasonic agitation. A 1 minute distilled water rinse, followed by dry nitrogen drying completed the device fabrication, except for the connection leads. The protruding connection pads were initially intended for gold wire bonds, however, the author experienced hardships in attaining good bonds with the available equipment. The extremely thin oxidized aluminum pads and the fragile finger structure could not sustain the acoustic bonding energy needed to make a good bond, with bonding attempts usually resulting in complete destruction of the circuit features. Alternatively, a second set of connection pads were fabricated using photolithographic techniques, which interfaced with the

delay line pads and brought these four connections out to large, readily accessible pads on the edge of the substrate. Hence a two stage or level processing technique was required to yield the final device. The second stage involved making a flexible mask from a rubylith master, and using the conformable mask exposure technique, along with photo lift-off to fabricate the extension pads. The procedure which was used follows that given in Appendix B very closely, where the alignment mark fabrication is outlined. The flexible chromium mask of the extension pads, along with the conformable mask vacuum jig, are illustrated in Figure 5.6 (a).

A 3cm x 3cm aluminum circuit frame with OSM type terminations was used to house the SAW delay line. The substrate was fixed onto a copper circuit board by means of General Electric #102 RTV sealant. The circuit board was designed and constructed such that 50Ω microstrip transmission lines formed the connection between the OSM terminations and the substrate. Fine gold-plated wire was used to connect the delay line to the 50Ω microstrip lines and the ground planes. Silver paint was used for connections on the substrate surface, while all other connections were soldered. Figure 5.6 (b) illustrates the final packaged delay line. The four machine screws were used to ensure a good ground connection from the metal case to the ground plane on the surface of the copper circuit-board.

5.5 Test Results

The frequency response of the SAW delay line was measured using a Hewlett Packard (HP) 8555 A spectrum analyzer in conjunction with an HP 8444 A tracking generator. The resulting frequency response is illustrated in Figure 5.7. The dip anomaly in the main lobe of the sinc

Figure 5.6 (a) Chromium mask for extension pads, with exposure jig.

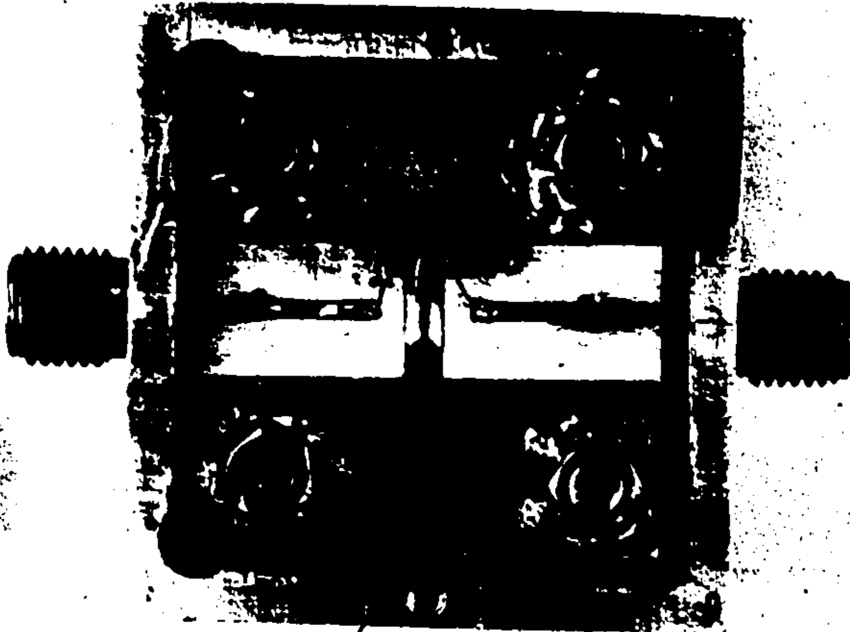
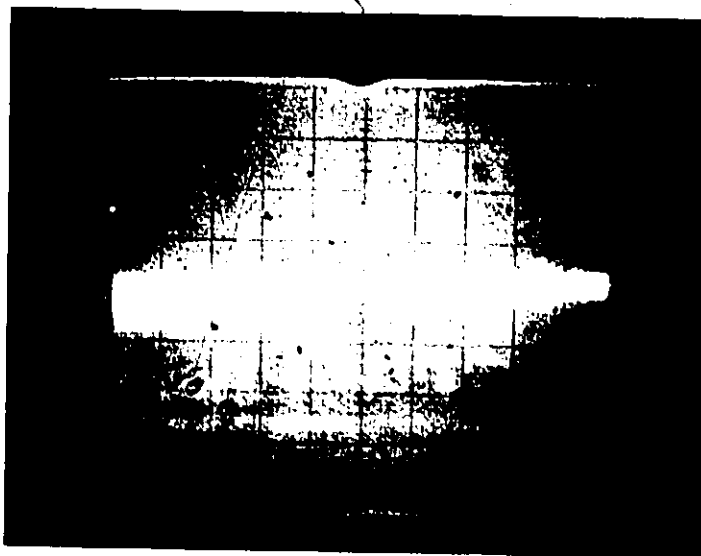
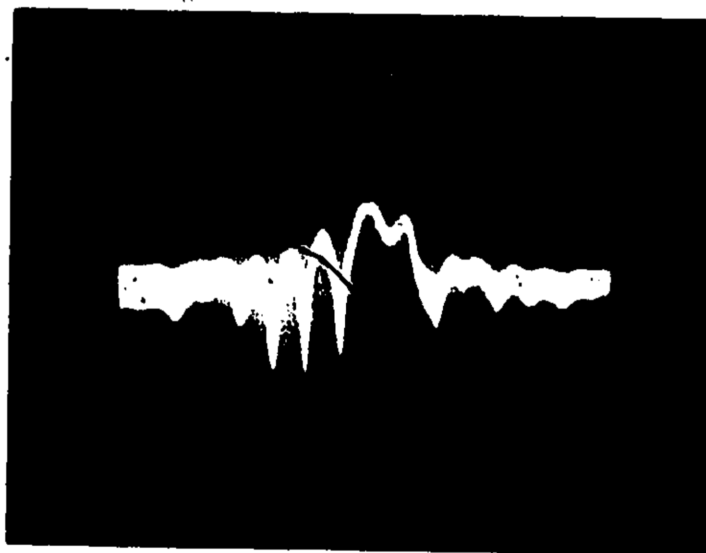


Figure 5.6 (b) SAW delay line mounted in 3 cm x 3 cm test package.



(a)



(b)

Figure 5.7 Frequency response of SAW delay line.
Log reference: 0 dB
Vertical: 10 dB/div.
Bandwidth: 300 kHz
Horizontal: (a) 20 MHz/div.
(b) 5 MHz/div.

response, as well as in the first higher sidelobe, will be discussed later in this section. The delay line centre frequency was determined by utilizing the manual scan facility on the tracking generator to position the output frequency right at the peak of the response. Having accomplished this, the output frequency of the tracking generator was measured with an HP 5340 A frequency counter. The centre frequency measurement was 1.0183 GHz. The expected centre frequency, allowing for the alignment error and based on the actual acoustic wavelength measurements, was 1.0254 GHz, yielding a 0.7% error. Mass loading of the surface wave was not accounted for in the design, although the aluminum layer was made quite thin. It is also anticipated that a slight upward shift in the centre frequency would occur if the dip anomaly were not present.

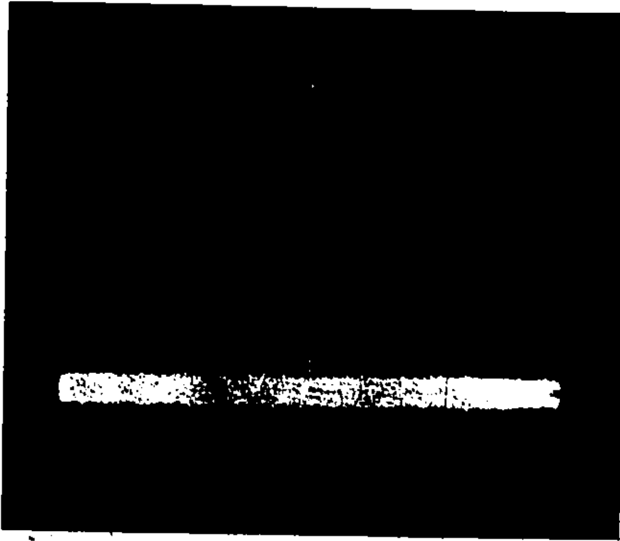
The measured insertion loss of the delay line at the centre frequency was 24.3 dB, which is quite respectable for an unmatched delay line at this frequency. The delay line was then matched, using single stub tuning, to determine the minimum insertion loss possible. By matching the output transducer only, (using 50Ω air line) a total insertion loss of 19.5 dB was achieved. Single stub tuning can be a useful planar technique for matching narrowband SAW transducers to 50Ω systems, and further details are presented by the author in [42].

The dip anomaly in the frequency response was repeated in three separate test circuits, although no readily visible defects could be observed in the developed patterns. The placement accuracy of the delay line fingers was suspected, and this prompted the testing of the X-axis D/A converter. The microcomputer was programmed to step slowly through the SAW delay line program, while the output voltage of the X-axis D/A

converter was being accurately measured and recorded. An HP 3450 A multi-function meter was used to measure the voltages, and a displacement error of almost 4 LSB was found to occur whenever the 'second' most significant bit changed. This resulted in almost 40 of the input transducer fingers being displaced by approximately 2,300 Å relative to the rest of the fingers. This offset would definitely cause phase cancellations at certain frequencies, and is most likely the sole cause of the dip anomaly observed in the frequency responses. The D/A converter error could not be corrected without resorting to a number of circuitry changes, and new D/A units could not be made available before the completion of this thesis work.

For SAW oscillator purposes, the shape of the delay line frequency response is not critical, as long as the response has a major peak, with sidelobe and spurious levels well below the peak value. An oscillator was implemented by incorporating the delay line in the feedback loop of an HP 8447F preamplifier/poweramplifier. A Narda Model 4012C-10 10 dB directional coupler was used at the amplifier output to couple the appropriate signal level back into the loop. A Kay Elemetrics Corp. Model 461B switchable attenuator was used to adjust the proper loop gain level, such that oscillation just occurs. The test set-up for observing and measuring the output power spectrum of the SAW oscillator is illustrated in Figure 5.8. The measured spectrum is illustrated in Figure 5.9. The power output of the SAW oscillator was +6 dBm into 50Ω. Figure 5.9 (a) demonstrates the absence of spurious modes from 500 MHz up to 1.5 GHz, and Figure 5.9 (b) gives an indication of the oscillator stability. Further tests were not made, since the oscillator was not fabri-

Figure 5.8 Test set-up for measuring SAW oscillator output spectrum.



Log Reference: +10 dBm

Vertical: 10 dB/div.

Horizontal: 100 MHz/div.

Bandwidth: 300 kHz

Log Reference: +10 dBm

Vertical: 10 dB/div.

Horizontal: 2 kHz/div.

Bandwidth: 0.3 kHz

Figure 5.9 Output power spectrum of 1 GHz SAW oscillator.

cated as a complete functional unit, but only used to demonstrate the behaviour and potential of an E-beam produced SAW delay line.

5.6 Conclusions

The basic characteristics of surface acoustic waves have been presented, and properties of the SAW delay line have been developed. The advantages and features of SAW delay lines were discussed in relation to their ideal application to delay line oscillators. Design details were then derived for a 1 GHz SAW delay line oscillator, followed by a description of the fabrication steps involved in building the delay line. Test results were presented for both the delay line response and the oscillator spectral response. The excellent resolution and contrast produced by E-beam lithography has been demonstrated by the developed patterns of the delay line. An error in the lithography system operation was detected, based on analysis of the delay line frequency response. A 4 LSB shift was detected in the X-axis D/A converter operation, which had the effect of offsetting an entire section of the pattern by 2,300 Å. Correction of this problem will yield an accurate and functional pattern generator design. A minor calibration error in the SEM X-channel processing electronics was also detected, and correction of this problem will ensure a repeatable and accurate alignment procedure.

CHAPTER 6

FURTHER EXPERIMENTAL STUDIES

6.1 Introduction

This chapter deals with the scanning of various patterns other than the 1 GHz SAW delay line, in order to further demonstrate the flexibility and operation of the designed pattern generator. Results for a 2 GHz SAW delay line scan will be given, along with the fabrication parameters used in its development. The definition and scanning of patterns by means of the monitor program will be covered, and the scanning of alphabetical letters will be used to demonstrate this process. Finally, a bubble memory circuit structure was scanned on a substrate, and made use of a pattern shape subroutine to achieve data compaction and shape flexibility. A section follows which summarizes the pattern generator characteristics, and possible modifications to the basic design, as well as its future potential, are also discussed.

6.2 2 GHz SAW Delay Line

It was desired by the author to test the ultimate resolution capability of the E-beam lithography system. This was achieved by scanning a 2 GHz version of the 1 GHz SAW delay line, which was already fabricated, and is covered in the previous chapter. Several simple modifications had to be made in order to successfully scan the higher frequency delay line. The first was to set the magnification setting

on the SEM to x200, since all dimensions would be exactly one half of their previous value for the 1 GHz design. The other consideration was the required scanning speed. A factor of two increase in scanning speed was immediately evident since the new scan field was half the size (½mm x ½mm), and the resulting single bit resolution was 312.5 Å. A further correction in the linear scanning speed was necessary, however, due to the increased effects of cooperative exposure. A summary of the SEM exposure parameters used for the 2 GHz delay line scan follows:

Accelerating voltage:	20 kV
Condenser lens currents:	#1 → 0.48 A #2 → 0.54 A #3 → 0.60 A
Filament current:	2.4 A (saturated)
Beam current:	166μA at bias #4
Magnification:	x192 (x200 setting)
Working distance:	11.8mm
Final aperture:	200μm
Specimen current:	5×10^{-10} A
Finger scan rate:	36 kHz
Pad scan rate:	32 kHz

The development procedure was similar to the one used for the 1 GHz device, with the only exception being the shorter development time of 50 seconds for the 2 GHz delay line exposure. Figure 6.1 illustrates the resulting patterns obtained in the 4000 Å PMMA resist layer. The results appear promising for the ability to scan 3000 Å linewidths routinely, with some additional research needed in the area of optimum apertures, working distance, lens currents, and beam dosages. It was observed that

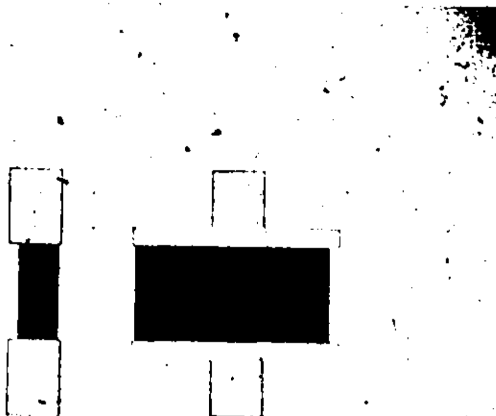


Figure 6.1 (a) x900 photograph of 2 GHz SAW delay line pattern in 4000 Å PMMA.

Figure 6,1 (b) x9,800 SEM photo of 3000 Å finger structure of delay line in (a)

the exposure parameters for these closely-spaced narrow linewidths were very sensitive, and had a small, limited range for proper development. Development times also became more critical and generally shorter in duration. Figure 6.2 illustrates the appearance of the developed test circuits on the substrate surface, and also shows the alignment-scan lines on the top right section of the substrate.

6.3 General Format Scanning

In order to demonstrate the use and flexibility of the pattern generator monitor program, an alphabetical pattern was designed. The letters were drawn on a grid, after the height and line thickness were chosen. The decimal coordinates of each letter (somewhere in the 16,000 x 16,000 pattern coordinate grid) were then entered directly into the pattern generator microcomputer by means of the keyboard/display unit. Total data entry time for the six alphabetical letters was approximately 2 minutes. By subsequently loading the general format scan program, the required pattern was monitored on a CRT storage oscilloscope. The correct data was then loaded onto cassette tape for permanent storage. The pattern was then scanned onto a 4000 Å PMMA-covered substrate, the results of which are illustrated in Figure 6.3 (a). The letters are 10μm high, with 1μm linewidths. This procedure has illustrated the simplicity of pattern data entry, as well as the pattern complexity and variety which are possible, by using the resident monitor program to generate the desired scan pattern. The further advantage of a fast turn-around time between the data specification on paper, and its final implementation in scanning a pattern, was also demonstrated.

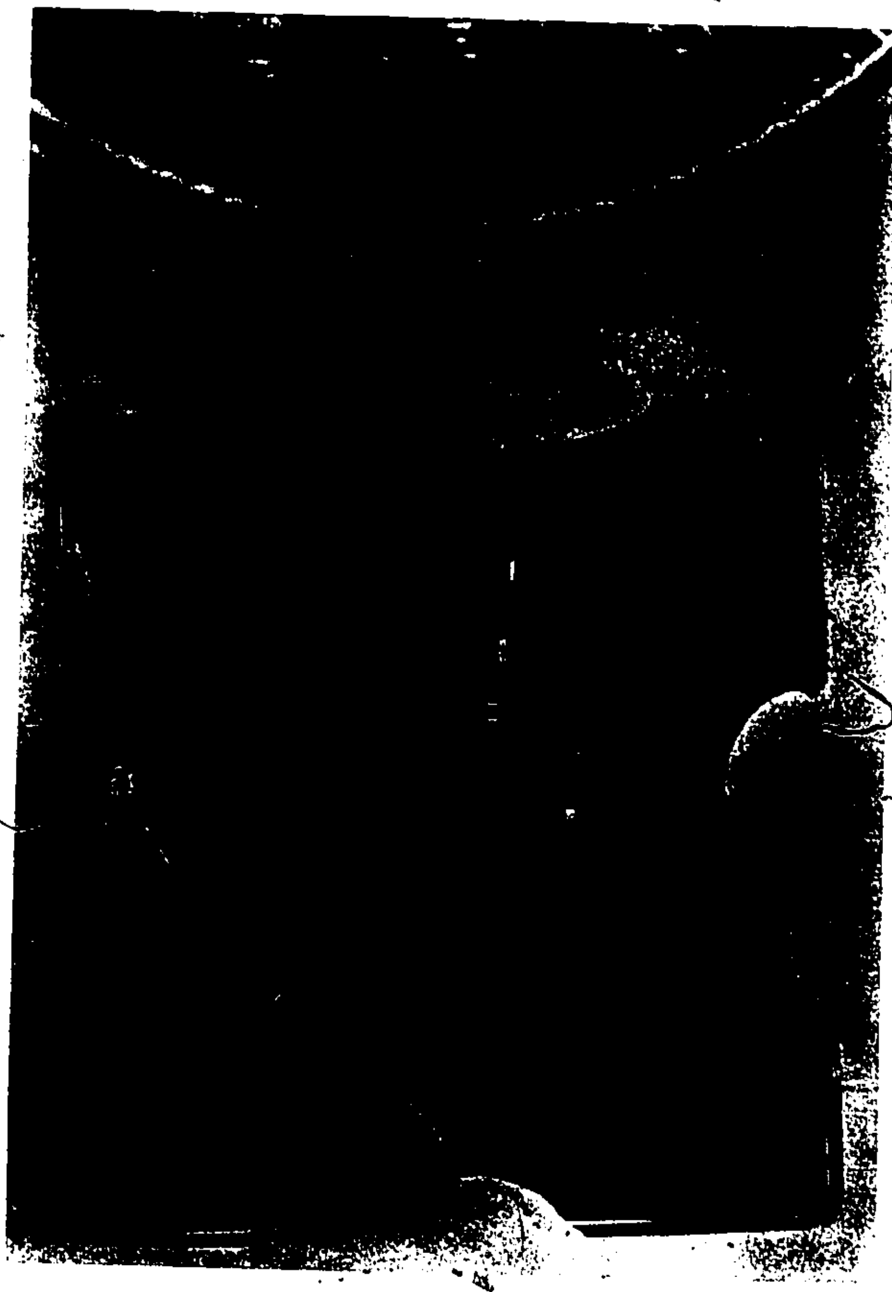


Figure 6.2 Several 480-finger 2 GHz SAW delay lines scanned on a substrate.

Figure 6.3 (a) Alphabetical pattern scanned in PMMA using general format scan program.

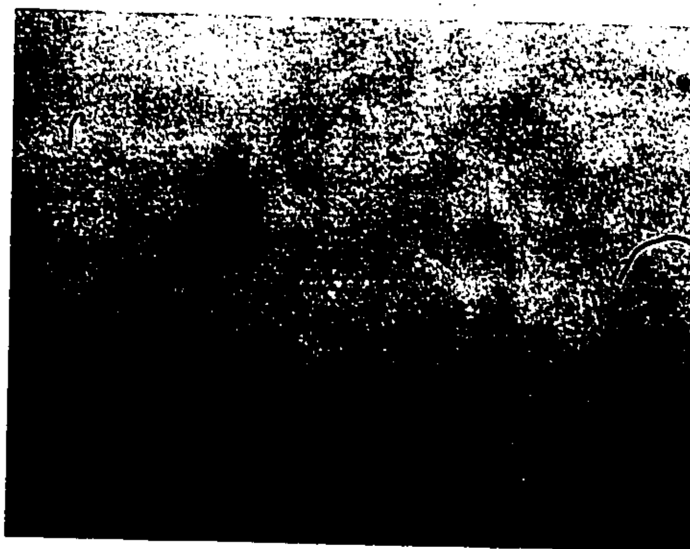
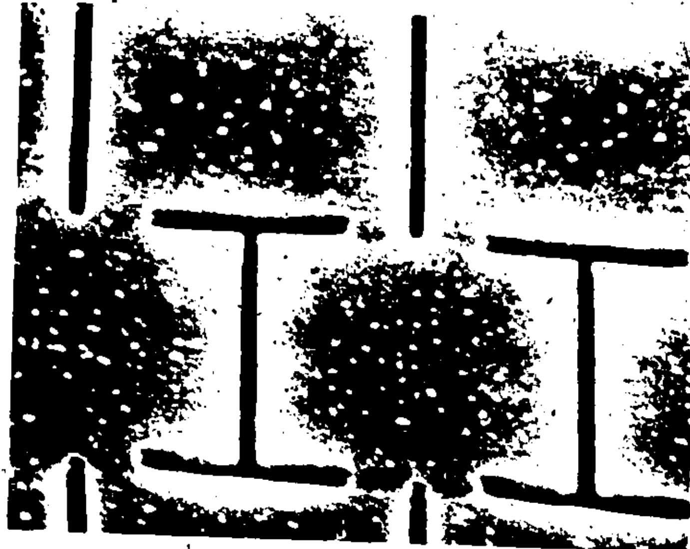


Figure 6.3 (b) 60µm x 60µm array of T-I bubble memory structures.

6.4 Bubble Memory Fabrication

Most pattern generators for E-beam lithography usually have a facility for filling in rectangular pattern features automatically, by using either a raster or spiral scan. The rectangle is coded by two corner coordinate points, which specify both its size and position, and are usually decoded by either the software or the hardware in the pattern generator. This process can be implemented by means of a subroutine, and to demonstrate the procedure, a T-I bar bubble memory pattern was chosen [43], [44]. In this case, rather than setting up simple start and stop points for the fill-in scan (as with rectangles), the subroutine is actually scanning a repetitive non-standard shape each time it is accessed. The T-I bubble memory required two subroutines, one for each unique circuit feature. The input data was coded with two bits per co-ordinate, one indicating an X or Y transition to the next circuit feature, and the other indicating that either a 'T' or an 'I' bar should be scanned. Hence, only one coordinate point (16 bits total) was used to completely define each circuit feature of the bubble memory pattern. A 60μm x 60μm 36 element bubble memory array was scanned, using the latter technique, and is illustrated in Figure 6.3 (b). Figure 6.4 illustrates details of the T-I bar exposure, which features 4,600 Å linewidths, with T and I-bar lengths of 10μm, and a T-bar width of 6μm. The SEM photos in Figure 6.4 are taken at a 45° tilt, facing away and into the plane of the page. A 16.5 kHz scan rate was used for the pattern exposure, and the other SEM parameter settings were similar to those used for the 1 GHz delay line. The total pattern writing time was just under 0.5 seconds. The high resolution capabilities of the E-beam lithography system are



(a)

(b)

Figure 6.4 Close-up SEM photos of 4,600 Å linewidth T-I bar circuit features.
(a) x 4,900 (b) x 19,500

demonstrated here again, as with the SAW delay line circuits. The bubble memory test scans were all made on quartz substrates, strictly for demonstration purposes, and exposure parameters would necessarily have to change when garnet-film substrates are used in bubble device fabrication.

6.5 Discussion and Conclusions

The scanning of several circuits has been discussed, with each one illustrating another facet or mode of operation for the microcomputer-controlled pattern generator. The 2 GHz SAW delay line scan has demonstrated the flexibility of changing the size of the scan field to suit the required pattern. The standard scan field was 1mm square, with a 625 Å resolution defined by the 14 bit D/A converters. Smaller scan fields are quite feasible, requiring only the appropriate alignment marks and matching alignment scan. A higher resolution is thus obtained, which beyond a certain point (~1000 Å) will affect only the beam placement accuracy, as opposed to the minimum linewidth which can be scanned. The variable scan field feature is extremely useful when working with devices which have frequency-determining dimensions, such as SAW devices. The SAW oscillator delay line is one example where the same software data and program can be used to scan delay lines covering an entire range of frequencies, merely by changing the scan field size. The mode selection and frequency response properties of the various delay lines remain the same, as well as the impedance matching characteristics. The variable scan-field technique is also being used in industry today to shrink standard-sized circuits (e.g. integrated circuit or bubble memories), which is followed by investigation of the resulting circuit oper-

ation and effects on its performance, in the interest of achieving higher circuit densities. All of the aforementioned features and applications can be readily implemented with the designed pattern generator.

The general format scan program and the use of the monitor routine have been discussed, with reference to the scanning of an alphabetical pattern. This procedure has demonstrated the ease and simplicity of programing a basic pattern using the pattern generator. The monitor routine for pattern data development is ideal for structures such as high frequency field-effect transistors (FETS), experimental bubble memory circuits, low finger count SAW devices, and many other planar devices which require, or could benefit from, high resolution pattern definition. The time required to establish a functional pattern-scanning program is relatively short, especially when compared to the photolithographic process of cutting and peeling a rubylith mask. The monitor program also allows quick and easy editing of the pattern data to be performed. Changes can be made in seconds, as compared to the necessity of generating an entirely new mask using the photolithographic process.

The scanning of a bubble memory circuit array has also been discussed. This procedure has demonstrated the use of memory-saving shape subroutines, which are able to scan entire circuit features, given only a 16-bit reference coordinate. The complexity of the stored shape is limited only by the available memory space, and the ability of the pattern generator hardware to scan the required pattern. The type of fill-in scan used for large area circuit features is also software programable, and not dependent on the scanner hardware. The coding scheme

used for the stored data, when interpreting the required scan conditions, can also be user-programable, and has no effect on how the pattern co-ordinates are handled by the hardwired scanner.

In summary, the pattern generator is able to scan virtually any shape or circuit configuration imaginable, with angled and irregular shapes being approximated to the accuracy given by the D/A converter resolution (or the minimum attainable linewidth in the resist, whichever is larger). This flexibility is possible due to the incorporation of a simple vector-scan hardwired scanner, and by allowing all the decision-making and specifications to be made by the microcomputer. This configuration prevents built-in obsolescence, since new scanning procedures and shapes can simply be programed into the pattern generator. Possible modifications to the pattern generator design may include software control of the D/A converter clock rate. This would allow linear beam dosage variation while scanning a pattern, which can be very useful when accounting for cooperative exposure effects. Varying the clock rate (i.e: scan rate) is preferable in this instance, since changing the incident beam current may affect other SEM parameters such as the beam diameter.

CHAPTER 7

CONCLUSIONS

The relevance of electron beam lithography in the present and near-future field of electronic circuit integration has been discussed, thereby justifying the need for further research in this area to meet the increased resolution demands. Several large-scale E-beam systems exist in the world today, and all can be characterized by their sophisticated control of the SEM scanning parameters, and extensive computer and associated peripheral support systems. In this thesis work, a complete electron beam lithography system has been designed and implemented. The design objectives involved the construction of a microcomputer-controlled pattern generator, and its interfacing with a commercially-available scanning electron microscope.

Design criteria for the pattern generator was based partly on a study made by the author of the various scanning techniques being used presently, and their relative advantages and disadvantages. Another factor that affected the overall system design was its projected end use, which entailed making experimental one-of-a-kind circuits or masks in a research oriented atmosphere. These factors led to the final design, which involved a hardwired vector scanner controlled by an 8-bit microcomputer. The pattern generator was also designed to be a development system, whereby a monitor program was used to transform a pattern's decimal coordinates into the appropriately-coded binary data. This fea-

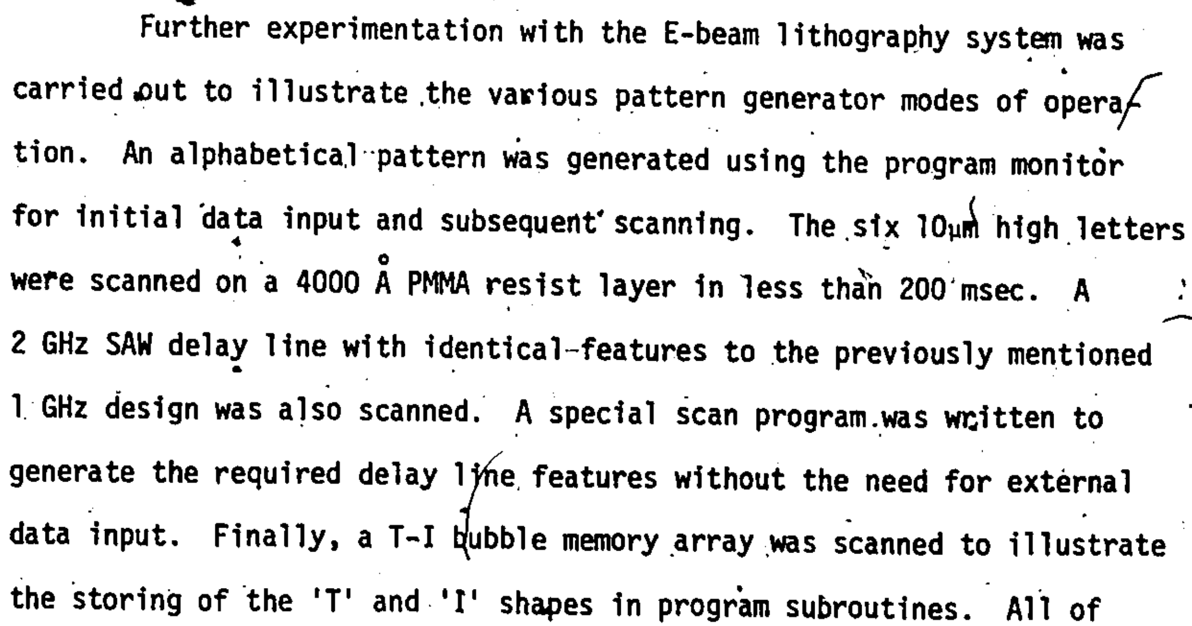
ture allows operator interaction by means of a keyboard and display, and subsequent data storage on cassette tape is also provided.

Several available variations in the operation of the pattern generator exist, due to the flexibility of software programing. The monitor program, in conjunction with the general format scan program, provide a quick and efficient manner of scanning a simple circuit pattern. Simple repetitive patterns such as gratings may be generated by writing customized software programs, which utilize loops for the repetitive scans, and do not require external coordinate data input. Repetitive structures which are more complex may be scanned by means of 'shape' subroutines. The essential scanning characteristics of each repetitive circuit shape are stored in separate subroutines, and are called upon whenever the proper code and a reference coordinate are detected. This latter mode of operation allows substantial savings in memory requirements for the storage of the pattern data. These three modes of pattern-generator operation offer the designer a means of generating a circuit pattern in the most efficient manner, suitable to the qualities and features present in the circuit structure.

The pattern generator was interfaced to a Stereoscan Mark II A scanning electron microscope, and the complete operational procedure of scanning sub-micron linewidth circuits was covered in detail. SEM parameters and their relationship to the successful exposure of circuit patterns in PMMA resist were derived and explained. Pattern development was outlined, and a general overview of the available types of post development processing was given. Several problems in the operation of the lithography system were encountered, and their effects on the quality

of the exposed patterns were demonstrated. Solutions to these problems were also discussed.

A 1 GHz surface acoustic wave delay line was fabricated to demonstrate the E-beam lithography system operation and accuracy. The delay line consisted of 480 aluminum fingers, each 7,680 Å wide, and separated by the same distance. SEM photographs of the exposed lines in the 4000 Å PMMA layer clearly illustrate the superior resolution and contrast obtainable with the electron beam lithography system. The delay line was then incorporated into the feedback loop of an amplifier with excess gain to implement a SAW oscillator. The centre frequency of operation was within 0.7% of the expected value, although it was 2.4% lower than the original design value due to an alignment problem in the SEM. Power output of the SAW oscillator was +6 dBm, and there were no spurious modes detectable in the output spectrum from 500 MHz to 1500 MHz. A dip anomaly was detected in the SAW delay line frequency response, and was later traced to a fault in the pattern generator D/A converters.



Further experimentation with the E-beam lithography system was carried out to illustrate the various pattern generator modes of operation. An alphabetical pattern was generated using the program monitor for initial data input and subsequent scanning. The six 10μm high letters were scanned on a 4000 Å PMMA resist layer in less than 200 msec. A 2 GHz SAW delay line with identical features to the previously mentioned 1 GHz design was also scanned. A special scan program was written to generate the required delay line features without the need for external data input. Finally, a T-I bubble memory array was scanned to illustrate the storing of the 'T' and 'I' shapes in program subroutines. All of

the stored data on the cassette consisted only of coded (2 bits/coordinate) reference coordinates. For the 36-element array which was scanned, only 37 coordinates (16 bits each) were needed to completely define the geometry.

In summary, an inexpensive and flexible pattern generator has been designed, which can be interfaced with a commercially available SEM to form an E-beam lithography system. The system features a fixed stage with a maximum usable field of view of 1mm x 1mm. Linewidths down to 3000 Å were obtained, and the lithography system operation was verified by the successful fabrication of a 1 GHz surface acoustic wave oscillator.

APPENDIX A

THE MONITOR PROGRAM

The monitor program was written in machine language format, based on the instruction set of the Intel 8008 microprocessor. The program was edited and assembled using the PDP 8/L_{o} minicomputer, which served as a host computer for the microprocessor editor and assembler programs [45].

The first program listing presented in this appendix applies to the general input program. This program must always be loaded before any data input can take place from the cassette. The instructions must be toggled into the microcomputer by hand, using the switch register on the front panel. This loader program is used to load either the monitor program, or any other program or data into the microcomputer RAM memory from the cassette tape. The program requires two user-selectable inputs, which are:

(a) destination memory address, i.e. the starting address where the input block of data will be transferred to

(b) data count in octal, i.e. the number of eight-bit bytes which are to be transferred

The destination memory address is specified in octal, and is loaded manually into the following locations:

least significant byte of address → *023#002

most significant byte of address → *023#004

The data count is also specified in octal, and is loaded manually into the following locations:

least significant byte of data count *023#010

most significant byte of data count *023#006

When loading the monitor program, the destination memory becomes *020#060, and the required data count is 002(H) 202(L), where H and L represent the high and low order bytes, respectively. The monitor listing follows the general input program listing, and contains four separate programs:

(a) the monitor program proper

S.A. = *020#100

(b) perimeter line scan alignment program

S.A. = *022#000

(c) general format scan program

S.A. = *022#100

(d) cassette loader program

S.A. = *022#220

When the monitor program is started, the converted data block resulting from the keyboard input coordinates is always stored with the starting address at *024#000. Upon completion of the input data entry, the monitor program automatically looks after the loading of appropriate data counts and starting addresses into the general format scan and cassette loader programs. The operator need only record the octal data count which appears on the keyboard display after typing the EXIT key, and this count will be needed when the data is to be retrieved from the cassette at a later date. The comments supplied with the program listings further explain their operation.

GENERAL INPUT PROGRAM

(For Monitor or Data)

```
*023#000 |250 XRA     /CLEAR ACCUMULATOR
      01 |066 LLI     /SET UP MEMORY POINTER
      02 |XXX         /LSB OF DESTINATION MEMORY
      03 |056 LHI
      04 |XXX         /MSB OF DESTINATION MEMORY
      05 |016 LBI     /SET UP DATA TRANSFER COUNT
      06 |XXX         /MSB OF DATA COUNT
      07 |026 LCI
      10 |XXX         /LSB OF DATA COUNT
      11 |103 INP1    /INPUT UART STATUS
      12 |044 NDI
      13 |040         /CHECK IF READY TO RECEIVE DATA
      14 |150 JTZ     /RETURN TO WAIT IF NOT
      15 |011
      16 |023
      17 |101 INP0    /INPUT 8-BIT BYTE
      20 |370 LMA     /STORE IN MEMORY
      21 |060 INL
      22 |110 JFZ     /INCREMENT MEMORY POINTER
      23 |026
      24 |023
      25 |050 INH
      26 |021 DCC     /DECREMENT COUNT LSB
      27 |302 LAC
      30 |004 ADI
      31 |001
      32 |110 JFZ
      33 |011
      34 |023
      35 |011 DCB     /DECREMENT COUNT MSB
      36 |120 JFS     /IF COUNT FINISHED, THEN HALT
      37 |011         /OTHERWISE RETURN FOR MORE DATA
      40 |023
      41 |000 HLT
```

MONITOR PROGRAM LISTING

```
OPDEF RKB;105;0        /READ KEYBOARD INPUT
OPDEF CKF;107;0        /CLEAR KEYBOARD FLAG
OPDEF BEAM;155;0       /E-BEAM ON--DISPLAY LED
OPDEF DPY1;157;0       /LED DISPLAY #1 LOAD (LEAST SIG. DIGIT)
OPDEF DPY2;161;0       /LED DISPLAY #2 LOAD
OPDEF DPY3;163;0       /LED DISPLAY #3 LOAD
OPDEF DPY4;165;0       /LED DISPLAY #4 LOAD
OPDEF DPY5;167;0       /LED DISPLAY #5 LOAD (MOST SIG. DIGIT)
OPDEF CLR;171;0        /CLEAR ALL DISPLAYS
OPDEF YLED;173;0       /Y-DISPLAY LED
OPDEF XLED;175;0       /X-DISPLAY LED
OPDEF ACUL;131;0       /LOAD OUTPUT PORT WITH ACCUMULATOR
OPDEF BMON;151;0       /SET BEAM ON FLAG
OPDEF STSN;147;0       /START SCAN
OPDEF YLSB;141;0       /LOAD LSB REGISTER OF Y
OPDEF YMSB;137;0       /LOAD MSB REGISTER OF Y
OPDEF XMSB;133;0       /LOAD MSB REGISTER OF X
OPDEF XLSB;135;0       /LOAD LSB REGISTER OF X
OPDEF STAT;103;0       /CHECK UART STATUS
OPDEF UOUT;121;0       /OUTPUT DATA VIA UART
OPDEF MCL;153;0        /MASTER CLEAR AND RESET
                       /
                       /
*020#060
HLT
HLT
HLT
HLT
HLT
HLT                    /HLT GENERATES AN ALL ZERO CODE IN THE
HLT                    /ASSEMBLER, WHICH CLEARS THESE LOCATIONS
HLT                    /INITIALLY FOR BLANK DISPLAY PURPOSES.
HLT
HLT
HLT
HLT
HLT
HLT
HLT
HLT
XRA                    /CLEAR ACCUMULATOR
LCA
LLI 076                /SET UP MEMORY POINTER FOR DATA STORAGE,
LHI 020                /STORED IN LOCATIONS *20#076 (LSB)
LAI 000                /AND *20#077 (MSB)
```

```
         LMA
         LAI 024
         INL
         LMA
START,   XRA                /CLEAR THE KEYBOARD DISPLAY
         ACUL
         CLR
READ,    LBI 350            /DELAY LOOP FOR DE-BOUNCING THE
AGAIN,   INC                /KEYBOARD
         JFZ AGAIN
         INB
         JFZ AGAIN
         CKF                /CLEAR KEYBOARD FLAG
CHECK,   RKB                /READ KEYBOARD
         LEA
         NDI                /CHECK FOR INPUT FLAG RAISED
         JFZ CHECK          /RETURN TO READ AGAIN IF NOT
         LAE
         NDI 017            /MASK-OUT 4 MSB
         LEA
         LAE
         SUI 012            /CHECK FOR X KEY TYPED?
         JTZ XDATA
         LAE
         SUI 013            /CHECK FOR Y KEY TYPED?
         JTZ YDATA
         LAE                /CHECK FOR END OF DATA INPUT?
         SUI 014            /IF NOT, IGNORE INPUT AND RETURN TO
         JFZ READ           /READ THE NEXT KEY
         LLI 077
         LAM
         SUI 024            /RETRIEVE MEMORY POINTER FOR START
         LBA                /OF EXIT ROUTINE, AND SUBTRACT THE
         DCL                /STARTING ADDRESS TO YIELD DATA COUNT IN
         LAM                /REGISTERS B(MSB) AND C (LSB)
         LCA
         LAB
         ACUL               /OUTPUT MSB OF DATA COUNT TO LED DISPLAY
         DPY4
         LAC
         NDI 007            /USE MASKING AND ROTATION TO OUTPUT
         ACUL               /THE LSB DIGITS OF DATA COUNT TO
         DPY 1              /LED DISPLAY
         LAC
         NCI 070
         RAR
         RAR
         RAR
         ACUL
         DPY2
         LAC
```

```
             NDI 300
             RLC
             RLC
             ACUL
             DPY3
             LEI 000
             LDI 350
    DEL,     INE                /DELAY ROUTINE FOR KEYBOARD DE-BOUNCE
             JFZ DEL
             IND
             JFZ DEL
             CKF                /CLEAR KEYBOARD FLAG
    LSTK,    RKB                /READ KEYBOARD
             NDI 020
             JFZ LSTK           /CHECK IF ANY KEY TYPED?
             XRA                /CLEAR KEYBOARD DISPLAY
             ACUL
             CLR
             LHI 022            /STORE DATA COUNT VALUE INTO
             LLI 226            /CASSETTE INPUT PROGRAM
             LMB
             LLI 230
             LMC
             XRA
             LAB                /DIVIDE DATA COUNT VALUE BY 2
             RAR                /AND STORE RESULT INTO GENERAL SCAN
             LBA                /PROGRAM
             LAC
             TAT
             LCA
             LLI 107
             LMB
             LLI 111
             LMC
             HLT                /END OF PROGRAM
    XDATA,   XRA                /START OF X DATA ENTRY ROUTINE
             XLED               /TURN ON X LED DISPLAY
             JMP CONT
    YDATA,   LAI 377
             YLED
    CONT,    LLI 075            /SET X/Y SOFTWARE FLAG
             LMA
             LDI 070            /SET UP COUNT PARAMETERS
             LEI 372
             LLI 060
             XRA
             LMA
    KEYRD,   LBI 350
             LCI 000
    MORE,    INC
             JFZ MORE           /SOFTWARE DELAY FOR KEYBOARD DE-BOUNCE
```

```
          INB
          JFZ MORE
          CKF                    /CLEAR KEYBOARD FLAG
WAIT,     RKB
          LBA                    /READ KEYBOARD INPUT DATA
          NDI 020                /CHECK INPUT FLAG
          JFZ WAIT               /RETURN AND WAIT IF NO INPUT
          LAB
          NDI 017                /MASK OUT THE FLAG BIT
          LBA
          LAB
          SUI 015                /CHECK FOR RUBOUT TYPED?
          JTZ START              /IF YES, RETURN TO START
          LAB
          SUI 016                /CHECK FOR NEXT TYPED?
          JTZ BCONV              /IF YES, GO TO BINARY CONVERSION ROUTINE
          LAB
          SUI 017                /CHECK FOR BEAM ON TYPED?
          JFZ BOFF
          LLI 060
          BEAM                   /ENABLE BEAM ON LED
          LAI 377
          LMA                    /SET BEAM ON FLAG
          JMP KEYRD              /RETURN FOR NEXT KEY
BOFF,     INE                    /TEST FOR MORE THAN 5 DIGITS?
          JTZ START              /IF YES, ABORT
          LAB
          LLD                    /ROUTINE TO DISPLAY ALL THE
          LMA                    /ENTERED DIGITS, AND ALSO STORE
          ACUL                   /THEM IN MEMORY
          DPY1
          DCL
          LAM
          ACUL
          DPY2
          DCL
          LAM
          ACUL
          DPY3
          DCL
          LAM
          ACUL
          DPY4
          DCL
          LAM
          ACUL
          DPY5
          IND
          JMP KEYRD
BCONV,    XRA                    /ROUTINE TO CONVERT HEXADECIMAL NO. TO BIN.
```

```
         DCD                   /THE FIVE HEXADECIMAL DIGITS WERE STORED
         DCD                   /PREVIOUSLY IN FIVE SEPARATE MEMORY
         LLD                   /LOCATIONS.  HERE, THEY ARE NOW GROUPED
         LAM                   /TOGETHER INTO THREE 8 BIT REGISTERS,
         RLC                   /(B,C,D) CALLED COLLECTIVELY NUMD
         RLC
         RLC
         RLC
         INL
         ADM
         LDA
         DCL
         DCL
         DCL
         LAM
         RLC
         RLC
         RLC
         RLC
         INL
         ADM
         LCA
         DCL
         DCL
         LBM
         LLI 050
         LMI 200               /INITIALIZE THE 16-BIT RESULT REGISTER
         INL                   /(NUM) FOR A SHIFT COUNT OF 16
         XRA
         LMA
LOOP,    LLI 050               /SET MEMORY POINTER FOR NUM MSB
         LAM
         RAR
         LMA                   /ROTATE NUM RIGHT ONCE
         INL
         LAM
         RAR
         LMA
         RAR
         NDI 200               /TEST IF LINK=1?
         JFZ DVFIN             /IF YES, CONVERSION IS FINISHED
         XRA
         LAB                   /START OF NUMD÷2 ROUTINE
         RAR                   /ROTATE AND STORE BCD DIGIT #5
         LBA
         LAC                   /ROTATE AND STORE BCD DIGITS #4 AND #3
         RAR
         LCA
         LAD                   /ROTATE AND STORE BCD DIGITS #2 AND #1
         RAR
         LDA
```

```
        RAR             /PRESERVE LINK (REMAINDER) AND STORE
        NDI 200         /IN MSB OF REGISTER B
        ADB
        LBA
        LAD             /START OF DECIMAL ADJUST ROUTINE
        NDI 010         /CHECK FOR BCD DIGIT #1≥8?
        JTZ BYT2        /GO TO NEXT DIGIT IF NOT
        LAD
        NDI 017         /DECIMAL ADJUST BCD DIGIT #1
        SUI 003
        LEA             /TEMPORARILY STORE RESULT IN REGISTER E
        LAD
        NDI 360
        ADE
        LDA
BYT2,   LAD
        NDI 200         /CHECK FOR BCD DIGIT #2≥8?
        JTZ BYT3        /GO TO NEXT DIGIT IF NOT
        LAD
        NCI 360         /DECIMAL ADJUST BCD DIGIT #2
        SUI 060
        LEA
        LAD             /COMBINE RESULT WITH BCD DIGIT #1
        NDI 017         /AND RE-STORE IN SAME LOCATION
        ADE
        LDA
BYT3,   LAC
        NDI 010         /CHECK FOR BCD DIGIT #3≥8?
        JTZ BYT4        /GO TO NEXT DIGIT IF NOT
        LAC
        NDI 017         /DECIMAL ADJUST BCD DIGIT #3
        SUI 003
        LEA             /TEMPORARILY STORE RESULT IN REGISTER E
        LAC
        NDI 360
        ADE
        LCA
BYT4,   LAC
        NDI 200         /CHECK FOR BCD DIGIT #4≥8?
        JTZ DAFIN       /JUMP TO DECIMAL ADJUST FINISHED
        LAC
        NDI 360         /DECIMAL ADJUST BCD DIGIT #4
        SUI 060
        LEA
        LAC
        NDI 017
        ADE             /COMBINE WITH BCD DIGIT #3 AND RESTORE
        LCA
DAFIN,  XRA             /ROTATE NUM AND RETURN FOR NEXT
        LAB             /DIVIDE BY 2 SEQUENCE
        RLC
```

```
          JMP LOOP
CVFIN,    XRA                /HEXADECIMAL TO BINARY CONVERSION FINISHED
          LLI 050
          LAM
          RLC
          LMA
          LLI 075            /SET MEMORY POINTER FOR X/Y FLAG
          LAM
          ADI 001            /GENERATE A CARRY IF FLAG IS SET FOR Y
          LLI 050
          LAM
          RAR                /MOVE X/Y FLAG VALUE INTO MSB OF NUM
          LBA                /(HIGHER BYTE) AND STORE IN REGISTER B
          LLI 060
          LAM                /LOAD ACCUMULATOR WITH BEAM ON/OFF FLAG
          ADI 001            /GENERATE A CARRY IF BEAM ON
          LLI 051
          LAM
          RAR                /MOVE BEAM FLAG VALUE INTO MSB OF NUM
          LCA                /(LOWER BYTE) AND STORE IN REGISTER C
          LLI 076
          LDM                /RETRIEVE MEMORY POINTER FOR DATA STACK
          INL
          LEM
          LHE                /SET UP MEMORY POINTER IN REGISTERS H AND L
          LLD
          LMB                /STORE THE CODED NUM IN DATA STACK
          INL
          LMC
          INL                /INCREMENT MEMORY POINTER FOR NEXT CYCLE
          JFZ RESET
          INH
RESET,    LDH                /TEMPORARILY STORE MEMORY POINTER
          LEL                /FOR DATA STACK
          LHI 020
          LLI 076
          LME
          INL
          LMD
          JMP START          /RETURN FOR MORE KEYBOARD ENTRY
                             /
                             /
                             /
                             /
                             /
                             /
                             /
                             /
          *022#000           /PERIMETER LINE SCAN PROGRAM FOR ALIGNMENT
          XRA
          MCL                /MASTER CLEAR AND RESET
```

```
RESCAN, LAI 060
        ACUL
        XLSB
        YLSB                /LOAD BOTH X AND Y LSB TO SCANNER REGISTER
        BMON                /TURN BEAM ON
        STSN                /START SCAN
        LAI 100
        ACUL
        YLSB                /LOAD NEXT Y LSB
        LAI 167
        ACUL
        YMSB                /LOAD NEXT Y MSB
        BMON
        STSN                /SCAN LINE WITH BEAM ON
        XMSB
        LAI 100
        ACUL
        XLSB                /LOAD X MSB THEN X LSB
        BMON
        STSN                /SCAN NEXT LINE
        LAI 060
        ACUL
        YLSB                /LOAD NEXT Y LSB (SAME AS AT START)
        LAI 010
        ACUL
        YMSB                /LOAD NEXT Y MSB (SAME AS AT START)
        BMON
        STSN                /SCAN THE FOURTH LINE
        JMP RESCAN          /RETURN TO REPEAT ALL SCANS CONTINOUSLY
                            /
                            /
                            /
                            /
                            /
                            /
                            /
                            /
        *022#100            /GENERAL FORMAT SCAN PROGRAM
        XRA
        MCL                 /MASTER CLEAR AND RESET
        LLI 000
        LHI 024             /INITIALIZE MEMORY POINTER TO DATA BLOCK
        LBI 000             /REGISTERS B AND C HAVE BEEN LOADED WITH
        LCI 000             /THE MSB AND LSB OF DATA COUNT÷2 RESP.
        JMP INPT
RSTR,   XRA
        DCC                 /DECREMENT DATA COUNT
        LAC
        ADI 001
        JFZ INPT            /RETURN FOR MORE DATA IF COUNT≠0
```

```
        DCB
        JTS END         /HALT WHEN COUNT=0
INPT,   LAM             /GET FIRST DATA BYTE FROM MEMORY
        RLC
        JFC XDTA        /CHECK X/Y FLAG BY ROTATING LEFT
        RRC             /RESTORE BIT POSITIONS FOR Y DATA
        ACUL
        YMSB            /OUTPUT MSB OF Y TO SCANNER REGISTER
        INL             /INCREMENT MEMORY POINTER
        JFZ NOVF
        INH
NOVF,   LAM             /LOAD REMAINING Y DATA BYTE INTO ACCUM.
        ACUL
        YLSB            /LOAD Y LSB INTO SCANNER REGISTER
        RLC
        JFC BMOF        /CHECK FOR BEAM ON FLAG STATUS
        BMON            /TURN E-BEAM ON
BMOF,   STSN            /START SCAN
        INL             /INCREMENT MEMORY POINTER
        JFZ CNTU
        INH
CNTU,   JMP RSTR        /RETURN FOR NEXT DATA PAIR
XDTA,   RRC             /RESTORE BIT POSITION OF X DATA
        ACUL
        XMSB            /LOAD X MSB INTO SCANNER REGISTER
        INL             /INCREMENT MEMORY POINTER
        JFZ PNT
        INH
PNT,    LAM             /LOAD REMAINING X DATA BYTE INTO ACCUM.
        ACUL
        XLSB            /LOAD X LSB INTO SCANNER REGISTER
        RLC
        JFC BEOF        /CHECK FOR BEAM ON FLAG STATUS
        BMON            /TURN E-BEAM ON
BEOF,   STSN            /START SCAN
        INL             /INCREMENT MEMORY POINTER
        JFZ MEM
        INH
MEM,    JMP RSTR        /RETURN FOR NEXT DATA PAIR
END,    HLT

        *022#220        /CASSETTE LOADER PROGRAM
        XRA
        LLI 000         /INITIALIZE MEMORY POINTER TO START OF
```

```
          LHI 024          /DATA BLOCK
          LBI 000          /REGISTERS B AND C CONTAIN DATA COUNT
          LCI 000          /LOADED BY MONITOR
INWT,     STAT             /CHECK STATUS OF UART
          NDI 020
          JTZ INWT         /IF NOT READY TO TRANSMIT, THEN WAIT
          LAM
          UOUT             /OUTPUT DATA BYTE VIA UART
          INL              /INCREMENT MEMORY POINTER
          JFZ NXT
          INH
NXT,      XRA
          DCC              /DECREMENT LSB OF DATA COUNT
          LAC
          ADI 001
          JFZ INWT         /RETURN TO OUTPUT MORE DATA IF COUNT≠0
          DCB
          JFS INWT
          HLT              /HALT WHEN COUNT=0
          $
```

APPENDIX B

ALIGNMENT MARK FABRICATION

The fabrication of the gold alignment marks on the quartz substrate surface will be covered in several sections:

B.1) Flexible Chromium Mask Production

B.2) Substrate Cleaning and Resist Coating

B.3) Exposure and Development

B.4) Vacuum Deposition

B.5) Photo Lift-off

B.1 Flexible Chromium Mask Production

1. the 45mm x 50mm Corning No. 1 cover glass slide was cleaned by spinning at 6000 RPM, and applying acetone, methyl alcohol, and distilled water respectively for 30 seconds each
2. slide was baked at 80° C for 20 minutes
3. surface of slide was covered with ∿8 drops of Shipley AZ-1350-B photo-resist, then accelerated to 3000 RPM and spun for 45 seconds
4. slide was baked at 80° C for 15 minutes
5. coated slide was put in close contact with 2" x 2" glass mask which had the required pattern on it, (fabricated from a rubylith original, using conventional photoreduction techniques), then exposed for 45 seconds to a 600 Watt projection lamp source at a 25cm distance
6. flexible slide was developed in a 50% mixture of Shipley AZ

developer with distilled water, for 40 seconds with moderate agitation, followed by a 15 second rinse in distilled water, and subsequently spun dry on the spinner for 45 seconds at 5000 RPM

7. slide was then baked at 80° C for 15 minutes
8. slide was placed resist side down, 15 cm above the filament source of an Edwards Model 12 E evaporator, and a vacuum of less than 1×10^{-5} torr was attained
9. approximately 800 Å of chromium was evaporated onto the surface, using a tungsten basket-type filament
10. after removal from the evaporator, the slide was placed in acetone, and lift-off occured in 5 to 10 seconds
11. flexible slide was then rinsed in distilled water for 60 seconds and hung with a clip to air-dry

B.2 Substrate Cleaning and Resist Coating

1. ST-X quartz substrates were cleaned according to the procedure outlined in Chapter 4, section 4.3.1 of this thesis
2. one drop of Shipley AZ-1350-B photoresist was applied to the spinning substrate from a 3cm height above the surface, which yielded a 4,500 Å resist layer when spun at 3000 RPM
3. substrates were baked at 80° C for 15 minutes, then were allowed to cool down

B.3 Exposure and Development

1. substrate was centred on the conformable-mask-vacuum jig

(illustrated in Figure 5.6 (a)) and the flexible mask was aligned to the quartz crystal edge using a Bausch and Lomb 7X to 30X microscope

2. upon achieving alignment, a vacuum was applied to the jig and the alignment was re-checked
3. resist-coated substrate was exposed by a 650 Watt projection lamp source, at a distance of 25cm for 35 seconds
4. exposed substrate was developed in a 50% solution of Shipley AZ developer and distilled water for 60 seconds
5. developed substrate was blown dry with dry nitrogen, examined for defects, and subsequently baked at 80° C for 15 minutes

B.4 Vacuum Deposition

1. substrates were placed, resist side down, 28cm above two evaporation sources in an Edwards Model 12 E evaporation unit, with two basket-type tungsten filaments arranged as in Figure 4.18
2. one tungsten basket was loaded with crushed chromium pellets, which were 99.999% pure, while the other was loaded with 0.03" diameter marz gold wire
3. at a vacuum of less than 1×10^{-5} torr, a 200 Å layer of chromium was evaporated first, followed by a 1000 →1500 Å layer of gold
4. a 30 minute cooling period was allowed before admitting air into the vacuum chamber

B.5 Photo Lift-off

1. coated substrates were immersed in acetone and gently agitated
2. lift-off occured within 10 minutes usually, and stubborn resist layers were ultrasonically agitated for 5 second intervals, with inspection of the pattern occuring between each interval
3. upon complete lift-off, the substrates were rinsed with distilled water for 2 minutes and subsequently blown dry with dry nitrogen

REFERENCES

[1] T.H.P. Chang, M. Hatzakis, A.D. Wilson, A.N. Broers, "Electron beam lithography draws a finer line", Electronics, Vol. 50, No. 10, May 12, 1977, pp. 89-98.

[2] "Vector-scan E-beam aims for wafers as well as masks", Electronics, Vol. 51, No. 23, Nov. 9, 1978, pp. 68-69.

[3] H.I. Smith, "Fabrication techniques for surface acoustic wave and thin-film optical devices", Proceedings of the IEEE, Vol. 62, No.10, October 1974, pp. 1361-1387.

[4] J.I. Goldstein et al., Practical Scanning Electron Microscopy, 1975, Plenum Press, New York.

[5] Stereoscan Scanning Electron Microscope Operator's Manual, TL 1022-OM-96113, Issue 1, Cambridge Scientific Instruments.

[6] J.D. Embury, C.M. Sargent, An Introductory Text in Transmission and Scanning Electron Microscopy, McMaster University.

[7] F.S. Ozdemir, E.D. Wolf, C.R. Buckey, "Computer-controlled scanning electron microscope system for high-resolution microelectronic pattern fabrication", IEEE Transactions on Electron Devices, Vol. ED-19, No. 5, May 1972, pp. 624-628.

[8] J. Pasiecznik, J. Frey, "A high-performance, low-cost digitally driven SEM system for materials studies and microfabrication", Journal of Vacuum Science and Technology, Vol. 10, No. 6, November/December 1973, pp. 1012-1015.

[9] D.R. Herriott, R.J. Collier, D.S. Alles, J.W. Stafford, "EBES: a practical electron lithographic system", IEEE Transactions on Electron Devices, Vol. ED-22, No. 7, July 1975, pp. 385-392.

[10] A.J. Speth, A.D. Wilson, A. Kern, T.H.P. Chang, "Electron-beam lithography using vector-scan techniques", J. Vac. Sci. Technol., Vol. 12, No. 6, Nov./Dec. 1975, pp. 1235-1239.

[11] E.V. Weber, H.S. Yourke, "Scanning electron-beam system turns out IC wafers fast", Electronics, Nov. 10, 1977, Vol. 50, No. 23, pp. 96-101.

[12] F.S. Ozdemir, C.R. Buckey, E.D. Wolf, "A pattern generation technique for serial electron-beam microfabrication systems", J. Vac. Sci. Technol., Vol. 12, No. 6, Nov./Dec, 1975, pp. 1246-1250.

[13] E.D. Wolf, P.J. Coane, F.S. Ozdemir, "Composition and detection of alignment marks for electron beam lithography", J. Vac. Sci. Technol., Vol. 12, No. 6, Nov./Dec. 1975, pp. 1266-1270.

[14] S. Miyauchi, K. Tanaka, J.C. Russ, "Automatic pattern positioning of scanning electron beam exposure", IEEE Transactions on Electron Devices, Vol. ED-17, No. 6, June 1970, pp. 450-457.

[15] G.L. Varnell, D.F. Spicer, A.C. Rodger, "E-beam writing techniques for semiconductor device fabrication", Journal of Vacuum Science, Vol. 10, No. 6, November/December 1973, pp. 1048-1051.

[16] A.M. Patlach, P.R. Jaskar, T.W. Studwell, "Electron-beam lithographic pattern generation system", J. Vac. Sci. Technol., Vol. 15, No. 3, May/June 1978, pp. 874-877.

[17] M.G.R. Thomson, "Design differences between electron beam lithography instruments and scanning electron microscopes", ITT Research Institute Proceedings of the 9th Annual Scanning Electron Microscope Symposium, Part IV, 1976, p. 633.

[18] H.I. Smith, S.R. Chinn, P.D. DeGraff, "Application of moiré techniques in scanning-electron-beam lithography and microscopy", J. Vac. Sci. Technol., Vol. 12, No. 6, Nov./Dec. 1975, pp. 1262-1265.

[19] T.H.P. Chang, R. Viswanathan, "Deflection distortion in scanning electron-beam systems", J. Vac. Sci. Technol., Vol. 15, No. 3, May/June 1978, pp. 878-882.

[20] T.H.P. Chang, B.A. Wallman, "A computer-controlled electron-beam machine for microcircuit fabrication", IEEE Transactions on Electron Devices, Vol. ED-19, No. 5, May 1972, pp. 629-635.

[21] W.J. DeVore, "A simple method for studying deflection aberrations in the scanning electron microscope", Electron and Ion Beam Science and Technology, Sixth International Conference, 1974, pp. 188-195.

[22] D.G. Seiler, C.K. Campbell, M.S. Suthers, "A low cost digital controller for an electron lithography system using a scanning electron microscope", IEEE Trans. on Industrial Elect. and Control Instr., Vol. IECI-23, No. 3, August 1976, pp. 325-328.

[23] W. Kinsner, D.G. Seiler, R. Britt, "FSK digital data converter for cassette tape recorder", Proc. of the International Symposium on Mini and Micro Computers, IEEE Cat. No. 76CH1180-9C, Nov. 1976, pp. 37-42.

[24] R.A. Harris, "Polymethyl methacrylate as an electron sensitive resist", Journal Electrochemical Society, Vol. 120, No. 2, February 1973, pp. 270-274.

[25] M. Hatzakis, "Recent developments in electron-resist evaluation techniques", J. Vac. Sci. Technol., Vol. 12, No. 6, Nov./Dec. 1975, pp. 1276-1279.

[26] E.D. Wolf, F.S. Ozdemir, W.E. Perkins, P.J. Coane, "Response of the positive electron resist elvacite 2041 to kilovolt electron beam exposure", IEEE 11th Symposium on Electron, Ion, and Laser Beam Technology, San Francisco Press, May 1971, IEEE Cat. No. 71C23-ED, pp. 331-336.

[27] R.J. Hawryluk, A. Soares, H.I. Smith, A.M. Hawryluk, "Experimental utilization of Monte Carlo models for electron beam lithography", Electron and Ion Beam Science and Technology, Sixth International Conference, 1974, pp. 87-94.

[28] T.H.P. Chang, "Proximity effect in electron-beam lithography", J. Vac. Sci. Technol., Vol. 12, No. 6, Nov./Dec. 1975, pp. 1271-1275.

[29] R.J. Hawryluk, A.M. Hawryluk, H.I. Smith, "Energy dissipation in a thin polymer film by electron beam scattering", Journal of Applied Physics, Vol. 45, No. 6, June 1974, pp. 2551-2566.

[30] M. Hatzakis, A.N. Broers, "Electron-beam techniques for fabricating fine metal lines", IEEE 11th Symposium on Electron, Ion and Laser Beam Technology, San Francisco Press, May 1971, IEEE Cat. No. 71C-23-ED, pp. 337-343.

[31] C.J. Mogab, W.R. Harshbarger, "Plasma processes set to etch finer lines with less undercutting", Electronics, Vol. 51, No. 18, Aug. 1978, pp. 117-121.

[32] T.M. Reeder, "Introduction to surface acoustic wave devices", Microwave System News, December/January 1974, Vol. 3, No. 6, pp. 24-26.

[33] J.D. Maines, E.G.S. Paige, "Surface acoustic wave devices for signal processing applications", Proceedings of the IEEE, Vol. 64, No. 5, May 1976, pp. 639-652.

[34] R.M. Hays, C.S. Hartmann, "Surface acoustic wave devices for communications", Proceedings of the IEEE, Vol. 64, No. 5, May 1976, pp. 352-371.

[35] S.C. Gratze, "Saw oscillators-their current status", Microwave Journal, Vol. 20, No. 12, December 1977, p. 45.

[36] D.G. Seiler, Design and Synthesis of a VHF Surface Acoustic Wave Oscillator, Masters Thesis, McMaster University, Dec. 1975.

[37] D.E. Cullen, M. Gilden, G.K. Montress, T.M. Reeder, "Design of stable SAW oscillators operating above 1 GHz, accepted for publication in 1978 IEEE Ultrasonics Symposium Proceedings.

[38] J. Crabb, M.F. Lewis, J.D. Maines, "Surface acoustic wave oscillators: mode selection and frequency modulation", Electronics Letters (GB), May 17, 1973, pp. 195-197.

[39] A.J. Slobodnik, Jr., "UHF and microwave frequency acoustic surface wave delay lines: design", Air Force Cambridge Research Laboratories, Pub. No. AFCRL-TR-73-0538, Aug. 1973.

[40] E.D. Wolf, R.D. Weglein, "Microwave acoustic surface wave delay lines", Contract for Air Force Cambridge Research Laboratories, contract # F19628-72-C-0127, August 1973.

[41] L.I. Maissel, R. Glang, Handbook of Thin Film Technology, McGraw Hill, 1970, pp. 1-107 to 1-113.

[42] D.G. Seiler, C.K. Campbell, M.S. Suthers, "A technique for measuring and matching the input impedance of a narrow-band surface acoustic wave filter", IEEE Trans. on Instrumentation and Measurement, Vol. IM-26, No. 2, June 1977, pp. 188-189.

[43] T.H.P. Chang, M. Hatzakis, A.D. Wilson, A.J. Speth, A. Kern, H. Luhn, "Scanning electron beam lithography for fabrication of magnetic bubble circuits", IBM Journal of Research and Development, July 1976, pp. 376-388.

[44] V. Sadagopan, M. Hatzakis, K.Y. Ahn, T.S. Plaskett, L.L. Rosier, "High density bubble domain shift register", AIP Conference Proceedings, No. 5, Pt. 1, Nov. 1971, pp. 215-219.

[45] MPS Microprocessor Series User's Handbook, Digital Equipment Corporation, DEC-08-UMPHA-A-D, November 1974.