Random Telegraph Signal Noise in CMOS Image Sensor (CIS) and Use of a CIS in a Low-Cost Digital Microscope

RANDOM TELEGRAPH SIGNAL NOISE IN CMOS IMAGE SENSOR (CIS) AND USE OF A CIS IN A LOW-COST DIGITAL MICROSCOPE

BY

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My Parents and Sister

Abstract

The introduction of the digital image sensor has triggered a revolution in the field of imaging. It has not only just replaced the conventional silver halide film based imaging system, but has also enormously widened the scope of imaging applications. Previously, charge-coupled devices (CCDs) were the most popular technology for image sensors. But in the past decade, they have been rapidly replaced by the CMOS image sensor (CIS) technology. The CCD image sensors offers higher sensitivity, wider dynamic range and better resolution compared to its CMOS imager counterparts. However, the lower power performance, higher speed of operation, easier integration with signal control and processing circuitries, and the use well-established mainstream fabrication process of CMOS technology, are key advantages that have served to propel CMOS imagers beyond CCDs in the market.

However, CIS suffers from higher temporal noise compared to that of CCDs. One of the major noise sources in CIS is the $1/f$ noise generated from the in-pixel active amplifier. Due to continuous shrinking of MOS devices, the random telegraph signal (RTS) noise is emerging as a dominant noise source over other low frequency noise in CMOS imagers, resulting into reduced imaging performance.

The RTS noise which evolves from trapping and de-trapping of electrons by the defects in the oxide, causes fluctuation in the drain current of the MOSFET. In this work, we have carried out time-domain measurement of RTS noise in CIS pixels. The time domain RTS measurements provide useful information about its characteristics in different operating conditions, which can be further used to extract the trap parameters and determine the optimum settings of operation of CIS.

The capability of integrating various on-chip operations, higher speed and lower fabrication cost has made the CIS a good choice for various imaging applications. In order to demonstrate the extent of possible applications of CIS, we have developed an imaging system using a CIS. Two major concerns of biomedical imaging systems are their speed and cost. The system presented here is implemented using a CIS and FPGA (field programmable gate array) that provides a low-cost and high frame rate solution for biomedical microscopy.

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Notation and Abbreviations

k	Boltzmann's constant
T	Absolute temperature
ρ	Charge density
q	Charge of an electron
ξ	Electricfield
ψ	Electrostatic potential
μ	Carrier mobility
N_A	Doping concentration of Acceptor atom
N_D	Doping concentration of Donor atom
ε_s	Permittivity of semiconductor
ε_0	Permittivity in vacuum
ε_r	Relative permittivity
p_0	Thermal equilibrium hole density
n_0	Thermal equilibrium electron density
D_p	Diffusion coefficient of hole
D_n	Diffusion coefficient of electrons
L_p	Hole diffusion length
L_n	Electron diffusion length
η	Quantum efficiency
h	Planck's constant
n_i	Intrinsic carrier concentration
m_{neff}	Effective mass of electron
m_{peff}	Effective mass of hole
N_c	Density of states in the conduction band
N_v	Density of states in the valance band
α_H	Hooge’s parameter
τ_h	Life time of hole
τ_n	Life time of electron
α	Absorption coefficient
g_m	Transconductance of the source-follower transistor
τ_e	Mean emission time of RTS
τ_c	Mean capture time of RTS
t_{ox}	Thickness of the oxide layer of a MOSFET
σ_n	Capture cross section
ΔE_a	Activation energy

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Overview of Image Sensor

In early days of imaging, it was mostly based on photo reactive silver halide films where the photo-reactive chemical reacts with light [1]. Depending on the intensity of the light incident on different points of the film plane, an image is formed which is stored chemically on the film. Thus the photographic film served as the photo sensor as well as a storage device. Another approach of imaging is to convert the optical signals into electrical signals, which is then transferred and stored in a separate storage device. The converted signal can either be in analog format or in digital format, if the image sensor has its own analog-to-digital converter (ADC).

The advantage of a digital image sensor based camera comes from its capability of integrating various image processing functions into the system, which offers high speed processing of images compared to the conventional silver halide film based camera. In addition, digital cameras are much cheaper, smaller and handy, and thus are rapidly replacing the film based conventional cameras.

The demand of digital image sensors is growing very fast with the rapid development in the fields of communication and information technology. The introduction of state-of-the-art third generation mobile telecommunication standard (3-G) allows services like video calls, video conferencing which require cellular phones with built-in cameras. Besides this, due to rapid expansion and development of communication services over the internet, digital image sensors have become an important accessory for computers [2]. Digital image sensors are also playing vital role in medical applications including fluorescence imaging and endoscopy [3], [4]. Other applications of image sensors can be found in guidance and navigation systems, automotive industries, robotics and machine vision [1], [2], [3], [5], [6].

Charge-coupled device (CCD) based image sensors are still a popular option for some scientific applications. The basic building block of a CCD is a MOS capacitor. In the MOS capacitor structure, photogenerated charge carriers are stored in a potential well formed at the $Si - SiO_2$ interface of the MOS device. The accumulated charges in the storage capacitor are then transferred to the next one by sequentially controlling their potential wells and thus the CCD functions like an analog shift register. The shifted charge is finally transferred to the output amplifier. Figure 1.1 shows the charge transfer mechanism in CCDs.

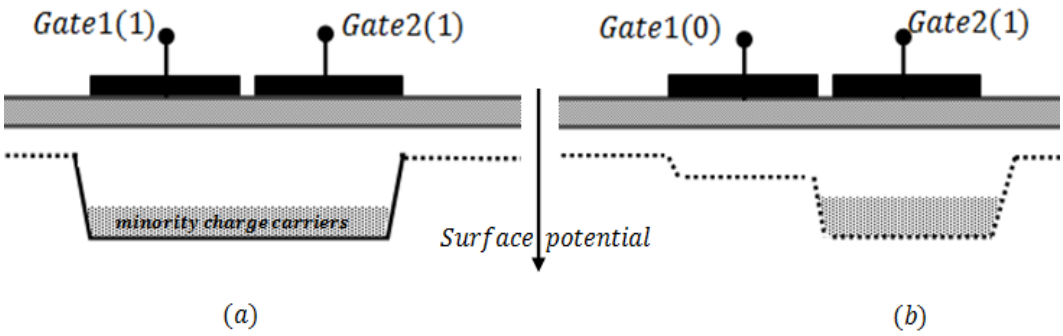


Figure 1.1: Charge transfer mechanism in CCD. a) Both pixel gates are biased at high potential. b) Gate 1 is biased at low potential and charge transfer occurs.

The key advantage of CCD comes from its capability of almost complete charge transfer from capacitor to capacitor that results into a very high signal-to-noise ratio (SNR) and uniformity. In addition to this, CCD offers high fill factor and smaller pixel size.

Despite having the advantages mentioned above, the performance of CCDs is limited by its slower readout speed due to the presence of highly capacitive elements [7]. Besides this, during the readout period, all the storage capacitors in CCD need to be switched simultaneously with high voltage, which demands a large amount of power consumption. Unlike CMOS (complementary metal-oxide-semiconductor) technology, CCD based image sensors are fabricated using a custom fabrication method which increases the price of the device. It also does not allow for integrating several camera functionalities on-chip. External chips need to be used to support all the camera functions which increase the overall size and cost of the camera system.

Currently, CMOS is the mainstream technology that is being used for almost all digital, analog, and mixed-signal electronic applications. The growth of this technology has been

immensely accelerated by some huge markets, which include central processing units (CPUs), solid-state memories, general-purpose logic integrated circuits, and now image sensors. The enormous advancement of CMOS analog circuit technology has reached to the point that most discrete analog components, except for very special, application-specific components, can be produced using modern CMOS technology.

Metal-oxide semiconductor field effect transistors (MOSFETs) offer very high input impedance that can be used for analog switches in chip circuits. It results in lesser current consumption by the MOS devices. They are also suitable for sample-and-hold and switched capacitor circuits, which are very important building blocks in CMOS image sensors. The power requirements of CMOS devices are also lowering with the continuous downscaling of CMOS technology [1], [2], [3], [5].

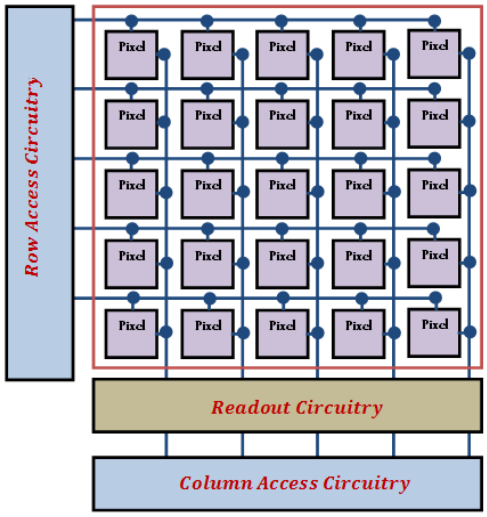


Figure 1.2: Array of CMOS pixels.

Thus designing image sensors using CMOS technology is a lucrative alternative of CCD based image sensors. Figure 1.2 shows the block diagram of a typical CMOS image sensor. Pixels are arranged in an array and any pixel can be selected and readout at any time in a CMOS image sensor (CIS), which is very similar to the working principle of a dynamic random access memory (DRAM). This characteristic of a CIS enables features like windowing, pixel addressing etc. Various functions, such as AD conversion can be implemented on-chip, which also widens the scope of implementing further digital signal processing (DSP) functions on the same chip.

Unlike the CCD pixels, where readout is performed sequentially, several pixels can be readout simultaneously in a CIS that greatly increases the readout speed. Power consumption of a CIS are also much lower compared to its CCD counterpart.

Table 1.1 presents the comparison between the performance of CCD and CMOS based image sensors [8].

Feature	CCD	CIS
Pixel output	Charge packet	Voltage
Chip output type	Analog	Digital
Fill factor	High	Moderate
Amplifier mismatch	N/A	Moderate
SNR	High	Low to moderate
Camera system Complexity	High	Low
Chip Complexity	Low	High
Responsivity	Moderate	Little better
Dynamic Range	High	Moderate
Uniformity	High	Low to moderate
Speed	Moderate to High	Higher
Windowing	Limited	Extensive
Biasing	Multiple	Single
Power requirement	High	Low to moderate

Table 1.1: Performance comparison between CCD and CMOS based image sensors [8].

1.2 Motivation of the work

Though the CIS offers high performance in the context of power consumption, ease of integration, speed etc., its noise performance is poorer compared to CCDs. A CIS suffers from high temporal noise that evolves from the photodiode reset noise at the floating diffusion (FD) capacitance node, photon and dark shot noise, and noise from the in-pixel source-follower amplifier. In addition to this, fixed pattern noise (FPN) that arises from pixel-to-pixel variation in dark current, photodiode sensitivity, sense node capacitance and amplifier characteristics due to

mismatch between the individual pixels also limits the noise performance of the CMOS image sensors. Thus, the signal-to-noise ratio (SNR) of the CIS is affected and so is its dynamic range (DR).

In the first uses of CMOS image sensor, FPN was a major concern, which helped CCDs to dominate the market of solid-state image sensors in the early days of solid-state imaging [9]. This FPN in CCD sensors arises only from the spatial variation in dark current and photodetector geometry, while the mismatches in transistors among different CMOS pixels produce additional pixel's FPN, and the mismatch among the column amplifiers produce column FPN. However, some signal processing techniques such as co-related double sampling (CDS), delta double sampling (DDS) have been developed to bring the FPN in CIS within an acceptable range. Further details about the FPN reduction methods can be found in [10], [11] and [12].

Temporal noise is still a big problem for CMOS image sensors. CCDs exhibit lower temporal noise, which usually evolves from the photodetector shot noise, low frequency noise (mostly $1/f$ noise) and thermal noise from the output amplifier. But in CIS the presence of in-pixel source follower amplifier transistor and the column amplifier produces additional thermal noise and low frequency noise. It is experimentally proved [13] that the in-pixel source follower transistor is the major source of low frequency noise in CIS. Several research groups have carried out the experimental study on the low frequency noise in CIS and have developed effective models to describe the results [14], [15].

The $1/f$ noise is believed to be caused from the trapping and de-trapping of electrons by the defects in the oxide layer [16], [17], [18] where each trap results into a Lorentzian shaped noise power spectral density (PSD). Since the size of the MOS device is decreasing rapidly, it could happen that only few traps reside within a few kT of the Fermi level. Therefore, in small-geomerty CMOS devices, the trapping and de-trapping of electrons at defects gives rise to fluctuations in the drain current between few discrete levels. Here each single trapping and de-trapping process produces a two level fluctuation, resulting a Lorentizian shaped noise PSD. This type of noise is called as random telegraph signal (RTS) noise and it significantly affects the performance of CMOS devices such as flash memories and image sensors [16], [17].

The RTS noise evolves from the presence of defects in the oxide layer of MOSFET and

thus is primarily process dependent. However, the important characteristic of RTS noise is that the time constants of the fluctuation follow a statistical distribution. It also depends on variables including temperature, gate voltage of the MOSFET, oxide thickness, and concentration of electrons in the channel.

In this work, we have performed experimental studies on RTS noise in CMOS image sensor. The time domain data of RTS noise was verified from the calculated noise PSD, which appeared to be a Lorentzian with a cut-off frequency corresponding to the time constants of the RTS. The capture time and emission time of RTS noise were measured and counted. It is found that, both the capture and emission times follow a Poisson distribution, and thus possess respective mean values. The mean capture time and mean emission time of the RTS changes with the pixel bias and operating temperature. It is observed that the mean capture time decreases dramatically with the increase of pixel bias , while the mean emission time shows a small increase. The data obtained from this experiment have been used to determine the trap location. The temperature dependence of the time constants have been studied. Both capture and emission time constants decreases drastically with increased temperature. Based on the experimental data, mathematical analysis have been performed to calculate the trap parameters such as trap energy level, capture cross section and activation energy.

As explained in section 1.1, CMOS image sensor exhibits some advantages over CCDs. The low-power requirement, high-speed readout, random pixel addressing and windowing capability of CIS makes it a good choice for applications where portability and high-speed imaging is a necessity [2], [3], [7]. In addition to this, the on-chip ADC provides digitized output which can be fed directly to computer for further processing. With its well developed fabrication process, CMOS technology based image sensors offer the cost-effective solution for consumer imaging systems. In this thesis work, we have also carried out research in order to develop a high-speed (high frames rate) camera system using a CMOS image sensor (LUPA-300) and a field programmable gate array (FPGA).

A higher frame rate camera is a necessity, specially when images of fast moving objects need to be captured [7]. The primary focus of this project is to implement this high speed camera system for the imaging of microscopic live objects e.g. *C.elegans*, a transparent model organism

that is used extensively for biomedical research due to its well developed cellular and molecular structures and similar genome pattern as human [19], [20]. Most of the digital microscopes available in the current market provides 10 to 60fps (frames per second) imaging speed, which is not enough for the imaging of live organisms that move very rapidly. Moreover, these systems are not cheap. In our developed system, a high-speed image sensor has been interfaced with a FPGA, which has the capability of faster data processing. The image stream is finally displayed on a VGA monitor. The implemented system provides imaging at a rate of 150fps with a 50MHz clock, which can be further increased up to ~1000fps by increasing the clock speed (80MHz) and/or by windowing. The total cost of the implemented system is less that $1000. Therefore, the high frame rate of our digital microscope along with its low cost makes it as a promising alternative to other imaging systems available in the market.

1.3 Main Contributions of this Thesis

The primary goal of this thesis is to explore the characteristics of random telegraph signal (RTS) noise in CMOS image sensors. It has been observed from the experimental study that,

1. The trapping and de-trapping of electron at a defect center is a Poisson process and the emission time and capture time of the RTS noise follow exponenetial distribution.
2. Both the emission time and the capture time shows dependence on the pixel bias voltage. At higher pixel bias, the concentration of electrons in the SF transistor channel increases, which results in a drastic decrease in the capture time. However, the emission time exhibits limited dependency (little increment) on the pixel bias.
3. The RTS time constants also changes with temperature. Both the time constants decreases exponentially as temperature increases, which might be resulted from the increased vibration of defect center at higher temperature.

Our work has been reported in several conferences and journals.

1. M. Jamal. Deen, **Sumit Majumder**, Ognian Marinov, and Munir M. El-Desouki, "Random Telegraph Signal Noise in CMOS Active Pixel Sensor," Proceedings of the 21st International Conference on Noise and Fluctuations (ICNF), 2011,pp. 208-211.
2. **S. Majumder**, M. M. El-Desouki, O. Marinov and M. J. Deen, “Random telegraph signal

noise in CMOS imagers and its impact on image quality," Fifth International Symposium on Integrated Optoelectronics, The 217th Meeting of the Electrochemical Society, Vancouver, BC, Canada,1 page, Wednesday 26 April 2010.

In another work of my thesis, we have developed a high speed imaging system for biomedical microscopy using a CMOS image sensor. This high speed system might be useful for the imaging of very fast moving objects, particularly for the imaging of C. elegans, an widely used nematode now a days in biomedical research. The total cost of the system is ~900 USD, which is much cheaper compared to other high speed imaging system available in the market.

1.4 Thesis Organization

The pixel is the functional unit of an image sensor. A CMOS pixel consists of one photosensitive device and a photo-conversion circuit. The photosensitive part can be implemented using different photodiodes. Depending on the capability of in-pixel signal amplification the pixels can also be classified. In chapter 2, we have discussed the operation principle of different photodiode structures. A comparative study on different pixel structures has also been presented.

Before moving to explain the RTS noise experiments and results, we would like to present an analytical discussion on different noise those are usually observed CMOS image sensors. Various noise sources in photodiodes and also in CMOS pixels are explained in Chapter 3 that includes shot noise, thermal noise, flicker noise, RTS noise etc.

Chapter 4 contains our experimental results. The chapter starts with a discussion of the experimental set-up and other important measures that were taken for proper identification of RTS noise. All the experiments were performed in a temperature controlled environment. In the following section, we have presented the experimental results that have been analyzed later, based on the literature. Experiments were carried out with varying temperature and bias voltage.

The implementation of high speed camera system is discussed in chapter 5. Three very important functional blocks of the system are the photosensing device, the control and processing device, and the display device. A video graphics array (VGA) monitor is used as a display device, whereas LUPA-300 implements the photosensing area. Controlling and processing is

performed by a FPGA. All the functional blocks are discussed here, which is followed by several results obtained from the camera system.

The thesis is concluded in chapter 6, which presents the summary of the whole work and also highlights the direction of further research.

Chapter 2

CMOS Image Sensor (CIS)

A CMOS Image Sensor (CIS) consists of an array of pixels. A pixel in the CMOS image sensor can be considered as a circuit consisting of a photodiode, a photodiode reset switch, signal amplification, and output circuits. In this chapter , we shall briefly discuss the structure and components of the CIS.

2.1 Photo Detectors in CMOS Pixel

Photodetectors are made of semiconductor devices, which can convert an optical signal into an electrical signal by generating electron-hole pairs (EHPs) with the absorption of photons. The photodetector plays the most significant role in a pixel. The response of a photodetector to light is processed by the other circuitry of the imager. Several types of photodetector are available, and common structures include

- $p-n$ junction photodiode,
- $p-i-n$ photodiode, and
- avalanche photodiode (APD)

The physical structure and working principle of the above mentioned photodiodes have been described in many text books [21], [22], [23]. In this section, we would have a brief review of the basic physical structures and the working principles of the three types of photodetectors listed above.

2.1.1 $p-n$ junction Photodiode

The $p-n$ junction based photodiodes are the most used photodetectors in CMOS imagers [22]. Figure 2.1 shows the basic structure of a $p-n$ junction photodiode. In a $p-n$ junction photodiode, the $p-$ side is heavily doped and generally kept very thin. The $n-$ layer is lightly doped. A depletion region, which is also called as space charge region (SCR) is formed between the $p-$ and $n-$ layer. Since the donor concentration in the $n-$ region is much lower than the

acceptor concentration in the $p-$ side, then almost the entire SCR is in the lightly doped $n-$ region.

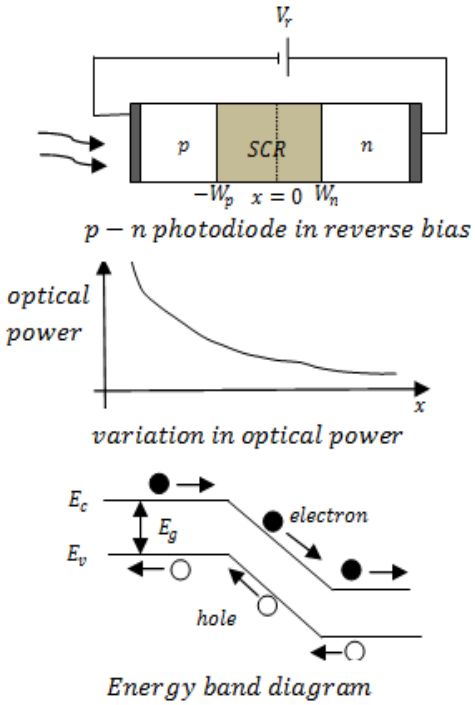


Figure 2.1: Operation of a $p-n$ photodiode

An inherent potential difference develops across the SCR due to presence of static charges in the depletion layer even when there is no external voltage is applied. This inherent potential difference is commonly referred as built-in potential (V_{bi}). An electricfield is developed in the depletion region due to presence of a net space charge density in the SCR. The potential, the electric field and the charge density across the depletion region are related through Poisson equation, written as,

$$-\frac{d^2\psi}{dx^2}=\frac{d\xi}{dx}=\frac{\rho(x)}{\varepsilon_s}. \tag{2.1}$$

Assuming complete ionization of the impurity atoms, the charge density at a position x in the depletion region depends on the concentration of the static impurity charge only because the concentration of free charges in the depletion region are negligible. Therefore, we can write,

$$\rho(x)=q[N_D-N_A] \tag{2.2}$$

The electricfield would be,

$$\xi(x)=-\frac{qN_A(x+W_p)}{\varepsilon_s} \qquad for \qquad -W_p\le x\le 0, \tag{2.3}$$

and

$$\xi(x) = -\frac{qN_D(W_n - x)}{\varepsilon_s} \qquad for \qquad 0 \le x \le W_n, \tag{2.4}$$

The electricfield is maximum at $x = 0$ which is,

$$|\xi_m| = \frac{qN_D W_n}{\varepsilon_s} = \frac{qN_A W_p}{\varepsilon_s}. \tag{2.5}$$

At the edge of the depletion region, that is at $x = W_p$ and $x = W_n$, the electric field is zero. The regions other than the depletion layer are considered as the neutral region carrying corresponding majority carriers, and these regions function as the resistive extensions of the electrodes to the depletion layer. When a photon of energy $h\nu$ is incident on a semiconductor, it gets absorbed by the semiconductor. An electron-hole pair (EHP) is generated if the energy of the photon is larger than the bandgap energy (E_g) of the semiconductor. Usually, for light of a specific wavelength, the $p-n$ junction is designed in such a way that the photogeneration takes place in the depletion region. The photogenerated EHPs are then driven in opposite directions by the electricfield, $\xi(x)$ developed in the depletion layer until the carriers reach the neutral region. The drift of the photogenerated carriers by the electricfield generates a current (I_{ph}) in the external circuit and the duration of the photocurrent depends on the transit time of the carriers which is the time required by the photogenerated electrons and holes to cross the depletion region and reach the neutral n- and p- region, respectively. In this way, the optical signal is converted into an electrical signal in a $p-n$ junction photodiode.

The photodiodes are usually operated at reverse bias with moderate biasing voltage for the visible and near-infrared wavelength range. This helps to reduce the transit time of the photo generated carriers and the diode capacitance. The reverse bias characteristic of a $p-n$ photodiode has been exhibited in Figure 2.2. When an external voltage (V_r) is applied across the photodiode it further widens the SCR and almost the entire V_r drops across the depletion width (W).

Therefore, the total voltage drop across the SCR would be $V_r + V_{bi}$ and the total current of the $p-n$ photodiode can be given by [24],

$$I \approx -I_0 - qAG_0(L_p + L_n). \tag{2.6}$$

where, G_0 is the generation rate of the EHPs and I_0 is the reverse saturation current and can be given by,

$$I_0 = qA\left[\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n}\right], \tag{2.7}$$

And the last term, which is the photocurrent of the diode can be given by,

$$I_{ph} = -qAG_0(L_p + L_n). \tag{2.8}$$

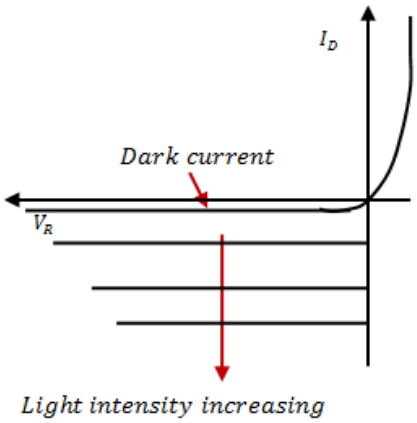


Figure 2.2: Reverse bias characteristic of a $p-n$ photodiode

Under reverse bias condition, $I = I_{ph}$ so the total current can be considered as proportional to G_0, which is also proportional to the optical power P_{opt}.

2.1.2 $p-i-n$ Photodiode

The $p-n$ junction photodiode has some drawbacks - the depletion layer in a $p-n$ junction photodiode is thin, which results in a large junction capacitance and thus the RC time constant becomes high. In spite of having small transit time of the photogenerated carriers due to thin depletion layer, the high RC time constant limits the frequency response of the photodetector. Light of longer wavelength have small absorption coefficients (α) and thus penetrates deeper into the semiconductor. The optical absorption within the diffusion lengths L_p and L_n is very small. Since L_p and L_n are very small, the contributions of the photocurrents are not high.

Again, due to the thin depletion layer in $p-n$ junction photodiode, the majority of photons are absorbed and thus EHPs are generated outside the depletion region. But there is no electricfield outside the depletion region to separate the EHPs and drift the carriers. We know that the quantum efficiency (η) of a photodetector is defined as the ratio of total number of free EHP generated and collected to the number of incident photons [23]. Since, most EHPs are

generated outside the depletion region, and most of them cannot be collected by the external circuit, then the quantum efficiency of $p-n$ junction photodiode is low at longer wavelengths.

In order to eliminate or reduce the problems mentioned above, and to enhance the responsivity and quantum efficiency of the photodiode, an intrinsic or very lightly doped region is grown between the $p-$ and the $n-$ regions. This intrinsic region functions as the major photon absorbing layer. Figure 2.3 shows the basic structure of a $p-i-n$ photodiode.

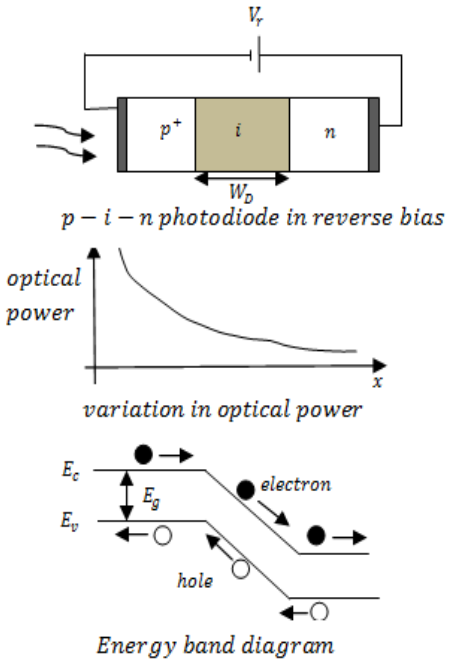


Figure 2.3: Operation of a $p-i-n$ photodiode.

The total current of a $p-i-n$ photodiode can be given by [24], [25]

$$I = -q\Phi_0\left[1-\frac{\exp(-\alpha W_D)}{1+\alpha L_p}\right]-\frac{qp_{n0}D_p}{L_p}, \tag{2.9}$$

Under normal operating conditions, the dark-current term involving I_0 is much smaller, so the last term can be neglected. Therefore the total photocurrent is I_{ph} can be written as,

$$I_{ph} \approx -q\Phi_0\left[1-\frac{\exp(-\alpha W_D)}{1+\alpha L_p}\right]. \tag{2.10}$$

Thus the quantum efficiency of the $p-i-n$ photodiode can be given by,

$$\eta = \frac{AI_{ph}/q}{P_{opt}/h\nu} = (1-R)\left[1-\frac{\exp(-\alpha W_D)}{1+\alpha L_p}\right]. \tag{2.11}$$

However, the quantum efficiency is reduced because of reflection R and light absorbed outside

the depletion region.

Therefore, for high quantum efficiency, the reflectivity R should be lower and W_D should be very large compared to α^{-1}. But if the length of the absorption region (W_D) is too long, the photogenerated EHPs would need longer time to cross that region i.e. the carrier transit time through the intrinsic region would be high, which will limit the response speed of the device. Therefore, the thickness of the intrinsic region should be optimized for the optical-signal wavelength and the modulation frequency. It was found that a reasonably good response speed and high quantum efficiency can be obtained if the thickness of the absorption region lies between $(1/\alpha)$ and $(2/\alpha)$ [22], [23], [24].

2.1.3 Avalanche Photodiode (APD)

When the electricfield across the $p-n$ junction becomes high enough, the photogenerated EHPs in the depletion region gain enough energy to excite more EHPs. The number of EHPs is thus increased rapidly as all the newly generated EHPs become a part of this process. This process is known as impact ionization or avalanche multiplication. The avalanche process is described further in section 3.1.2. However, this carrier multiplication phenomena is exploited in avalanche photodiodes (APD) by applying high reverse bias voltage across the APD so that a strong electricfield can be developed in the intrinsic/depletion region that would initiate the avalanche. Enhanced photocurrent response can be achieved in this way since, at a given optical illumination more free carriers are generated and collected by the external circuit. The avalanche process is shown in figure 2.4.

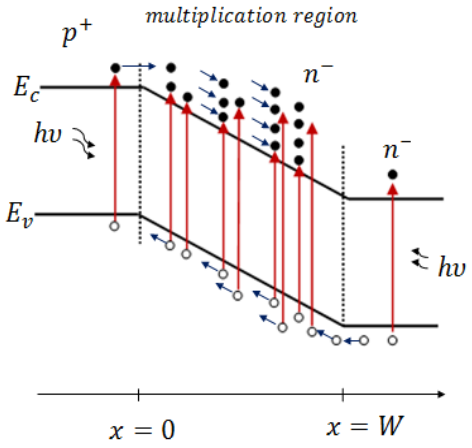


Figure 2.4: The energy band diagram for an avalanche photodiode.

Considering the ionization coefficients are position independent, the multiplication gain of electrons injected at $x = 0$ is given by [25]

$$M = \frac{((1-\alpha_p/\alpha_n)exp\,[\alpha_n W(1-\alpha_p/\alpha_n)])}{(1-(\alpha_p/\alpha_n)exp\,[\alpha_n W(1-\alpha_p\,\alpha_n)])}. \tag{2.12}$$

The multiplication of photogenerated EHPs for high light intensity is given by,

$$M_{ph} \approx \frac{I}{I_p} = \left[1 - \left(\frac{V_r - IR_s}{V_{brk}}\right)^n\right]^{-1}. \tag{2.13}$$

where, I is the total multiplied current, I_p is the primary (unmultiplied) current, V_r is the reverse-bias voltage, V_{brk} the breakdown voltage, n is a constant that depends on the semiconductor material, doping profile, and radiation wavelength and R_s is the effective series resistance of the APD.

When the reverse bias voltage approaches to breakdown voltage of the APD, then the photocurrent multiplication can be written as,

$$M_{ph} \approx \frac{V_{brk}}{nI\,R_s}. \tag{2.14}$$

Although APDs provide high current gain and high speed response, the random process involved in carrier multiplication produces excess noise which is explained in section 3.1.2. Besides this, due to its high reverse bias voltage requirement, APDs are not suitable in imagers fabricated using standard CMOS technology [5], [6]. Recently, APDs are being used in single photon avalanche photodiode (SPAD) sensors, where a triggered avalanche (Geiger-mode) is performed to detect single photons [26], [27]. The SPAD sensors are very useful for low light level applications, e.g. fluorescence imaging [27],[28].

2.2 Structure of CMOS Pixel

A pixel is the basic building block of an image sensor. A photodetector along with some additional circuitry constitutes a pixel. Depending upon the inherent signal amplification capability, the CMOS pixels can be divided into two principal classes.

- Passive Pixel Sensor (PPS)
- Active Pixel Sensors (APS)

2.2.1 Passive Pixel Sensor (PPS)

The PPS was the first developed image sensor using CMOS technology and the concept was originally introduced by Weckler in 1967 [29]. The PPS possesses a very simple structure with

only a photodiode and a switching transistor (Figure 2.5).

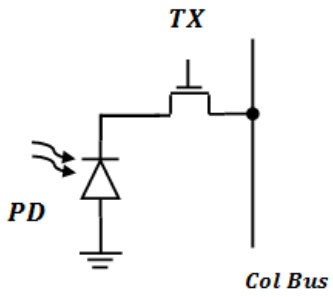


Figure 2.5: Passive Pixel Sensor.

The operation of a PPS is very similar to the analog DRAMs. The photogenerated charge is directly read out from the pixel and amplified by a charge detection amplifier located outside the pixel array.

Due to its simple structure, it has the highest design fill factor for a given pixel size, which in turn results in a high quantum efficiency - the ratio between the number of generated electrons to the number of incident photons. The large capacitive load in the PPS results into large thermal (KTC) noise. Besides this, it gives a high RC time constant during the pixel readout since the large bus gets directly connected to each pixel during the readout process. The high RC time decreases the speed of the readout. Large smear is also observed in PPS when the signal charges are transferred into the column signal line. Furthermore, the readout noise in PPS is high compared to that observed in commercial CCDs. In addition, due to the large capacitive load, a column switching transistor is required with a large driving capacity. It requires a MOS switch with large gate size. This causes a large overlap gate capacitance, which produces large switching noise and column FPN. Because of the factors mentioned above, PPS is not well-suited for larger array sizes or faster pixel readout rates [5], [6].

2.2.2 Active Pixel Sensor (APS)

In order to alleviate the problems associated with the PPS, a new pixel structure with an in-pixel active amplifier (a source follower transistor) was proposed [30]. In 1992, this new pixel structure was termed the Active Pixel Sensor [31]. Since the pixel in APS has its own amplification capability; then the image quality is greatly improved in comparison to a PPS. The inclusion of an active amplifier reduces the fill factor of an APS, which is only $50 - 70\%$.

However, the reduced capacitance in each pixel results in better noise performance, which increases both the dynamic range (DR) and the signal-to-noise ratio (SNR).

Depending on the number of transistors used in APS, it can be classified into two categories-

- Three transistor APS (3T-APS), or
- Four transistor APS (4T-APS).

Three Transistor APS (3T-APS)

Figure 2.6 shows the basic structure of a 3T-APS, which contains three transistors within each pixel. In comparison with a PPS, a 3T-APS contains a source follower (M_{SF}) as an active amplifier. The source follower acts like a voltage buffer. It has a current amplification capability, but has no voltage gain. The charge-to-voltage conversion occurs at the sense node capacitance, which comprises the photodiode capacitance and all other parasitic capacitances connected to that node. In this case, these are the source capacitance of the reset transistor (M_{RS}) and the gate capacitance of the source follower transistor. The select transistor (M_{SEL}) is used to transfer the signal to the vertical output line.

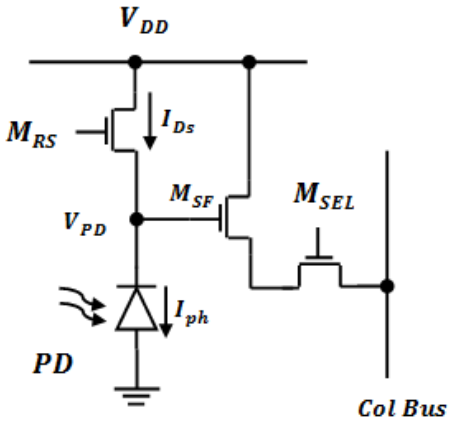


Figure 2.6 : Basic pixel structure of a 3T-APS.

In a 3T-APS configuration, the voltage gain (A_v) of the source follower is less than one, while the charge gain is determined by,

$$A_c = A_v.\left(\frac{C_{SH}}{C_{PD}}\right). \tag{2.15}$$

where, C_{PD} is the charge of the accumulation node and C_{SH} is the charge of the sample and the hold node.

When the reset transistor M_{RS} is turned on, the PD is reset to the value $V_{DD} - V_{th}$, where V_{th} is the threshold voltage of transistor M_{RS}.The PD becomes electrically floating as soon as the reset transistor turns off. When light is incident on the photodiode, the photo-generated carriers starts to accumulate in the photodiode node capacitance, C_{PD} and the voltage on the photodiode (V_{PD}) node starts to decrease. After an accumulation time, the select transistor, M_{SEL} is turned on and the output signal in the pixel is read out in the vertical output line. After the completion of the read-out process, M_{SEL} is turned off and M_{RS} is again turned on to repeat the above process. The most useful feature of the APS is that the accumulated signal charge is not destroyed, which makes it possible to read the signal multiple times.

Although the 3T-APS overcomes the shortcomings of the PPS (e.g. SNR is improved), it exhibits some other problems as follows.

- The thermal (kTC) noise in 3T APS is difficult to suppress.
- The photodetection and photoconversion take place on the same node, which sets a limitation in the photodiode design.
- The full-well capacity of the photodiode (and thus the DR) and the conversion gain have a trade-off relationship in a 3T-APS. This is due to the fact that the full-well capacity increases as the photodiode node capacitance, C_{PD} increases while the conversion gain, which is a measure of the increase of the photodiode voltage according to the amount of accumulated charge, decreases with $1/C_{PD}$.

The above mentioned drawbacks associated with the 3T-APS are resolved in the 4T-APS.

Four Transistor APS (4T-APS)

The 4T-APS is developed to surmount several weaknesses of the 3T-APS. In order to separate the photodetection region from the photoconversion region one transistor (M_{TG}) is added between the photodiode and the floating diffusion (FD). Thus total number of transistors becomes four, and hence this pixel structure is called 4T-APS. The transistor M_{TG} transfers the accumulated photo-generated carriers to the FD. Figure 2.7 shows the pixel structure of the 4T-APS.

When light is incident on the pixel, the photogenerated charge starts to accumulate in the PD. The FD is reset just before transferring the accumulated charge in PD by turning the reset transistor, M_{RS} on. The reset value is read out and stored for correlated double sampling (CDS)

operation. After the completion of the reset readout, the accumulated signal charge in PD is

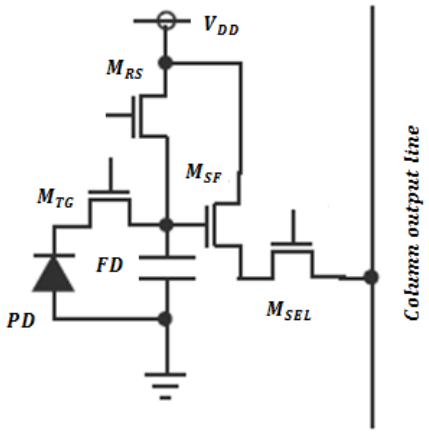


Figure 2.7: Basic pixel structure of a 4T-APS.

transferred to the FD node by turning the transfer gate, M_{TG}, following the signal readout by turning on the select transistor, M_{SEL}. The process is repeated and the signal charge and the reset charge are read out every time. The reset charge can be read out just after the completion of the signal charge readout. This timing is very important for an effective CDS operation and can only be realized if the charge accumulation region (PD) and the charge readout region (FD) are separated. kTC noise can be removed in this way which is not possible to achieve with the 3T-APS. The CDS operation also helps to alleviate the low frequency noise performance of the APS. It should be noted that the accumulated charge in PD of the 4T-APS must be drained out completely during the readout process. A well designed potential profile is necessary to ensure a complete transfer of accumulated charge to the FD through the transfer gate.

Although the 4T-APS provides better noise performance in comparison with the 3T-APS, there are also some problems associated with the 4T-APS, as follows:

- The inclusion of additional transistor reduces the fill factor of the pixel in comparison with the 3T-APS.
- Image lag may occur if the accumulated signal charge in the photodiode node is not completely transferred to the FD.
- Designing the 4T-APS components (e.g. photodiode, transfer gate, FD, reset transistor, and other units) with appropriate fabrication process parameters for better noise and better image lag performance is a great challenge.

Chapter 3

Noise in CIS

According to Ramo's theorem, when charge flows through a conductor bounded by two electrodes, the induced current depends on the spacing, d_r between the two electrodes

$$i = \frac{qnv}{d_r}. \tag{3.1}$$

where, n is the number of electrons and v is the velocity of electrons. From this expression, the fluctuation of current can be originated from the carrier number fluctuation and/or from the carrier velocity fluctuation. If both the fluctuations are statistically uncorrelated, then the fluctuation of current can be given by the total differential,

$$\langle di \rangle^2 = \left(\frac{qn}{d}\langle dv \rangle\right)^2 + \left(\frac{qv}{d}\langle dn \rangle\right)^2. \tag{3.2}$$

Velocity fluctuations of carriers are caused by the thermal excitation and hence get superimposed on the average drift velocity of the charges. The random velocity fluctuation of charges due to thermal agitation gives rise to *thermal noise*.

The number of carriers can fluctuate in various ways [32]. For example, in a semiconductor diode, the thermionic emission or current flow over a potential barrier is a statistical process. The individual emissions are random and not correlated with other carriers. When a diode is operated under reverse-bias condition, the current is determined by the statistically independent generation and recombination of carriers. This gives rise to *shot noise*, which has a *white* spectrum i.e. the PSD of shot noise is independent of frequency.

Number fluctuations of carriers can also occur from carrier trapping. A crystal lattice contains impurities or imperfections, which acts as traps for carriers. They can trap charge carriers and release them after a characteristic lifetime. The trapping and de-trapping of charged particles leads to a frequency-dependent power spectrum and generally has $1/f^{\alpha}$ characteristics, , where α is typically in the range of 0.5 - 2 [33].This type of noise is known as *flicker noise*.

The two important sources of noise in CMOS Pixel are from the photodiode and the in-pixel transistors. In this chapter we will discuss various noise sources that originate in the CMOS pixel.

3.1 Noise Associated with the Photodiode

The photodiode is one of the most important components of a pixel. In the photodiode, optical energy is converted into electrical charges, so it plays a very significant role from the noise point of view. In photodiodes, the noise observed in can be categorized as follows.

- Thermal noise
- Shot noise
- Flicker noise

3.1.1 Thermal Noise

Thermal noise is a common phenomena in any conductor or semiconductor device. It originates from the thermal agitation of electrons in a conductor. The current carriers are always in random motion. The electrons' response to an applied potential is disrupted by heat (see figure 3.1). It adds a random component to their motion. The thermal noise is independent of frequency, which means that the power spectral density of thermal noise is constant up to very high frequencies [24]. For that reason, thermal noise is sometimes called as white noise. This type of noise is also known as *Johnson-Nyquist* noise. Thermal noise only stops at absolute zero temperature for which the resistance of the sample is believed to be zero Ohms.

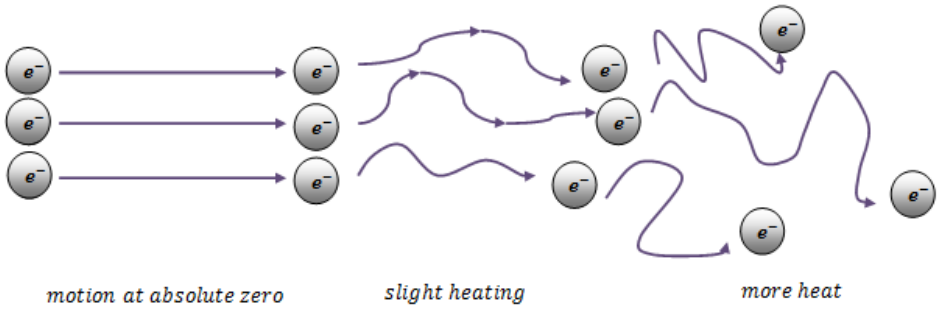


Figure 3.1: Thermal noise.

The thermal noise in a conductor of resistance R results in a random potential difference, $V_n(t)$ across the conductor, which can be characterized according to *Nyquist* relation by a noise current power spectral density $S(f)$ at temperature T [24], where

$$S(f) = \frac{4}{R}\frac{hf}{exp\,(hf/kT)-1}. \tag{3.3}$$

Where, k = Boltzmann's constant ($1.38 \times 10^{-23} JK^{-1}$), T = Absolute temperature (Kelvin), f =The frequency, h =Planck's constant ($6.626 \times 10^{-34} Js$). At low frequency,

$$hf = kT\ ,$$

Therefore, for low frequency eq.(3.3) can be simplified as,

$$S(f) \approx \frac{4kT}{R}. \tag{3.4}$$

Hence, the open circuit mean-square voltage of thermal noise would be,

$$\langle V_n^2(f)\rangle = R^2 \int_0^{\Delta f} S(f)df = R^2 \int_0^{\Delta f} \frac{4kT}{R} df = 4kTR\Delta f. \tag{3.5}$$

Here, Δf = Noise bandwidth in Hertz.

The mean- square thermal noise current power would be,

$$\langle i_n^2(f)\rangle = \int_0^{\Delta f} S(f)df = \frac{\langle V_n^2\rangle}{R^2} = \frac{4kT\Delta f}{R}. \tag{3.6}$$

Thermal noise in a photodiode arises from the parasitic resistances. This resistance includes -series resistance (R_s), junction resistance (R_j), external load resistance (R_l), and input resistance of following circuit or amplifier (R_i) [5]. The equivalent circuit of a photodiode has been shown in figure 3.2

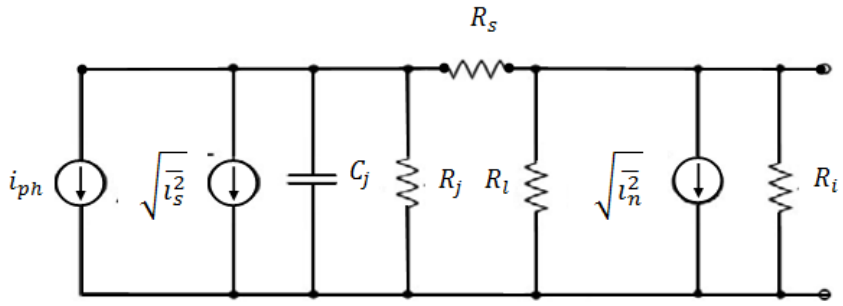


Figure 3.2: Equivalent circuit of a photodiode [5].

In figyre 3.2, C_j is the junction capacitance. The contribution of R_s is negligible since, it is much smaller than other resistances. Therefore, the equivalent resistance of a photodiode R_{eq} can be given as,

$$R_{eq} = \left[\frac{1}{R_j} + \frac{1}{R_i} + \frac{1}{R_l}\right]^{-1}. \tag{3.7}$$

Hence, the mean-square thermal noise current power of a photodiode would be,

$$\langle i_n^2 \rangle = \frac{4kT\Delta f}{R_{eq}}. \tag{3.8}$$

3.1.2 Shot Noise

Shot noise was first reported by Schottky in 1918. He stated that, even after eliminating all possible sources of noise in ideal vacuum tubes, there are still two types of noise, described by him as the *Wrmeeffekt* and the *Schroteffekt* [34]. The first of these is now known as Johnson-Nyquist or thermal noise and the second is the *shot noise* Shot noise is also referred to as *quantum noise*.

Shot noise is caused by random fluctuations in the motion of charge carriers. In fact, the flow of current is not a continuous effect. It arises from the flow of discrete electrons, charged particles. When an electron encounters a potential barrier, potential energy starts to build up. When it gains enough potential energy to surmount the barrier, the potential energy is abruptly transformed into kinetic energy as the electrons cross the barrier. As each electron randomly crosses a potential barrier, such as the depletion region of a $p-n$ diode, energy is stored first as the electron encounters the barrier and released when it passes over the barrier. Each electron contributes a little noise as its stored energy is released when it crosses the barrier. The combined effect of all of the electrons shooting across the barrier is the shot noise.

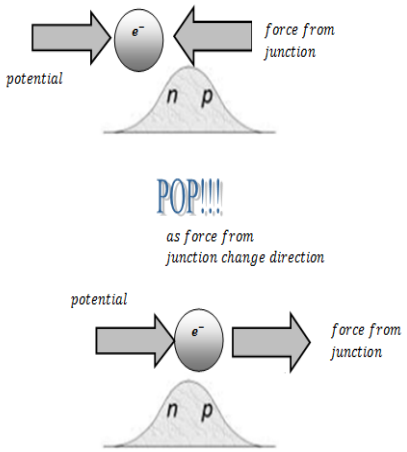


Figure 3.3: Generation of shot noise.

In a photodiode, shot noise arises from three sources [5]

- The photocurrent I_p, which is the current that arises from the absorption of the optical

signal.

- The background radiation induced photocurrent I_B, which is generated by the black-body radiation from the detector housing at room temperature [5].
- The dark current I_D,which is the leakage current when the photodiode is biased but not exposed to light.

For monochromatic radiation of wavelength λ, the number of photons per second per unit area i.e. the photon flux density is ϕ, the root-mean- square photocurrent can be written as [7],

$$I_p = q\eta\phi A, \tag{3.9}$$

where, A is the photodetector's illumination area, η is the quantum efficiency of the photodiode including the effects of its internal quantum efficiency, reflection, and absorption depth.

If P is the root-mean-square input optical power at wavelength, λ then,

$$P = \frac{m P_{opt}}{\sqrt{2}}, \tag{3.10}$$

where, P_{opt} is the average optical-signal power and m is the modulation index. Hence, the photon flux density,

$$\phi = \frac{P/h\nu}{A} = \frac{m P_{opt}}{\sqrt{2}h\nu A}, \tag{3.11}$$

Therefore from equation (3.9), the root-mean-square photocurrent would be,

$$I_p = \frac{q\nu m P_{opt}}{\sqrt{2}h\nu}. \tag{3.12}$$

Similarly, if the photon flux density due to the background radiation is ϕ_B then the background induced photocurrent would be

$$I_B = q\eta\phi_B A. \tag{3.13}$$

The dark current I_D in photodiodes has several sources [6].

- Diffusion current
- Band to band tunnel current
- Trap assisted tunnel current
- Generation current
- Impact ionization
- Surface leak current

Diffusion current (I_{diff})

From the ideal-diode equation, we know that the total diode current in the $p-n$ junction [5], [25] is given by,

$$I_d = \left[\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}\right]\left[exp\left(\frac{eV}{kT}\right) - 1\right]. \tag{3.14}$$

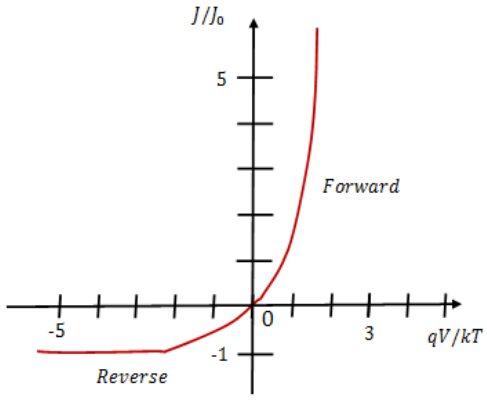


Figure 3.4: Ideal current-voltage characteristics of a $p-n$ diode.

In equation (3.14), V is the applied biasing voltage. The photodiodes are usually operated with a moderate reverse bias which makes the exponential term of equation (3.14) negligible and thus the diffusion current saturates at

$$I_{diff} = -\left[\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}\right], \tag{3.15}$$

The saturation current in reverse bias mode is commonly referred to as the reverse saturation current, I_{sat}. Hence,

$$I_{sat} = \left[\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}\right], \tag{3.16}$$

In our example, since, the p region is heavily doped in the $p-n$ junction photodiode, then we can consider that

$$p_{n0} \gg n_{p0}, \tag{3.17}$$

The second term of equation (3.16) thus can be neglected and can be re-written as,

$$I_{sat} \approx \frac{qD_p p_{n0}}{L_p}. \tag{3.18}$$

We know that, in thermal equilibrium,

$$n_{n0}p_{n0} = n_i^2. \tag{3.19}$$

Assuming that all the donor atoms are ionized to provide free electrons, we can write

$$n_{n0} = N_D. \tag{3.20}$$

Again we know that,

$$n_i^2 = N_c N_v exp\left[\frac{-E_g}{kT}\right], \tag{3.21}$$

and

$$N_c = 2\left(\frac{2\pi m_{neff}\, kT}{h^2}\right)^{3/2}, \tag{3.22}$$

$$N_v = 2\left(\frac{2\pi m_{peff}\, kT}{h^2}\right)^{3/2}, \tag{3.23}$$

Where, m_{neff} and m_{peff} are the effective mass of electron and hole, respectively. If we consider,

$$\frac{D_p}{L_p} = AT^B. \tag{3.24}$$

where A and B are constants, then using all the equations from equation (3.19) to (3.24), we can obtain from equation (3.18) that

$$I_{sat} \propto T^{(B+3)} exp\left[\frac{-E_g}{kT}\right]. \tag{3.25}$$

The effect of $T^{(B+3)}$ on I_{sat} is not so important compared to $exp\left[\frac{-E_g}{kT}\right]$. Thus, it can be said that the diffusion current in a photodiode at reverse bias increases exponentially as the temperature increases.

Band to band tunnel current (I_{tunb-b})

According to quantum mechanics, an electron can be represented by a wave function. Unlike an electron described in classical mechanics, the electron's wave function can penetrate into and through a potential barrier of finite height (see figure 3.5). The tunneling probability and thus the tunneling current depends on the height and width of the potential barrier. If the height and width of the potential barrier is U_0 and d, respectively than the probability of tunneling would be [25],

$$T_t \approx \frac{16E(U_0-E)}{U_0^2} exp\left(-2\sqrt{\frac{2m_{neff}\,(U_0-E)}{\hbar^2}}\, d\right), \tag{3.26}$$

where, E is the energy of the electron. From equation (3.26) it is found that the probability of tunneling increases as the energy of the electron increases and the width of the potential barrier decreases.

When a $p-n$ photodiode is operated under reverse bias, which is a typical case in

operating the photodiodes the potential barrier takes a triangular shape with a maximum height that is equal to the energy gap, E_g of the semiconductor material used in the photodiode. For a triangular shape barrier (see figure 3.6), the tunneling probability can be given as,

$$T_t \approx exp\left(-\frac{4\sqrt{2m_{neff}}E_g^{3/2}}{3q\xi\hbar}\right). \tag{3.27}$$

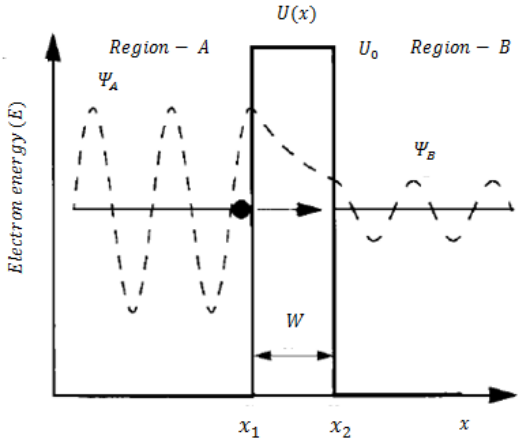


Figure 3.5: Tunneling of electron through a rectangular barrier.

When a diode is heavily doped and has a breakdown voltage less than approximately 6*V*, significant current starts to flow in reverse bias through tunneling of electrons directly from the valence band to conduction band. The direct transition of electrons from valence band to conduction band is known as band to band tunnelling. Band-to-band tunneling is also observed in forward bias for very heavily doped diodes like Esaki diodes [35]. The tunneling current of a

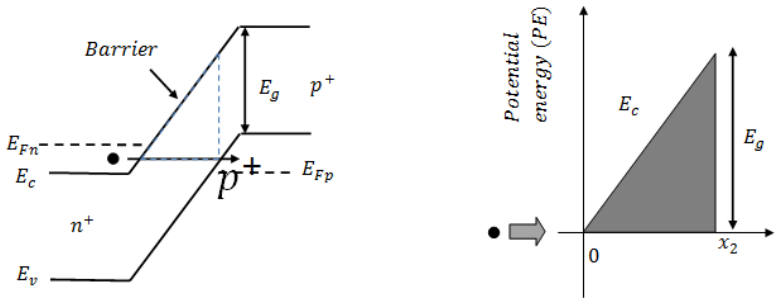


Figure 3.6: Tunneling of electron through a triangular potential barrier in $p-n$ diode.

Here A is the device area. ξ is the average electric field in the depletion region, which eventually depends on the concentration of the impurity atoms N_A, N_D and the applied bias voltage V_R pn

junction diode is given by [25]

$$I_{tunb-b} = \frac{\sqrt{2m_{neff}}\, q^3 \xi V_R A}{4\pi\hbar^2\sqrt{E_g}} exp\left(-\frac{4\sqrt{2m_{neff}}\, E_g^{3/2}}{3q\xi\hbar}\right). \quad (3.28)$$

through the relation-

$$\xi = \sqrt{\frac{q(V_{bi}-(-V_R))N_A N_D}{2\varepsilon_s(N_A+N_D)}}. \quad (3.29)$$

Since ε_s, N_A, N_D are constant for a given $p-n$ diode, considering $V_{bi} = V_R$, we can write

$$\xi = K_1 V_R^{1/2}. \quad (3.30)$$

where, $K_1 = \sqrt{\frac{qN_A N_D}{2\varepsilon_s(N_A+N_D)}}$ Therefore, the band to band tunneling current would be,

$$I_{tunb-b} = \frac{\sqrt{2m_{neff}}\, q^3 \xi K_1 V_R^{3/2} A}{4\pi\hbar^2\sqrt{E_g}} exp\left(-\frac{4\sqrt{2m_{neff}}\, E_g^{3/2}}{3qK_1 V_R^{1/2}\hbar}\right). \quad (3.31)$$

From equation (3.31) it is obvious that the band to band tunnel current strongly depends on the applied reverse bias voltage. This tunnel current exhibits little temperature dependence, which arises from the dependence of the bandgap energy E_g on temperature [36]. In fact, the band-to-band tunneling phenomenon is significant when the $p-$ and $n-$ regions are highly doped so that the depletion region becomes thin and thus the tunneling distance becomes shorter [35]. Such a diode with highly doped $p-$ and $n-$ junctions is called a Zener diode.

Trap-assisted tunnel current (I_{trap})

Tunneling can also occur through the traps located in the SCR of the diode. An electron may tunnel into a localized state inside the forbidden gap if the state is energetically aligned with an

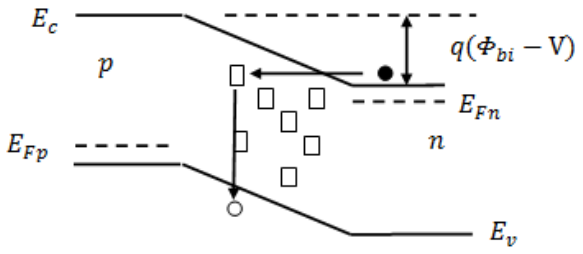


Figure 3.7: Tunneling of electron through trap.

occupied state of the conduction band of the $n-$ region. It can later recombine with a valence band hole of the $p-$ region through a Shockley-Read-Hall (SRH) recombination process, as

shown in figure 3.7.According to [6],[25] the trap assisted tunneling current can be given as,

$$I_{trap} \propto exp\left(-\frac{k_2}{V}\right)^2. \tag{3.32}$$

where k_2 is a constant. Equation (3.32) shows that the trap-assisted tunneling current has the exponential dependence on bias voltage.

In fact, trap-assisted tunneling is significant in forward bias whereas, in the reverse bias condition, band-to-band tunneling mechanism dominates over the trap-assisted tunneling [10], [13]. For that reason, the trap-assisted tunneling current has negligible contribution to dark current in photodiodes, which are usually operated with a moderate reverse bias voltage.

Generation-Recombination current (I_{gr})

The SRH recombination rate of excess holes and electrons [22] is given by,

$$R = \frac{v_t \sigma_n \sigma_p N_t (np - n_i^2)}{[\alpha_p (p + p_t) + \alpha_n (n + n_t)]}. \tag{3.33}$$

where, speed of the electron is v_t and the electron and hole-capture cross section is σ_n, σ_p respectively. The concentration of electrons in conduction band is n and concentration of holes in valence band is p. Under reverse bias condition, the SCR contains negligible amount of free carriers. Therefore, in the SCR,

$$p \approx 0 \text{ and } n \approx 0 .$$

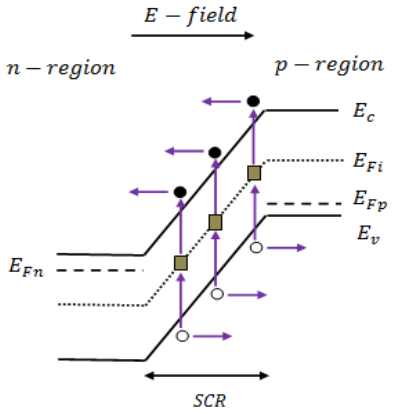


Figure 3.8: Generation of carriers in the depletion region of a $p-n$ diode in reverse bias.

And assuming the trap energy level is very near to the intrinsic Fermi level, we can write

$$n_t \approx n_i \text{ and } p_t \approx n_i .$$

Hence, equation (3.33) becomes

$$R = \frac{-v_t \alpha_n \alpha_p N_t n_i}{[\alpha_p + \alpha_n]}. \tag{3.34}$$

The negative sign in equation 3.34 indicates a negative recombination rate i.e. positive generation rate (G), which means that under reverse bias condition the generation of EHPs in the SCR dominates over recombination rate. The generated electron and holes are then swept out of the SCR by the electric field and thus generates a current (see figure 3.8). Also, equation (3.34) can be written as,

$$G = \frac{n_i}{[\tau_n + \tau_p]}, \tag{3.35}$$

where the mean life time of electrons in an $p-$type semiconductor τ_n is,

$$\tau_n = \frac{1}{v_t \alpha_n N_t}, \tag{3.36}$$

and the mean life time of holes in an $n-$type semiconductor τ_p is,

$$\tau_p = \frac{1}{v_t \alpha_p N_t}, \tag{3.37}$$

If the average lifetime of carriers is τ then,

$$\tau = \frac{\tau_n + \tau_p}{2}, \tag{3.38}$$

Now, equation (3.35) can be written as,

$$G = \frac{n_i}{2\tau}. \tag{3.39}$$

Therefore the generation current would be,

$$I_{gr} = A \int_0^{W} qG dx = \frac{AWq\, n_i}{2\tau}. \tag{3.40}$$

where, A =area of the SCR and W= width of the SCR. Again, we know that the width of the SCR is given by,

$$W = \sqrt{\frac{2\varepsilon_s}{q} \frac{(N_A + N_D)}{N_A N_D} (V_{bi} - (-V_R))}. \tag{3.41}$$

Using equations (3.21) and (3.41), then equation (3.40) can be written as,

$$I_{gr} = \frac{Aq}{2\tau} \left(\frac{2\varepsilon_s}{q} \frac{(N_A + N_D) N_c N_v}{N_A N_D} \right)^{1/2} (V_{bi} + |V_R|)^{1/2} exp \left[\frac{-E_g}{2KT} \right]. \tag{3.42}$$

Equation (3.42) shows that generation current depends on the applied reverse bias voltage and if the average lifetime τ varies slowly with temperature then I_{gr} will show some temperature dependence through the exponential term [5].

Impact ionization

When the electric field across the $p-n$ junction crosses a certain value, the photogenerated EHPs created in the depletion region gain enough energy to excite more EHPs. This process is known as impact ionization or avalanche multiplication. In case of Si and Ge, impact ionization in the depletion region is observed when the applied reverse bias voltage becomes larger than $4E_g/q$ [6].

The avalanche multiplication (see figure 3.9) is a statistical process. Generation of each EHP at a given distance in the depletion region is independent and does not experience same multiplication [37]. Therefore, this process causes an *excess noise* in photocurrent.

If carriers created at x' causes a multiplication at x then according to [38] the multiplication gain M will be,

$$M = \frac{exp\left[\int_x^{W} (\alpha_n - \alpha_p)dx'\right]}{1-\int_0^{W} \alpha_n \, exp\left[-\int_{x'}^{W} (\alpha_n - \alpha_p)dx''\right]dx'}. \tag{3.43}$$

where, α_n and α_p are the electron and hole ionization coefficient, respectively.

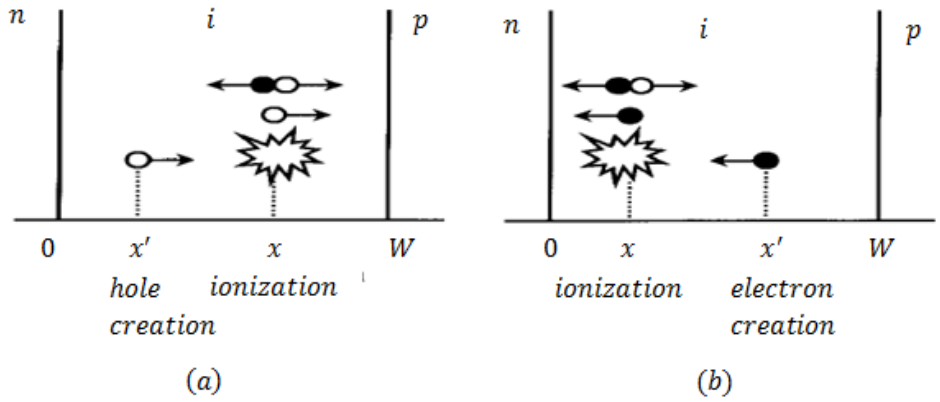


Figure 3.9: Schematic of the spatial notation for (a) holes and (b) electrons in the history-dependent theory [39].

The excess noise associated with avalanche multiplication can be defined by a noise factor F.

$$F(M) = \frac{\langle M^2 \rangle}{\langle M \rangle^2}, \tag{3.44}$$

where, $\langle\,\rangle$ means ensemble average. The excess noise factor depends on the ratio of the ionization coefficients. The noise factor for electron injection only is,

$$F_n = kM + \left(2 - \frac{1}{M}\right)(1-k). \tag{3.45}$$

and for hole injection only is,

$$F_p = k'M + \left(2 - \frac{1}{M}\right)(1 - k'). \tag{3.46}$$

where, $k = \alpha_p/\alpha_n = 1/k'$.

From equations (3.45) and (3.46), it can be shown that when there is no multiplication ($M = 1$) no additional noise would be added since at $M = 1, F_n = F_p = 1$.

Figure 3.10 shows the dependence of noise factor on k (for electron injection) or k' (for hole injection). From the figure 3.10, it is obvious that multiplication noise is minimized for small value k (for electron injection) or k' (for hole injection).

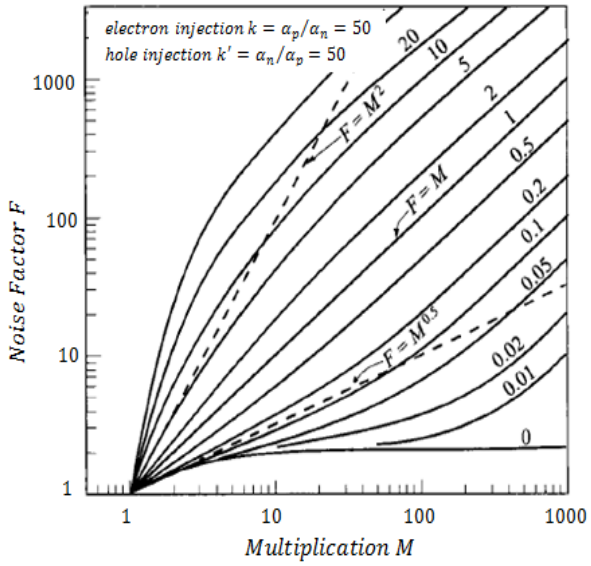


Figure 3.10:Theoretical plot of noise factor (F) vs multiplication (M) [25].

So in order to achieve low multiplication noise, the ionization coefficients should be as different as possible and the ionization process should be initiated by the carrier which has higher ionization rate. For example, for Si $p-n$ junction, the noise factor for electron injection is considerably lower than that for hole injection because for Si, α_n is much larger than α_p that means $k \ll 1$.

Figure 3.11 shows that at high electric field the ratio of ionization coefficients tend to unity. Therefore, in an avalanche photodiode (APD), the multiplication region is kept thicker in order to reduce the electricfield in that region and thus maximize the difference between α_n and α_p. This process eventually reduces the excess multiplication noise but at the same time results

in lower speed and higher operating voltage.

Experiments on *GaAs* APDs shows that avalanche noise can be reduced significantly by decreasing the multiplication region below one micron [40], [41]. This improvement in noise performance cannot be explained through McIntyre's local field model. Since, the operating electric field in the small multiplication region APD is considerably higher which would result in unity ratio of ionization coefficients.

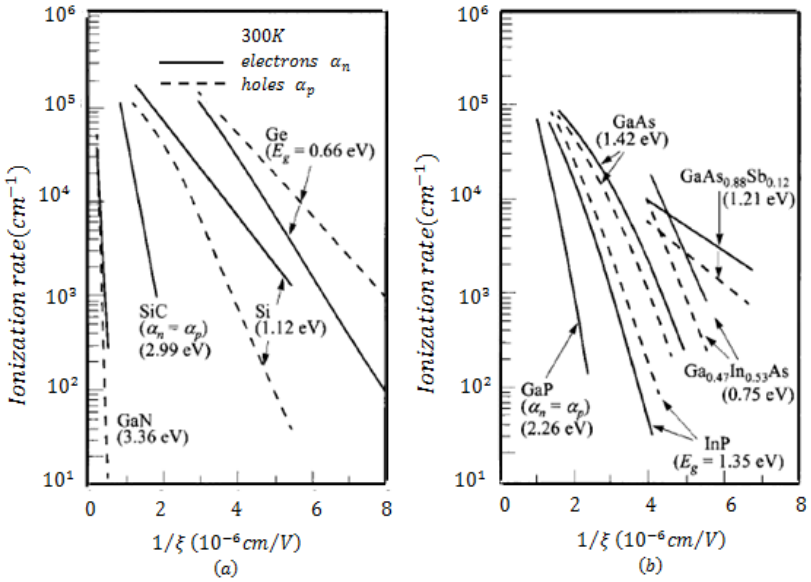


Figure 3.11: Ionization rates vs reciprocal electric field for *Si, GaAs* and some IV-IV and III-V compound semiconductors at 300K [25].

Monte Carlo simulation is presented in [42] to investigate the multiplication noise in $GaAs\ p-i-n$ avalanche photodiodes. It shows that the excess noise factor depends strongly on the probability distribution of ionization path length. For thick multiplication region (Figure 3.12 a), where the electric field is low, the probability distribution exhibits a conventional exponential decay and thus satisfies McIntyre's assumption. But in thinner devices with higher electricfield (Figure 3.12 b), the probability distribution function is found to be shifted by a *dead space* where carriers are prohibited to get ionized. The *dead space* in thinner structures reduces the regions where the carriers can ionize and thus reduces the randomness in ionization and also the multiplication noise. Multiplication process is utilized in avalanche photodiodes to enhance the photocurrent response so that more EHPs and hence more photocurrent can be generated.

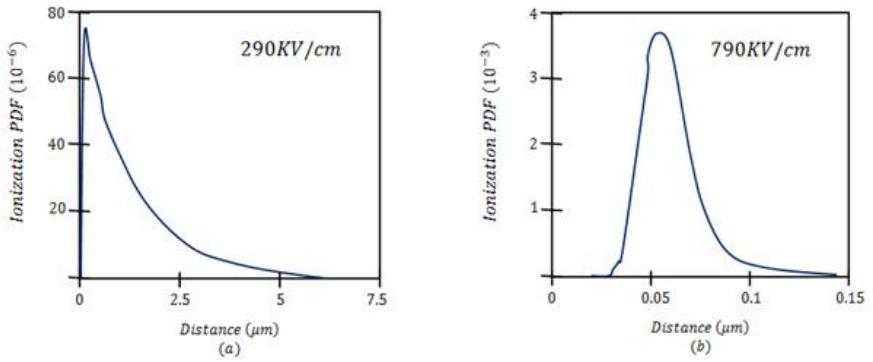


Figure 3.12: PDF of ionization (a) at low E- field (b) at high E- field [42].

A newly generated carrier needs to travel a certain distance before it can attain sufficient energy form the electric field so that it can initiate a new ionization event [19]. This distance travelled by the new carrier is commonly referred to as *dead space* The effect of *dead space* is negligible when the thickness of multiplication region is large compared to it. But when the thickness of the multiplication region is thin, the effect of *dead space* becomes prominent and McIntyre's assumption of continuous ionization becomes invalid [39].

But multiplication noise does not have much importance in $p-n$ or $p-i-n$ photodiodes since, these photodiodes are usually operated under moderate reverse-bias voltages. This reduces the carrier transit time and lowers the diode capacitance also. The reverse voltage is not large enough to initiate avalanche multiplication.

Surface leakage current

The surface leakage current in a photodiode is caused by generation or recombination of carriers in the depletion region surface or from the creation of surface channel. A single-crystal semiconductor lattice has a perfect periodic structure. But at the surface, the lattice faces an abrupt change in the periodicity due to presence of numerous unfulfilled bonds. The disturbance at the surface of the semiconductor results in many allowed energy states between the valence band and the conduction band. These discrete energy states at the surface function as SRH trapping centers for carriers (see figure 3.13). According to Brattain and Bardeen, these trapping centers can either be of donor type lying high in the band, or of acceptor type lying low, or both.

In addition, the surfaces and interfaces are more likely to contain impurities since they are exposed during the device fabrication process. For this reason at the surface, the density of traps is larger than that in the bulk of the semiconductor. The traps on the surface of the depletion

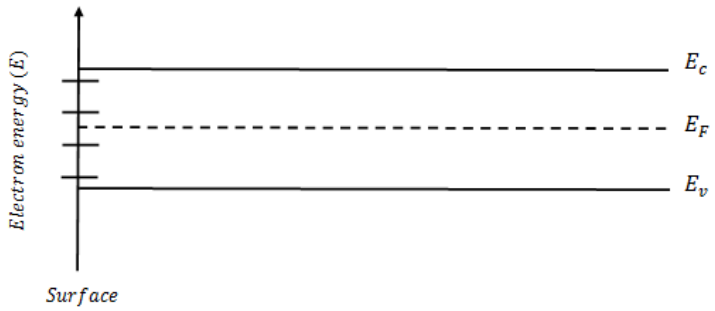


Figure 3.13: Distribution of surface states within the forbidden bandgap.

region of a $p-n$ junction are responsible for surface recombination generation current. The surface recombination generation current has significant contribution to surface leakage current if a surface channel is not formed [43]. The surface recombination rate in the depletion region can be written from equation (3.34) as

$$R_s = \frac{-v_t \sigma_n \sigma_p N_t n_i}{[\sigma_p + \sigma_n]}, \tag{3.47}$$

Assuming the capture cross section for both type of carriers are equal i.e. . $\sigma_n = \sigma_p = \sigma$ and we can write the surface generation rate,

$$G_s = \frac{1}{2} v_t \sigma N_{st} n_i, \tag{3.48}$$

$$G_s = \frac{1}{2} n_i S_0, \tag{3.49}$$

where, N_{st} is the density of traps on the surface and surface recombination velocity, $S_0 = v_t \sigma N_{st}$. From equation (3.35), the surface generation recombination current can be deduced as,

$$I_{surf} = \frac{1}{2} q n_i S_0 A, \tag{3.50}$$

where, n_i and A are the intrinsic carrier concentration and surface area of the depletion region, respectively. Using equation (3.21), we can write,

$$I_{surf} = \frac{1}{2} q S_0 A \sqrt{N_c N_v} exp\left[\frac{-E_g}{2kT}\right]. \tag{3.51}$$

From equation (3.34) it can be shown that the temperature dependence of I_{surf} is insignificant.

The presence of ionic charges on or outside the semiconductor surface can induce image charges in the semiconductor. Therefore, field lines in the junction depletion region can be terminated on these charges [44]. It causes the formation of the so called surface channels or surface depletion regions. Once a channel is formed, it modifies the junction depletion region and the field distribution within the depletion region near the surface. It acts as another source of

surface leakage current. For Si planar $p-n$ junctions, the surface channel current is generally much smaller than the generation-recombination current in the depletion region. Therefore, the dark current (I_D) in a photodiode is a combined effect of all the current described above. Now, the spectral density function for shot noise is given by [24],

$$S(f) = 2q\langle I\rangle, \tag{3.52}$$

Now, the mean-square shot noise current power within a frequency interval between f and $f + \Delta f$ would be,

$$\langle I_s^2(f)\rangle = 2q\langle I\rangle\Delta f, \tag{3.54}$$

Since, all currents that contributes to shot noise are independent to each other, then the mean-square shot noise current power would be,

$$\langle I_s^2(f)\rangle = 2q(\langle I_p\rangle + \langle I_B\rangle + \langle I_D\rangle)\Delta f. \tag{3.55}$$

If an avalanche process takes place (such as in APDs) the shot noise will also face a multiplication. Therefore, the mean-square shot-noise current after multiplication would be,

$$\langle I_s^2(f)\rangle = 2q(\langle I_p\rangle + \langle I_B\rangle + \langle I_D\rangle)\langle M^2\rangle\Delta f. \tag{3.55}$$

Using equation (3.44), we can write

$$\langle I_s^2(f)\rangle = 2q(\langle I_p\rangle + \langle I_B\rangle + \langle I_D\rangle)\langle M\rangle^2 F\Delta f. \tag{3.56}$$

3.1.3 Flicker Noise

Flicker noise is commonly known as $1/f$ noise or *pink* noise. The origin of $1/f$ noise is somewhat ambiguous. Some researchers believe that the fluctuation in the mobility of carriers is responsible for $1/f$ noise while others consider the presence of imperfections in the device structure as the predominant source of this type of noise.

Hooge [45] proposed an empirical formula for $1/f$ noise, where the fluctuation in current was considered as an effect of fluctuating resistance. According to Hooge,

$$\frac{S_I(f)}{I^2} = \frac{S_R(f)}{R^2} = \frac{\alpha_H}{fN}. \tag{3.57}$$

where, $S_I(f)$ is the fluctuation in the current, $S_R(f)$ is the fluctuation in resistance, f is the frequency, N is the number of the carriers in the semiconductor, R is the resistance of the device that fluctuate and α_H is the Hooge parameter which is in the order of 10^{-2} [45].

The resistance R is inversely proportional to the product of carrier mobility (μ) and number of carrier (N) i.e.

$$R \propto \frac{1}{\mu N}, \tag{3.58}$$

Since the fluctuation of mobility and fluctuation of carrier number are uncorrelated, it can be written that

$$\frac{S_R(f)}{R^2} = \frac{S_\mu(f)}{\mu^2} + \frac{S_N(f)}{N^2}. \tag{3.59}$$

If the fluctuation of carrier mobility dominates over the fluctuation of carrier number, then

$$\frac{S_R(f)}{R^2} \approx \frac{S_\mu(f)}{\mu^2} = \frac{\alpha_H}{fN}. \tag{3.60}$$

The mobility of carrier arises from scattering. Scattering of carriers can be originated from the lattice scattering due to phonon (acoustic lattice vibrations). Other scattering mechanisms like impurity scattering and electron scattering may also be involved. The combined influence on carrier mobility due to lattice scattering and impurity scattering can be given by Matthiessen's rule,

$$\frac{1}{\mu} = \frac{1}{\mu_{lattice}} + \frac{1}{\mu_{impurity}}. \tag{3.61}$$

Experimental results show that the dependence of α_H on mobility can be explained well considering the presence of lattice scattering only [46]. Then we can write,

$$\frac{\Delta\mu}{\mu} \approx \frac{\Delta\mu_{lattice}}{\mu_{lattice}}. \tag{3.62}$$

Therefore,

$$\alpha_H = \left(\frac{\mu}{\mu_{lattice}}\right)^2 \alpha_{lattice}\ . \tag{3.63}$$

If the fluctuation of carrier number dominates, then

$$\frac{S_R(f)}{R^2} = \frac{S_N(f)}{N^2}. \tag{3.64}$$

In 1955, McWhorter explained the generation of $1/f$ noise in semiconductor devices [47]. He proposed a carrier number fluctuation theory, which was based on Shockley-Read-Hall (SRH) process. In spite of having some limitations, the McWhorter model has been used by many authors to interpret the origin of $1/f$ noise in semiconductor devices [48],[49], [50].

As, we stated earlier, a semiconductor contains many defects. These defects function as trapping center for carriers. Figure 3.14 shows the four SRH processes that may occur in a $p-n$ junction when the depletion region contains a trapping center.

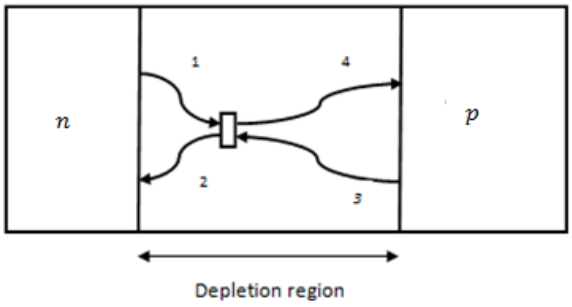


Figure 3.14: A single SRH trap in the depletion region of a $p-n$ junction and four SRH process- (1) electron capture (2) electron emission (3) hole capture and (4) hole emission.

When carriers get trapped and released afterwards, the current in the external circuit also fluctuates. This trapping and de-trapping events occur independently in time in a random sequence. Therefore, according to equation (3.64), the spectral density of resistance fluctuation can be given by [51]

$$S_R(f) = \left(\frac{R}{N}\right)^2 . S_N(f) = R^2 . \frac{\langle \Delta N \rangle}{N^2} . \frac{4\tau}{1+(2\pi f \tau^2)}. \tag{3.65}$$

where, τ is the time constant for a single trap level, N is the number of carriers in the sample and $\langle \Delta N \rangle^2$ is the variance of fluctuation ΔN in N. The noise spectrum due to number of carrier fluctuation $S_N(f)$ gives rise to a Lorentzian spectrum [52].

$$S_N(f) = 4\langle \Delta N \rangle^2 \frac{\tau}{1+(2\pi f \tau)^2}. \tag{3.66}$$

From equation (3.65), when $2\pi f\tau \ll 1$ i.e. at frequencies well below $1/2\pi\tau$, the spectrum becomes independent of frequency, which is similar to *white noise* . At high frequencies well above the corner frequency where, $2\pi f\tau \gg 1$ the spectral density falls off with $1/f^2$..

However, in typical $p-n$ juctions used as photodiodes, it is rare that only a single trap is involved. For discrete multiple-trap levels, the GR spectra would be according to the following equation

$$S_N(f) = 4\sum_i \langle \Delta N \rangle^2 \frac{\tau_i}{1+(2\pi f \tau_i)^2}. \tag{3.67}$$

where, ΔN_i is the variance of the fluctuation in the number of carriers for each individual trap level and τ_i is the time constant associated to each trap level. By a proper distribution of the time constants, the discrete multiple-trap levels yields a $1/f$ spectrum over the full frequency range rather than Lorentzian spectrum.

The distribution of time constants is proposed by McWhorter [47] in the following form,

$$g(\tau)d\tau = \frac{d\tau/\tau}{ln\left(\frac{\tau_2}{\tau_1}\right)} \qquad for \quad \tau_1 < \tau < \tau_2,$$
$$= 0 \qquad otherwise \qquad . \tag{3.68}$$

where, $g(\tau)d\tau$ is the time constant distribution and τ_1 and τ_2 are the two limits of the time constant of the traps. The discrete multiple trap levels merge to form a continuous trap distribution. The resulting noise spectral density can then be found by integrating over all trap levels through the associated continuum of trap constants. Considering the fluctuation of carriers expressed in equation (3.66) in conjunction with the distribution function of the time constants given in equation (3.68), the noise spectral density due to carrier number fluctuation would be,

$$S_N(f) = 4\langle \Delta N\rangle^2 \int_0^\infty \frac{\tau g(\tau)d\tau}{1+(2\pi f\tau)^2}. \tag{3.69}$$

By substituting the McWhorter distribution of time constants from equation (3.68) into equation (3.69) and integrating, the $1/f$ low-frequency noise spectrum $S_N(f)$ [52] can be obtained as follows-

$$\mathrm{S}_N(f) = \frac{\langle \Delta N\rangle^2}{fln\left(\frac{\tau_2}{\tau_1}\right)} \qquad for \quad \frac{1}{2\pi\tau_2} < f < \frac{1}{(2\pi\tau_1)},$$
$$= \frac{2\langle \Delta N\rangle^2}{\pi fln\left(\frac{\tau_2}{\tau_1}\right)} tan^{-1}(2\pi f\tau_2) \qquad for \quad 2\pi f\tau_1 \ll 1,$$
$$= \frac{2\langle \Delta N\rangle^2}{\pi fln\left(\frac{\tau_2}{\tau_1}\right)}\left[1 - \frac{2}{\pi} tan^{-1}(2\pi f\tau_1)\right] \qquad for \quad 2\pi f\tau_1 \gg 1. \tag{3.70}$$

The above derivation is valid only when the traps at different energy level do not interact with each other. In the case of interaction among the traps, a Lorentzian spectrum would be found instead of $1/f$ noise spectrum [53].

While deriving the above equation, it has been assumed that the concentrations of traps are same, but it is generally not the case. Therefore, in practice, it shows a $1/f^{\alpha}$ pattern where α varies between 0.5-2 [54]. Trapping and de-trapping of carriers are non-fundamental sources of noise. The magnitude of spectra is proportional to the trap density and the noise effect can be reduced significantly by eliminating most of the traps [52].

But this model has some limitations. McWhorter stated that $1/f$ noise evolves from the interaction between free charge carriers and the traps which are distributed near the surface oxide layer on the semiconductor [45]. But it is well known that metal, semiconductors without oxide

layer also exhibit $1/f$ noise. Besides this, McWhorter model fails to explain the origin of $1/f$ noise in thermoelectric emf and Hall voltage [51].

Hooge proposed that the origin of $1/f$ noise is due to the fluctuation of the mobility of carriers. Experimental results also support this model [45], [51]. If the fluctuation of carrier mobility dominates over fluctuation of the carrier number, then from equation (3.60) we find that,

$$\frac{S_R(f)}{R^2} = \frac{S_\mu(f)}{\mu^2}. \tag{3.71}$$

The relation between the diffusion coefficient (D) and the carrier mobility can be obtained from the well-known Einstein equation for non-degenerate semiconductors, given by,

$$\frac{D}{\mu} = \frac{kT}{q}. \tag{3.72}$$

Therefore, equation (3.71) can be written as,

$$\frac{S_R(f)}{R^2} = \frac{S_\mu(f)}{\mu^2} = \frac{S_D(f)}{D^2}. \tag{3.73}$$

where, $S_D(f)$ is the spectral density due to fluctuation of the diffusion coefficient. From equation (3.73), it can be said that semiconductor devices involving diffusion process like $p-n$ junction diodes also causes $1/f$ noise. According to Hooge, the $1/f$ noise is a bulk effect.

3.2 Noise Associated with CMOS Pixel

The noises observed in a CMOS pixel can be classified as-

- Thermal noise
- Shot noise
- Flicker noise, and
- RTS noise

All the above-mentioned noise sources fluctuate over time, and therefore, they are commonly referred as temporal noise by many texts [1], [5], [6].The temporal noise is the fundamental limiting factor in the performance of the image sensor, particularly under low levels of illumination and in video applications [55].

3.2.1 Thermal Noise

In a CMOS pixel, thermal noise comes mostly from the reset transistor and from the source-follower transistor. The thermal noise, originated from the MOS reset switch is usually referred

to as *Reset noise.* A MOS transistor can be considered as a resistance, R_{MOS} when it is 'ON' and due to the resistive effect, it causes thermal noise. This noise is sampled and held by the

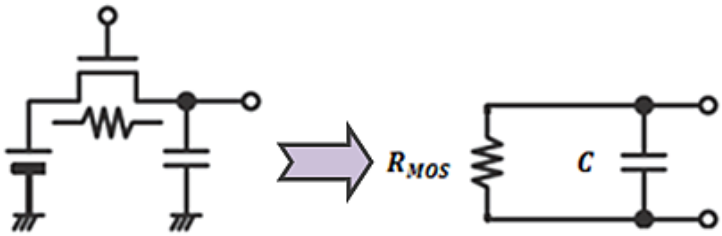


Figure 3.15: Equivalent circuit that produces reset noise.

accumulation node, which is the photodiode junction capacitance in a 3T-APS and the floating diffusion (FD) capacitance in a 4T-APS.

The open circuit mean-square of thermal noise voltage power is given by equation (3.5),

$$\langle (V_n)^2(f) \rangle = 4kTR_{MOS}\Delta f. \tag{3.74}$$

The voltage on the accumulation node can be obtained from the voltage divider rule.

$$\begin{aligned} V_{pd} &= \left| \frac{1/j2\pi fC}{R_{MOS} + \frac{1}{j2\pi fC}} \right| V_n, \\ &= \left| \frac{1}{1 + j2\pi f R_{MOS} C} \right| V_n, \\ &= \frac{1}{1 + (2\pi f R_{MOS} C)^2} V_n. \end{aligned} \tag{3.75}$$

Therefore, the reset noise is given by [5], [6] as,

$$\langle V_{reset}^2 \rangle = \langle V_{pd}^2 \rangle = \int_0^\infty \left| \frac{4kTR}{1 + (2\pi f R_{MOS} C)^2} \right| df = \frac{kT}{C}. \tag{3.76}$$

The noise power of the charge would be,

$$Q_{pd}^2 = \left(CV_{pd} \right)^2 = kTC. \tag{3.77}$$

The reset noise is therefore also called as kTC noise, which is a function of the temperature and the capacitance value. From equations (3.76) and (3.77), it is seen that the reset noise is independent of R_{MOS}. This is due to the fact that, the bandwidth decreases as R_{MOS}. increases and vice versa. Therefore, the increase of thermal noise voltage due to increase of R_{MOS}. is nullified by the decrease of bandwidth and vice versa.

The kTC noise can be eliminated by using correlated double sampling (*CDS*) technique in 4T-APS. But CDS technique is difficult to implement in 3T-APS [6].

Reset noise depends on the operation mode of the reset transistor. When the reset transistor operates in the sub-threshold region, the electrons stored in the photodiode node slowly moves toward the reset drain during the reset period. As a result, the photodiode node is not fully discharged within the reset time period. This type of reset is known as *Soft reset*. This problem can be avoided by using a pMOS device as a reset transistor. But a pMOS transistor requires more area than the nMOS since it needs an n-well area [1].

On the other hand, when the reset transistor operates in its linear region, the electrons stored on the photodiode node can quickly get discharged by delivering the electrons to the drain. This type of reset is called a *Hard Reset*.

The reset noise in the soft reset mode is reduced to approximately $1/2$, which is due to the current rectification effect during the reset [1]. Therefore, the mean square thermal noise voltage power due to soft reset is given by,

$$\langle V_{reset}^2 \rangle \approx \frac{kT}{2C}. \tag{3.78}$$

A drawback of the soft reset is that it introduces image lag which is caused by the residual charge that remains in the PD node after the reset period. This charge remains in the pixel during the next consecutive exposed frame and may corrupt the image, especially images of bright objects in low-light scenes.

The hard reset has the advantage that it can establish maximum possible potential on the photodiode, and can remove the charges due to previous potential on the photodiode. Thus, there remains no image lag or excess or deficit charge on the PD node from the previous exposure to light.

To get rid of the image lag and at the same time to decrease the kTC noise in 3T-APS, a combination of hard reset and soft reset is used and this technique is called flushed reset. In a flushed reset, the PD is first reset by a hard reset to flush the accumulated electrons completely. It is then reset by a soft reset which reduces the kTC noise. A flush reset requires a switching circuit to alternate the bias voltage of the gate in the reset transistor [56].

Reset noise has significant impact on temporal noise floor and thus it limits maximum achievable dynamic range (*DR)* [56].

The thermal noise generated by the source-follower (*SF*) transistor is given by,

$$\langle V_{thSF}^2 \rangle = \frac{4\overline{\gamma}kT}{g_m} \Delta f. \tag{3.79}$$

where, g_m is the transconductance of the source-follower transistor and $\overline{\gamma}$ is a coefficient that depends on the mode of operation of the transistor and is $2/3$ for long-channel transistors [1].

Therefore, for a long channel SF transistor the mean-square voltage power of thermal noise would be

$$\langle V_{thSF}^2 \rangle = \frac{8kT}{3g_m} \Delta f. \tag{3.80}$$

and the mean-square thermal noise current power would be,

$$\langle i_{thSF}^2(f) \rangle = \langle V_{thSF}^2 \rangle g_m^2 = \frac{8kT\, g_m}{3} \Delta f. \tag{3.81}$$

3.2.2 Shot Noise

The photodiode is the main contributor of shot noise in the CMOS pixel. In section 3.1.2, we have discussed the various sources of shot noise in photodiode. In CMOS pixel, shot noise is associated with incident photon and dark current, and thus, is classified as photon shot noise and dark current shot noise, respectively.

The probability that N particles are emitted during a certain time interval is given by the Poisson probability distribution, which can be represented as,

$$P(N) = \frac{(\overline{N}).exp\,(-\overline{N})}{N!}. \tag{3.82}$$

where N is the number of particles and $\overline{N}$ is the average number of particle. According to Poisson distribution, the variance is equal to the average value.

$$n^2 = \langle (N - \overline{N})^2 \rangle = \overline{N}, \tag{3.83}$$

If N_{dark} is the average number of dark charge and N_{ph} is the average number of signal charge, then

$$n_{dark}^2 = N_{dark}\,, \tag{3.84}$$

$$n_{ph}^2 = N_{ph}, \tag{3.85}$$

The dark charge reduces the pixels' dynamic range because the capacity of the well is limited. It also changes the output level corresponding to dark (no illumination) conditions. Therefore, it is necessary to clamp the dark level to provide a reference value for a reproduced image [1]. The

amount of dark charge, Q_{dark} and signal charge, Q_{ph} is proportional to the integration time, Δt_{reset} .Therefore,

$$N_{dark} = \frac{Q_{dark}}{q} = \frac{I_{dark} . \Delta t_{reset}}{q} = n_{dark}^2 . \quad (3.86)$$

$$N_{ph} = \frac{Q_{ph}}{q} = \frac{I_{ph} . \Delta t_{reset}}{q} = n_{ph}^2 . \quad (3.87)$$

Now, the dark current shot noise,

$$\langle v_{dark} \rangle^2 = \left[\frac{(q n_{dark})^2}{C^2}\right] = \frac{q^2\left(\frac{I_{dark} . \Delta t_{reset}}{q}\right)}{C^2} = \frac{I_{dark} . \Delta t_{reset}}{C^2} q \quad .(3.88)$$

Similarly, the photon shot noise would be,

$$\langle v_{ph} \rangle^2 = \frac{I_{ph} . \Delta t_{reset}}{C^2} q. \quad (3.89)$$

where C is the accumulation capacitance, which is the photodiode junction capacitance for a 3T-APS and a floating diffusion capacitance for a 4T-APS, respectively. Since, these two processes are mutually independent, the total shot noise in a CMOS pixel would be,

$$\langle v_{shot} \rangle^2 = \langle v_{dark} \rangle^2 + \langle v_{ph} \rangle^2 = \frac{(I_{dark} + I_{ph}) . \Delta t_{reset}}{C^2} q. \quad (3.90)$$

3.2.3 Flicker Noise

In a CMOS APS, flicker or $1/f$ noise originates mostly from the buffering source-follower nMOS transistor between the photodetector in APS and the readout matrix in the imager. The column bias nMOS transistor can also contribute to $1/f$ noise [5]. As we have discussed in section 3.1.3, the photodiode in the imager can also function as a source of $1/f$ noise in a CMOS pixel.

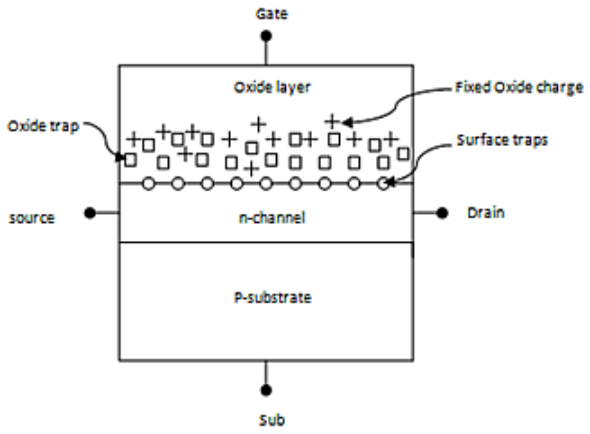


Figure 3.16: Distribution of traps in nMOS transistor.

Here we shall discuss the $1/f$ noise in a nMOS transistor. In section 3.1.3, we have discussed two popular theories which have been proposed to explain the physical origins of the $1/f$ noise. One is based on carrier number fluctuation theory, originally proposed by McWhorter where the origin of $1/f$ noise is explained by the random trapping and de-trapping of charge carriers in oxide traps with different relaxation times near the Si-SiO_2 interface. Another theory is based on the fluctuation of carrier mobility, proposed by Hooge where $1/f$ noise is assumed to be originated from the semiconductor bulk instead of surface [51], [53].

The origin of $1/f$ noise in a nMOS transistor can be explained well by McWhorter's number fluctuation theory as the charge flows near the oxide-semiconductor interface. Experimental results also shows the same $1/f$ behaviour in nMOS that is predicted by the carrier fluctuation model [57].

The density of traps near the oxide-semiconductor interface is high. These traps can capture and emit carriers very fast, and thus commonly named as *fast traps*. Again, the oxide layer itself contains traps. The traps get distributed in the oxide layer within a few Angstroms from the oxide-semiconductor interface. These traps are slow in capturing and emitting electrons, and thus are called *slow traps*.

The fast surface states undergo SRH process to exchange carriers with the conduction band or the valence band. The surface states can also exchange carriers with the slow oxide traps through tunnelling. In a nMOS transistor, when an electron is captured from the conduction band by an empty surface state, it causes a net charge fluctuation in the n-channel. Thus the drain current fluctuates. This captured electron can jump to conduction band if it is thermally excited or recombine with a hole by capturing it from the valence band. Anyway, the exchange of a hole between the valence band and the surface states does not make any net charge fluctuation in the conduction channel and thus have no impact on low frequency noise.

The electron captured by a surface state can be acquired by a slow oxide trap through tunnelling. Using McWhorter's model, Reimbold developed a relation for power spectral density of drain current assuming uniform distribution of traps across the whole channel [18].

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{q^4 \lambda_t}{AkT} \frac{1}{f} \frac{N_t}{(C_{ox} + C_D + C_{it} - \beta Q_n)^2}. \tag{3.91}$$

Where, λ_t = tunneling constant for electrons, N_t= density of traps, A= device area, C_{ox}= oxide capacitance, C_D= depletion capacitance, C_{it}=interface trap capacitance per unit area, Q_n= channel

charge per unit area and $\beta = \frac{q}{kT}$. For weak inversion $|\beta Q_n| \ll C_{ox} + C_D + C_{it}$, then

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{q^4 \lambda_t}{AkT} \frac{1}{f} \frac{N_t}{(C_{ox}+C_D+C_{it})}. \tag{3.92}$$

At low gate bias voltage, equation (3.92) predicts a constant plateau at a given frequency since C_D varies very slowly with bias and variation of C_{ox} and C_{it} is very small. In strong inversion, Q_n increases with gate voltage and $|\beta Q_n| \gg C_{ox} + C_D + C_{it}$, then

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{q^4 \lambda}{AkT} \frac{1}{f} \frac{N_t}{\beta^2 Q_n^2}. \tag{3.93}$$

Therefore, at a given frequency, $S_{I_D}(\ )/\ ^2$ falls sharply with gate voltage.

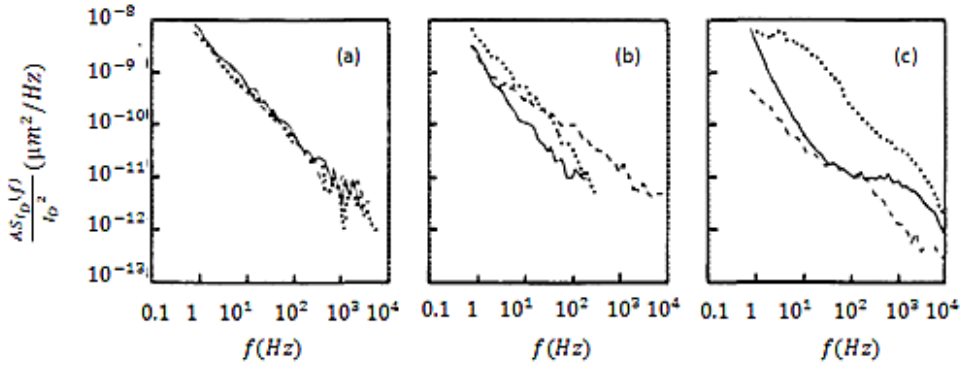


Figure 3.17: Noise PSD of *n*MOS transistor's at $V_g = 2V, T = 293K$. (a) Three $20 \times 20\mu m$ devices, active area 350 μm^2, $V_d = 100$ mV,$I_D = 3.5\mu A$; (b) three $20 \times 20\mu$m devices, active area 15 μm^2,$V_d = 20mV$,$I_D = 15\mu A$; c) three$2 \times 2\mu$m devices, active area 0.4 μm^2,$V_d = 20mV$,$I_D = 500nA$ .The white noise has been removed [16].

Figure 3.17 describes the experimental results on the dependency of the power spectral density of the drain current on the device area [16]. The experiment was performed in strong inversion mode, keeping the gate voltage unchanged. To compare the results between devices of different active area $S_{I_D}(\ )/\ ^2$ was scaled by the device area. From the experiment, it was found that the PSD curves didn't exhibit smooth $1/f$ behaviour as the device area shrinks.

3.2.4 RTS Noise

In small area devices, only a few traps remain within a few kT of the Fermi level, and they produce specific low noise behaviour [17]. According to [16], in these small area devices, the noise power spectral density for each device consists of a few individual Lorentzians. And if the

noise power spectral density of many such devices are averaged, it would give the same spectral distribution as it can be observed in large area devices as shown in Figure 3.17 (a).

The Lorentzian is caused by the trapping and de-trapping of an electron by an individual interface defect near the $Si - SiO_2$ interface. In small area devices, trapping and de-trapping process causes random fluctuation in the drain current of the MOS transistor between two discrete levels and produces Random Telegraph Signal (RTS) noise in the drain current. The RTSs are thus considered as one of the fundamental components of $1/f$ noise in MOSFETs. The RTS behaviour in submicrometer area MOSFETs, originating from trapping and de-trapping of an electron provide a strong base to support the carrier fluctuation model [16], [42].[58]

Figure 3.18 shows the random behaviour of the drain current in MOS transistor. When an electron is captured by a trap, the drain current switches to the lower value and remains at the same state as long as the electron remains trapped. When the trapped electron is released, the drain current jumps to the high value and remains at the same state as long as another electron is captured by the trap. The mean trapping and de-trapping time, which are commonly named as mean capture time (τ_c) and mean emission time (τ_e), respectively, are V_{GS} and temperature dependent [59].

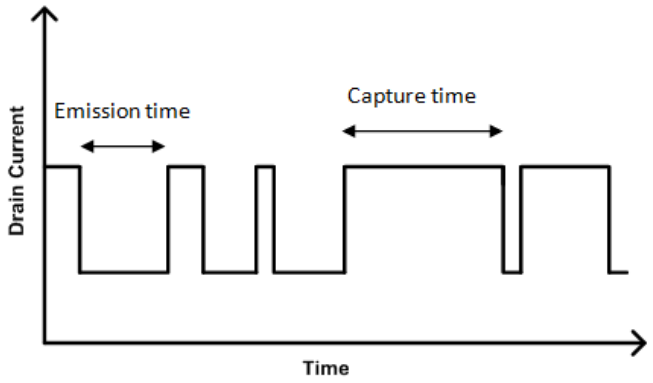


Figure 3.18: Random telegraph behaviour of drain current of a MOS device.

The capture time and emission time, as well as the magnitude of the voltage or drain current fluctuation determine the characteristics of the RTS noise. The capture and emission process can be explained by Shockley-Read-Hall (SRH) theory. The SRH theory [60] was originally developed to describe the generation-recombination process through bulk states. But it can also be used to describe the trapping and de-trapping of carriers by the interface traps. Figure 3.19 shows the charge exchange process between an interface trap and the conduction or valence

band of a semiconductor.

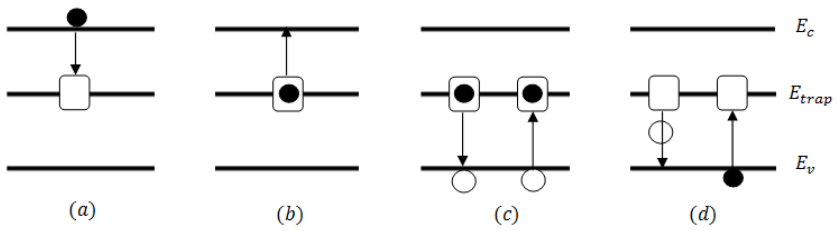


Figure 3.19: Four SRH processes involved in recombination by trapping: (a) electron capture, (b) electron emission, (c) hole capture and (d) hole emission.

The probability that a trap of energy E_{trap} is occupied can be obtained from the Fermi-Dirac statistics [60].

$$f(E_{trap}) = \frac{1}{1+exp\left[\frac{E_{trap}-E_F}{kT}\right]}, \tag{3.94}$$

where, E_{FT} is the Fermi-level associated with the trap. The probability that a trap is empty is given by,

$$1 - f(E_{trap}) .$$

Therefore, the rate of capture of an electron can be given by,

$$R_c = v_t \sigma_n n[1 - f(E_{trap})], \tag{3.95}$$

where, v_t is the speed of the electron , σ_n is the electron-capture cross section at the oxide semiconductor interface and *n* is the concentration of electrons at the interface, given by,

$$n = N_c exp\left[\frac{E_F - E_c}{kT}\right], \tag{3.96}$$

where, N_c represents the density of states in the conduction band. And the rate of emission of an electron from the trap to the conduction band is given by

$$R_e = v_t \sigma_n n_t f(E_{trap}), \tag{3.97}$$

Here, n_t is the electron concentration in the conduction band when the Fermi-level falls at E_{trap} and can be given by

$$n_t = N_c exp\left[\frac{E_{trap}-E_c}{kT}\right], \tag{3.98}$$

From equations (3.96) and (3.98), we get,

$$\frac{n}{n_t} = exp\left[\frac{E_F - E_{trap}}{kT}\right], \tag{3.99}$$

The mean capture time can be given by,

$$\tau_c = \frac{1}{v_t \sigma_n n}. \tag{3.100}$$

And the mean emission time would be,

$$\tau_e = \frac{1}{v_t \sigma_n n_t}. \tag{3.101}$$

Using equations (3.99), (3.100) and (3.101), we get,

$$\tau_e = \frac{n}{n_t}\tau_c = \tau_c exp\left[\frac{E_F - E_{trap}}{kT}\right]. \tag{3.102}$$

If $E_F = E_{trap}$, then from equation (3.102), we find that $\tau_e = \tau_c$ which means that the mean capture time and the mean emission time would be same if the trap energy (E_{trap}) coincides with the Fermi energy level (E_F).

The time constants can be controlled by controlling the gate voltage [61]. From equation (3.100), we can see that the mean capture time is inversely proportional to the concentration of electrons at the interface. Therefore, any change in n would affect the mean capture time. In an nMOS, if the gate-to-source voltage (V_{GS}) is increased, the concentration of electrons near the interface (n) also increases due to increased band banding which ultimately reduces the mean capture time (τ_c) according to equation (3.100).

Figure 3.20 shows the effect of increasing V_{GS} on the energy bands of an nMOS. The dotted lines show the change corresponding to an increase in the gate voltage V_{GS}. $\Delta\psi_s$ is the change in the surface potential and ϕ_B denotes the potential of the bulk Fermi-level, E_F with respect to the intrinsic level, E_i.

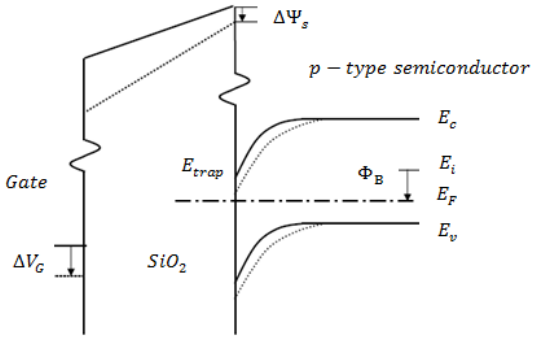


Figure 3.20: Change of band bending in an nMOS due to gate voltage V_{GS}.

From equation (3.102), we can see that at a given temperature, the emission time depends on the trap energy (E_{trap}). The trap energy is given by [61], [62],

$$E_{trap} = E_{trapFB} - \frac{qd}{t_{ox}}[V_{GS} - \psi_s - V_{FB}]. \quad (3.103)$$

where d is the distance of the trap from the oxide-semiconductor interface, t_{ox} is the thickness of the gate-oxide, ψ_s is the surface potential, V_{FB} is the flatband voltage of the transistor and E_{trapFB} denotes the trap-energy at flat-band.

It is evident from equation (3.103) that, the energy of the traps at the interface ($d = 0$) is independent of gate-to-source voltage and thus the mean emission time for an interface trap is independent of V_{GS}. But the energy of the traps located in the oxide layer exhibit dependency on V_{GS}. For this sort of traps, E_{trap} decreases with increasing V_{GS}, which, according to equations (3.98) and (3.99) , reduces n_t and it ultimately increases the mean emission time (see equation (3.101)).

Equations (3.100) and (3.101) also indicates that the time constants are inversely proportional to the capture cross-section σ_n. The capture cross-section is the effective area of the trap which indicates the probability of capturing an electron by the defect [60]. A large cross-section indicates higher probability of capturing an electron and thus reduces the capture and emission times.

As stated earlier, an electron needs to tunnel through the oxide in order to get captured by a trap, located in the oxide. According to Schrödinger's equation, the wave-function $\varphi(x)$ decays exponentially as the electron tunnels deeper into the oxide [23], [61]. That is $\varphi(x)$ is given by

$$\varphi(x) = Aexp(-k_1 x). \quad (3.104)$$

Where k_1 is the decay constant and can be given by,

$$k_1 = \sqrt{\frac{2m_{eff}}{\hbar^2}(V_0 - E)}. \quad (3.105)$$

In equation (3.105), m_{eff} is the effective mass of the electron, $\hbar$ is Planck's constant, V_0 is the potential barrier which is the difference between the electron affinities of semiconductor (Si) and the oxide (SiO_2), and E is the kinetic energy of the electron.

The probability of finding an electron $(|\varphi(x)|^2)$ inside the oxide layer reduces exponentially. The capture cross section of the trap also exhibits a similar expression as equation (3.104), which is given by [61], [63],

$$\sigma_n = \sigma_{n0} exp(-2k_1 d). \quad (3.106)$$

where d is the distance of the trap in the oxide, and σ_{n0} is the intrinsic capture cross section of

the trap at the interface.The probability that the trap is filled or occupied i.e. the steady-state trap-occupancy can be expressed in terms of emission time and capture time. Again, we know that,

$$f(E_{trap}) = \frac{1}{1 + exp\left[\frac{E_{trap} - E_F}{kT}\right]}$$

$$= \frac{1}{1 + \frac{\tau_c}{\tau_e}} \qquad from(equation\ 3.102)$$

$$= \frac{\tau_e}{\tau_c + \tau_e}.$$

(3.107)

The drain current fluctuation, ΔI_D due to RTS is calculated by assuming the fact that the conductivity of the channel is changed by an elementary electron charge [64], [65]. The magnitude of the fluctuation depends on instantaneous bias conditions. The relative RTS amplitude can be expressed as a combined contribution of the number of carriers and the carrier mobility fluctuation [64], [65]. This is given by

$$\frac{\Delta I_D}{I_D} = \frac{\Delta N}{N} + \frac{\Delta \mu}{I\mu} = -\frac{1}{WL}\left[\frac{1}{V_{th}(C_{ox}+C_D)+N_s} \pm \overline{\alpha}\mu\right]. \qquad (3.108)$$

where, N_s is the surface concentration of carriers in the channel, μ is the carrier mobility, W/L is the width/length of gate, $\overline{\alpha}$ is the mobility scattering coefficient and $V_{th} = kT/q$ is the thermal voltage. The sign in front of the second term is determined by the condition of the trap i.e. whether a trap is neutral or charged after capturing an electron. The first term of equation (3.108) expresses the screening of charged traps by channel electrons. Thus, at a given drain bias, the behaviour of the RTS amplitude is determined by the carrier number fluctuations. Also, $\overline{\alpha}$ can be considered constant if the gate-voltage does not change significantly.

In weak inversion, $N_s \ll V_{th}(C_{ox} + C_D)$ and thus $(\Delta I_D)/I_D$ remains almost constant as we have said earlier that C_D and C_{ox} varies very slowly with bias. But in strong inversion, $N_s \geq V_{th}(C_{ox} + C_D)$ and $(\Delta I_D)/I_D$ drops sharply. The second term of equation (3.108) describes the effect of mobility fluctuations, which arises mainly from Coulomb scattering by charged traps. Traps that are further away from the semiconductor-oxide interface produce a smaller$(\Delta I_D)/I_D$. And scattering is higher for those traps that become charged after capturing electron.

Considering the capture cross section is thermally activated ,it can also be expressed as,

$$\sigma_n = \sigma_{n0} exp\left(-\frac{\Delta E_a}{kT}\right). \quad (3.109)$$

where ΔE_a is the activation energy required for capturing an electron.This relation evolves from the multiphonon mechanism in bulk semiconductors. Therefore from equation (3.100) we can write,

$$\tau_c = \frac{exp\left(-\frac{\Delta E_a}{kT}\right)}{v_t \sigma_{n0} n}. \quad (3.110)$$

This equation can be used to explain the temperature dependence of the mean capture and emission times.

Chapter 4

RTS Noise in CIS

As the CMOS technology continues to downscale toward the deep sub-micron range, the low frequency noise in MOS devices is dominated by the random telegraph signal (RTS) noise. It is now well established that, the in-pixel source-follower (SF) transistor in the APS is the most dominating contributor of RTS noise and thus causes significant performance degradation [13].

Two important performance parameters of CIS pixel are the quantum efficiency (η) and fill factor (*FF*). Quantum efficiency is a measure of generated electron-hole pairs (EHPs) per incident photon, while the fill factor is the percentage of the photo sensitive area compared to the total area of a pixel.

$$QE = \frac{no.\ of\ \ EHPs\ \ generated\ \ \ per\ \ sec}{no.\ of\ \ Photon\ \ \ incident\ \ \ per\ \ sec} = \frac{I_{ph}/q}{\phi}. \tag{4.1}$$

$$FF = \frac{photosensitive\ \ \ area}{total\ \ \ pixel\ \ \ area} \times 100\%. \tag{4.2}$$

In order to improve both performance parameters, a larger photosensitive area is necessary. This requires transistors of reduced channel area.

As we have already discussed earlier, these smaller area transistors are most likely to get afflicted by RTS noise. The sensitivity of the pixel at low light level is degraded due to the presence of RTS noise that gives rise to flickering [13], [58],[66], as shown in Figure 4.1.

Also, as discussed in section 3.2.4, we can see from equations (3.102) and (3.110) that the three RTS parameters in time domain - mean capture time (τ_c), mean emission time (τ_e) and the magnitude of fluctuation (ΔI_d) or (ΔV) vary with the gate to source voltage (V_{gs}) of the MOS device, and actually change with the concentration of electrons (n) in the channel, temperature (T), channel area (WL), oxide thickness (t_{ox}), trap position (x_{trap}) and trap energy level (E_{trap}) etc. RTS time constants and amplitude also get affected by *Fowler-Nordheim* stress [67] and radiation [68].

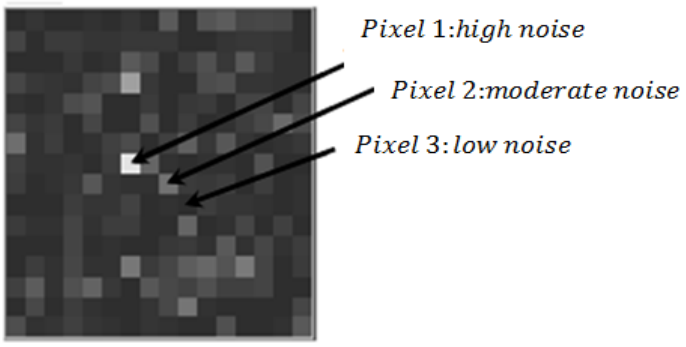


Figure 4.1: Flickering pixels in an array of APSs [66].

In this chapter, we shall discuss the experiments on RTS noise that were carried out on active pixel sensors. The objectives of these experiments were to observe and analyze the response of the time constants and amplitude of RTS with varying bias voltage (V_{bias}) and temperature (T).

4.1 Measurement Set-up and Procedure

Figure 4.2 shows the experimental set-up to characterize the RTS noise in CMOS APS. All the experiments were carried out in dark. In order to avoid other electromagnetic interference that can hamper the noise measurement, the DUT was kept in a metal box. Since RTS noise is temperature sensitive, all the experiments was performed in a temperature controlled environment.

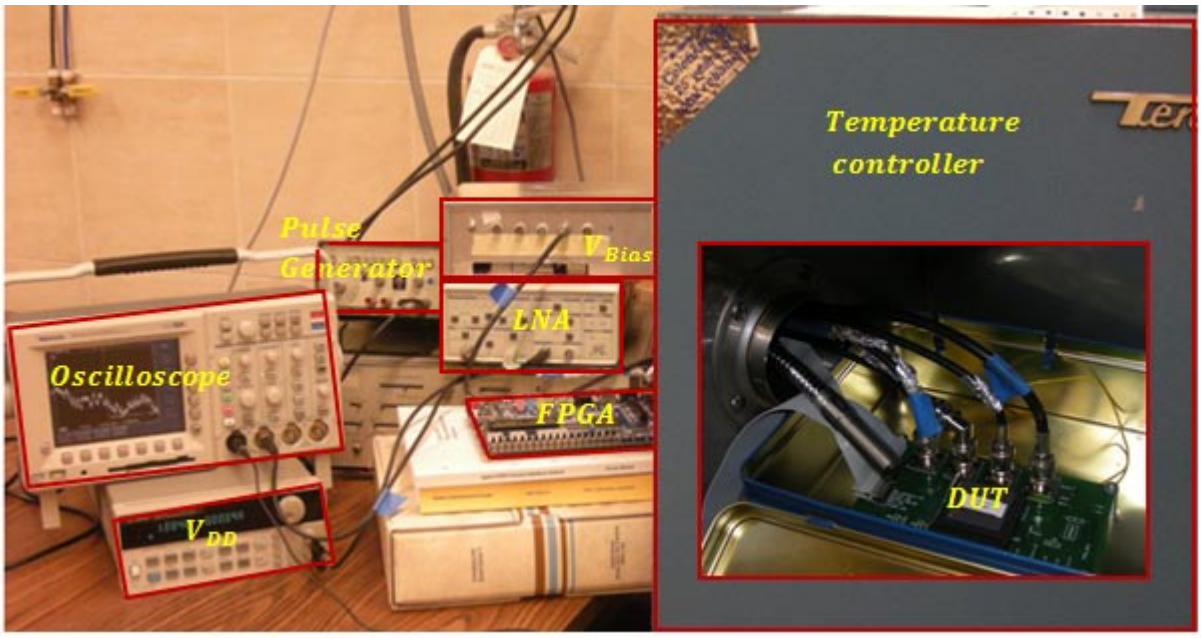


Figure 4.2: Experimental set-up.

The DUT board contains the image sensor chip (see figure 4.3), which is a 16×16 array of 3T-APS having a FF of 60%. The chip was fabricated in a standard 0.18 μm CMOS technology and a chip micrograph is shown in Figure 4.3. The pitch of each pixel is 30 μm $\times$ 20 μm. The important sensor characteristics are provided in Table 4.1.

A pulse generator was used to provide the reset pulse for the APS. V_{DD} was applied from a regular power supply while a battery bank was used for pixel biasing (V_{bias}). The gain of the low noise amplifier (LNA) was kept in the range of $5 - 10$ times since the RTS fluctuation occurs in the millivolt (mV) range. The output DC offset is much larger than the measured noise.

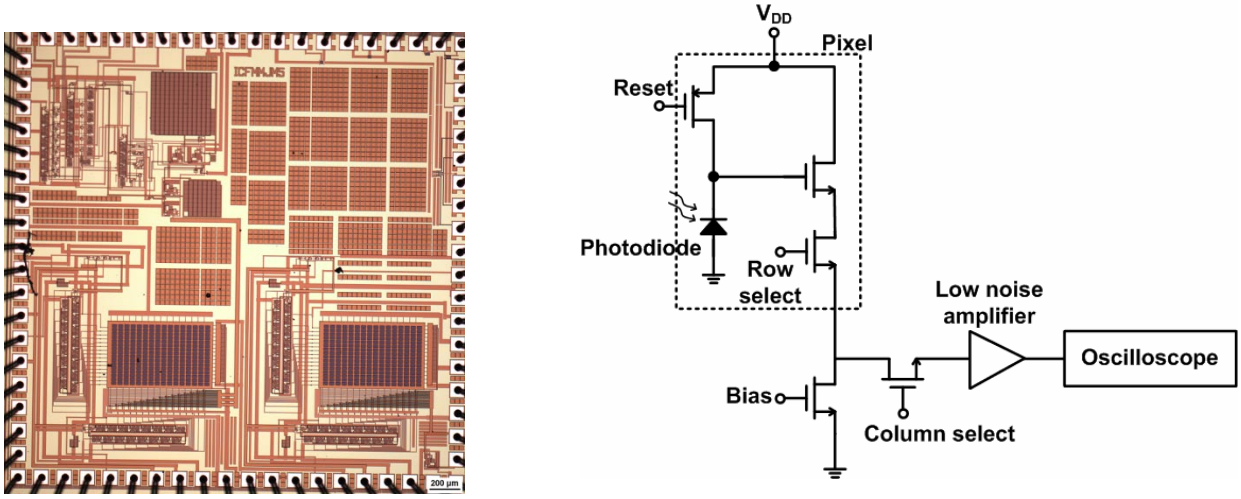


Figure 4.3: Photomicrograph of the CMOS image sensor chip (left) and schematic of the experimental set-up from pixel level (right).

Technology	Standard 0.18 μm CMOS
Number of Pixels	16×16
Pixel Area	30 μm $\times$ 20 μm
Fill Factor	60%
Transistors per pixel	3
Channel area of SF transistor (W×L)	1μm × 180nm
Oxide thickness of SF transistor	4nm

Table 4.1: 16 ×16 CMOS APS characteristics

In order to keep the output signal within the range of the oscilloscope, the DC offset signal needs to be eliminated. This offset cancellation was achieved by setting the high-pass

filter (HPF) of the LNA at 0.03 Hz. The low-pass filter (LPF) helps to eliminate the high frequency noise. This LPF setting was varied in the range of $3K - 10K$ Hz. A field programmable gate array (FPGA) board was used to select the APS manually from the array.

4.1.1 60Hz Noise Removal

In our experiment, we used a regular power supply, a pulse generator and a LNA which were directly driven by the AC power supply. As a result, our measurement was affected largely by the 60Hz line pick up noise. Though the time constants and amplitude of RTS noise fluctuation were not affected by the 60Hz noise, the presence of line pick up noise made it difficult to plot the amplitude histogram of the RTS noise.

In our work, we took the advantage of digital signal processing (DSP). The original signal was processed by using a 60Hz notch filter in MATLAB. As shown in figure 4.4 the output of the notch filter produces better result compared to the original one.

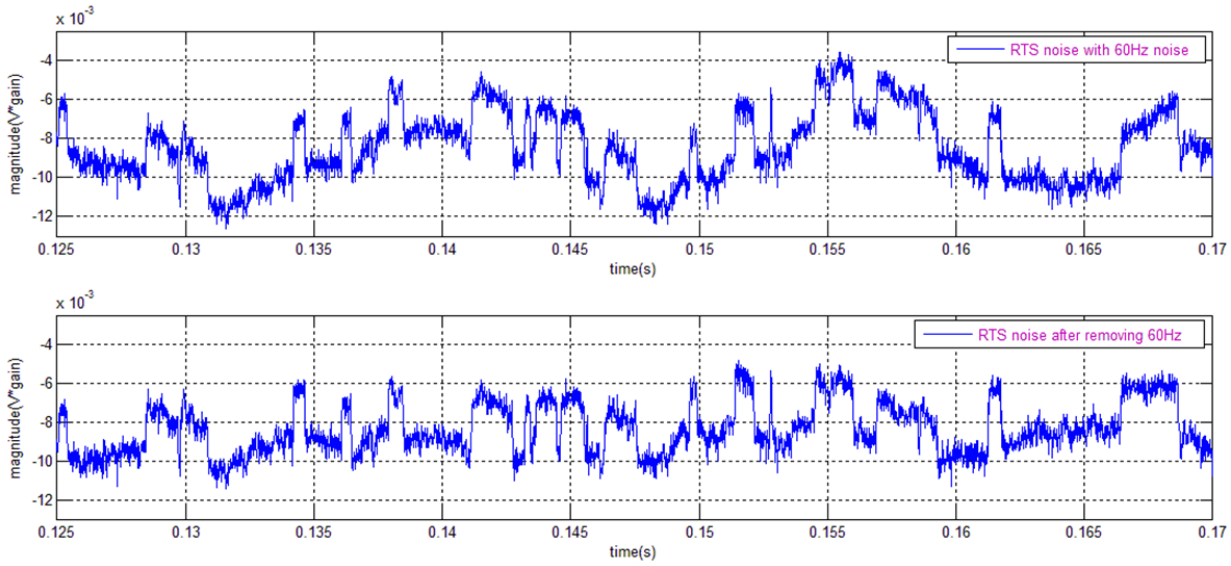


Figure 4.4: RTS noise with (top) and without (bottom) 60Hz noise.

4.1.2 RTS Noise Identification

As stated earlier, the time constants of the RTS noise are of great importance. Therefore, it is necessary to measure the time constants more accurately and efficiently. We have measured the time constants from the time derivative of the original signal.

Before performing the time derivation, a five point triangular smoothing was carried out on the

signal.

$$S_j = \frac{(Y_{j-2}+2Y_{j-1}+3Y_j+2Y_{j+1}+Y_{j+2})}{9} \quad (4.3)$$

Smoothing helps to reduce the high frequency components from the signal. A five point triangular smoothing is very useful when peaks of a signal are very important. Figure 4.5 (a) and (b) show the signals before and after smoothing, respectively.

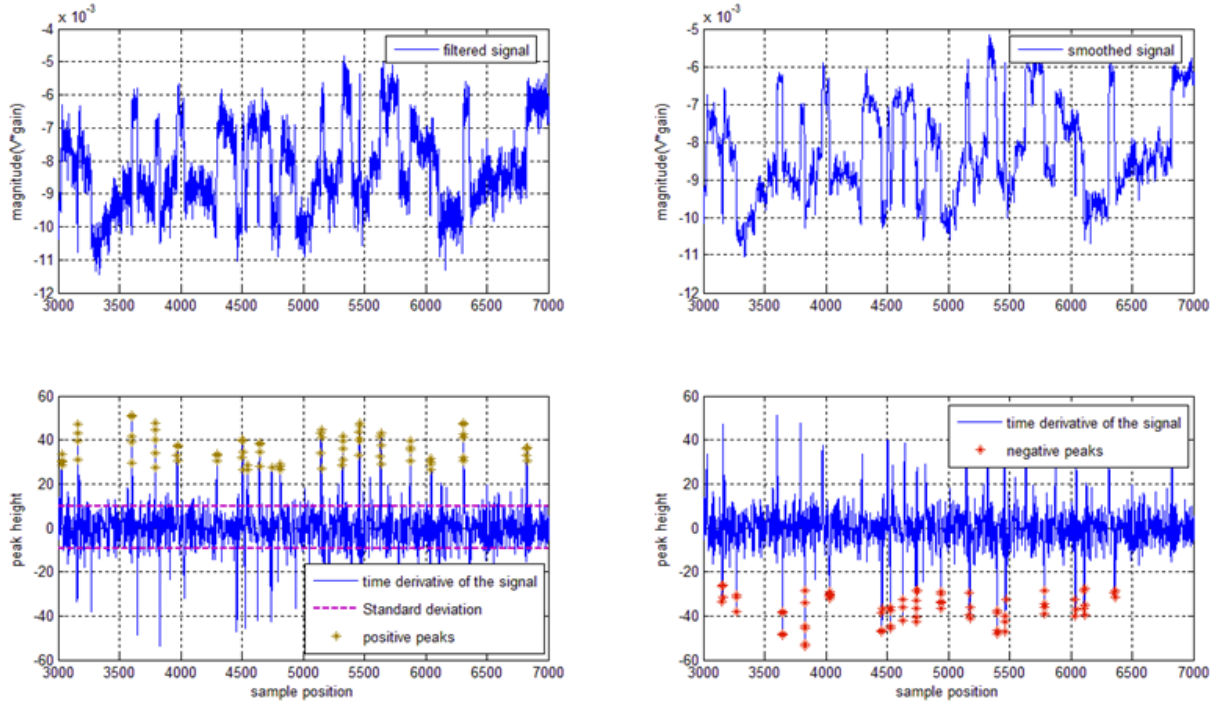


Figure 4.5: RTS noise a) before smoothing b) after smoothing c)positive transitions d) negative transitions.

After the smoothing of the signal, the time derivative of the smoothed signal was taken. The time derivative of a signal helps to find out the rapid changes in a signal and produces large spikes when a transition occurs. From the time derivative of the smoothed signal, the standard deviation (*SD*) was calculated. At the point of RTS noise transitions, the value of the derivative is much higher than the *SD*. Those transition points were identified and the time constants were calculated using an automated process which speeds up the calculation.The time derivative of the smoothed signal is shown in figure 4.5 (c) and (d). Those peaks were selected when,

$$\left|\frac{\Delta S}{\Delta t}\right| \geq 2.7 \times SD \quad (4.4)$$

where, ΔS is the change in the magnitude of the smoothed signal within the time interval of Δt.

4.2 Experimental Results and Discussion

The RTS noise experiment was carried out using the set-up and procedure described in the section above. All measurements were performed in time domain, since all the RTS parameters can be extracted easily from the time domain data. From the frequency domain measurements only the corner frequency (f_C) can be obtained. But these measurements cannot give complete information about the RTS noise. In this section, we present and explain our experimental results obtained from a 16×16 array of 3T-APS fabricated in a standard 0.18 μm CMOS technology.

4.2.1 RTS Noise in t and f Domain

As discussed earlier, the trapping-detrapping process due to a single carrier gives rise to a Lorentzian-shaped noise spectrum [17], [52]. Equation (3.66) can be re-arranged as,

$$PSD = \frac{P}{1+\left(\frac{f}{f_C}\right)} \tag{4.5}$$

where, f_C is the corner frequency, τ is the characteristic time constant of the trap and P is the plateau at low frequency. In equation (4.5),

$$f_c = \frac{1}{2\pi\tau} \tag{4.6}$$

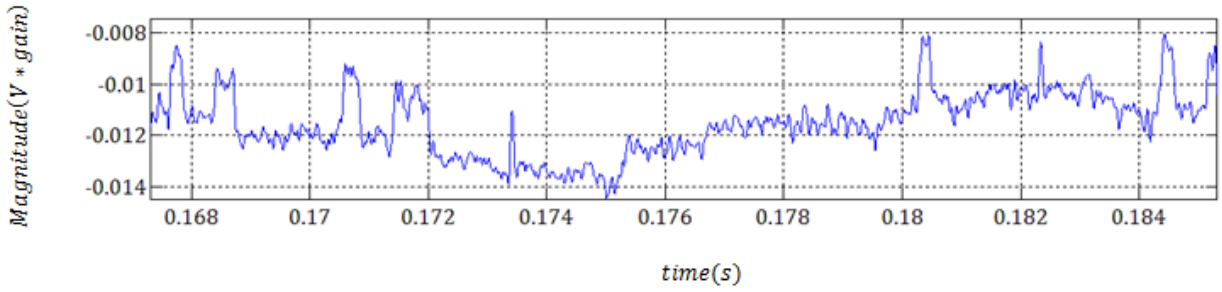
and

$$\tau = \left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)^{-1} \tag{4.7}$$

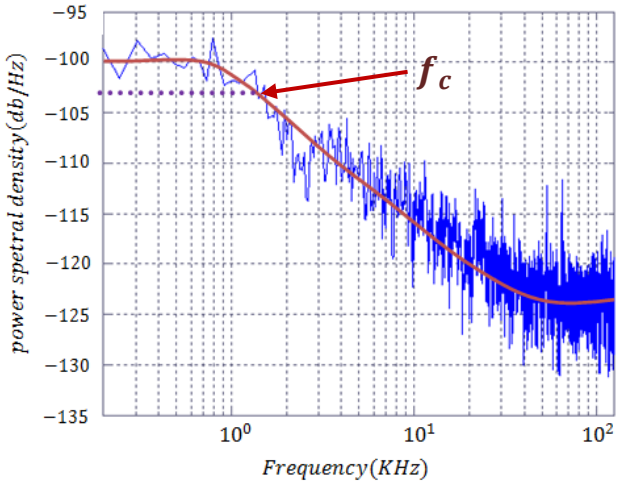
From equation (4.6), we note that the corner frequency can be calculated from the time domain data and the PSD rolls of as f^{-2} (20db/decade) above this frequency. Figure 4.6(a) shows an example of a time domain RTS noise obtained from our experiment. From this time domain data, the mean capture time, τ_c and mean emission time, τ_e have been calculated as 0.15ms and 2.99ms, respectively.

Therefore, the characteristic time constant, τ can be calculated from equation (4.7) and it is 0.143 ms. Thus, using equation 4.6 the calculated corner frequency would be $1.11kHz$.

The PSD of this time domain signal has been estimated using Welch's method in MATLAB. Figure 4.6(b) shows the estimated PSD, from which the corner frequency can be found as $\sim 1.3kHz$. Above $1.3kHz$, the PSD follows $\sim 15db$/decade roll-off. Table 4.2 shows the operating conditions of this measurement.



(a)



(b)

Figure 4.6: RTS noise in a) time domain and b) frequency domain.

Pixel Reset frequency	2Hz
Bias Voltage, V_{bias}	1.5V
Amplifier Gain	10
Temperature	26°C

Table 4.2: Operating Conditions

4.2.2 Amplitude of RTS Noise

The amplitude of the RTS noise can be obtained from the signal level histogram. The low frequency and broadband noise are modulated by the RTS fluctuations and thus produces different Gaussian distributions that are shifted by the different levels of RTS noise. As a result, for a two-level RTS noise, two Gaussian distributions are obtained. The peak of each distribution corresponds to the “high” and “low” levels of RTS noise. The RTS amplitude is calculated from

the difference between these two peaks.

From the filtered and smoothed signal, a small window of data has been chosen for producing the amplitude histogram. Figure 4.7 shows the signal-level histogram of RTS noise that was obtained in an operating condition described in Table 4.3. From the figure, we see two peaks of the Gaussian distributions that are $2.432\ mV$ apart. This result was obtained with an amplifier gain of 10. Therefore, the actual magnitude of RTS noise fluctuation is $0.24\ mV$. As shown in Table 4.1, the channel area (WL) of the source-follower (*SF*) is 1 μm × 180nm and the thickness of oxide , t_{ox} is 4 nm. Therefore, for an interface trap, the amplitude of RTS noise can be estimated as [66],

$$\Delta V \approx \frac{q}{WLC_{ox}} = \frac{q}{WL\frac{\varepsilon_{ox}}{t_{ox}}} = \frac{q}{WL\frac{\varepsilon_{rox}\,\varepsilon_0}{t_{ox}}} = 0.1mV. \tag{4.8}$$

Here, C_{ox} is the capacitance per unit area of the SiO_2 layer, ε_{ox} is the permittivity of SiO_2, ε_{rox} is the relative permittivity of $SiO_2 = 3.9$. Also, ε_0 is the permittivity in vacuum $= 8.854 \times 10^{-12} Fm^{-1}$ and q is the charge of an electron $= 1.6 \times 10^{-19} C$.

The RTS noise fluctuation is maximum for an interface trap which is calculated as $0.1\ mV$ in our case. But from the experiment, we have found a voltage fluctuation of $0.24\ mV$ which is considerably higher than the calculated maximum value.The anomaly in the RTS amplitude cannot be explained by the simple SRH process, according to which the fluctuation is caused due to trapping and de-trapping of electron by a single bulk defect. Different generation enhancement mechanism has been proposed by many authors [68], [69] to explain the origin of this large

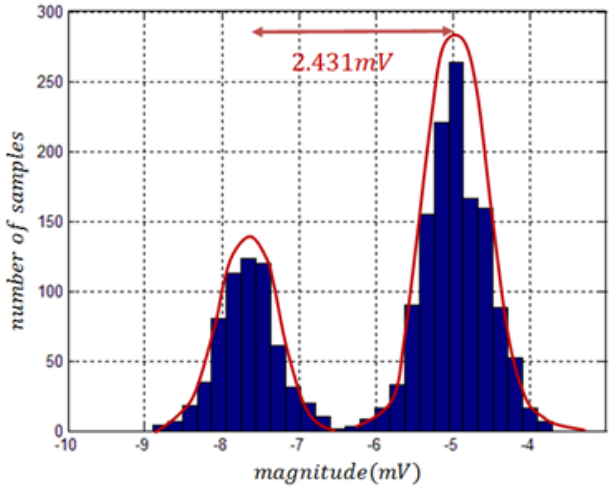


Figure 4.7: Signal-level histogram of RTS noise.

fluctuation in RTS.

Pixel Reset frequency	2Hz
Bias Voltage, V_{bias}	926.5 mV
Amplifier Gain	10
Temperature	35°C

Table 4.3: Operating Conditions

The RTS amplitude can be considered to be caused by the fluctuation of the capture cross section and the energy position of the bistable defects located at the Si-SiO_2 interface [69]. This sort of defects can either be formed by a two-state fast interface state or by an interacting pair of a fast interface state with a slow neighbouring border trap. The phonon-assisted tunneling current through the fast state gives rise to the larger amplitude in RTS that has been observed in some APSs.

4.2.3 Time Constants of RTS Noise

The time constants of RTS noise follow statistical distribution. For a two level RTS noise, considering the high-voltage level as state 1 and the low-voltage level as state 0 , the probability of RTS transition from state 1 to state 0 can be given by $1/\tau_{10}$ and the probability of RTS transition from state 0 to state 1 can be given by $1/\tau_{01}$.

Consider that $P_{11}(t)$ represents the probability that the RTS noise remains in state 1 and does not make a transition for time t. Then the probability of remaining in state 1 for a time span t and making a transition between t and $t + dt$ is given by,

$$P_1(t) = P_{11}(t)\left(\frac{1}{\tau_{10}}\right). \tag{4.9}$$

Now from the theory of probability,

$$P_{11}(t + dt) = P_{11}(t)\left(1 - \frac{dt}{\tau_{10}}\right). \tag{4.10}$$

where, $P_{11}(t + dt)$ is the probability that the RTS noise remains in state 1 and does not make any transition for a time period of $t + dt$. Equation (4.10) can be written as,

$$P_{11}(t + dt) - P_{11}(t) = -P_{11}(t)\left(\frac{dt}{\tau_{10}}\right), \tag{4.11}$$

$$\frac{dP_{11}}{dt} = -\frac{P_{11}(t)}{\tau_{10}}.$$

Solving equation (4.11) we get,

$$P_{11}(t) = exp\left(\frac{-t}{\tau_{10}}\right), \tag{4.12}$$

Substituting $P_{11}(t)$ in equation (4.9) we can find,

$$P_1(t) = \frac{1}{\tau_{10}} exp\left(-\frac{t}{\tau_{10}}\right). \tag{4.13}$$

Similarly for state 0 we can write,

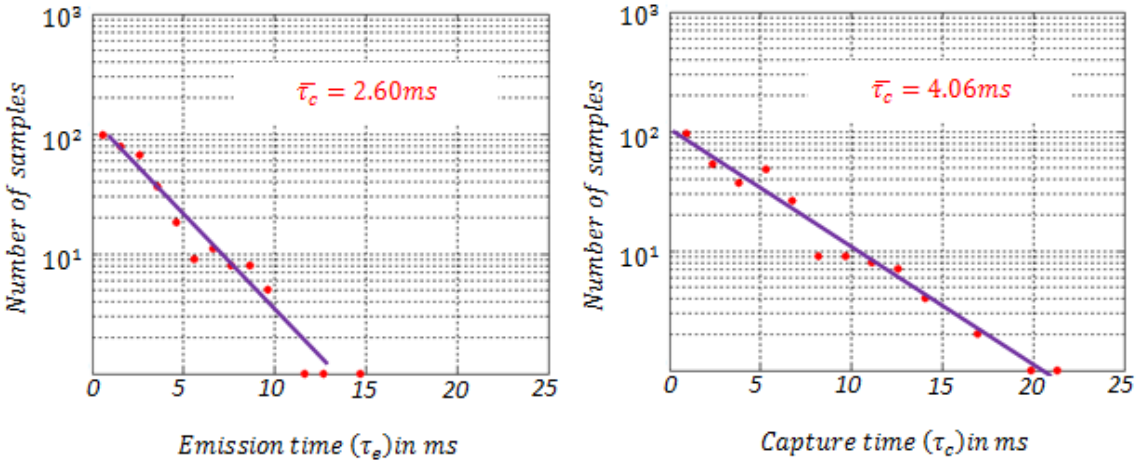
$$P_0(t) = \frac{1}{\tau_{01}} exp\left(-\frac{t}{\tau_{01}}\right). \tag{4.14}$$

Equations (4.13) and (4.14) follow exponential distribution, which is a Poisson process having a mean value τ_{10} and τ_{01}, respectively. Therefore, in RTS noise, the mean time spent in the high-voltage level, i.e. the average capture time, $\tau_c = \tau_{10}$, and the mean time spent in the low-voltage level, i.e. the average emission time, $\tau_e = \tau_{01}$. Therefore, equations (4.13) and (4.14) can now be re- written as,

$$P_{\tau c}(t) = \frac{1}{\tau_c} exp\left(-\frac{t}{\tau_c}\right). \tag{4.15}$$

$$P_{\tau e}(t) = \frac{1}{\tau_e} exp\left(-\frac{t}{\tau_e}\right). \tag{4.16}$$

where, $P_{\tau c}(t)$ and $P_{\tau e}(t)$ are the probability distribution of the higher-voltage level and lower-voltage level times, respectively.



(a) **(b)**

Figure 4.8: Measured a) emission time and b) capture time from an APS.

Figure 4.8 shows the statistical distribution of emission time and capture time of RTS noise that was measured at $25°C$ with a pixel bias voltage, (V_{bias}) 926.5 mV. It can be seen that,

both the emission time and capture time follows exponential distributions, which is in close agreement with the theory discussed above.

From the experiment, the calculated mean capture time (τ_c) and mean emission time (τ_e) are 4.06 ms and 2.60 ms, respectively. The calculated standard deviation (*SD*) for mean capture time (τ_c) and mean emission time (τ_e) are 4.02 ms and 2.56 ms, respectively. It can be seen that, the *SD* closely follows the mean values, which is an important characteristic of exponential distribution [70].

4.2.4 Effect of Bias voltage on RTS Parameters

Figure 4.9 shows the dependence of pixel bias voltage (V_{bias}) on RTS noise parameters measured in an APS at 26 °C The gain of the LNA was kept at 10. From the figure, it can be seen that the time in the higher-voltage state i.e. the capture time, decreases drastically as the V_{bias} increases. On the other hand, the time in the lower-voltage state i.e. the emission time increases very little.

When the V_{bias} is increased, the drain current (I_D) flowing through the *SF* also increases. The output resistance of a SF transistor can be given by,

$$R_{out} \approx \frac{1}{g_m} = \left(2\frac{W}{L}\mu_n C_{ox} I_D\right)^{-\frac{1}{2}}. \tag{4.17}$$

where, g_m is the transconductance of the SF transistor. From equation (4.17), we can see that the output resistance, R_{out} decreases as the drain current, I_D through the *SF* increases which in turn increases the V_{GS} of the *SF*.

The concentration of electrons (n) at the $Si - SiO_2$ interface of the *SF* is also raised due to the increase of V_{GS}. An increased concentration of electrons enhances the probability of trapping of an electron by a trap. Thus, the capture time (τ_c) increases. It can also be seen from equations (3.100) and (3.110) that, the capture time (τ_c) is inversely proportional to the concentration of electrons (n) at the interface. This further explains the decrease of the capture time with the increase of V_{bias}.

As discussed earlier, the energy E_{trap} of a trap that resides near the interface of a MOS device exhibits very little dependence on the gate to source potential, V_{GS} (equation (3.103)). For the traps residing deeper in the SiO_2 layer, according to equation (3.103), E_{trap} tends to decrease with the increase of V_{GS}. Therefore, from equation (3.102), it can be said that the emission time,

τ_e varies very little for an interface trap, but exhibits significant increment with the concentration of electrons (n) for the traps located in the oxide layer.

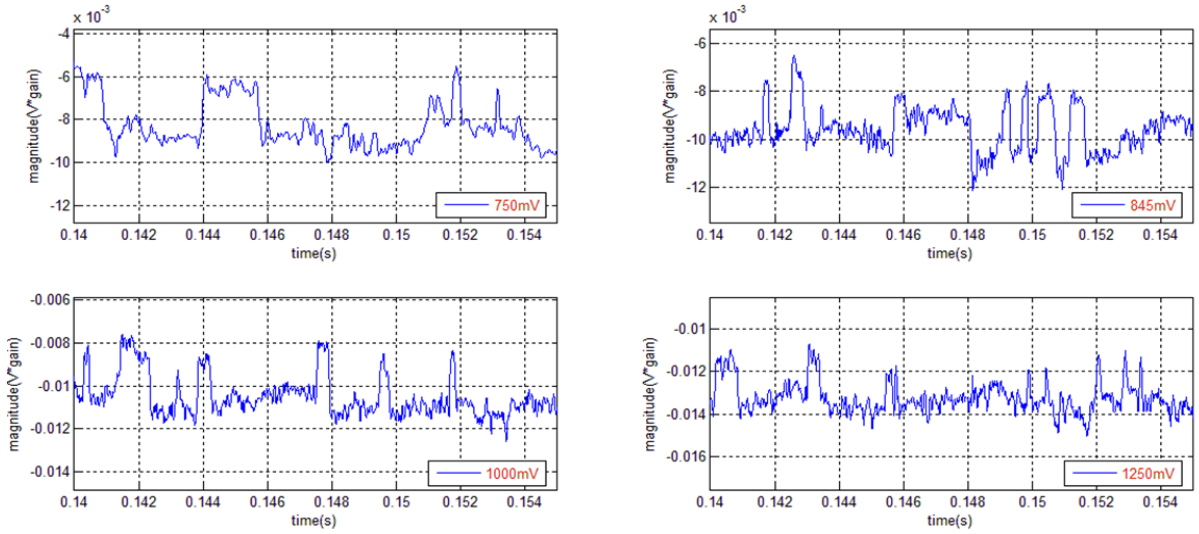


Figure 4.9: RTS noise measured from an APS at different V_{bias} .

The average capture time and average emission time measured from an APS at different V_{bias} has been plotted in figure 4.10. It can be seen that, both the time constants are equal when V_{bias} is near to $700mV$, which indicates according to equation (3.102) that the trap energy coincides with the Fermi level at this voltage for this particular trap.

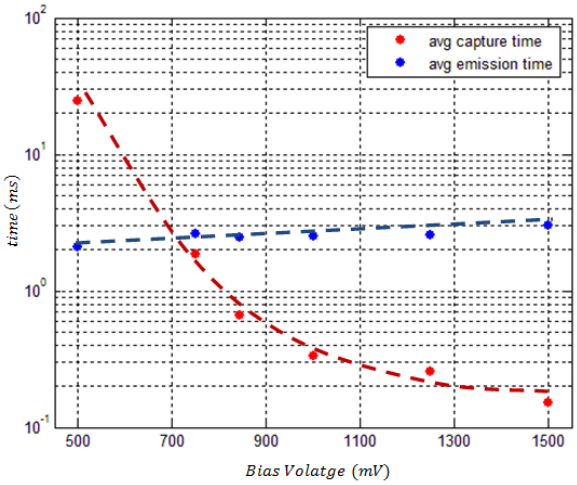


Figure 4.10: Measured RTS time constants as a function of V_{bias}.

From equations (3.102) and (3.103), we get [see Appendix A],

$$\frac{d}{dV_{bias}}\left[ln\left(\frac{\tau_c}{\tau_e}\right)\right] \approx -\frac{q}{kT}\frac{d}{t_{ox}}. \tag{4.18}$$

Integrating equation (4.18), we find,

$$ln\left(\frac{\tau_c}{\tau_e}\right) = -\left[\frac{q}{kT}\frac{d}{t_{ox}}\right]V_{bias} + const. \tag{4.19}$$

Equation (4.19) is the equation of a straight line, where the slope is $\frac{q}{kT}\frac{d}{t_{ox}}$. From the slope, the location of the trap (d) can be calculated. Figure 4.11 shows the plot of $ln\left(\frac{\tau_c}{\tau_e}\right)$ against the bias voltage, V_{bias}. kT/q is the thermal voltage, which is ~26mV at 26°C and the thickness of oxide t_{ox} is 4nm. From the slope of the plot the trap location is calculated as ~0.56nm, which is very close to the interface and thus satisfy the explanation that has been given earlier for the slow varying emission time with V_{bias} in figure 4.10.

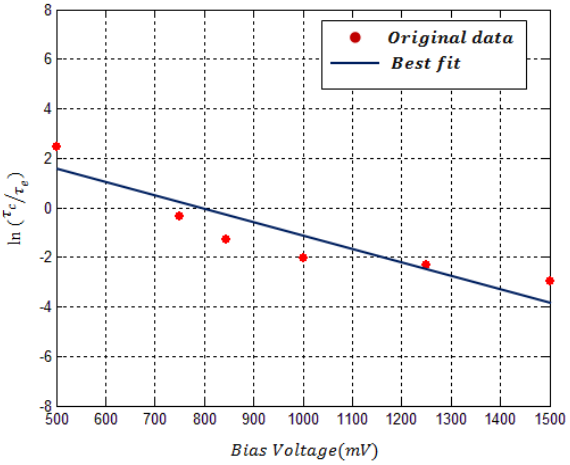


Figure 4.11: $ln\left(\frac{\tau_c}{\tau_e}\right)$ Vs. V_{bias} plot

4.2.5 Effect of Temperature on RTS Parameters

As discussed earlier, the capture cross section, σ_n can be considered as a thermally activated process and can be given by

$$\sigma_n = \sigma_{n0} exp\left(-\frac{\Delta E_a}{kT}\right). \tag{4.20}$$

And the average capture time is given by,

$$\tau_c = \frac{exp\left(-\frac{\Delta E_a}{kT}\right)}{v_t \sigma_{n0} n}. \tag{4.21}$$

The temperature dependence of RTS noise time constants can be explained completely by these two equations. Figure 4.12 exhibits the RTS noise observed from an APS at different

temperature. The extracted time constants have been plotted in figure 4.13. From figures 4.12

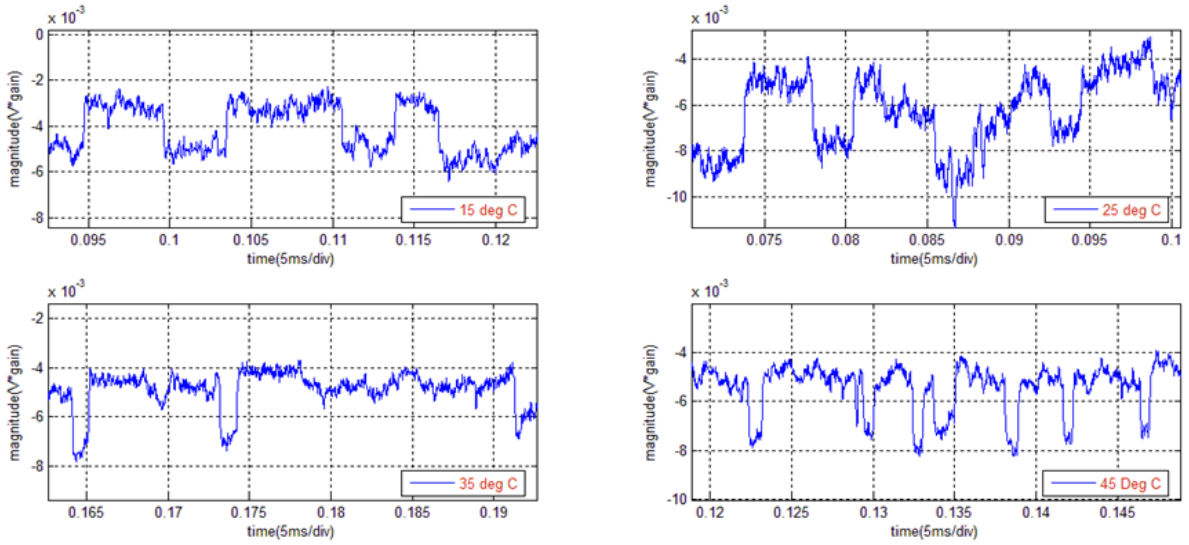


Figure 4.12: RTS noise measured from an APS at different temperatures .

and 4.13, it can be seen that both the emission time and capture time follows an exponential reduction as the temperature increases.

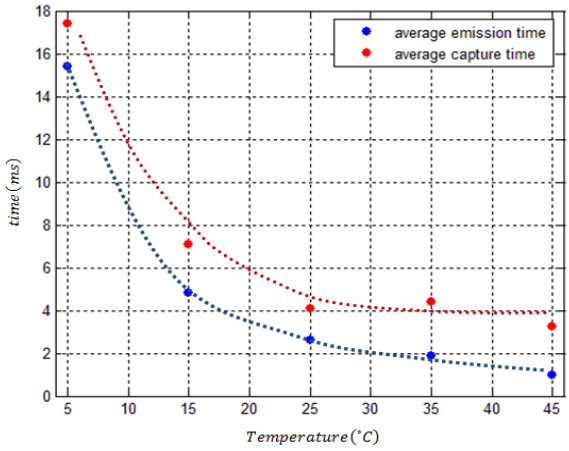


Figure 4.13: Plot of extracted time constants at different operating temperatures.

The temperature dependence of RTS time constants can be explained using a non-radiative type multi-phonon emission process [71], [72]. According to multi-phonon emission theory, an empty defect center is thermally agitated and vibrates around its equilibrium position. The lattice vibration increases with temperature. When the defect center resides near the conduction band, there is a probability that the equilibrium position can cross the conduction band and capture an electron. After the capturing process, the equilibrium position is shifted to a

new coordinate within the energy gap, by releasing excess energy through multi-phonon process. The equilibrium position can shift back and forth very frequently at higher temperatures, which makes the time constants smaller.

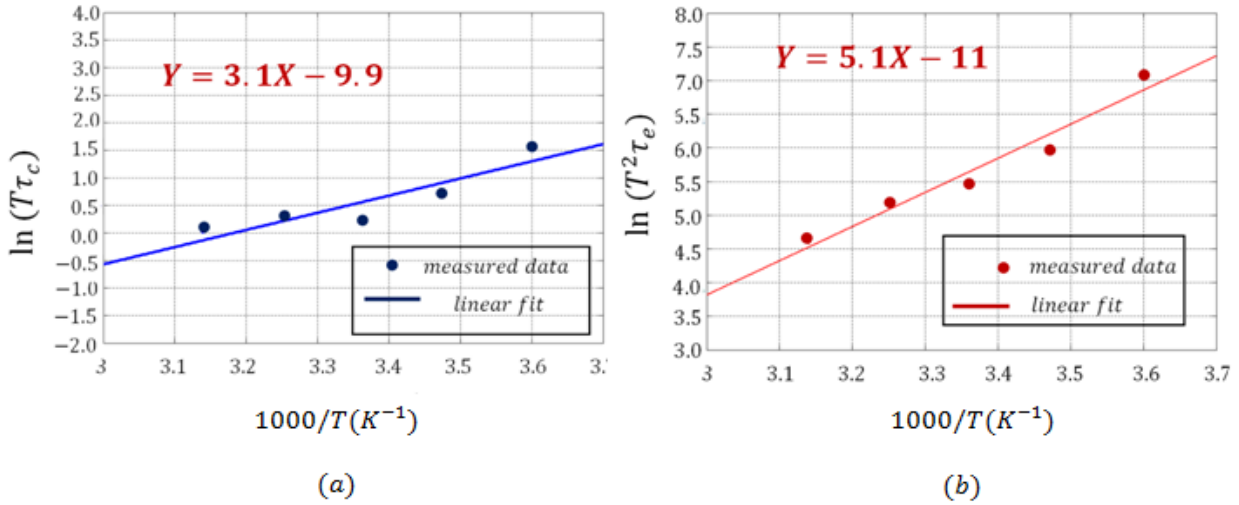


Figure 4.14: Temperature dependence of (a) mean capture time and (b) mean emission time.

In order to calculate the thermal activation energy (E_a), the equations of time constants can be re-arranged as,

$$ln(\tau_c T) \equiv ln(P) + \frac{\Delta E_a}{k}\frac{1}{T}. \quad (4.22)$$

$$ln(\tau_e T^2) \equiv ln(Q) + \frac{\Delta E_a + \Delta E_{CT}}{k}\frac{1}{T}. \quad (4.23)$$

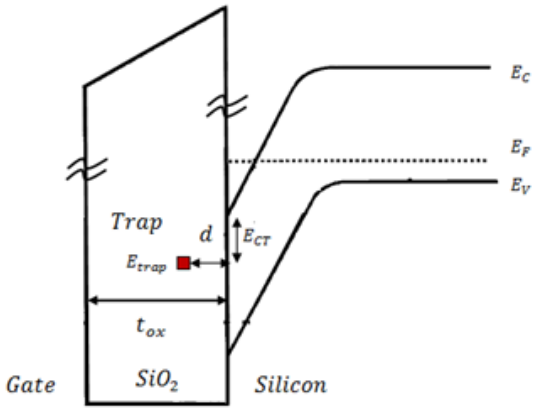


Figure 4.15: Energy band diagram for the trap.

where, P and Q are constants and $E_{CT} = E_C - E_T$ is the energy difference between the conduction band and the trap energy levels. The detailed calculation has been shown in

Appendix B. Figure 4.14 is used to calculate the E_a and E_{CT} which are $0.27eV$ and $0.17eV$,respectively. The calculated capture cross section is $\sim 9.07 \times 10^{-18} cm^2$, which falls within the range of the typical values of capture cross section ($\sim 10^{-14} cm^2 - \sim 10^{-19} cm^2$) [73]. Figure 4.15 demonstrates the corresponding energy band diagram of the source follower MOSFET of this particular APS.

4.3 Summary

In this chapter, we discussed our experimental results on RTS noise in CMOS image sensors. An estimate about the magnitudes of RTS fluctuations was obtained. Such estimates often vary from the measured values due to the possible involvement of different generation mechanisms [68], [68, 69]. The mean time constants, which are the most important characteristics of RTS noise, are measured at different pixel bias voltages and at different temperatures. Three samples of RTS pixels are used for measuring the bias dependence of the time constants and two samples of RTS pixels are used for temperature dependent measurements.

The emission time and the capture time of the RTS noise are found to follow a statistical distribution. The standard deviation of the emission time and the capture time closely matches with their respective mean values, which confirms the distribution as a Poisson process [70]. From the bias-dependent experiments, it was found that the mean capture time (τ_c) decreases very rapidly with increased pixel bias. On the other hand, the mean emission time (τ_e) increases slowly. From this dependency on the pixel bias voltage of the time constants, the trap depth has been calculated.

The temperature dependence of the time constants has also been measured. Both time constants are found to decrease drastically with temperature, which is due to the increased phonon vibration at higher temperatures. Three very important trap parameters - trap activation energy (E_a), energy difference between the conduction band and the trap energy level (E_{CT}) and the capture cross section (σ_{n0}), have been calculated from these measurements.

As mentioned earlier, RTS noise has a significant impact on the imaging performance at low light levels, giving rise to unexpected bright flickering pixels. Therefore, reduction of RTS fluctuations may lead to better image quality, especially under low light illumination levels. Since RTS noise originates from the defects in the oxide layer, a complete remedy from RTS

noise is not possible unless an expensive, customized fabrication process is adopted [74], [75]. The usefulness of pulsed biasing technique in CMOS image sensor is still ambiguous [76], [77]. So, it is perhaps preferable to control the operating conditions of CIS in order to optimize the impact of RTS noise. The experiments about the RTS noise that we have carried out on CMOS image sensor thus provide very valuable information about the characteristics of this particular noise. From the experiments, we saw that the rate of RTS fluctuation decreases significantly at lower pixel biases and lower operating temperatures. These results provide insights about the possible operating conditions of the CIS for better imaging performance.

Chapter 5

Low-cost, High-speed Imaging System for Biological Microscopy

Imaging system designers are now increasingly using CMOS image sensors (CIS) because they offer many advantages compared to charge coupled device (CCD). These advantages include lower power requirement, capability of integrating various on-chip functionality, constantly decreasing size and lower cost. Further, the on-chip analog to digital (ADC) converter in CIS provides digitized output which can be fed directly to digital systems such as microcontrollers or FPGAs for further processing.

A field-programmable gate array provides much flexibility compared to microcontroller for digital systems implementation. The main advantage of a FPGA is its reprogramming capability and low cost. Besides this, in a real-time image acquisition system, a large volume of image data is generated and transmitted by the CIS. Therefore, in order to process this large volume of data in real-time, a very high performance hardware having parallel processing capability is a necessity. An FPGA is a good choice for such applications.

The objective of this part of our work is to develop a low-cost, high frame rate imaging system for biological microscopy. The real-time image data is transferred to the FPGA which then further processes the data to display as live video on a VGA monitor. In our work, we have used LUPA 300 as the CIS and Altera DE2-70 development board which contains Altera Cyclone II FPGA .

5.1 Structure of the System

Figure 5.1 shows the structure of the implemented system. The image sensor converts the optical signal into an electrical signal. The analog signal is digitized by an on-chip ADC. The FPGA controls the operating conditions of the image sensor through a 3-wire serial-to-parallel (SPI)

interface and senses the digital output from the image sensor by the general purpose input-output (GPIO) port. A synchronous dynamic random-access memory (SDRAM) is used as the temporary storage medium of the image data. This data is then sent to the video graphics array (VGA) monitor for displaying the image. All the necessary control signals required for the SDRAM and VGA display are generated by the FPGA. In this section, we shall briefly discuss different building blocks of the imaging system.

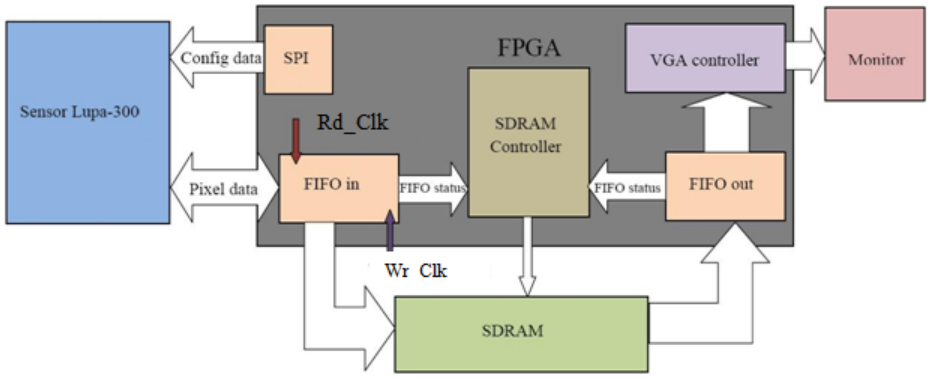


Figure 5.1: Block diagram of the FPGA based imaging system.

5.1.1 Image Sensor

The image sensor is the key component of any imaging system .The objective of this work is to develop a low-cost, high frame rate imaging system, which requires a high speed image sensor. For our system, we chose the LUPA-300 which can provide a frame rate of 250 frames per second (fps) at full resolution (640 × 480) with a master clock of 80MHz. The specification of LUPA-300 has given in Table 5.1.

Pixel architecture	6 transistor pixel
pixel area	9.9 μm × 9.9 μm
Number of Pixels	640 × 480
ADC resolution	10 bit
Maximum clock rate	80MHz
Frame rate	250 fps

Table 5.1: Specification of LUPA-300 image sensor

Figure 5.2 (a) shows the picture of the image sensor and its pixel architecture. Each pixel of LUPA-300 consists of one photodiode and six transistors (figure 5.2(b)). This 6-T architecture offers the global synchronous shutter feature. All the pixels are reset simultaneously and the pixel values are sampled on its V_{mem} capacitor after a common integration period, which is then followed by a sequential readout from the storage capacitor, V_{mem} . The readout speed and thus the frame rate (FR) depends on the master clock period (CP), the frame overhead time (FOT) and the row overhead time (ROT). The speed can also be increased by sub-sampling or windowing but at the cost of reduced resolution and field-of-view, respectively. The frame period (FP) can be calculated by the equation,

$$FP = FOT + n_r \times (ROT + np_r \times CP). \quad (5.1)$$

where n_r is the number of row , and np_r is the number of pixels in a row. In our work, we chose a 50 MHz clock which gives a *CP* of 20ns.

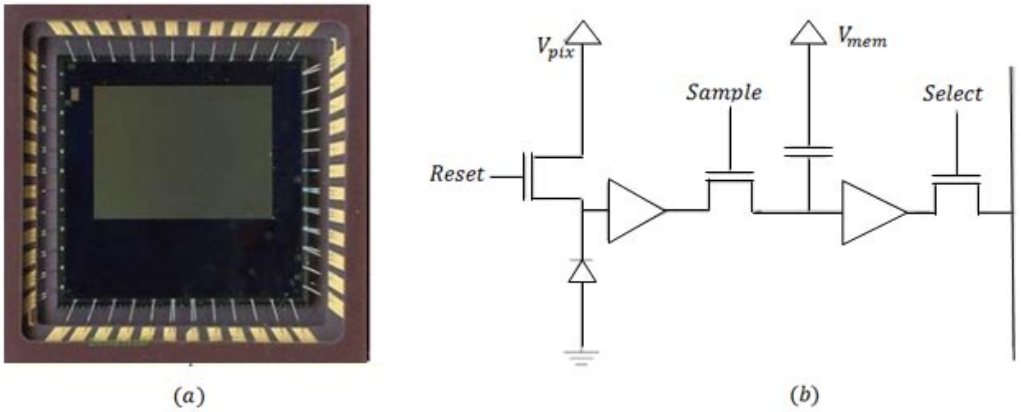


Figure 5.2: Lupa-300: a) the image sensor and b) 6-T pixel architecture [78].

According to the datasheet, for a 50MHz clock, the FOT and ROT are 624 and 32 clock periods, respectively. Therefore, the frame rate at full resolution with 50 MHz pixel rate would be,

$$FR = FP^{-1} = [624 \times 20 + 480(32 \times 20 + 640 \times 20)]^{-1} = \frac{1}{6.46ms} = 154.7fps.$$

Read out of the n^{th} frame and the integration of the $(n+1)^{th}$ frame occur simultaneously. The readout of a frame begins with FOT. During the FOT, the charge generated on the photodiode is transferred to the pixel storage "capacitor", V_{mem} .The sensor is then read out row by row. The readout begins with ROT, which is the time required to transfer the pixel value on

the column lines. Here, 4 pixels can be read out simultaneously. The on-chip sequencer generates the necessary internal timing based on the internal register settings. Figure 5.3 shows the timing diagram during global read out.

The dynamic range (*DR*) of the sensor can be extended using multiple slope configurations. The LUPA -300 has dual slope and triple slope exposure capability which can be chosen by selecting $Res2\_timer$ or $Res3\_timer$ registers. In the dual slope mode, a normal exposure is performed first and a second reset is given at a certain time within the integration period, which resets those pixels to a new reset level that have already reached to saturation before the integration period is over. In the triple slope mode, a third reset pulse is given within the integration period.

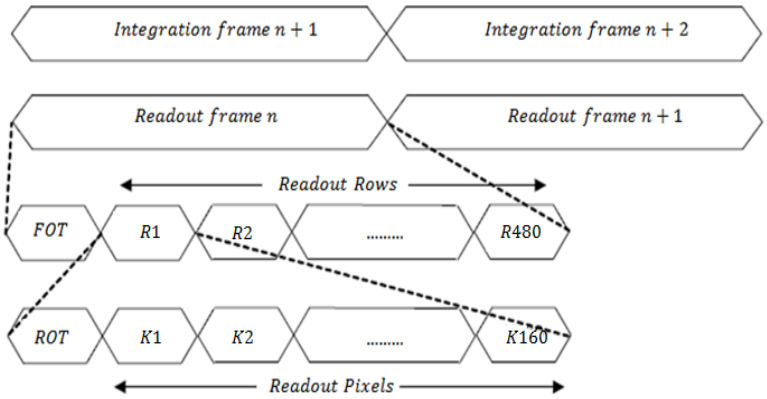


Figure 5.3: Parallel integration and readout timing.

The configuration settings and the behavior of the LUPA-300 is defined by setting the internal registers. The image sensor has 16 internal registers which can be selected by a 4 bit address. The 4 address bits and the 12 controlling data bits are sent over a 3 wire SPI interface.

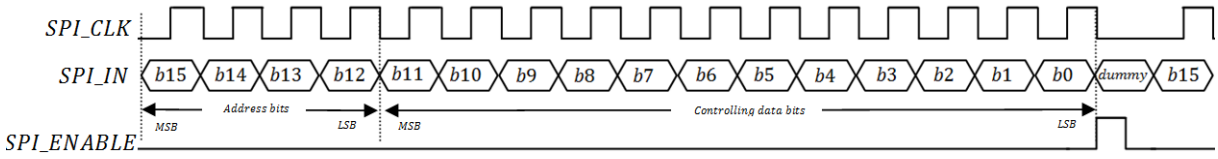


Figure 5.4: Timing diagram for SPI interface.

The SPI_in pin on the image sensor receives 16 bit serial data, which is shifted in a shift register buffer. When the SPI_ENABLE becomes high, the data stored in the shift register buffer is

uploaded on one of the 16 internal registers depending on the address bits. The maximum clock frequency for the SPI interface is 20 MHz. Figure 5.4 shows the timing diagram for the SPI interface.

The image sensor needs two levels of power sources, 2.5V for the digital blocks (V_{DDD}) and 3.3V for the analog blocks, (V_{DDA}). The V_{DDD} should rise before or together with other power supplies. During the rise of V_{DDD}, the SPI registers are reset to the default values. The SPI settings can be uploaded after the V_{DDD} becomes stable. The $RESET\_N$ should be kept low until all the SPI settings are uploaded. Further details about the operation of LUPA-300 can be obtained from the data sheet [78].

5.1.2 Field Programmable Gate Array (FPGA)

All the controlling, processing and interfacing required for the imaging system is implemented using Altera DE2-70 development board (see figure 5.5 on the next page). The board contains Altera Cyclone II 2C70 FPGA chip, which can be programmed to generate all the necessary signals for controlling the image sensor, SDRAM, VGA display. It can aso be used to process the image data coming from the image sensor.

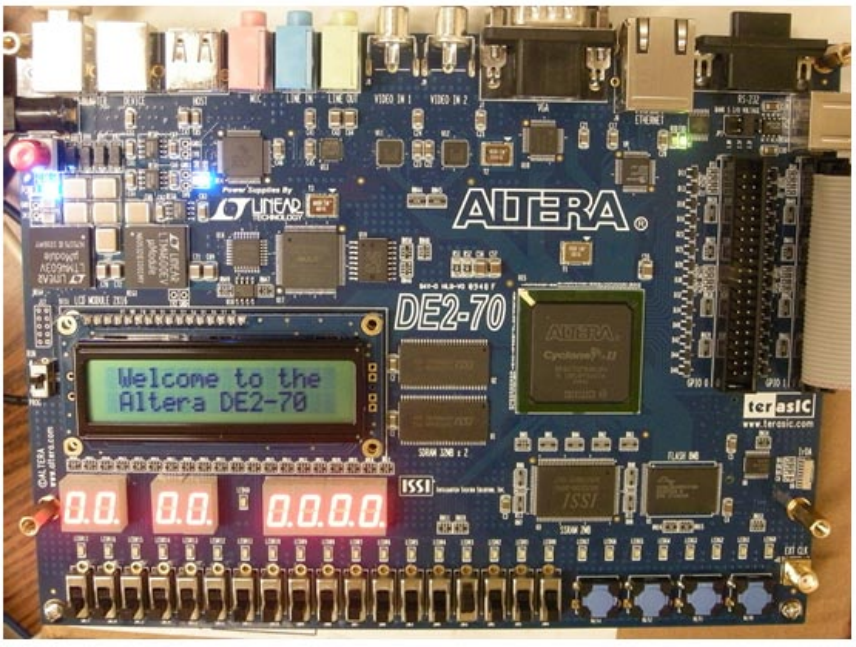


Figure 5.5: ALTERA DE2-70 FPGA board.

The Altera DE2-70 board comes with different hardware components. Proper FPGA pin mapping and controlling modules are necessary to bring the hardware into operation. We have

used the following on-board hardware in our work:

- Altera Cyclone® II 2C70 FPGA device
- One 32-MByte SDRAM as a temporary storage of image data
- 50-MHz and 28.63-MHz oscillator for clocking the image sensor, SDRAM and VGA port
- 10-bit high-speed triple VGA DACs with VGA-out connector
- One 40- pin expansion header that contains I/O pins

The FPGA chip is programmed in JTAG programming mode using the on-board USB blaster. In this section, we will briefly discuss the controlling modules that is implemented on the FPGA using Verilog HDL [79] . Figure 5.5 is the picture of the FPGA board that was used in this project.

SPI Controller

As mentioned earlier, the image sensor uses a 3-wire serial-to-parallel interface (SPI) to communicate with the controlling device. Various operation and control parameters of the image sensor, such as pixel selection, gain, offset, reset time, integration period can be set using the SPI settings stated in the datasheet. The maximum allowable clock for the SPI registers is 20 MHz.

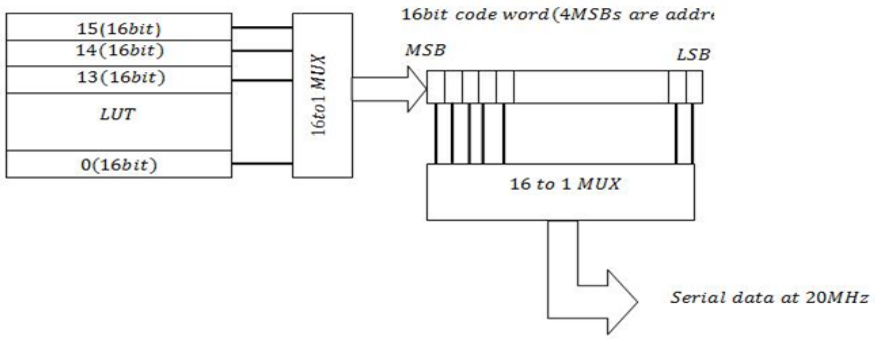


Figure 5.6: Block diagram of the implemented SPI interface.

Also, as discussed earlier, the LUPA-300 has 16 internal registers which obtain their information from a 16 bit shift register buffer. The first 4 MSBs (b15-b12) contain the register address and the rest of the bits (b11-b0) contain the setting for that particular register. The LUPA -300 sensor receives the SPI bits serially, but it does not send any acknowledgement. Therefore, the SPI communication is a one-way. The FPGA acts as the master and the sensor serves as a

slave.

A simple SPI interface has been designed using Verilog and implemented on the FPGA. A lookup table (LUT) of 16 indexes was created in which each index contains a 16 bit code word representing the information required by an internal register. Figure 5.6 shows the block diagram of the implemented SPI interface. As LUT index increases by one, the 16 bit LUT data of that index is transferred to a 16 bit buffer register thorough a 16×1 MUX. The 16 bit data is sent

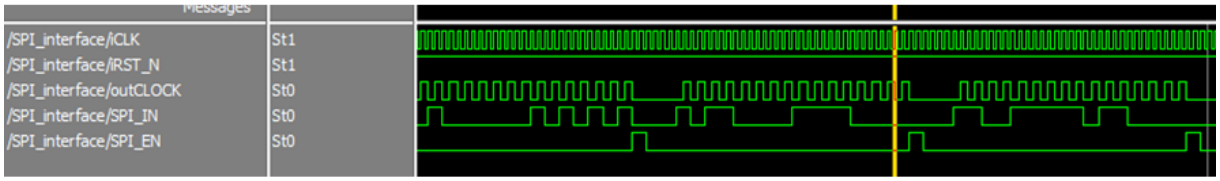


Figure 5.7: Generated signals by the SPI controller. Clock frequency is 20 MHz.

serially with the MSB first over the *SPI_IN* wire by a 16×1 MUX at a clock rate of 20MHz. After sending a complete 16 bit code word to the shift register buffer of the image sensor, a pulse is given on the *SPI_EN* wire, following which the information stored in the register buffer is uploaded on a certain internal register. Figure 5.7 shows the timing generated by the SPI interface module. The Verilog source code of SPI controller has been given in Appendix C.

VGA Controller

A video graphics array (VGA) interface is a display system of computer, which was developed by IBM primarily for cathode ray tube (CRT) monitors. It has become a standard display system for computers and currently all the computer display monitors such as the liquid-crystal displays (LCDs) are compatible to this interface system. A standard VGA monitor consists of an array of at least 640×480 pixels. For a colour display system, each pixel can display three primary colours, red, and green and blue (RGB) simultaneously. The intensity of the colours depends on the incoming RGB data signals.

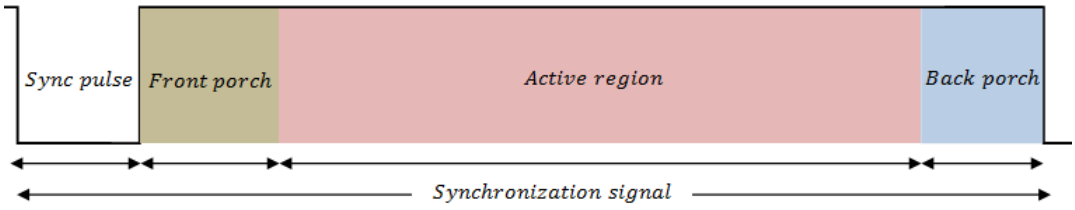


Figure 5.8: Timing of VGA synchronization pulse (not scaled)

The VGA interface carries synchronization or control signals (V_sync and H_sync) which refresh the pixels at a certain time interval. Figure 5.8 shows the waveform of the two synchronization signals. The horizontal synchronization signal, H_{sync} can be classified into four regions: active region (H_sync_act), front porch (H_sync_front), synchronization pulse (H_sync_cyc) and back porch (H_sync_back). The vertical synchronous signal, V_sync is also classified in a similar fashion.

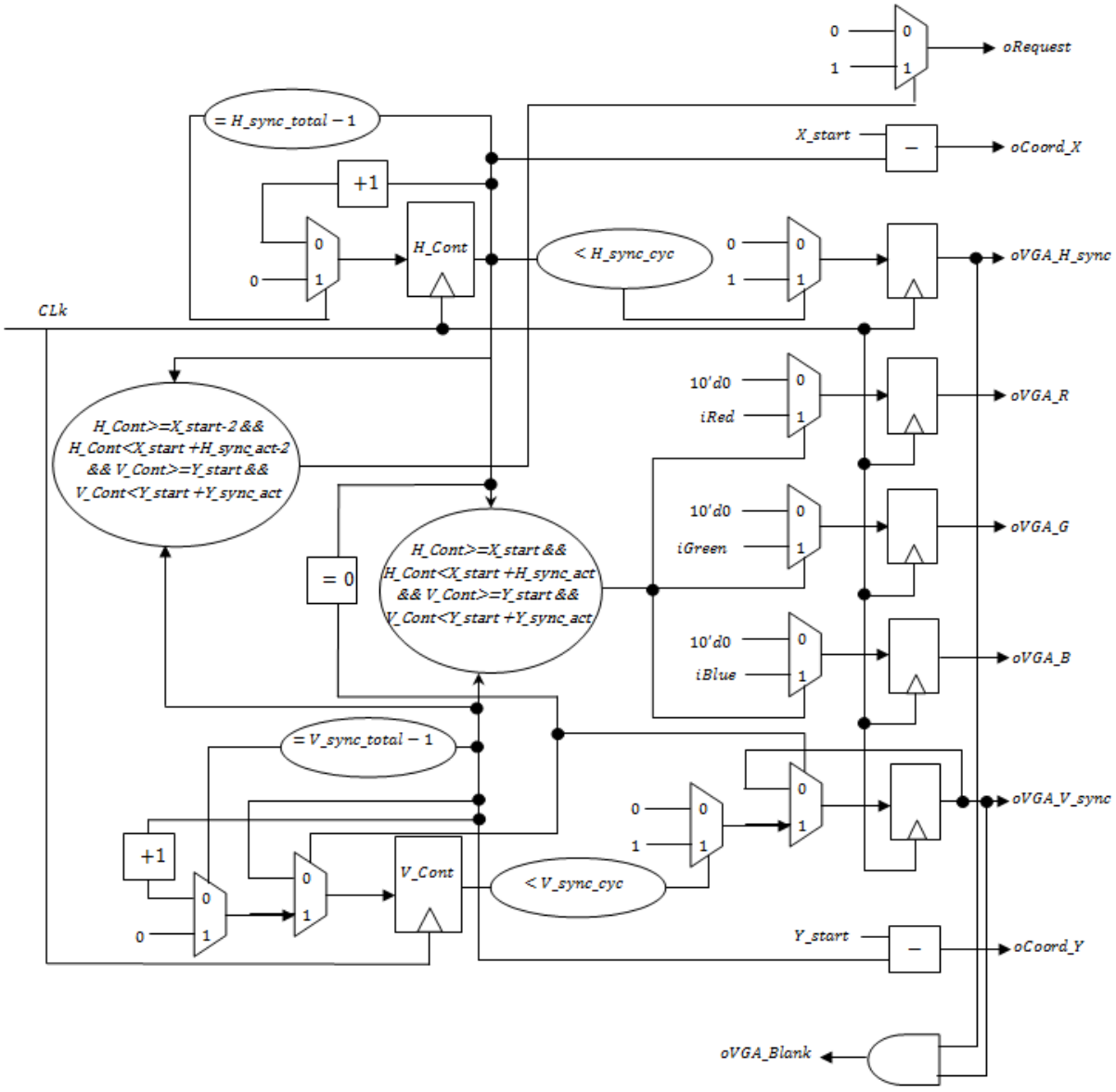


Figure 5.9: Implementation of VGA controller [79].

Valid RGB information is carried by the interface during the active periods only (H_syn_act and

H_sync_act).The remaining time span in the V_sync and H_sync signals are known as vertical blanking period and horizontal blanking period, respectively. No information is displayed on the monitor during these blanking periods.

The pixels are refreshed one by one. When the monitor receives the active low horizontal synchronization pulse (H_sync_cyc), it starts refreshing the pixels in the next row. The process continues until it receives the vertical synchronization (V_sync_cyc) pulse (active low) after refreshing all the pixels in the bottom (480^{th}) row. When the interface receives the V_sync_cyc pulse, the monitor begins the refreshing process again from the first pixel in the first row. Thus, the interface generates one complete H_sync signal for each row and one complete V_sync signal for each frame. When the frames are refreshed at a rate of 60 frames per second, it creates a perception of motion in the human eye.

Table 5.2 presents the industry standard timing of a 640×480 VGA display. The reference clock frequency should be 25MHz in order to achieve a 640×480 resolution.

H_sync			***V_sync***		
Parameter	**Clocks**	**Time(µs)**	**Parameter**	**Lines**	**Time(ms)**
H_sync	800	31.78	V_sync	525	16.683
H_sync_act	640	25.42	V_sync_act	480	15.25
H_sync_front	16	0.636	V_sync_front	10	0.32
H_sync_back	48	1.907	V_sync_back	33	1.049
H_sync_cyc	96	3.81	V_sync_cyc	2	0.064
Frame refresh rate			60Hz		
Reference clock			25MHz		

Table 5.2: Standard timing of VGA signal.

Figure 5.8 shows the flowchart of the implemented VGA controller [79]. The core part of the controller consists of two modulo counters, H_cont and V_cont. Both counters reset themselves when they reach $H\_sync\_total - 1$(779) and $V\_sync\_total - 1$ (524), respectively. Two flip-flops, $oVGA\_H\_sync$ and $oVGA\_V\_sync$ provide horizontal and vertical synchronization pulse, respectively to the VGA port. Since, the synchronization pulses are active

low, these two flip-flops remain at zero until the two modulo counters are less than H_sync and V_sync, respectively. The starting coordinates of the display is provided by the $oCoord\_X$ and $oCoord\_Y$, which generate a request signal, $oRequest$ to the SDRAM for sending the image data. This request signal also drives the input RGB signals ($iRed, iGreen, iBlue$) to buffer them in the registers so that they can be synchronized with $oVGA\_H\_sync$ and $oVGA\_V\_sync$. The input RGB signals are discarded during the blanking periods.

The 25MHz control clock for the VGA interface is generated by the phase-locked loop (PLL). The input of the PLL is a 50 MHz on-board clock. Since we have used the monochrome version of LUPA-300 as the imaging device which gives 10bit grayscale output, then all the input RGB signals are fed by the same image data.

5.2 Optics of the Microscope

A conventional optical microscope consists of several parts including – illumination source, objective lens, tube, eyepiece etc. The illumination source (or illuminator) consists of a light source, a reflector and a condenser lens in order to maximize the light collection. A diaphragm is often used to control the amount of light and the extent of the illuminated area that is incident on the specimen. The objective lens collects light from the specimen and forms a real image inside

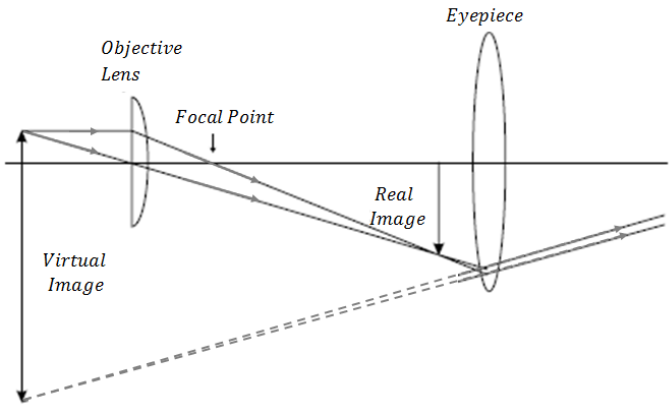


Figure 5.10: Optical path diagram of a microscope system.

the microscope tube. The objective lens also determines the magnification and the resolution of the obtained image. In order to view the real image, the tube length between the objective and the eyepiece is adjusted in such a way that the image plane can be set at the focus of the eye. The eyepiece can provide further magnification of the image. Figure 5.10 shows the optical path diagram of a microscope system.

In a digital microscope, the eyepiece is replaced by a digital image sensor – the LUPA-300 in our system. The sensor, placed at the intermediate image focal plane of the objective lens allows for a real image formed by the objective lens to be on the surface of the image sensor. The sensor responds accordingly and delivers a digital output, which is then processed electronically (e.g. by a microcontroller or FPGA) for display. Figure 5.11 shows the block diagram of the digital microscope. In this section, we discuss some key parameters of our digital microscope system.

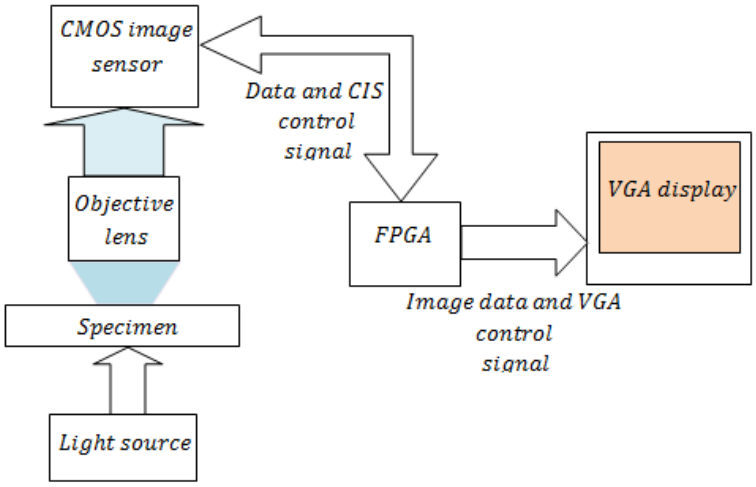


Figure 5.11: Block diagram of the digital microscope.

Focal Length of the Objective Lens, (f)

Focal length (f) is the fundamental property of a lens. It is the length between the center of the lens and the point whether a group of parallel rays converges (convex lens) or appears to be diverged from (concave lens). Figure 5.12 shows the focal point and focal length pictorially. In other words, the focal length gives the measure of lens' ability to converge or diverge the light.

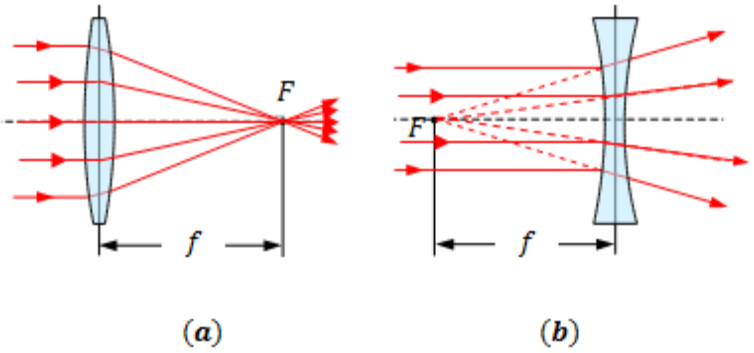


Figure 5.12: Focal point, (F) and focal length, (f) of (a) convex lens (b) concave lens.

The optical power (P) of a lens can be given by,

$$P = \frac{1}{f}. \tag{5.2}$$

From equation (5.2), it can be seen that the optical power of a lens is inversely related to its focal length. Thus, a high power lens has shorter focal length. Figure 5.13 shows the comparison between a shorter focal length and a longer focal length lens through the ray diagram.

In order to form an image at a particular plane, the specimen should be kept closer to the objective lens compared to its low power counterparts. Lens with shorter focal length also gives higher magnification (M) compared to longer focal length lenses, while the image is formed on the same plane.

The focal length is calculated from,

$$\frac{1}{f} = \frac{1}{U} + \frac{1}{V}. \tag{5.3}$$

where, U is the distance from the specimen to the center of the lens and V is the distance between the image and the center of the lens. The linear magnification is given by,

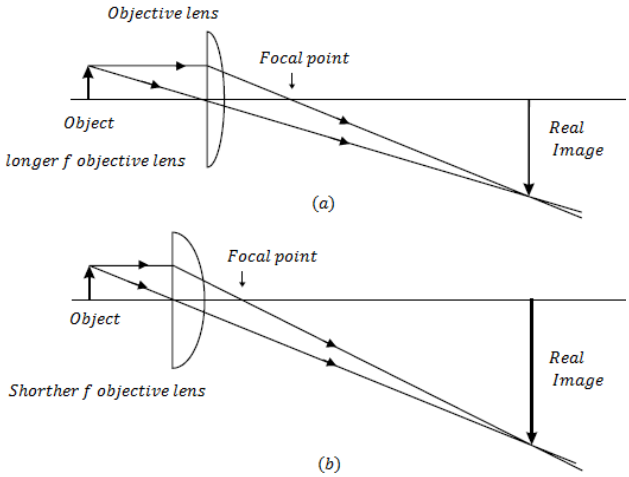


Figure 5.13: Comparison between a (a) shorter focal length and (b) longer focal length lens. The specimen is closer to the lens in (b) and the image is greatly magnified, while the image plane is same.

$$M = -\frac{V}{U} = \frac{f}{f-U}. \tag{5.4}$$

Here, the negative sign means that the image is inverted.

Images formed by simple lenses are subject to distortion or aberration that evolves from the physical limitations of single lens. The spherical surface of a lens is responsible for *spherical*

aberration which does not allow the parallel rays to converge at exactly the same point. When parallel rays coming from an object are not aligned with the optical axis, they are focused at different points on the image plane and causes an aberration called *coma*. The variation in velocity of different light in a material of certain refractive index (n) causes *chromatic aberration*. Properly designed compound lenses can alleviate these problems.

Numerical Aperture, (NA)

The numerical aperture (NA) of an objective lens is a measure of its light-gathering capability (see figure 5.14). Lens of higher NA can gather more light compared to the lower NA lenses. NA of an objective lens can be given by

$$NA = nSin\theta = \frac{nD}{2f}. \tag{5.5}$$

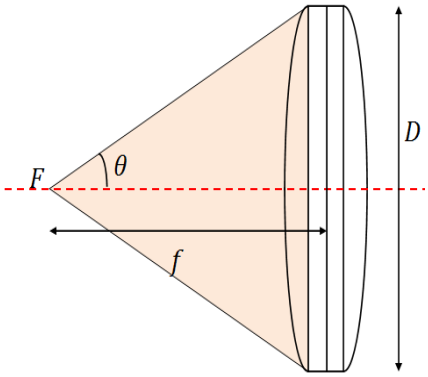


Figure 5.14: Cone of light entering into an objective lens originating from the focal point.

In equation (5.5), n is the refractive index of the medium where the lens is working and θ is one half of the angle of the maximum cone of light that a lens can gather. From equation (5.5), it can be seen that NA increases with n which can vary from 1.0 (air) to maximum 1.515 (most immersion oils) depending on the medium used between the lens and the specimen. The maximum size of the emanated light cone from the specimen that an objective lens can gather; also depends on its focal length (f). As the focal length of the objective lens decreases, the volume of the light cone that a lens can capture increases, resulting in a proportionate increase in numerical aperture. Figure 5.15 shows the picture different objective lenses. The numerical aperture is always less than the refractive index of the medium since, the maximum value of

Figure 5.15: Different microscope obejective lens, from left to right 4x/0.10, 10x/0.25, 50x/0.50.

$sin\theta$ is 1. As a result, for an objective operating in air ($n = 1$) the numerical aperture will always be less than 1. If the NA is higher than 1 it would be immersion objective ($n > 1$).

Optical Resolution, (r_{opt})

Magnifying the image of an object is not much helpful if the details within it cannot be resolved. This type of magnification is often termed "empty magnification". Resolution can be defined as the capability of a lens to retrieve the detail from the specimen. In other words, resolution is a measure of how well adjacent point sources can be identified. For example, two points shown in figure 5.16(a) are distinguishable since their intensities are non-overlapping.

The optical resolution (r_{opt}) of a microscope depends on the wavelength (λ) of the light and the numerical aperture (*NA*) of the objective (NA_{obj}) and the condenser (NA_{cond}) lenses. In the case of a diffraction-limited lens, the optical resolution can be estimated using the Rayleigh criterion [80]. According to this criterion, the optical resolution is given by,

$$r_{opt} = \frac{1.22\lambda}{NA_{obj} + NA_{cond}}. \tag{5.6}$$

From equation (5.6), it can be seen that the minimum resolvable distance improves with shorter wavelength light and lenses with higher NA. As an example, using a microscope system having (NA_{obj}) of 0.65 and (NA_{cond}) of 0.95, then the minimum resolvable distance obtained for a green light (λ =550nm) would be 0.42 μm.

When no condenser is used, equation (5.6) can be written as [80]

$$r_{opt} = \frac{0.61\lambda}{NA_{obj}}. \tag{5.7}$$

When two points are separated by a distance of Rayleigh resolution, the intensity between these two points drops to around 75% of the peak intensity, and thus are distinguishable (see figure

5.16b). If two points are close enough that the distance between them is less than the FWHM (full width at half maximum), then no dips in the intensity can be observed between the two peaks (figure 5.16c). Thus, FWHM sets the limiting resolution beyond which further detail cannot be obtained.

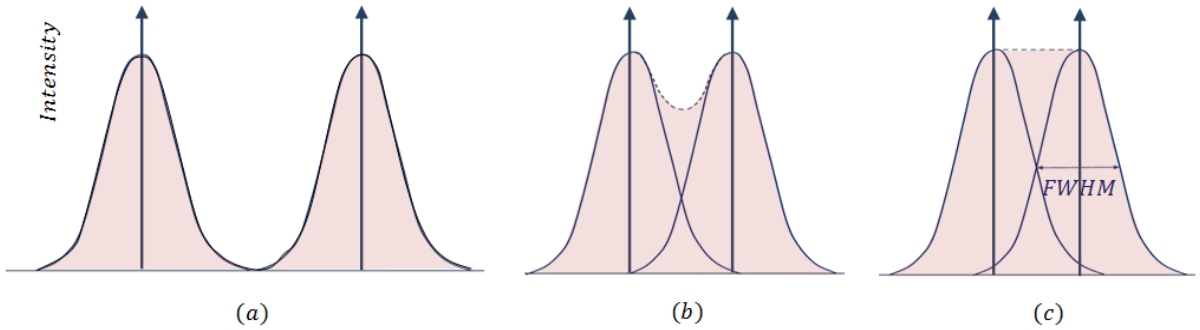


Figure 5.16: Intensity plot of the first peak of two point sources. The shaded area is the combined intensity when a) two point sources are well separated b) two point sources are separated by the Rayleigh's distance and still distinguishable c) two point sources are separated by FWHM and thus undistinguishable.

The result obtained from the Rayleigh criterion is similar to what is obtained from Abbe's approach that employs Fourier analysis to calculate the optical resolution .According to Abbe's theorem the optical resolution of an objective lens can be given as [80], [81], [82].

$$r_{opt} = \frac{0.5\lambda}{NA_{obj}}. \tag{5.8}$$

Spatial Resolution

The optical resolution of a microscope is its ability to resolve the details in the specimen. But in order to record the image in digital format, it is also necessary to know whether the image sensor has enough pixels within the minimum resolved distance. The minimum number of pixels required for a particular spatial resolution is given by Nyquist criterion [80], [81],[83],[84]. According to Nyquist criterion, at least 2.3 pixels are needed within the minimum resolvable distance (r_{opt}). If too few pixels are allocated within the optical resolution, then the spatial details of the specimen cannot be distinguished in the final image. A small amount of oversampling is often performed, which helps to remove the aliasing effects and capture the small details more clearly. It has been shown that three to six pixels within the optical resolution offers greater spatial resolution for cell microscopy on a VGA display [81], [83],[85] [86].

However, excessive oversampling is not justified. not only because no additional information can be obtained, but since the secondary diffraction minima is also captured by the pixels, then spurious details would be found on the image [80], [81], [82]. Therefore, in order to occupy the minimum resolvable distance with an optimal number of pixels, a sampling rate of 2 or 3 pixels are good enough.

As we have calculated in the previous subsection, a 40x/0.65 objective lens along with a condenser having NA_{cond} of 0.95 results into an optical resolution 0.42 μm at 550 nm light. Therefore according to the Nyquist theorem, if the sampling rate is 3 pixels per optical resolution, then the size required for the pixel should be,

$$Pixel\ \ size = \frac{Mr_{opt}}{nr.\ of\ \ pixels} = \frac{40 \times 0.42}{3} = 5.6\mu m. \tag{5.9}$$

This result means that, in order to achieve 40x zoom of 0.42μm resolution at $550nm$ light, the pixel pitch should be $\sim$5.6μm.

5.3 Specification and Outcome of the Implemented System

The performance of the microscope system is largely dependent on the property of the image sensor. Therefore, proper selection of the sensor should be the primary concern. Of course, we are using CMOS image sensor since it provides the low cost and high speed solution for imaging. Determining the required pixel pitch d_p, is equally important so that it matches with the optical resolution. Table 5.3 shows the calculated value of pixel pitch, d_p that is required for some commonly available objective lenses at 550nm wavelength. Both the Rayleigh (R) and Abbe (A) approaches has been considered.

The CMOS pixel pitch is limited by the size of in-pixel transistors and the size of the photodiode. The minimum achievable APS size is 4-5 μm [7] but those are very expensive and not very common in market. From Table 5.3, we see that pixels of 7 μm -10 μm pitch are suitable to cover a wide range of commonly used objective lenses. We have chosen LUPA 300, which offers a pixel pitch of 9.9$\mu m \times$ 9.9μm and thus a good choice for our system. Figure 5.17 shows the designed PCB (printed circuit board) for the biasing and interfacing the imager sensor. The speed of the sensor can be calculated according to equation (5.1),

$$FP = FOT + n_r \times (ROT + np_r \times CP).$$

Thus, the imaging speed is 154 fps with a master clock of 50 MHz and 247.6 fps with a master clock of 80 MHz.

no. of pixels/resolution			2		2.5		3	
M/NA	r_{opt}(R)	r_{opt}(A)	d_p(R)	d_p(A)	d_p(R)	d_p(A)	d_p(R)	d_p(A)
4/0.10	3.36	2.75	6.71	5.50	5.37	4.40	4.47	3.67
10/0.25	1.34	1.10	6.71	5.50	5.37	4.40	4.47	3.67
20/0.40	0.84	0.69	8.39	6.88	6.71	5.50	5.59	4.58
40/0.65	0.52	0.42	10.32	8.46	8.26	6.77	6.88	5.64
50/0.50	0.67	0.55	16.78	13.75	13.42	11.00	11.18	9.17
60/0.85	0.39	0.32	11.84	9.71	9.47	7.76	7.89	6.47

Table 5.3: Calculated resolution and corresponding required pixel pitch for commonly used objective lenses.All the distances has been given in μm.

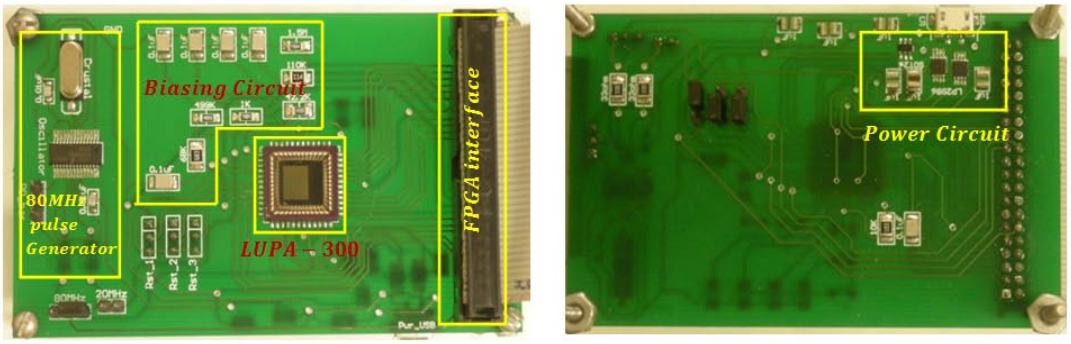


Figure 5.17: The printed circuit board for the camera system: a) top view and b) bottom view.

In this work, we have used 50 MHz master clock which can be directly supplied from the Altera-DE2 board. However, while designing the PCB, a 80MHz clock generator circuit has also been implemented so that further improvement on the imaging speed can be achieved. The frame rate is verified by calculating the number of frames within a certain time interval. The frame counter is implemented within the FPGA which counts the number of image frames. In an experiment, the frame counter counted 10,418 frames within 1 min 8 s.Therefore, the achieved frame rate is

153 fps with a clock of 50 MHz. The complete imaging system has been shown in figure 5.18.

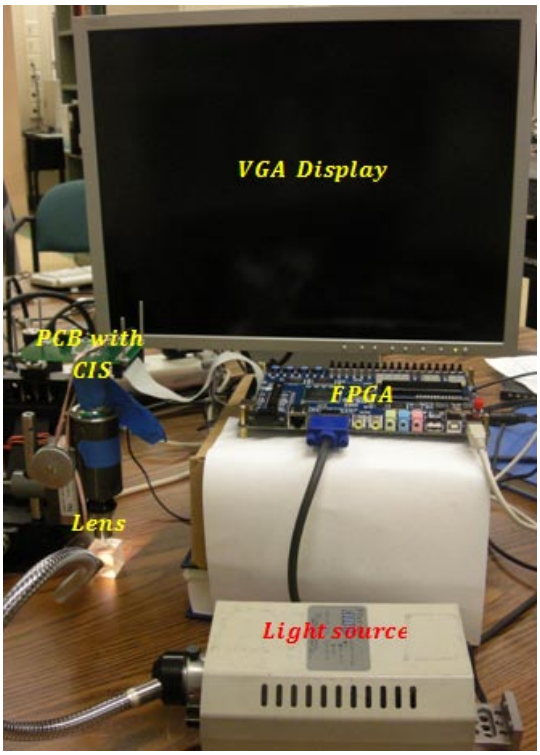


Figure 5.18: The imaging system.

The total system costs less than $1000. Table 5.4 shows the comparison between our system and different digital microscopes that are available in market.

Product	Array size	Speed (fps)	Objectives	Cost (in USD)
Unitron Z850 [87]	2048 × 1536	12	1x-5x	2,589
Motic DM-143 [88]	2048 × 1536	10	1x, 4x	1,499
Motic BA310 [89]	2048 × 1536	10	10x, 20x, 40x, 100x	2,449
National Optical DC4-155 [90]	640 × 480	30	4x, 10x, 40x	785
National Optical DC5-163 [91]	1600 × 1200	10	4x, 10x, 40xR, 100xR	1,735.00
Our work	640 × 480	150-250	4x, 5x, 10x, 20x, 50x	~900

Table 5.4: Comparison between our system and different available microscope in market.

Figures 5.19 to 5.23 show several images taken with the implemented CMOS digital imaging system.

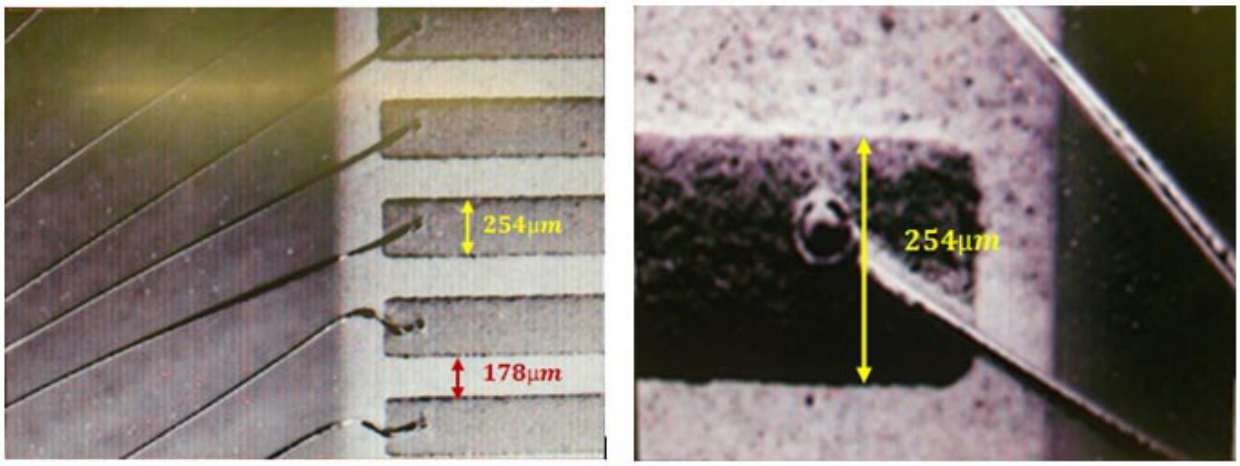


Figure 5.19: Image of bonding fingers of an 84-pin PGA chip carrier by a) 4/0.10 b) 10/0.25 objective lens.

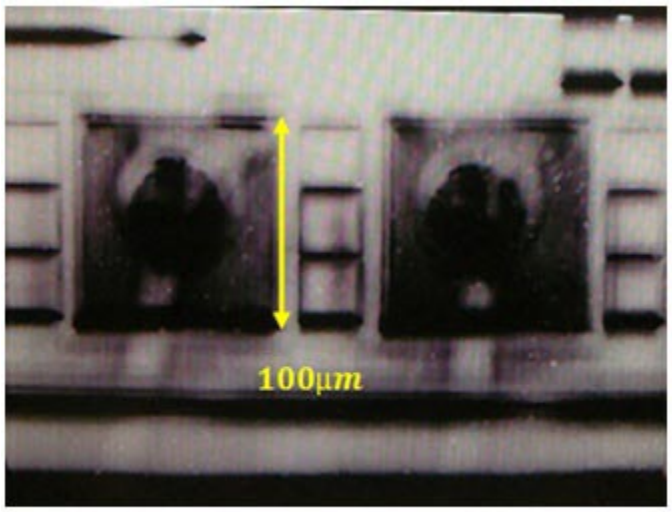


Figure 5.20: Image of bonding pad of a chip by 20/0.25 objective lens.

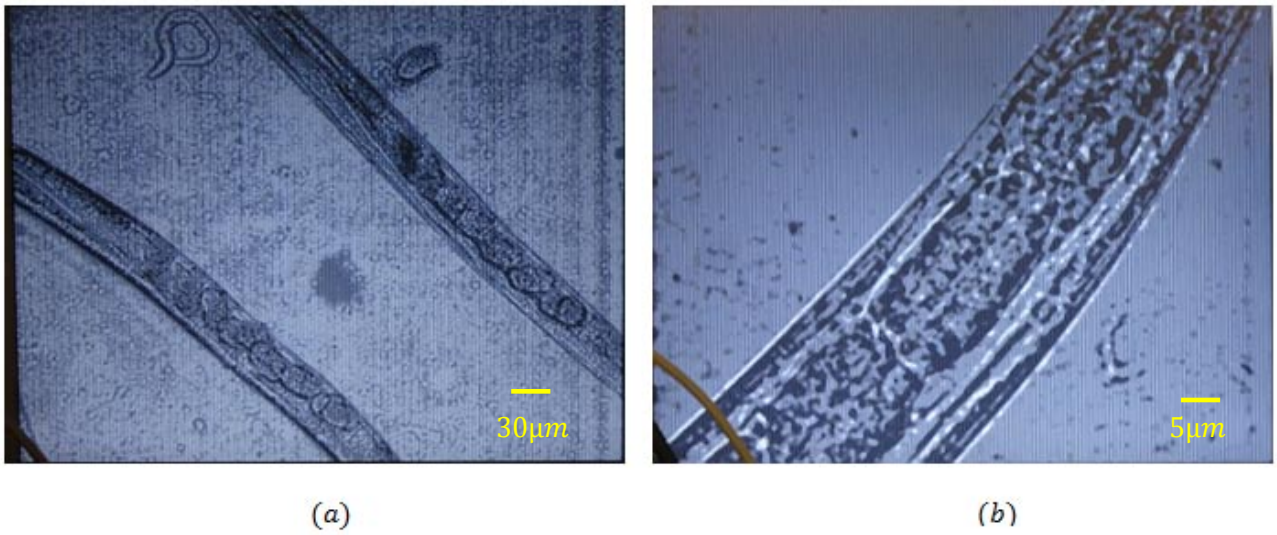


Figure 5.21: Image of adult *C. elegans* by a) 10/.25 b) 50/0.50 objective lens.

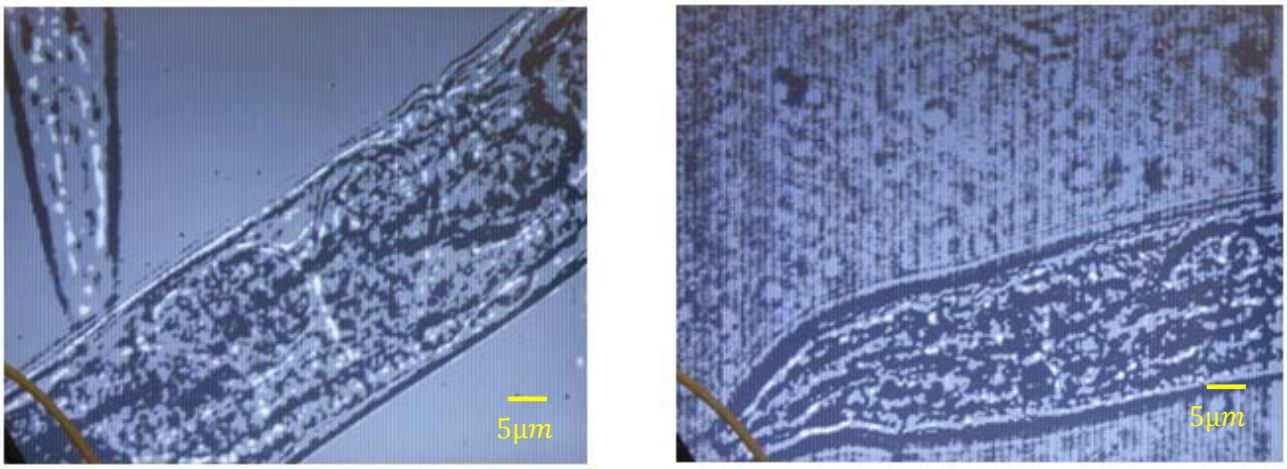


Figure 5.22: Image of adult *C. elegans* by 50/0.50 objective lens.

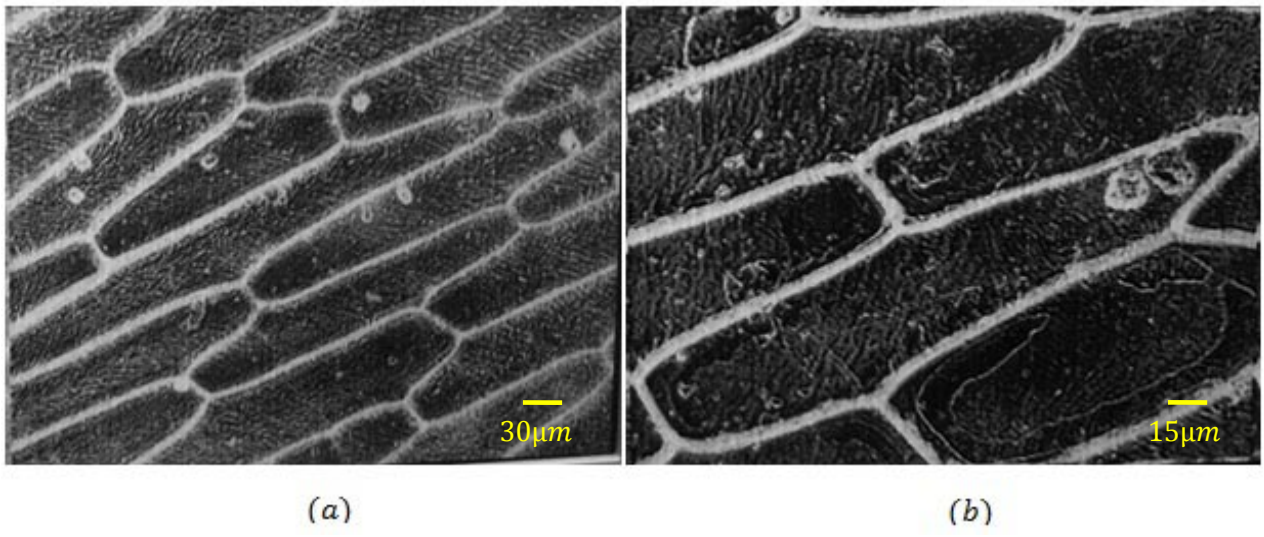


Figure 5.23: Image of *A. cepa* (onion) cell by a) 10/.25 b) 20/0.25 objective lens.

5.4 Summary

In this chapter, we discussed a low-cost imaging system that was implemented by using a high speed CMOS image sensnor –LUPA 300 and an FPGA. The system is capable of capturing 150 image frames per second with a master clock of 50MHz which is being fed from the FPGA board. However, the image sensor itself can deliver much higher frame rate at higher clock (80MHz) or through windowing.

The image sensor has an array of 640× 480 pixels and each pixel gives 10bit output at a 50MHz rate. The GPIO (general purpose input-output) pins of the FPGA board sense the pixel output, which is then further processed by the FPGA in order to display the image on a VGA monitor. The image sensor has 16 internal registers, the value of which determines the operating mode of the sensor. The register values are uploaded on the image sensor through an SPI interface that is also controlled by the FPGA.

Determining the appropriate size of the pixel is of great importance while chosing an image sensor. According to Nyquist criterion, the pixel size should be such that, the optical resolution legth should be covered by 2-3 pixels. Too many pixels can increase the spatial noise in the image, whereas too few pixels can deteriorate the spatial resolution. Therefore, the optical resolution, which is also a function of the numerical aperture of the objective lens and the wavelength of light source; plays a vital role in determining the pixel pitch. Considering

different approaches (Rayleigh and Abbe) for calculating the optical resolution, the optimized value of the pixel pitch was found within 7 μm -10 μm.

The total cost of the system is not more than 1000 USD, thus it could be a cost effective solution for biomedical microscopy, specially for the imaging of rapidly moving objects like *C. elegans*.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The thesis dealt with two different aspects of CMOS image sensors. On one hand, we have investigated the characteristics of the increasingly important random telegraph signal (*RTS*) noise in CMOS image sensors, as the technology scales towards a few nanometer dimensions. On the other hand, we have shown the prospect of CIS by developing a high frame rate digital microscope system which will be very attractive as a low-cost solution of high speed biological microscopy, cell biology etc.

Time domain measurements have been carried out to explore the time constants and amplitude of the RTS noise. The RTS noise produces Lorentizian type of PSD. The cut-off frequency obtained from the calculated PSD is well matched with that found from the time domain measurement, which validates the correctness of the measurement. The amplitude of RTS noise is measured and compared with calculations. The measured value varies somewhat from the approximation which could be due to the involvement of some enhanced trap generation mechanism [68], [69].

The pixel bias dependence and temperature dependence of RTS time constants has also been observed. From the bias dependence experiment, it has been found that the mean capture time decreases drastically with pixel bias because of the increased trapping probability of electrons. The mean emission time is approximately independent of the bias voltage. From the measured time constants, the location of the trap in the oxide layer has been calculated.

Both capture and emission time constants are dramatically reduced with increasing temperatures. The reduction in time constants is believed to be caused by the increased vibration of defect center with temperature, which is responsible for more frequent capturing and releasing of electrons. The temperature dependence of mean capture and emission times has been measured and used to calculate the thermal activation energy.

In another work of this thesis, we have developed a low-cost, high frame rate digital

microscope system using a CMOS imager sensor (CIS). The image sensor converts the optical signal into digital pulses which is processed by the FPGA. The FPGA controls all the systems including the sensor and the VGA monitor. The processed data was then fed to the VGA monitor for display. The SPI interface, the controller bus for the image sensor was also designed with VerlogHDL and implemented in FPGA. The speed of the implemented system is 150fps at 50MHz clock and the total cost is ~$900, which is cheap compared to different digital microscopes and high speed cameras available in the market.

The purpose of this work was to build a microscope system primarily for *C. elegans* imaging. As we have mentioned earlier, *C. elegans* is a widely used model organisms due to its well developed physiological structure. The implemented high speed imaging system allows us to grab images of *C. elegans* at a rate of 150 frames per second. As a result, several phenotypical information about the *C. elegans* e.g. the development of the gonad [92], response with external stimulations such as electric potential [93], chemicals or drugs [94], [95] can be obtained with great detail. Other than the imaging of *C. elegans*, this high frame rate digital microscope can be useful for the imaging of other model organisms and also in plant research. The imaging speed can be further increased by increasing the master clock speed. Alternatively, if a lower resolution is required, then windowing of the pixels can lead to a speed of ~1000 frames per second.

The system is developed in order to display the image in real time. The on-board SDRAM functions as a temporary storage of the image data.

6.2 Future Work

From our experiments, it was observed that the rate of RTS fluctuation decreases rapidly at lower pixel bias and lower temperature. This important observation may help us in setting the proper operating conditions of the CMOS image sensor to achieve better noise performance in low light level imaging situations. Moreover, the extracted parameters of a trap - depth, activation energy, capture cross section are important characteristics which can be measured from the bias and temperature dependence of RTS time constants. Therefore, accurate measurements of those parameters can be found very useful for further modeling of RTS noise in CMOS image sensors.

In the noise area, we have only addressed RTS noise in the pixel. However, other sources of noise should also be studied. There is temporal noise, a fundamental noise source that is the

time-dependent fluctuations in the signal level. Temporal noise can be present in the pixel, column and gain amplifiers and analog to digital converters. There is also the stationary (not time dependent) spatial fixed pattern noise due to mismatches in pixels, color filters, column amplifiers, programmable gain amplifiers and analog-to-digital converters.

As CMOS technology scales to deep-submicron and deca-nanometer dimensions, smaller pixel sizes and larger format digital cameras become feasible. However, to keep the same image quality, low noise operation becomes crucial. Unfortunately, the noise level does not reduce by the same factor as the full-well capacity or quantum efficiency. Such a study on these small dimension pixels would answer the important question if noise will limit the pixel size in scaled CMOS technologies. It would also be useful to determine of new sampling techniques, analogous to correlated double sampling, can be developed to improve the noise characteristics of CMOS pixels.

For the digital CIS microscope, further improvement can be done where the image data from the FPGA can be transferred to the computer in order to save the image or the video stream in the computer memory. The image data from the FPGA can be transmitted to the computer over the RS-232 or USB (Universal Serial Bus) interface. This will allow to perform several image processing techniques on the saved image or video afterwards in order to achieve the desired result.

In addition, for high frame rate applications, faster CMOS image sensors are required. However, at these high frame rates, the clock speeds will increase to several hundreds of MHz or even GHz. At these high frequencies, the design of the clock will be challenging as both careful layout, proper grounding and other high frequency design techniques must be invoked. It would also be useful to have a color high-frame rate digital microscope. So high speed processing of the raw image for subsequent display must be addressed.

Finally, it would be useful to test the high-frame rate digital microscope in real biological applications. With capabilities of higher speed acquisition, it is feasible to observe various dynamic biological processes e.g. cell division, osmosis etc. to be observed in real time or faster, or be stored and played back later. The higher frame rate of the imaging system would also be useful for fluorescence imaging of live tissues/cells that requires higher imaging speed.

Appendix A– Trap Depth

The equation (3.102) can be re-written as ,

$$E_{trap} - E_F = kTln\left(\frac{\tau_c}{\tau_e}\right), \tag{A.1}$$

considering the Fermi level as constant, differentiating equation (A.1) with respect to the gate voltage, V_g of the SF we get,

$$\frac{dE_{trap}}{dV_g} = \frac{kT}{q}\frac{d}{dV_g}\left[ln\left(\frac{\tau_c}{\tau_e}\right)\right], \tag{A.2}$$

Again by differentiating equation (3.103) with respect to V_g we get,

$$\frac{dE_{trap}}{dV_g} = -\frac{d}{t_{ox}}\left(1 - \frac{d\psi_s}{dV_g}\right), \tag{A.3}$$

Comparing equations (A.2) and A.3 we can write,

$$-\frac{d}{t_{ox}}\left(1 - \frac{d\psi_s}{dV_g}\right) = \frac{kT}{q}\frac{d}{dV_g}\left[ln\left(\frac{\tau_c}{\tau_e}\right)\right], \tag{A.4}$$

Neglecting the change of surface potential with V_g, the equation can be written as

$$-\frac{d}{t_{ox}} \approx \frac{kT}{q}\frac{d}{dV_g}\left[ln\left(\frac{\tau_c}{\tau_e}\right)\right], \tag{A.5}$$

The equation can be re-arranged as,

$$\frac{d}{dV_g}\left[ln\left(\frac{\tau_c}{\tau_e}\right)\right] \approx -\frac{q}{kT}\frac{d}{t_{ox}}, \tag{A.6}$$

Since the same drain current is flowing through the SF and the biasing transistor, it can be considered that,

$$\frac{dE_{trap}}{dV_g} \approx \frac{dE_{trap}}{dV_{bias}}, \tag{A.7}$$

Therefore equation (A.6) can be written as, $\frac{d}{dV_{bias}}\left[ln\left(\frac{\tau_c}{\tau_e}\right)\right] \approx -\frac{q}{kT}\frac{d}{t_{ox}}$. (A.8)

Appendix B – Activation Energy

The average velocity of electrons can be given by [25] as,

$$v_t = \left(\frac{8kT}{\pi m_{avg}}\right)^{1/2}, \tag{B.1}$$

Here, m_{avg} is the average mass of an electron in the inversion layer. Conduction in a MOSFET arises from the drift current and diffusion current. In inversion mode, the diffusion current can be considered negligible compared to the drift current, which originates from the drift of electrons due to the presence of electric field. The drift velocity of electrons can be written as,

$$v_n(T) = -\mu_n(T).\frac{dV_{ds}}{dx}, \tag{B.2}$$

and the drift current would be,

$$I_D = -q\mathrm{n}(T)A_{ch}(T)v_n(T), \tag{B.3}$$

where, n is the density of electrons per unit area, A_{ch} is the cross-section of the channel and $\mu_n(T)$ is the temperature-dependent electron mobility. From equations (B.2) and (B.3), we get,

$$I_D = qn(T)\mu_n(T)t_{ch}(T)V_{DS}\frac{W}{L}, \tag{B.4}$$

Here, $t_{ch}(T)$ is the temperature-dependent channel thickness,and W, L are the channel width and length respectively. Since, the source-follower transistor of an APS operates in saturation, the I_D can be considered as independent of V_{DS} and the I_D can be written as,

$$I_D = qn(T)\mu_n(T)t_{ch}(T)V_{Dsat}\frac{W}{L}, \tag{B.5}$$

According to [25]the temperature dependence of electron mobility can be written as,

$$\mu(T) \equiv \mu_0 T^{-1.5}, \tag{B.6}$$

and the channel thickness in inversion is given by [25],

$$t_{ch}(T) \equiv t_0 T, \tag{B.7}$$

Therefore, equation (B.5) can be re-arranged as,

$$n(T) \equiv \frac{I_d T^{0.5}}{q\mu_0 V_{Dsat}\, t_0 (W/L)}, \tag{B.8}$$

Replacing $n(T)$ and v_t in equation (4.21), we get,

$$\tau_c \equiv \frac{q\mu_0 V_{Dsat}\, t_0 (W/L) exp\,(\Delta E_a/kT)}{\sigma_{n0}\left(\frac{8kT}{\pi m_{avg}}\right)^{1/2} I_D T^{0.5}}. \tag{B.9}$$

Equation (B.9), can be re-arranged as,

$$ln(\tau_c T) \equiv ln(P) + \frac{\Delta E_a}{k}\frac{1}{T}. \tag{B.10}$$

where, P can be considered as a constant and is given by,

$$P = \frac{q\mu_0 V_{Dsat}\ t_0 (W/L)}{\sigma_{n0}\left(\frac{8k}{\pi m_{avg}}\right)^{1/2} I_D}. \tag{B.11}$$

Note that τ_c can be replaced in equation (3.102), and by doing so, we get

$$\tau_e = \frac{exp\,(\Delta E_a/kT)}{\sigma_{n0}\left(\frac{8kT}{\pi m_{avg}}\right)^{1/2} n(T)} exp\left(\frac{E_F - E_{trap}}{kT}\right). \tag{B.12}$$

From equation (3.96), we find the concentration of electron at the interface is,

$$n(T) = N_c exp\left(\frac{E_F - E_C}{kT}\right), \tag{B.13}$$

The density of states in conduction band, N_C is temperature dependent and is given by [25]

$$N_C \equiv N_{C0} T^{1.5}, \tag{B.14}$$

Therefore, from equations (B.12), (B.13) and (B.14) we get,

$$\tau_e = \frac{exp\,(\Delta E_a/kT)}{\sigma_{n0}\left(\frac{8kT}{\pi m_{avg}}\right)^{1/2} N_{C0} T^{1.5} exp\left(\frac{E_F - E_C}{kT}\right)} exp\left(\frac{E_F - E_{trap}}{kT}\right). \tag{B.15}$$

Equation (B.15) can be re-arranged as,

$$ln(T^2 \tau_e) \equiv ln(Q) + \frac{\Delta E_a + \Delta E_{CT}}{kT}. \tag{B.16}$$

where,Q is a constant, given by,

$$Q = \frac{(\pi m_{avg})^{0.5}}{\sigma_{n0} N_{C0} (8k)^{0.5}}. \tag{B.17}$$

and

$$E_{CT} = E_C - E_{trap}\,. \tag{B.18}$$

Appendix C– SPI Interface

```
module SPI_interface (  //        Host Side
                                                  iCLK,
                                                  iRST_N,
                                                  //iExposure,
                                                  outCLOCK1,
                                                  outCLOCK,
                                                  SPI_EN,
                                                  SPI_IN,
                                                  SENSOR_RST_N
                                                  );

input                   iCLK;
input                   iRST_N;
output SPI_IN;
output SPI_EN;
output SENSOR_RST_N;
output outCLOCK;
output outCLOCK1;
reg     [15:0]  mSPI_DATA;
reg     [15:0]  LUT_DATA;
reg     [5:0]   LUT_INDEX;
reg     [3:0]   mSetup_ST;
reg [4:0] SPI_CLK_COUNT;
reg spi_in;
reg spi_en;
reg sensor_rst_n;
reg     [5:0]   P;
reg outCLK;
reg outCLK1;

parameter       LUT_SIZE        =       16;

assign outCLOCK = outCLK;
assign outCLOCK1 = outCLK1;
assign SPI_IN = spi_in;
assign SPI_EN = spi_en;
assign SENSOR_RST_N = sensor_rst_n;

always@(posedge iCLK or negedge iRST_N)
begin
        if(!iRST_N)
        outCLK1 <=0;
 else
 outCLK1 <= ~outCLK1;
 end
```

```
always@(posedge iCLK or negedge iRST_N)
begin
        if(!iRST_N)
        begin
                outCLK <=0;
    P <=0;
        end
        else
        begin
          if(P!=10'd40)
                P       <=      P +1;
                if(P>=10'd4)
                outCLK <= ~outCLK;
          if(P>=10'd35)
          outCLK <=0;
                if(P >= 10'd37)
                P <=0;
        end
end

always@(negedge outCLOCK1 or negedge iRST_N)
begin
        if(!iRST_N)
          begin
                LUT_INDEX <=      0;
                 mSetup_ST   <=      0;
                 SPI_CLK_COUNT <= 0;
                 spi_in <=0;
                 spi_en <=0;
                 sensor_rst_n <=0;
          end
        else
          begin
if (LUT_INDEX < LUT_SIZE)
  begin
    case(mSetup_ST)
      0:begin
        mSPI_DATA <=LUT_DATA;
        SPI_CLK_COUNT <= 0;
        mSetup_ST <= 1;
      end
      1:begin
        if (SPI_CLK_COUNT<16)//to pass 16 bit as serial output 16 count is required.
                                                begin
                                                spi_in <= mSPI_DATA[15-SPI_CLK_COUNT];//serial data is
being transferred form each location of the register
                                                SPI_CLK_COUNT <= SPI_CLK_COUNT+1;// register counter
is being updated
                                                spi_en <=0;//SPI_EN is 0 till all the bits are transmitted.
                                                end else
```

```
                                        begin
                                        spi_en <=1;//after transmitting all the bits SPI_EN is setting as 1
to upload the bits.
                                        SPI_CLK_COUNT <= 0;
                                        spi_in <=0;// counter is being reset
                                        mSetup_ST <=2;
        end
       end
    2: begin
         spi_en <=0;
         spi_in <=0;
         LUT_INDEX    <=      LUT_INDEX+1; // LUT_INDEX is updated
                                        mSetup_ST    <=      0; // starting the SPI upload once agian
     end

      default:
       begin
                        LUT_INDEX  <=      0;
                        mSetup_ST    <=      0;
                        SPI_CLK_COUNT <= 0;
                        spi_in <=0;
                        spi_en <=0;
              end
    endcase
   end else
       begin
        sensor_rst_n =1'b1;
       end
  end
end

always @(LUT_INDEX)
begin
         case(LUT_INDEX)
         0       :       LUT_DATA    <=      {4'b0000,12'b00000101001}; //SEQUENCER
         1       :       LUT_DATA    <=      {4'b0001,12'b00000000}; //Start pointer X readout
         2       :       LUT_DATA    <=      {4'b0010,12'b000000000};//Start pointer Y readout
         3       :       LUT_DATA    <=      {4'b0011,12'b10100000};//Number of kernels to read
out (4 pixel kernel)
                 ////////////////////////need to play with this value////////////////////////////////
         4       :       LUT_DATA    <=      {4'b0100,12'b000000000010};//Length of reset_1 pulse
(in number of lines)
                 default is 12'b000000000010};)
         ////////////////////////////////////////////////////////////////////////////////////////
         5       :       LUT_DATA    <=      {4'b0101,12'b0};//Position of reset DS pulse in number
of lines
         6       :       LUT_DATA    <=      {4'b0110,12'b0};//Position of reset TS pulse in number
of lines
                 ////////////////////////need to play with this value////////////////////////////////
```

```
        7       :       LUT_DATA    <=      {4'b0111,12'd1018};//integration time in terms of no .
                //lines(default 12'b000111100001 )
        ////////////////////////////////////////////////////////////////////////
                ////////////////////// need to play with this values//////////////////////////////////////
        8       :       LUT_DATA    <=      {4'b1000,12'd74}; //DAC input for vcal(default is
12'b01001010=74}
        9       :       LUT_DATA    <=      {4'b1001,12'd107};//DAC input for vblack(default is
12'b01101011==107 )
        10      :       LUT_DATA    <=      {4'b1010,12'd85}; //DAC input for voffset(default is
12'b01010101==85};)
        ////////////////////////////////////////////////////////////////////////////////////
        11      :       LUT_DATA    <=      {4'b1011,12'b000011110000};   //Activate analog ADC
input
                // //////////////////////need to play with this values//////////////////////////////////////
        12      :       LUT_DATA    <=      {4'b1100,12'b111110110000}; //PGA Setting(default
12'b111110"1"10000 )
        ////////////////////////////////////////////////////////////////////////////////////
        13      :       LUT_DATA    <=      {4'b1101,12'b101011011111};//CALIB_ADC <11:0>
        14      :       LUT_DATA    <=      {4'b1110,12'b011011011011};//CALIB_ADC <23:12>
        15      :       LUT_DATA    <=      {4'b1111,12'b000011011011};   //CALIB_ADC
<32:24>
        //16    :       LUT_DATA    <=      16'hF119;               //281
        default:LUT_DATA    <=      {4'b0000,12'b00000101001};
        endcase
end
endmodule
```

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