IMPACT OF SCALING ON NOISE BEHAVIOR OF SUB-100NM MOSFETS

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GE TAN, B.A.Sc.

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AUTHOR: Ge (Kevin) Tan, B.A.Sc. (Elec. Eng.) (Tsinghua University)

SUPERVISOR: Chih-Hung (James) Chen, Professor, Electrical and Computer Engineering Department

B.Sc. (National Central University)

M.S. (Simon Fraser University)

Ph.D. (McMaster University)

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Abstract

With the device advancement which meets the manufacturing requirement in modern integrated circuits (IC), complementary metal-oxide-semiconductor (CMOS) technology attracts lots of attention for low-cost and high-speed analog applications. In recent years, device scaling has been the engine driving the microelectronics revolution as described in Moore's Law. Along with this device size decreasing, on the other hand, the noise behavior of modern metal-oxide-semiconductor field-effect transistors (MOSFETs) becomes an important issue for low-power and mobile applications, because the longer operation time between two battery charges is required. Since in wireless communications only a limited amount of noise can be tolerated due to this requirement, studying the impact of the device scaling on MOSFET noise along with accurate noise prediction becomes a critical issue.

This thesis presents the noise characterization, modeling, and simulation of deep sub-100nm bulk MOSFETs and predicts the noise behavior for future technology nodes. There are two main subjects discussed in this thesis. First, we present the impact of scaling of MOSFETs on channel thermal noise. Second, we investigate how the technology development can affect noise performance of a single transistor.

In the first topic, analytical MOSFET channel thermal noise expressions are presented and verified. We calibrate our model using experimental data from devices in 60 nm technology node. The technology scaling issue of MOSFETs on noise performance is also examined by applying the parameters predicted in the International Technology Roadmap of Semiconductor (ITRS). Noise parameters such as minimum noise figure

(NF_{min}) and equivalent noise resistance (R_n) are calculated and verified using dc and noise models.

In the second topic, a new figure of merit, namely equivalent noise sheet resistance, is defined for the first time to demonstrate the impact of scaling. This new figure of merit represents the intrinsic part of the equivalent noise resistance that excludes the geometry information of the device, which captures the technology related parameters of transistors. By defining equivalent noise sheet resistance, we can provide process information not only for IC designers but also for process engineers.

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List of Symbols

Symbol	Definition
B_{opt}	optimized source susceptance
C_{OX}	dioxide capacitance
E_C	critical electrical field at which carriers travel at saturated velocity
g_m	transconductance
G_{opt}	optimized source conductance
$i_n(f)$	rms thermal noise current
I_{dc}	dc current
$I_{d,sat}$	saturated current
k	Boltzmann's constant
L	transistor channel length
L'	length of gradual channel region
N_a	doping concentration
NF_{min}	minimum noise figure
q	electronic charge
Q_{inv}	total charge in inversion layer
R_{eq}	MOSFET equivalent resistance
R_n	equivalent noise resistance
S_{id}	power spectral density for channel thermal noise current
T	temperature in Kelvins
t_{ox}	oxide thickness
v_{sat}	saturation velocity
$v_n(f)$	rms thermal noise voltage
V_{BS}	voltage between substrate and source terminal
V_{DS}	voltage between drain and source terminal
V_{DSAT}	voltage potential at pinch-off point with bias condition $V_{DS} > V_{DSAT}$ in saturation
V_{GS}	voltage between gate and source terminal

V_{th}	threshold voltage
W	transistor width
X_{dep}	depletion width
x_j	junction depth
λ	fitting parameter in CLM effect
τ	lifetime of carriers
γ	body effect coefficient
ω	angular frequency
μ_{eff}	effective mobility
Δf	frequency interval
ΔL	length of velocity saturation region
ΔN	number of carriers in a small section along channel

List of Abbreviations

Symbol	Definition
CLM	channel length modulation
CMOS	complementary metal-oxide-semiconductor
FBB	forward body bias
G-R	Generation – Recombination
IC	Integrated Circuit
ITRS	International Technology Roadmap of Semiconductor
MOSFET	metal–oxide–semiconductor field-effect transistor
$NF^{(1)}$	number of fingers
$NF^{(2)}$	noise factors
PSD	power spectral density
RBB	reverse body bias
RF	radio-frequency
rms	root mean square
SCE	short channel effect
SNR	signal-to-noise ratio
VCO	voltage-controlled oscillator

Chapter 1:

INTRODUCTION

1.1 NOISE

What is noise? Noise is one kind of unwanted perturbation that exists everywhere which can conceal real information from a wanted signal. We use "noise" to describe random fluctuation which results from physical mechanisms in electrical devices. Noise exists universally in electronic devices and systems. In both analog and digital electronics, electronic noise is a random signal in all circuits. For example, when measuring the voltage by using equipment, one may see fluctuations in the voltage, which is one example of electronic noise.

Noise is always a factor that limits the sensitivity of circuits and systems, because it limits the minimum signal that can be detected. With the noise, sometimes the wanted signal is masked by the random fluctuations and thus people cannot get the output signal that they want, especially when the signal is small. In other words, if the noise level is comparable to the real signal, people might fail to identify what is the desired signal, because the desired information in the real signal is overwhelmed by noise.

Since noise is a random process, its instantaneous value at certain time cannot be predicted. Then the question is how to measure the noise? One possibility is to measure the 'average power' in the frequency domain. If the noise voltage from a load resistor R_L is given by $v_{noise}(t)$, then the average power in a period T is given by

$$P_{noise} = \frac{1}{T}\int_0^T \frac{v_{noise}^2(t)}{R_L} dt \tag{1-1}$$

People use power spectral density (PSD) to show the strength of the variations (average power) carried by a noise waveform in a 1Hz bandwidth, denoted by the symbol, $S_x(f)$. For instance, $S_V(f)$ can represent the PSD of a voltage source with the unit V^2/Hz. The square root of PSD can be then taken as the input noise voltage, and the result is with the unit V/$\sqrt{\text{Hz}}$, considered as noise voltage generator. Similarly, $S_I(f)$ can represent the PSD of a current sources with the unit A^2/Hz, and the square root of it can be considered as noise current generator.

1.2 MODERN MOSFETS AND SCALING ISSUE

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a device used for amplifying electronic signals. It is the basic unit which is widely used in CMOS technology. Since the invention of the first field-effect transistor in 1960, modern integrated circuits have been developing rapidly and MOSFET emerges as the dominant technology in ICs. People already see the increasing use of this technology in wireless products such as laptops, digital cameras, sensors, and cell phones.

Nowadays, as fabrication and manufacturing methods advance, it is possible to integrate millions of transistors on a single chip, and device scaling has been the engine which drives the revolution of integrated circuits. On the other hand, as the device size is getting smaller, people begin to consider the minimum dimension that can be fabricated and the limiting factor that prevents further scaling, etc. So far, device noise becomes a more complicated and important issue as this trend goes. For low-power applications, it is

hard for the system to distinguish between desired signal and noise, which may result in system error or failure. As the characteristic dimension of modern technology scales down from 0.18 μm around the year 2000 to dozens of nano-meter scale, it is crucial for people to know if dimension scaling is profitable or not.

Another reason why people are motivated to do research in scaling impact of deep sub-100nm MOSFETs is that the unity gain frequency of MOSFETs nowadays can reach up to hundreds of GHz. This makes the deep sub-100nm MOSFETs very attractive for radio-frequency (RF) applications because of lower cost compared with other III-V technologies. However, when working in the RF region, noise becomes particularly important. Although people know that the minimum noise figure (NF_{min}) decreases as the transistor scales down, this decreasing rate slows down. Therefore, what we concern about is whether there exists any limit in this scaling trend or not. Consequently, we want to see how noise behaves when the transistor scales down and that is the reason why we focus on the noise modeling for deep sub-100nm MOSFETs.

1.3 CONTRIBUTION OF THIS THESIS

This thesis investigates the impact of scaling on MOSFETs and second order effects in the noise characteristics. Generally, there are three main contributions in the thesis. First, it develops a noise model with the lateral field effect for deep sub-100nm MOSFETs. Second, it predicts the noise behavior of transistors and analyzes future noise trend and device performance by examining noise parameters as well as signal-to-noise ratio (SNR). This procedure presents a clear picture to describe the noise performance in future devices. Finally, it introduces a new figure-of-merit - equivalent noise sheet

resistance, which provides the information during the technology development for both circuit designers and process engineers.

1.4 THESIS ORGANIZATION

This thesis consists of five chapters. In Chapter 1, the motivation of research purposes is described, and contribution and organization of this thesis are presented. Chapter 2 introduces the basics and classification of noises in semiconductor devices, along with the physical mechanisms and noise modeling of short-channel MOSFETs.

Chapter 3 talks about the accuracy issues of on-wafer noise characterization and noise measurements. It starts with the two-port noisy theory and noise parameters, and then gives the description of a microwave noise measurement system setup. The methods to extract the physical noise parameters are also presented. It also introduces the extraction algorithm of the induced gate noise of experimental data, followed by detailed procedure of extraction method.

In Chapter 4, based on the experimental data in 60nm CMOS process, model parameters are calibrated to set up a benchmark of this work. Furthermore, for devices shorter than 60nm, process parameters in ITRS Roadmap 2009 are used to predict noise performances. Equivalent noise sheet resistance is introduced as a new figure-of-merit for the first time, and the impact of its increasing trend as transistor scales down is also explained.

Finally, Chapter 5 concludes the thesis and recommend future work.

Chapter 2:

NOISE SOURCES IN SEMICONDUCTOR DEVICES AND NOISE MODELS IN MOSFETS

2.1 NOISE SOURCES IN SEMICONDUCTOR DEVICES

The noise in a device is the result of spontaneous fluctuations in current and voltage in the device. In this chapter we focus on the physical noise sources in MOSFETs. There are four types of noise sources, namely: (1) thermal noise; (2) shot noise; (3) 1/*f* noise (flicker noise); (4) generation - recombination (G-R) noise [1]-[5]. Noise modeling of each noise source will be presented in each section.

2.1.1 Thermal Noise (Johnson-Nyquist Noise)

One of the most common forms of noise is known as thermal noise (Johnson-Nyquist noise). Thermal noise was first observed by J. B. Johnson and given theoretical analysis by H. Nyquist, and that is why thermal noise is also called Johnson-Nyquist noise [2]. Thermal noise is a random fluctuation in voltage caused by random motion of charge carriers at a temperature above absolute zero Kelvin. The collisions among those carriers and between carriers and atoms cause carriers to change their speed and motion directions, and then lead to the fluctuation of current. Although we know the average current in a conductor is zero, the instantaneous current vibration is not, which gives rise to voltage/current fluctuation when measuring them. In a conductor, the noise power is proportional to its temperature which can be expressed as [1]

$$S = kT\Delta f \tag{2-1}$$

where k is the Boltzmann's constant, Δf is the frequency interval and T is temperature in degrees Kelvin. For a resistance, the root mean square (rms) thermal noise voltage can be expressed as [1][2]

$$v_n(f) = \sqrt{4kTR\Delta f} \tag{2-2}$$

with the rms thermal noise current as

$$i_n(f) = \sqrt{\frac{4kT}{R}\Delta f}\ . \tag{2-3}$$

Equations (2-2) and (2-3) are widely used to describe the power spectral density of the thermal noise. The noise generated by a physical resistor can be modeled as the equivalent circuit shown in Fig. 2.1.

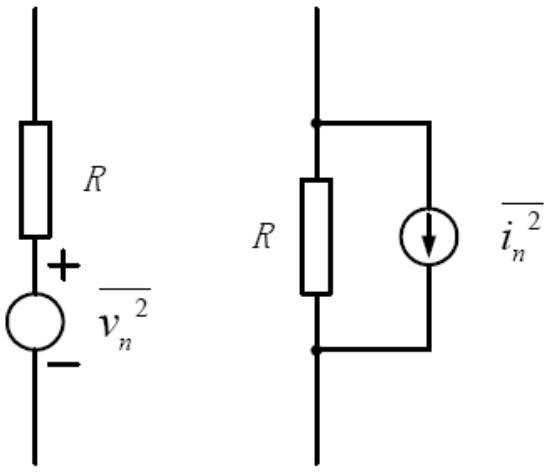


Figure 2.1: Thermal noise models of a resistor with: (a) a noise voltage generator and (b) a noise current generator [64].

In MOSFETs, the most dominant noise source is the channel thermal noise. A MOSFET normally works with an inverse resistive channel between the drain and the

source. The terminal resistance of MOSFET will contribute to total thermal noise of MOSFET as well. Compared with the channel thermal noise, their contribution is small except for the gate resistance. Therefore when analyzing thermal noise of MOSFETs, channel thermal noise is the major concern.

2.1.2 Shot Noise

Shot noise exists in semiconductor devices such as transistors or diodes. It is generated when carriers are injected into a sample volume independently of one another (where a potential barrier exists) and caused by discreteness of electron charges. Electrons arrive at the barriers discretely at random time, and that is why this type of noise is called shot noise. Shot noise is well known to occur in devices such as solid-state devices, tunnel junctions, Schottky barrier diodes and p-n junctions. The shot noise current spectral density is proportional to the bias current and the electron charge, which is presented as [2]

$$\overline{i_n^2} = 2qI_{dc}\Delta f \tag{2-4}$$

where q is the electronic charge and I_{dc} is the dc current.

According to [6], there is another type of shot noise - gate shot noise. Gate shot noise is usually neglected in radio-frequency (RF) models, whose impact is always associated with gate leakage current in MOSFETs. Gate leakage becomes important when there is a charge carrier tunnelling through gate dioxide [7]. When gate thickness is in nanometer-scale, this phenomenon is more obvious and cannot be neglected.

2.1.3 Flicker Noise (1/f Noise)

Another important noise source is the flicker noise, which is found in many different physical systems such as insulators, semiconductor devices, and normal metals. It is called 1/*f* noise or low frequency noise because its spectral density is proportional to $1/f^{\beta}$, where β is, in the range from 0.8 to 1.3 in different devices. The spectral density increases as frequency decreases and it is an important noise source in low frequency circuits. It causes an increment of phase noise in the voltage-controlled oscillators (VCO) since it can be up-converted in such circuits. There are three different theories to explain the physical mechanisms of flicker noise: the McWhorter number fluctuation theory model [10], the Hooge mobility fluctuation theory model [11] and the unified 1/*f* noise theory model [13]. It has been reported that all theories are possible mechanisms which lead to the 1/*f* noise in MOSFETs.

a) McWhorter number fluctuation theory

In McWhorther's theory [10], the physical mechanism of 1/*f* noise is caused by the random trapping and detrapping of mobile carriers in the trap located at Si-SiO_2 interface and within the gate oxide. It has been verified by lots of experiments that the 1/*f* noise is proportional to the effective trap density near the quasi-Fermi level. An efficient and applicable method to decrease flicker noise is to improve the surface quality of the devices.

The 1/*f* noise current in the drain and the source channel is given by [10]

$$\overline{v_f^2}(f) = \frac{K_F}{2 \cdot \mu \cdot C_{OX}^2 \cdot W \cdot L \cdot f} \tag{2-5}$$

where K_F is the constant which depends on the manufacturing process, f is the operational

frequency, μ is the mobility, C_{OX} is the dioxide capacitance, W is the device width, and L is the total length.

b) Hooge mobility fluctuation theory

Hooge's empirical model considers the 1/*f* noise as a result of carrier mobility fluctuation due to the lattice scattering. Based on his model, the 1/*f* noise spectrum density is given by [11],[12]

$$\frac{\overline{i_f^2}(f)}{I^2} = \frac{\alpha_l}{N \cdot f} \tag{2-6}$$

where α_l is the dimensionless Hooge 1/*f* noise constant with values between 10^{-7} and 10^{-3} and N is the total number of charges. This expression is an empirical equation.

c) Unified 1/f noise theory

A unified model for the flicker noise in MOSFETs has been developed in [13] which incorporates both theories mentioned above, since the mechanisms stated in those two different theories exist together, and it is difficult to verify the noise generation mechanism independently. This unified model extends the carrier fluctuation theory and includes the free charge Coulomb scattering mechanism. The number of total charges are correlated with mobility fluctuations. This unified model has been verified by simulations and experimental data, which can be applied to many compact models such as BSIM4 [21] and MOS Model 11 [65]. The analytical expression is given by [13]

$$S_{I_d}(f) = \frac{kTI_d^2}{\gamma f WL^2} \int_0^L N_t(E_{fn}) [\frac{1}{N(x)} \pm \alpha\mu]^2 \, dx \tag{2-7}$$

where L is the channel length, W is the channel width, k is the Boltzmann constant, I_d is the dc current, N is the number of channel carriers per unit area, N_t is the number of interface traps, E_{fn} is the quasi Fermi level, γ is the attenuation coefficient of electron wave function in oxide, and T is the absolute temperature in Kelvin.

2.1.4 Generation-Recombination Noise (GR Noise)

There are two states of electrons and holes in semiconductor devices – delocalized states and localized states. An electron or a hole can transit between those two states and this process is the so called generation-recombination. Noise generated by the generation-recombination process is straightforward as its name reveals: it is due to the random emission of charge carriers at defect centers in semiconductors [14]. Trapping centers in the bulk of the device can cause generation-recombination noise. The GR noise strongly depends on the quality and properties of the semiconductor. Along with the 1/*f* noise, it is one of the major noise sources in low-frequency circuits. The noise power spectral density of generation-recombination process is given by [15]

$$S_i(f) = \frac{4q\mu\alpha}{L^2} I_d V_d \frac{\tau}{1+\omega^2\tau^2} \tag{2-8}$$

where τ is the lifetime of carriers, ω is the angular frequency, V_d is the drain voltage, I_d is dc current, and L is the channel length. The parameter α is defined by a relation equation as

$$\alpha = \frac{\overline{\delta\Delta N^2}}{\Delta N} \tag{2-9}$$

where ΔN is the number of carriers in a small section along the channel.

2.2 DC MODELS IN MOSFETS

2.2.1 I-V Model in MOSFETs

The dc and noise models assume that the device channel can be divided into two consecutive regions: the gradual channel region (Region • in Fig. 2.2) and the velocity saturation region (Region • in Fig. 2.2), between the source and drain terminals.

The physics-based dc model used in this thesis to calculate the drain current is given by [5],[46],[47],[48]

$$I_D = \begin{cases} \dfrac{W}{L}\dfrac{C_{OX}u_{EFF}}{1+V_{DS}/(E_C L)}(V_{GS}-V_{TH}-\dfrac{\alpha}{2}V_{DS})V_{DS}, & (for\ V_{DS} \le V_{DSAT}) \\ \dfrac{W}{L'}\dfrac{C_{OX}u_{EFF}}{1+V_{DSAT}/(E_C L')}(V_{GS}-V_{TH}-\dfrac{\alpha}{2}V_{DSAT})V_{DSAT}, & (for\ V_{DS} > V_{DSAT}) \end{cases} \quad (2\text{-}10)$$

where μ_{EFF} is the effective mobility, V_{TH} is the threshold voltage, C_{ox} is gate oxide capacitance, α describes the bulk charge effect on the threshold voltage, V_{DSAT} is the voltage potential at pinch-off point with bias condition $V_{DS} > V_{DSAT}$ in saturation, and L' is the channel length for the gradual channel region ($L' = L - \Delta L$, where ΔL is defined in (Eqn. 2-13)). Here V_{DSAT} is given by

$$V_{DSAT} = \frac{E_C L(V_{GS}-V_{TH})}{\alpha E_C L + (V_{GS}-V_{TH})} \quad (2\text{-}11)$$

where E_C is the critical electrical field at which carriers travel at their saturated velocity. In this dc model, non-ideal effects as lateral field effect, short channel effect, vertical field effect and CLM effect are included, as stated in the following section. For the CLM

effect, we also use the fitting parameter λ to tune the length (ΔL) in order to have an appropriate dc current.

2.2.2 Non-Ideal Effects in MOSFETs

a) Channel Length Modulation (CLM) Effect

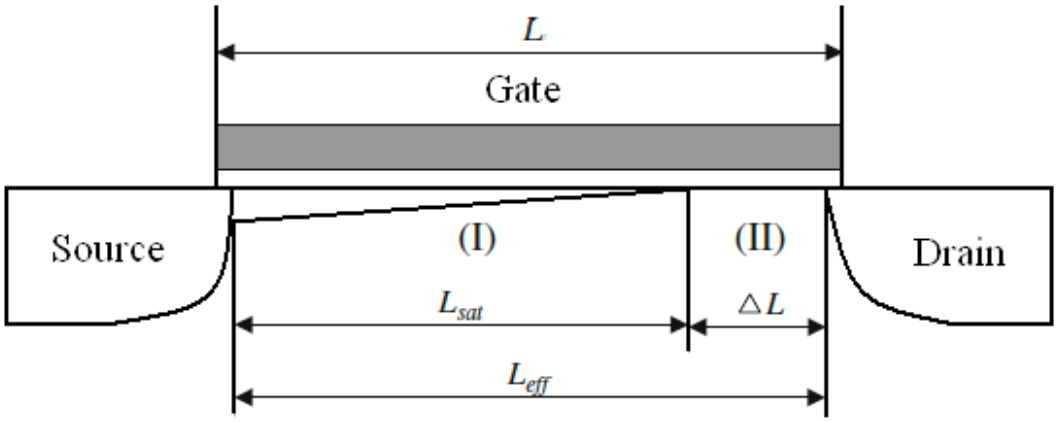


Figure 2.2: Schematic of a MOSFET channel divided into the gradual channel region (I) and the velocity saturation region (II).

When MOSFETs work in the saturation region with $V_{DS} > V_{DSAT}$, the mobile carriers travel at their saturated velocity at the so-called "pinch-off" point. The channel of a MOSFET is now divided into two regions, namely the gradual channel region (I) and the velocity saturation region (II), as shown in Fig. 2.2. The channel length L_{eff} in the gradual channel region is reduced from L_{eff} to L_{sat} ($L_{sat} = L_{eff} - \Delta L$). This results in the increment of the dc current.

For deep sub-100nm MOSFETs, the channel length modulation effect becomes important in the channel thermal noise modeling [16]. The models for ΔL in the velocity saturation region have been given in [17]-[19]. The ΔL model is given by [16]

$$\Delta L = \frac{1}{\alpha}\ln(\frac{\alpha(V_{DS} - V_{DSAT}) + E_D}{E_C}), \quad (2\text{-}12)$$

$$E_D = E_C\sqrt{1 + (\frac{\alpha(V_{DS} - V_{DSAT})}{E_C})^2}, \text{ and} \quad (2\text{-}13)$$

$$\alpha = \lambda\sqrt{\frac{3}{2}\frac{C_{OX}}{x_j\varepsilon_{si}\varepsilon_o}} \quad (2\text{-}14)$$

where x_j is the junction depth, E_C is the critical electrical field at which carriers travel at their saturated velocity, ε_{Si} is the silicon dielectric constant, ε_o is the vacuum dielectric constant, and λ is the fitting parameter to model the CLM effect. For deep sub-100nm MOSFETs, the PSD of the channel thermal noise will be much lower than the experimental data if the CLM effect is not included [16].

b) Short Channel Effect (SCE)

In long channel MOSFETs, the gate voltage controls all space charge in the inversion layer along the channel. As channel length decreases, the total charges in the depletion region under the gate controlled by gate terminal will decrease since they are shared by depletion region at both drain and source terminals [20]. As a result, the threshold voltage (V_{th}) will then decrease. The SCE model of threshold voltage is given by [21],[22]

$$\Delta V_{th} = -\frac{0.5 \cdot DVT0}{\cosh(DVT1 \cdot \frac{L_{eff}}{l_t}) - 1}(V_{bi} - \Phi_s) \quad (2\text{-}15)$$

where *DVT0*, *DVT1* are the first and the second body bias coefficients of short-channel effect on V_{th}, respectively. V_{bi} is the built-in voltage of the source/drain junctions and Φ_s is the surface potential. Here l_t is given by

$$l_t = \sqrt{\frac{\varepsilon_{si} \cdot TOXE \cdot X_{dep}}{EPSROX}} \cdot (1 + DVT2 \cdot V_{bs}) \tag{2-16}$$

where *DVT2* is the body bias coefficient of short-channel effect on V_{th}, X_{dep} is the depletion width, *TOXE* is the electrical gate oxide thickness, and *EPSROX* is one gate dielectric constant as an alternative approach to model high-*k* dielectrics.

c) Mobility Variation

In MOSFET I-V characteristics, carrier mobility is one of the most important parameters. As carriers travel in channel, they are attracted to the oxide-semiconductor into surface, and their motion will be inhibited by carrier scattering. Carrier scattering will directly affect two characteristics of conductors, which are the stochastic activity of carriers (noise) and the hindrance to the flow of charges (resistance) [23]. In other words, it gives rise to the stochastic motion of carriers in the material, while it can be seen as the obstacles that limit the motion of carriers as well.

In the modern technologies, the phenomenon of scattering has a great influence on mobility of carriers, and consequently the carrier velocity decreases due to scattering. The scattering mechanisms in MOSFETs are more complicated than those in their constituent elements. Several surface effects in MOSFETs add and sometimes dominate the scattering mechanisms presented in the device. The most dominant scattering mechanisms for MOSFET devices are phonon scattering, surface roughness scattering,

ionized bulk impurity scattering and charge scattering from the Si/SiO_2 surface. As the device scales down with the gate oxide thickness decreasing, the vertical electric field increases and more electrons are attracted to the oxide-semiconductor surface, where there exists varieties of unstable chemical bond and impurity ions. That's why the modeling of carriers becomes a major concern for device engineers. The mobility degradation which includes the effects of Coulombic scattering, surface roughness scattering, and phonon scattering can be expressed as [25],[26]

$$\mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{bseff})(\frac{V_{gseff} + 2V_{th}}{TOXE}) + UB(\frac{V_{gseff} + 2V_{th}}{TOXE})^2} \tag{2-17}$$

where *U0* is the effective mobility at low transverse field, V_{th} is the threshold voltage, *TOXE* is the oxide thickness, and *UA*, *UB*, *UC* are the fitting coefficients used to characterize first and second order mobility degradation.

d) Velocity Saturation

In the analysis of traditional long channel MOSFETs, the mobility is considered to be constant, which is the ideal case. As the characteristic dimension shrinks, the electric field along the horizontal direction increases and thus, the carrier velocity saturates. The velocity saturation effect happens when the horizontal electric field is approximately 10^4 V/cm [20]. The velocity degradation due to the lateral field effect can be expressed as [40]

$$v(x) = \begin{cases} \dfrac{u_{eff} E(x)}{1 + \dfrac{E(x)}{E_c}} & E(x) < E_c \\ v_{sat} & E(x) \geq E_c \end{cases} \tag{2-18}$$

where μ_{eff} is the effective mobility, $E(x)$ is the horizontal electrical field, E_c is the critical field, and v_{sat} is the saturation velocity which is the maximum velocity carriers travel in the channel.

e) Hot Carrier Effect

With technology scaling down, the hot carrier effect becomes increasingly significant because the electric field in short-channel devices are greater than that in the traditional long channel devices. Most of the time, MOSFETs will in the saturation region. For short-channel devices, their electric field in the velocity saturation region becomes stronger since the voltage supply does not decrease as the device dimension does. As a consequence, high electric field gives rise to the kinetic energy of some mobile carriers and these carriers then become "hot". The energy of hot carriers is far higher than those of thermal equilibrium charges. The hot carriers also have a severe impact on MOSFETs' transconductance, carrier mobility, current, and noise. For instance, charges may tunnel into the oxide, or overcome the potential barrier and generate gate current, which is the cause of the gate tunnelling noise. Another example for the impact of hot carriers on MOSFETs is, the damages in form of interface traps. These traps will lead to mobility degradation as well as increment of threshold voltage [27]-[29].

f) Substrate Bias Effect

In previous discussions, the substrate terminal is connected to the source and those terminals are with ground potential. In real circuits, they may not be connected together. The voltage difference between the source and the substrate will lead to the change in the threshold voltage. Threshold voltage is defined as the voltage to be

overcome in order to create the inversion charge in the channel. If there is a voltage difference between the source and the substrate ($V_{SB} \neq 0$), the surface potential changes, as a result, the threshold voltage is altered, which is given by [20]

$$V_{TH} = V_{TH0} + \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}}[\sqrt{2|\phi_{FP}| + V_{SB}} - \sqrt{2|\phi_{FP}|}] \tag{2-19}$$

where V_{TH} is the threshold voltage, N_a is the doping concentration , ϕ_{FP} is the potential difference between E_{Fi} and E_F in semiconductor, ε_{Si} is the silicon dielectric constant, V_{SB} is the substrate voltage, and q is the electrical charge. It is revealed from the equation that once a forward substrate voltage is applied ($V_{BS} > 0$), it will suppress threshold voltage and increase the drivability, which has been proved in [30]. As channel length decreases, the threshold voltage becomes less sensitive to the substrate-source voltage [20]. For deep sub100nm MOSFETs, if the characteristic length is defined by [66]

$$l = \sqrt{\frac{\varepsilon_{Si}T_{OX}X_{dep}}{\varepsilon_{OX}\eta}} \tag{2-20}$$

where the threshold voltage can be modeled by

($L >> l$)

$$\Delta V_{th}(L) = [2(V_{bi} - \phi_s) + V_{DS}](\exp^{-L/2l} + 2\exp^{-L/l}) \tag{2-21}$$

and

($L << l$)

$$\Delta V_{th}(L) = \exp^{-L/l}[3(V_{bi} - \phi_s) + V_{DS}] + 2\exp^{-L/2l}\sqrt{(V_{bi} - \phi_s)(V_{bi} - \phi_s + V_{DS})} \tag{2-22}$$

where V_{bi} is the built-in voltage of the source/drain junctions and ϕ_s is given by

$$\phi_s = 2|\phi_{FP}| + V_{SB}. \tag{2-23}$$

This model includes effects of V_{DS}, channel length, and body bias on threshold voltage.

2.3 NOISE MODELS IN MOSFETS

2.3.1 Noise Sources in MOSFETs

Thermal noise, induced gate noise and their correlation noise are three major noise sources in MOSFETs [31]. The increasingly usage of CMOS technology in analog and radio frequency applications requires more research on the noise modeling. Noise models of these sources will be reviewed and models for short channel devices will be discussed in this section.

a) Channel Thermal Noise

Channel thermal noise is due to the random thermal motion of mobile carriers in the channel of MOSFETs. It attracts lots of attention for noise modeling since it is the dominant source in MOSFETs. The conventional channel noise model for long channel MOSFETs is given by [40]

$$S_{iD} = 4kT\gamma g_{d0} \tag{2-24}$$

where g_{d0} is channel transconductance at zero drain bias, and γ is a parameter with $2/3 < \gamma < 1$ in the linear region and $\gamma = 2/3$ in the saturation region. The deficiency of this model is it cannot be applied to devices down to nano-meter scale, especially in saturation region [40]. Another commonly used charge based model which is valid for both triode and saturation region is given by [5]

$$S_{iD} = \frac{4kT\mu}{L^2} Q_{inv} \tag{2-25}$$

where k is the Boltzmann's constant, T is the absolute temperature in Kelvins, μ_{eff} is the effective mobility and Q_{inv} is the total charge in inversion layer. This model can provide excellent predictions of thermal noise behavior for long channel devices working in saturation region.

b) Induced Gate Noise

MOSFETs can be considered as RC distribution network with capacitive coupling between the gate and the channel [2]. At high frequencies, the thermal noise originated in the channel will be capacitive coupled to the gate through the gate capacitance of MOSFET [32]. Then it will induce a gate noise current which is known as induced gate noise and is correlated with the channel thermal noise. It was shown in [2] that the induced gate current noise is given as

$$\overline{i_g^2} = 4kT\beta g_g \tag{2-26}$$

where $\beta = 4/3$ for MOSFETs, and g_g is the real part of gate admittance, which is given by [2]

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}. \tag{2-27}$$

Here, C_g is the gate-channel capacitance and ω is the angular frequency.

c) Correlation Noise

In MOSFETs, the induced gate noise $\overline{i_g^2}$ is correlated with the channel thermal noise current $\overline{i_d^2}$ due to the same physical origin (charge fluctuations in the channel). For

long channel devices, correlation noise can be acquired from integrating the spectral density of a small section over the channel, which is given by [2]

$$\overline{i_g i_d^*} = \frac{1}{3} j\omega C_g 2kT \tag{2-28}$$

where C_g the gate capacitance. As channel length shrinks, this type of noise is negligible [2]. The gate–drain correlation coefficient c is defined as in [33],[34]

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g i_g^*} \cdot \overline{i_d i_d^*}}}. \tag{2-29}$$

This coefficient is mainly an imaginary quantity which has a theoretical value of $0.395j$ for long-channel devices. For short-channel devices it decreases [33],[34].

2.3.2 Review of Channel Thermal Noise Modeling for Short Channel MOSFETs

The use of deep sub-100nm transistors which aims at increasing the functionality and packaging density has brought people many advantages. With this high integrated trend, together with increasing the operational frequency towards to RF range, enhanced channel thermal noise in the short channel MOSFETs has been observed and attracts great attention [41]. Traditional models for long channel devices are no longer valid, and second order effects, such as the channel length modulation (CLM) effect and short channel effect, must be considered. The excessive noise in short channel devices has led to the developments of various noise models, such as in [35]-[41]. Here we present a review for these models to reveal the key features in each model.

a) A. J. Scholten Model [36]

By using the Klaassen-Prins model in [42], the thermal noise model derived by Scholten is given by

$$S_{iD}(f) = \frac{1}{I_D L^2} \int_0^{V_{DSAT}} 4kT_e g(V)^2 \, dV \tag{2-30}$$

where T_e is the charge carrier temperature. Here the conductance $g(V)$ is given by

$$g(V) = W \mu Q_{inv}(V) \tag{2-31}$$

where Q_{inv} is inversion charge density and V is the quasi-Fermi potential. In this model, the charge carrier temperature is elevated with respect to lattice temperature T and is given by

$$T_e = T \cdot (1 + \frac{E}{E_c})^n \tag{2-32}$$

where n is an integer value (n= 0, 1, 2). When $n \neq 0$, it represents the situation that the hot carrier effect is taken into account. This model has two limitations. First, it does not have an analytical expression for the channel thermal noise. Second, the CLM effect is not taken into consideration in this model.

b) Abidi Model [67]

In this model, the enhanced channel thermal noise generated from the short-channel devices is observed comparing with conventional theory prediction. The excess noise of factors shows 4 to 5 times greater than expected from long-channel theory that is obtained in MOSFETs with 0.7-μm length. This phenomenon suggest that in short-channel devices, the large electric fields may produce “hot” carriers. As a result, the noise

temperature is significantly above the lattice temperature. By taking this hot carrier effect into account, the excess channel thermal noise can be explained.

c) C. H. Chen Model [37]

In this model, in order to acquire the analytical expression for the channel thermal noise, the channel is divided into two consecutive regions. By integrating the noise current spectral density from each small section along the channel, the total power spectral density of channel noise can be obtained by [37]

$$S_{i_d^2} = \frac{4kT_o}{L_{elec}^2}\mu_{eff}\left|Q_{inv}\right| + \delta\frac{4kT_oI_D}{L_{elec}^2E_{crit}^2}V_{DSSAT} \tag{2-33}$$

where Q_{inv} is total inversion charge in gradual channel region, L_{elec} is the length of gradual channel region, T_o is the standard temperature 290K. This model suggests no noise current for the velocity saturation region since the carriers in this region travel at their maximum velocity, and they don't respond to local change of electric field. Therefore these carriers do not contribute to noise current, which has been proved and verified by experimental results. Therefore, the noise current from the velocity saturation region is zero [37]. In [37], it includes the channel length modulation effect, and hot carrier effect.

d) S. Asgaran Model [48]

In this model, by dividing the channel into two consecutive regions and calculate the current noise PSD at each small section of the channel, the drain current noise spectral density of the device is obtained by

$$S_{i_d^2} = 4kT \frac{4V_{GT}^2 + V_0^2 - 2V_0 V_{GT}}{3V_{GT}^2 (V_{GT} - V_0)} \alpha I \tag{2-34}$$

where $V_{GT} = V_{GS} - V_{th}$, V_{th} is the threshold voltage, $V_0 = I/WC_{ox}v_{sat}$, α is the bulk-charge effect coefficient and I is the dc current. This model with simple analytical expressions can provide good agreement between model and experimental data, but it fails to predict noise PSD when the drain to source voltage is zero. At the condition of $V_{ds} = 0$, the dc current is zero, but the channel thermal noise spectral density is not.

e) A. S. Roy Model [68][69]

In Roy model, a physics based analytical model is developed by using an expression of carrier temperature that is consistent with the mobility model. By calculating the current noise source of a small segment and integrating the overall spectral density along the channel, the total PSD of drain current noise is given by [68]

$$S_{i_d^2} = 4kT_L \frac{W}{L_{eff}^2 (1 + \frac{1}{L_{eff}} \int_{V_s}^{V_{deff}} \frac{u_{eff}^{'}}{u_{eff} + u_{eff}^{'} E} \cdot dV)^2} \times \int_0^{L_{eff}} (-Q_i) \frac{u_0^{'}}{u_{eff} + u_{eff}^{'} E} \cdot dx \tag{2-35}$$

where μ_{eff} is the effective mobility, Q_i is the inversion layer charge, L_{eff} is the effective channel length, T_L is the lattice temperature in absolute temperature in Kelvin, and E is the lateral electric field. This model is a charge based model which also provides good prediction for transistors working in triode region. The mobility degradation effect is also considered in this model.

In [69], noise model in lateral nonuniform MOSFET is presented. Depending on noise mechanisms and doping profile, uniformly doped MOSFET noise models based on

Klaassen-Prins (KP) model [42] may give erroneous prediction of transistor working at triode region. The KP method overestimates noise by 2-3 orders of magnitude at low bias condition. For lateral nonuniformly doped MOSFETs, this effect should be considered.

2.3.3 Channel Thermal Noise Model in MOSFETs

By applying Wang's model in [40] and calculate total inversion layer charge in channel, the power spectral density for channel thermal noise current can be presented as

$$S_{id} = \frac{\overline{i_d^2}}{\Delta f} = 4kT \frac{u_{EFF}^2 W^2 C_{OX}^2}{L^2 I_D}[(V_{GS} - V_{TH})^2 V_{DS} - \alpha(V_{GS} - V_{TH})V_{DS}^2 + \frac{\alpha^2}{3}V_{DS}^3] - 4kT \frac{u_{EFF} W C_{OX}}{L^2 E_C}[(V_{GS} - V_{TH})V_{DS} - \frac{\alpha^2}{2}V_{DS}^2] + \delta \frac{4kTI_D}{L^2 E_C^2} V_{DS} \quad (for\ V_{DS} \le V_{DSAT}) \tag{2-36}$$

or

$$S_{id} = \frac{\overline{i_d^2}}{\Delta f} = 4kT \frac{u_{EFF}^2 W^2 C_{OX}^2}{L'^2 I_D}[(V_{GS} - V_{TH})^2 V_{DSAT} - \alpha(V_{GS} - V_{TH})V_{DSAT}^2 + \frac{\alpha^2}{3}V_{DSAT}^3] - 4kT \frac{u_{EFF} W C_{OX}}{L'^2 E_C}[(V_{GS} - V_{TH})V_{DSAT} - \frac{\alpha^2}{2}V_{DSAT}^2] + \delta \frac{4kTI_D}{L'^2 E_C^2} V_{DSAT} \quad (for\ V_{DS} > V_{DSAT}) \tag{2-37}$$

In this noise model, there are three parts of noise power spectral density – the CLM enhanced PSD, lateral field degraded PSD and hot carrier enhanced PSD. The δ in hot carrier effect is also a fitting parameter for which can be tuned to fit with experimental data.

Chapter 3:

NOISE CHARACTERIZATION

3.1 TWO-PORT NOISY THEORY AND NOISE PARAMETERS

The noise figure, is defined as the ratio of the signal-to-noise at the input port and the signal-to-noise at the output port of a two port network. For one two port network with load impedance (Z_L) and source impedance ($Z_S = R_S + jX_S$), the noise figure of this system can be expressed as [29]

$$NF = \frac{(G_a \cdot 4kT_0 \cdot R_s + N_{DUT})G_a}{4kT_0 \cdot R_s} \tag{3-1}$$

where G_a is the gain of the device under test (DUT) and N_{DUT} is the DUT generated noise power. From the above expression, we can see that the value of noise figure is always greater than one. Noise figure can also be defined as the summation of two noisy parts – the source impedance at the input port of the network and the noise sources within the two port network itself. This is expressed as

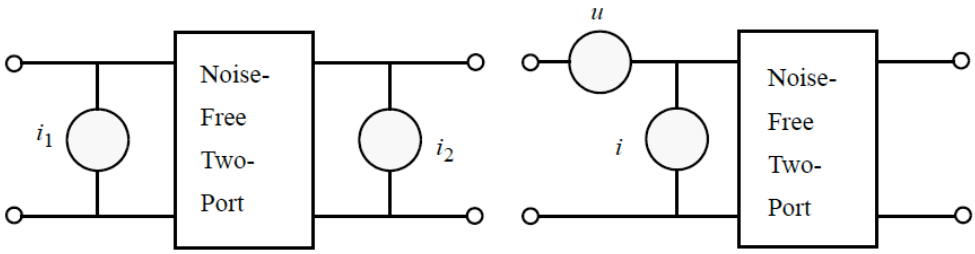
$$NF = NF_{\min} + \frac{R_n}{G_s} \cdot \left| Y_s - Y_{opt} \right|^2 \tag{3-2}$$

or

$$NF = NF_{\min} + 4R_n \frac{|\Gamma_s - \Gamma_{opt}|^2}{(1-|\Gamma_s|^2)|1+\Gamma_{opt}|^2} \tag{3-3}$$

where NF_{min} is the minimum noise figure of the DUT, R_n is the equivalent noise resistance of the DUT, G_s is the source conductance, Y_s is the source admittance presented to the input of the two port, Y_{opt} is the optimum source admittance that results in minimum noise figure, Γ_s is the source reflection coefficient which is given by $\Gamma_s = (Y_o - Y_s)/(Y_o + Y_s)$, and Γ_{opt} is the optimal source reflection coefficient required to achieve $NF_{\min}$.

A noisy two-port may be represented by a noise-free two-port and two current noise sources connected in parallel with input and output terminals, which is shown in Fig. 3.1 [31].



(a) (b)

Figure 3.1: Different representations of a noisy two-port network [31].

These two noise sources are usually correlated with each other. By using the Y-parameters, Fig. 3.1 (a) can be transformed into Fig. 3.1 (b) from the noisy two-port to a noise free two port. In Fig. 3.1 (b), it is shown a noise current source with a serial noise voltage source. As a result, we have the following relationships as

$$i = i_{un} + uY_{cor} \tag{3-4}$$

and

$$\overline{iu^*} = Y_{cor}\overline{|u|^2} \tag{3-5}$$

where

$$u = -\frac{1}{Y_{21}} i_2, \tag{3-6}$$

$$i = i_1 - \frac{Y_{11}}{Y_{21}} i_2, \text{ and} \tag{3-7}$$

$$Y_{cor} = Y_{11} - Y_{21}\frac{\overline{i_1 i_2^*}}{\overline{|i_2|^2}} = G_{cor} + jB_{cor}. \tag{3-8}$$

The mean-square values for u and i are given by

$$\overline{|u|^2} = \frac{\overline{|i_2|^2}}{|Y_{21}|^2} = 4kT\Delta f R_u , \tag{3-9}$$

$$\overline{|i|^2} = \overline{|i_1|^2} + \overline{|i_2|^2}\left|\frac{Y_{11}}{Y_{22}}\right|^2 - 2\,\mathrm{Re}\{\overline{i_1 i_2^*}\cdot\frac{Y_{11}^*}{Y_{22}^*}\} = 4kT\Delta f G_i , \tag{3-10}$$

From equations (3-7) - (3-9), the four noise parameters can then be obtained by [70]

$$R_n = R_u , \tag{3-11}$$

$$G_{opt} = \sqrt{\frac{G_i}{R_n} - B_{cor}^2} , \tag{3-12}$$

$$B_{opt} = -B_{cor} , \tag{3-13}$$

and

$$NF_{\min} = 1 + 2R_n(G_{cor} + G_{opt}) . \tag{3-14}$$

3.2 SYSTEM SETUP

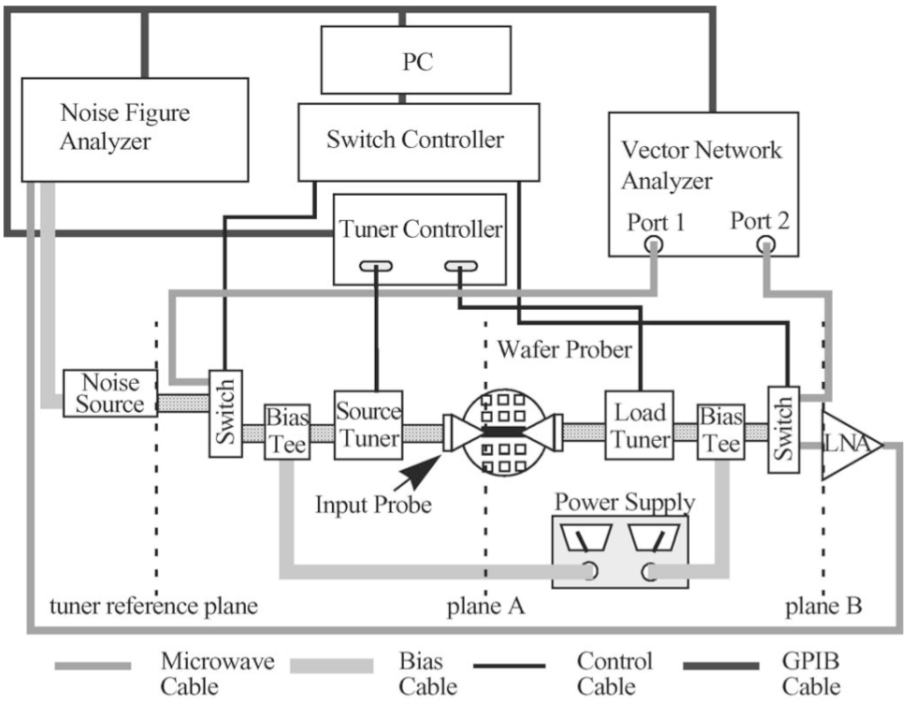


Figure 3.2: System configuration for microwave noise measurements [60].

Fig. 3.2 shows a noise measurement system which consists of a noise source, a vector network analyzer, a noise figure analyzer, microwave tuners, a low-noise amplifier (LNA), vector network analyzer, and other components like a PC, etc. The purpose of using the noise source is to generate two different temperatures, namely hot (T_h) and cold (T_c) temperatures during the noise measurements. The source tuner is to provide different source admittances for the receiver, and in order to realize a maximum power transfer, the load tuner is used to match the output of the device under test (DUT). By using the LNA, we can boost the weak noise signal to increase the accuracy of the measured noise power. It also helps to reduce the noise factor of the receiver to increase the noise factor

accuracy of the DUT by using LNA, especially at the time when Friis' equation is applied to remove receiver's noise contribution.

3.3 NOISE FACTOR MEASUREMENT

The microwave power meter is embedded in the noise figure analyzer as shown in Fig. 3.2. It is the major component responsible for noise power measurement. Generally, a microwave power meter consists of two components: a power meter for microwave power detection, and a mount (or impedance tuner) for impedance transformation [61],[62]. In the power meter, the core element could be a calorimeter, a bolometer, a thermoelectric meter, a diode sensor, or other types of detectors, as suggested in [63]. In a 50 Ω measurement system, the input impedance of the power meter is usually not 50 Ω (e.g., 200 Ω for the bolometer-based power meter [61]). In order to achieve the maximum power transfer, we need to transform the input impedance of the power meter from original mount to 50 Ω.

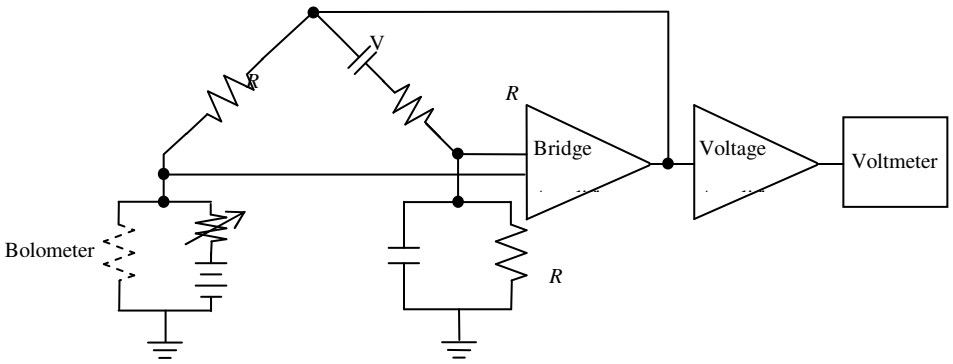


Figure 3.3: Basic circuit diagram for a bolometer-based power meter [61],[63].

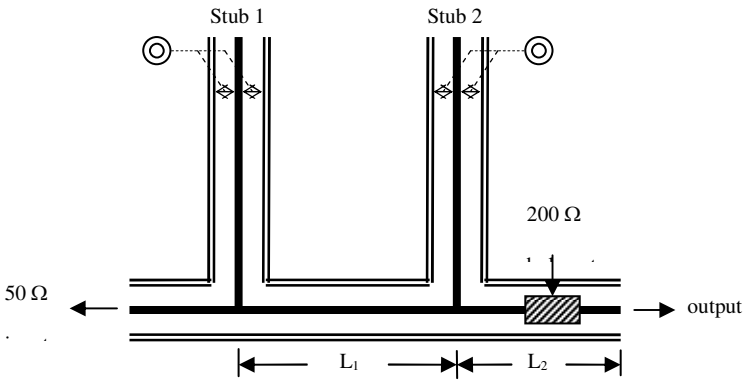


Figure 3.4: Schematic diagram for a double-stub impedance tuner [61],[63].

Fig. 3.3 shows the diagram of a bolometer-based power meter, and Fig. 3.4 shows a double-stub impedance tuner [61], [63]. In Fig. 3.3, most of the modern bolometric power meters are equipped with a self-balancing dc bridge. The bridge is to supply automatically controlled dc power P_{dc} to the bolometer so that its resistance is kept to be constant and the bridge is maintained in balance. For the circuit shown in Fig. 3.3, the absorbed dc power by the bolometer is given by

$$P_{dc} = \frac{V^2}{4R} \tag{3-15}$$

where V is the dc voltage across the bridge, and R is the resistance of both the bolometer and the three fixed resistors in the bridge.

Now we introduce the sources of error in microwave power measurement. When the microwave power is received, its energy heats the bolometer and a change in its resistance is followed. Ideally, the dc power supplied to the bridge is automatically changed by an amount which would be equal to the microwave power being received [63]. However, in practice, this change in the dc power is less than the microwave input

power. This is because some input power is absorbed by the mount during this progress, which causes the first source of error in the microwave power measurement.

The second source of error is from the uneven current distribution in the bolometer for the microwave and dc signals. Because of this uneven distribution, it results in a difference in the corresponding temperature distributions. This is known as the equivalence error of the bolometer. It is reported in [63] that this error is usually smaller than the one that is due to the mount loss. However, it may be either positive or negative which is different from the mount loss.

In the previous paragraphs, we talk about how the microwave noise power is measured, and the possible sources of errors associated with the measured noise power. In the following section we present how to characterize the noise performance of a noisy two-port. As stated before, the noise factor in equation (3-2) can be obtained using the so-called Y-factor method, in which the "hot" P_h (the noise source is turned on) and "cold" P_c (the noise source is turned off) noise powers are measured first. The Y-factor and the noise factor are then calculated by [71]

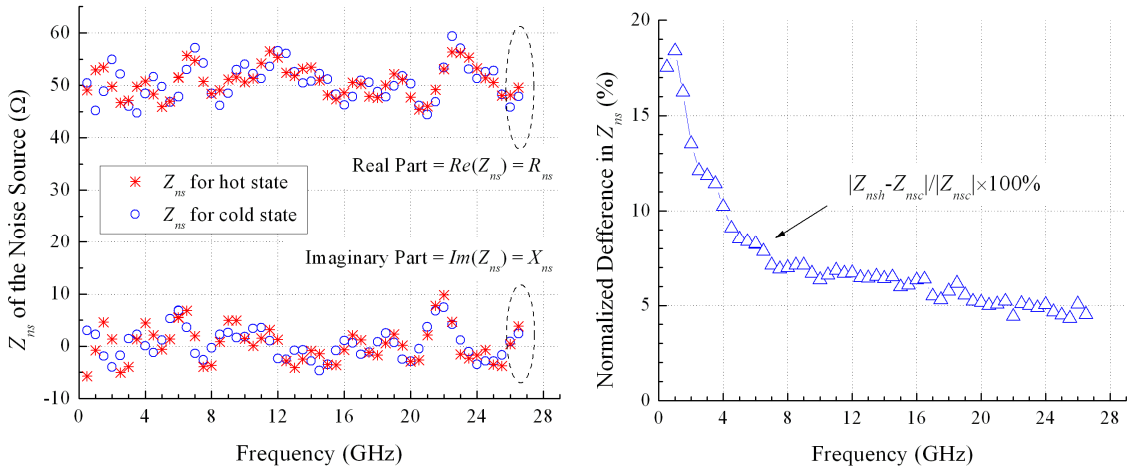
$$Y = \frac{P_h}{P_c} \tag{3-16}$$

and

$$F = \frac{ENR}{Y - 1} \tag{3-17}$$

where *ENR* is the excess noise ratio of the noise source calibrated by manufacturers at T_o. To calculate the noise factor by using (3-17), the major assumption that made is, the output impedances Z_{ns} of the noise source in its hot (Z_{nsh}) and cold (Z_{nsc}) states are the same. However, although Z_{nsh} and Z_{nsc} are close to each other practically, this assumption

is not hold in general. Therefore it introduces error in the calculated noise factor *NF*, which is pointed out by Kuhn in [72]. It is shown in Fig. 3.5 (a) that the measured output impedances (Z_{ns}) versus frequency characteristics of an Agilent 346C noise source in both hot and cold states from 0.5 GHz to 26.5 GHz. At most of the frequencies studied, Z_{ns} is about 50 Ω in both states. However, we found that there exist finite differences (△ Z_{ns}) between its Z_{nsh} and Z_{nsc}. As shown in Fig. 3.5 (b), the normalized impedance difference between Z_{nsh} and Z_{nsc}, which decreases from 18.4% to 5% when the operation frequency increases from 0.5 GHz to 26.5 GHz, as seen from experimental data.



(a) (b)

Figure 3.5: (a) Measured output impedances (Z_{ns}) vs. frequency characteristics of an Agilent 346C noise source in both hot (Z_{nsh}) and cold (Z_{nsc}) states, and (b) normalized impedance difference between Z_{nsh} and Z_{nsc} [60].

In this section, the importance of noise parameter accuracy is presented. Noise parameters are used to calibrate a noise measurement system [60], to obtain the noise sources of interest in devices [43],[74],[75], and to remove the parasitic effects of metal interconnection in a device-under-test [45],[73]. Noise parameters also helps in assisting with device noise modeling [37],[45],[47]. We would like to present one example in the

noise parameter de-embedding so as to demonstrate the importance of noise parameter accuracy in the following section.

It is well known that at high frequencies, parasitic effects from the probe pads and interconnections have great impacts on the high-frequency noise measurements [45],[73]. In order to remove the parasitic impact of the pads and interconnects from the extrinsic noise parameters of the DUT, noise and scattering parameter de-embedding are required, and the accuracy of the extrinsic noise parameters becomes a even more critical issue when transistor's size reaches to the sub-100nm regimes. Fig. 3.6 shows the extrinsic and intrinsic (or de-embedded) noise parameters for long- and short-channel transistors. In short-channel transistors (L = 0.18 μm or below), we can see from Fig. 3.6 that the variations/uncertainties in the de-embedded noise parameters become larger, comparing with long-channel devices. For instance, the variation in the de-embedded $NF_{\min}$ is more than 100% at around 6 GHz, and the de-embedded $|\Gamma_{opt}|$ becomes not physical (i.e., $|\Gamma_{opt}|$ = 1), which is caused by the computational errors in the extrinsic noise parameters.

There is one way to resolve this accuracy problem, which is to perform on-wafer calibration to the device input and output reference planes [45]. In this approach, during the on-wafer calibration, the impact of parastitic effects is removed. Therefore, we do not need to performance the parameter de-embedding, which is required in the first approach.

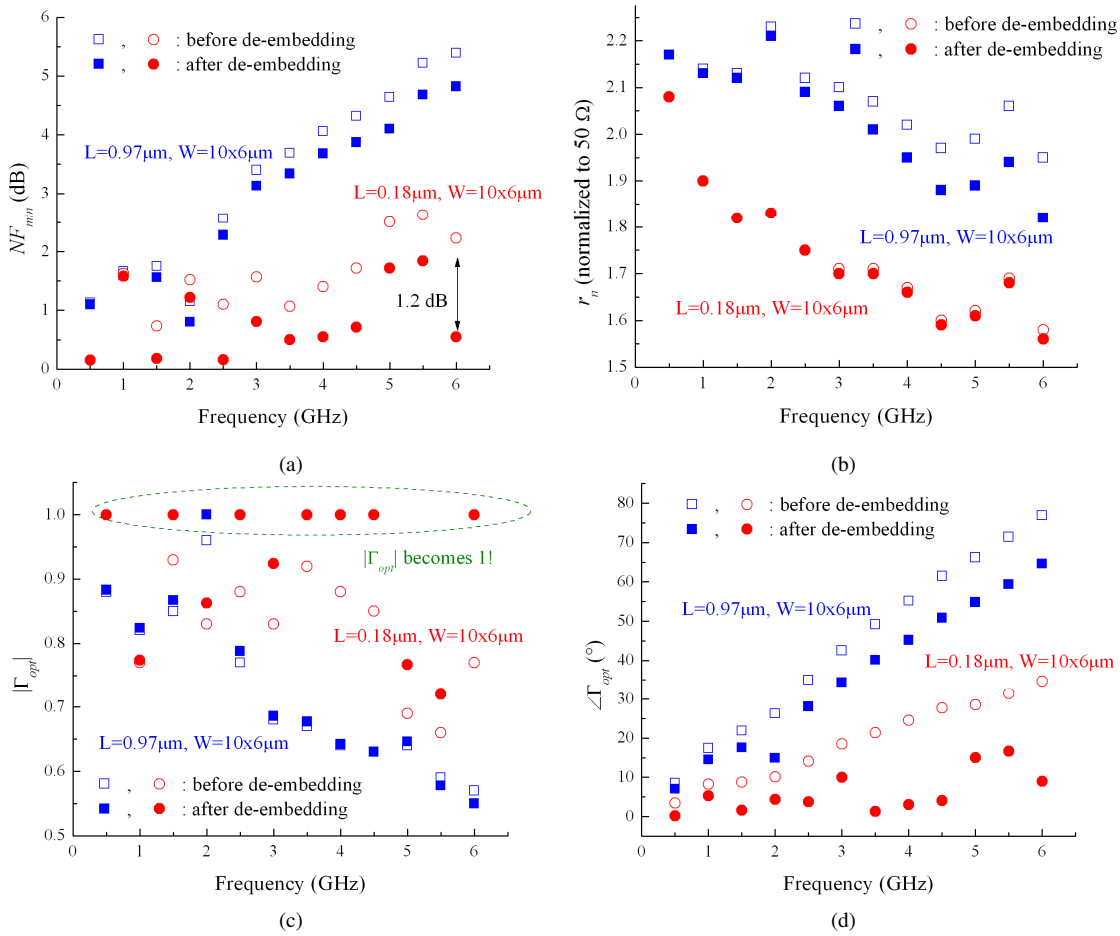


Figure 3.6: Extrinsic and intrinsic (or de-embedded) (a) NF_{min}, (b) r_n (R_n normalized to 50 Ω), (c) $|\Gamma_{opt}|$, and (d) $\angle\Gamma_{opt}$ for long- and short-channel transistors, respectively [80].

3.4 NOISE PARAMETER EXTRACTION

Due to the experimental errors and/or uncertainties in the measured noise powers, noise factors, source admittances, and noise parameter extraction has to take the errors into consideration. In this section, we provide the review of the most commonly used method (Lane's method), which is proposed to extract the noise parameters in equation (3-2) or (3-3) in the presence of experimental errors.

In order to obtain the noise parameters in equation (3-2), Lane re-arranged the noise factor equation and reformatted it as [76]

$$NF = A + G_s \cdot B + \frac{C + B_s^2 \cdot B + B_s \cdot D}{G_s} \tag{3-18}$$

where

$$NF_{\min} = A + \sqrt{4BC - D^2}\ , \tag{3-19}$$

$$R_n = B\ , \tag{3-20}$$

$$G_{\text{opt}} = \frac{\sqrt{4BC - D^2}}{2B}\ , \tag{3-21}$$

and

$$B_{\text{opt}} = -\frac{D}{2B}\ . \tag{3-22}$$

Analytical expressions for one of the noise parameters (equivalent noise resistance) can also be given by [44],[45]

$$R_g \approx \frac{RSHG \cdot wf \cdot nf}{3 \cdot lf \cdot nf^2}\text{, and} \tag{3-23}$$

$$R_n \approx R_g + R_g^2 \frac{S_{ig}}{4kT} + \frac{S_{id}}{4kTg_m^2} \tag{3-24}$$

where *RSHG* is the gate electrode sheet resistance, *wf* is the transistor width, *lf* is the transistor length, *nf* is the number of fingers, R_g is the effective gate resistance, S_{ig} is the PSD of the shot noise and induced gate noise, and S_{id} is the PSD of channel thermal noise. Because of the experimental errors in the measured noise factor F^m, the parameters A, B, C, and D used in (3-18) are obtained by applying a least-squares fit to *n*

(where $n \geq 4$) measured noise factors at n different source admittances. The fit starts with defining the error term ε, which can be written as

$$\varepsilon \equiv \frac{1}{2}\sum_{i=1}^{n} w_i \cdot [A + (G_{si} + \frac{B_{si}^2}{G_{si}}) \cdot B + \frac{1}{G_{si}} \cdot C + \frac{B_{si}}{G_{si}} \cdot D - F_i^m]^2 \tag{3-25}$$

where the index i represents the i^{th} data point, and w_i is the weighting factor for the i^{th} noise factor. However, in [76], it is not mentioned how to determine the value of w_i. This method also tells the fact that the minimum value of ε happens when the first order derivatives of ε with respect to A, B, C, and D are zeros. Consequently, parameter A, B, C, and D can be then obtained by solving

$$\frac{\partial \varepsilon}{\partial A} = 0, \ \frac{\partial \varepsilon}{\partial B} = 0, \ \frac{\partial \varepsilon}{\partial C} = 0, \text{ and } \frac{\partial \varepsilon}{\partial D} = 0 . \tag{3-26}$$

Fig. 3.7 shows the 12 measured (symbols) and calculated (line) noise factors based on Lane's least-squares fit for an n-type MOSFET with dimension size W/L = 80 μm/70 nm which is biased at V_{DS} = 1.0V and V_{GS} = 1.1V at 10 GHz [45]. In Lane's method, it assumes that the errors happen only in the noise factors, but not in the source admittances. We can see from Fig. 3.7 that not all of the noise factors are on the fitted line, which is due to the errors in the noise factors obtained by using the Y-factor method.

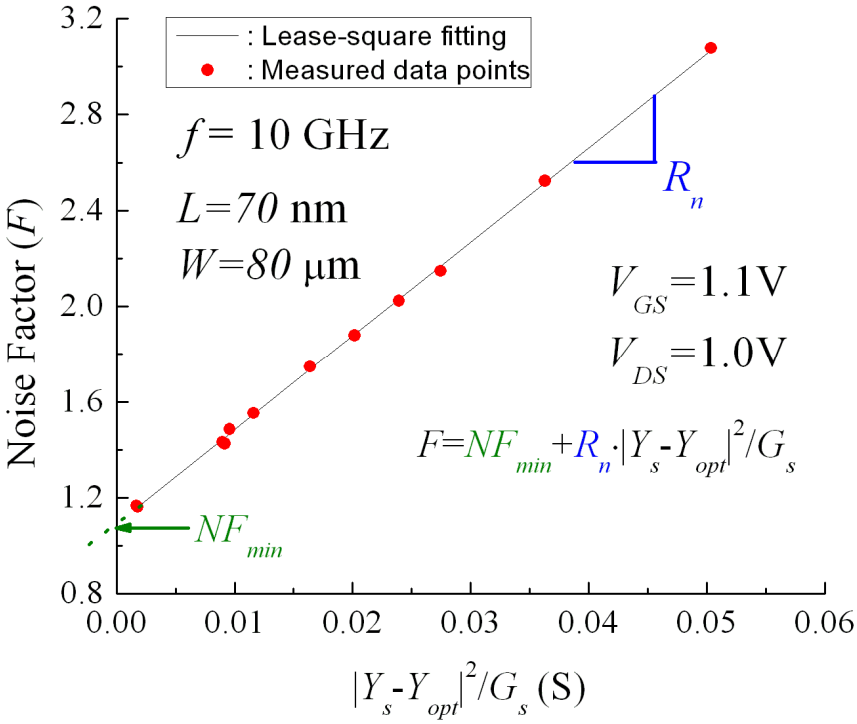


Figure 3.7: Measured (symbols) and fitted (line) noise factors vs. $|Y_s-Y_{opt}|2/G_s$ [45].

3.5 NOISE SOURCE EXTRACTION

The random fluctuations in the MOSFET channel producing in the channel noise will be coupled to the gate terminal through the oxide capacitance when transistors work in GHz. This coupling generates the induced gate noise. The induced gate noise is always correlated with channel noise, and this correlation will cause difficulties in the extraction of channel noise. Some noise models, such as [32], have been presented to solve this issue. However, the models presented in such papers could not be verified directly with the noise source obtained from the RF noise measurements. Therefore, accurate extraction of the induced gate noise from RF measurements is important for MOSFETs high frequency noise modeling.

The following section presents the extraction procedure for induced gate noise ($\overline{i_g^2}$), channel noise ($\overline{i_d^2}$) and their cross-correlation ($\overline{i_g i_d^*}$) directly from the s-parameter. RF noise parameter measurements is also presented. The extracted noise currents are fed back to the equivalent noise model to the calculation of the four noise parameters - NF_{min}, R_n, R_{opt} and X_{opt} for comparing them to the measured data for the verification of the extracted noise sources.

In this section, we present a general and systematic procedure to extract the power spectral densities of the induced gate noise ($\overline{i_g^2}$) and its correlation noise ($\overline{i_g i_d^*}$) with channel noise. The induced gate noise and its correlation noise are frequency dependant noises. As a result, the extraction at each measured frequency should be done.

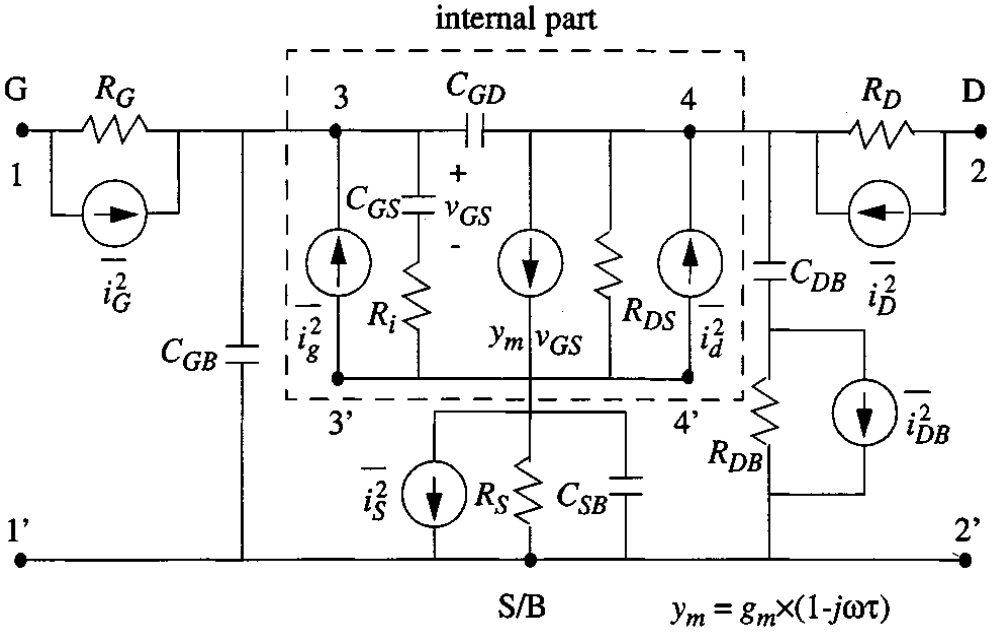


Figure 3.8: RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications [78].

Fig. 3.8 shows the noise model of an intrinsic MOSFET. In this figure, the internal part is defined as the part that contains C_{GS}, C_{GD}, R_i, R_{DS}, $\overline{i_g^2}$ and $\overline{i_d^2}$. The external part, on the other hand, consists of the all the other components such as C_{GB}, C_{DB}, R_s, C_{SB}, R_S, $\overline{i_G^2}$ and $\overline{i_D^2}$. As shown in this figure, ports 1-1' and 2-2' do not share a common reference with ports 3-3' and 4-4'. The induced gate noise, channel noise, and their correlation in MOSFETs can be then extracted by using the following 15-step procedure [77][78].

1. Measure the scattering parameters S_{DUT}, S_{OPEN}, S_{THRU1} and S_{THRU2} of the device-under-test (DUT), OPEN, THRU1, and THRU2 dummy structures, respectively.

2. Measure the noise parameters $NF_{min,DUT}$, $Y_{opt,DUT}$ and $R_{n,DUT}$ and of the DUT.

3. Perform a parameter de-embedding to get the intrinsic scattering (Y_{dev}) and noise parameters ($NF_{min,dev}$, $Y_{opt,dev}$ and $R_{n,dev}$) [79].

4. Perform a parameter extraction based on Y_{dev} and other measured data to get all element values such as C_{GS}, C_{GD}, in the RF noise model.

5. Calculate the correlation matrix C_{Adev} of the transistor based on the intrinsic noise parameters, where the correlation matrix is given by

$$C_{Adev} = 2kT_o \begin{bmatrix} R_{n,dev} & \frac{NF_{\min,dev}-1}{2} - R_{n,dev}(Y_{opt,dev})^* \\ \frac{NF_{\min,dev}-1}{2} - R_{n,dev}(Y_{opt,dev}) & R_{n,dev}\left|Y_{opt,dev}\right|^2 \end{bmatrix} \quad (3\text{-}27)$$

where k is Boltzmann's constant, T_o is the standard reference temperature (290K), and the asterisk denotes the complex conjugate.

6. Calculate the four port admittance matrix Y_{extr} of the extrinsic part in the RF transistor model by excluding C_{GS}, C_{GD}, R_i, R_{DS}, and R_i. Y_{extr} which define the intrinsic part. Y_{extr} is given by

$$Y_{extr} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \tag{3-28}$$

where the sub-matrixes Y_{ee}, Y_{ei}, Y_{ie}, Y_{ii} are 2×2 matrixes.

7. Calculate the two-port admittance matrix Y_{intr} of the intrinsic part in the RF transistor model.

8. Calculate the matrix D as follows

$$D = -Y_{ei}(Y_{ii} + Y_{\text{intr}})^{-1}. \tag{3-29}$$

9. Convert the noise correlation matrix C_{Adev} to its admittance form C_{Ydev} by using

$$C_{Ydev} = T_Y C_{Adev} T_Y^{\dagger} \tag{3-30}$$

where the $\dagger$ in the $T_Y^{\dagger}$ denotes the Hermitian conjugation (transpose and complex conjugate), and the transformation matrix T_Y is given by

$$T_Y = \begin{bmatrix} -Y_{11,dev} & 1 \\ -Y_{21,dev} & 0 \end{bmatrix}. \tag{3-31}$$

10. Calculate the admittance noise correlation matrix C_{Yextr} of the extrinsic part by

$$C_{Yextr} = KT(Y_{extr} + Y_{extr}^{\dagger}) \tag{3-32}$$

or

$$C_{Yextr} = 2KT\Re(Y_{extr}) \tag{3-33}$$

where T is the device temperature, $\Re()$ denotes for the real part of the matrix elements and, partition C_{Yextr} as

$$C_{Yextr} = \begin{bmatrix} C_{ee} & C_{ei} \\ C_{ie} & C_{ii} \end{bmatrix} \tag{3-34}$$

where the sub-matrixes C_{ee}, C_{ei}, C_{ie}, C_{ii} are 2×2 matrixes.

11. Calculate the admittance correlation matrix C_{Yintr} of the intrinsic part in the RF transistor model from

$$C_{Y\text{intr}} = D_i(C_{Ydev} - C_{ee})D_i^{\dagger} - C_{ie}D_i^{\dagger} - D_iC_{ei} - C_{ii} \tag{3-35}$$

where $D_i = D^{-1}$.

12. Convert Y_{Yintr} to its chain representation A_{intr} using the conversion formula which is given by

$$A_{\text{intr}} = \frac{-1}{Y_{21,\text{intr}}} \begin{bmatrix} Y_{22,\text{intr}} & 1 \\ Y_{11,\text{intr}}Y_{22,\text{intr}} - Y_{12,\text{intr}}Y_{21,\text{intr}} & Y_{11,\text{intr}} \end{bmatrix}. \tag{3-36}$$

13. Convert C_{Yintr} to its chain matrix form C_{Aintr} by using

$$C_{A\text{intr}} = T_A C_{Y\text{intr}} T_A^{\dagger} \tag{3-37}$$

where T_A is given by

$$T_A = \begin{bmatrix} 0 & A_{12,\text{intr}} \\ 1 & A_{22,\text{intr}} \end{bmatrix}. \tag{3-38}$$

14. Calculate the noise parameters ($NF_{min,dev}$, $Y_{opt,dev}$ and $R_{n,dev}$) of the intrinsic part in the RF transistor model from the noise correlation matrix C_{Aintr} by using

$$NF_{\min} = 1 + \frac{1}{kT_o}(\Re(C_{12A,\text{intr}}) + \sqrt{C_{11A,\text{intr}}C_{22A,\text{intr}} - (\Im(C_{12A,\text{intr}}))^2}), \tag{3-39}$$

$$Y_{opt} = \frac{\sqrt{C_{11A,\text{intr}}C_{22A,\text{intr}} - \Im((C_{12A,\text{intr}}))^2} + j\Im(C_{12A,\text{intr}})}{C_{11A,\text{intr}}}, \text{ and} \tag{3-40}$$

$$R_{\mathrm{n}} = \frac{C_{11A,\mathrm{intr}}}{2kT_o} \tag{3-41}$$

where $\Im()$ stands for the imaginary part of elements and j is the imaginary unit.

15. Calculate the power spectral density of the induced gate noise ($\overline{i_g^2}$), channel noise ($\overline{i_d^2}$) and their cross-correlation ($\overline{i_g i_d^*}$) from

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kT_o R_n \left|Y_{21,\mathrm{intr}}\right|^2, \tag{3-42}$$

$$\frac{\overline{|i_g|^2}}{\Delta f} = 4kT_o R_n \left\{ \left|Y_{opt}\right|^2 - \left|Y_{11,\mathrm{intr}}\right|^2 + 2\Re[(Y_{11,\mathrm{intr}} - Y_{cor})Y_{11,\mathrm{intr}}^*] \right\}, \text{ and} \tag{3-43}$$

$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT_o R_n (Y_{11,\mathrm{intr}} - Y_{cor})Y_{21,\mathrm{intr}}^* \tag{3-44}$$

where Y_{cor} is given by

$$Y_{cor} = \frac{NF_{\min} - 1}{2R_n} - Y_{opt}. \tag{3-45}$$

In the extraction procedure, accurate element values used in the RF noise model are crucial to obtain the noise source power spectral density. The Y-parameters of the small-signal equivalent circuit of Fig. 3.8 is shown as

$$y_{11} \approx \omega^2 (R_g C_{gg}^2) + j\omega C_{gg}, \tag{3-46}$$

$$y_{12} \approx -\omega^2 R_g C_{gg} C_{gd} - j\omega C_{gd}, \tag{3-47}$$

$$y_{21} \approx g_m - \omega^2 R_g C_{gg}(C_m + C_{gd}) - j\omega(C_m + C_{gd} + g_m R_g C_{gg}), \text{ and} \tag{3-48}$$

$$y_{22} \approx g_{ds} + \omega^2 R_g C_{gg}(C_{bd} + C_{gd}) + j\omega(C_{bd} + C_{gd} - g_{ds} R_g C_{gg}). \tag{3-49}$$

Here we assume that $\omega R_g C_{gg} << 1$. By using the simplified expressions from (3-46) to (3-49), element values in the equivalent circuit can be extracted.

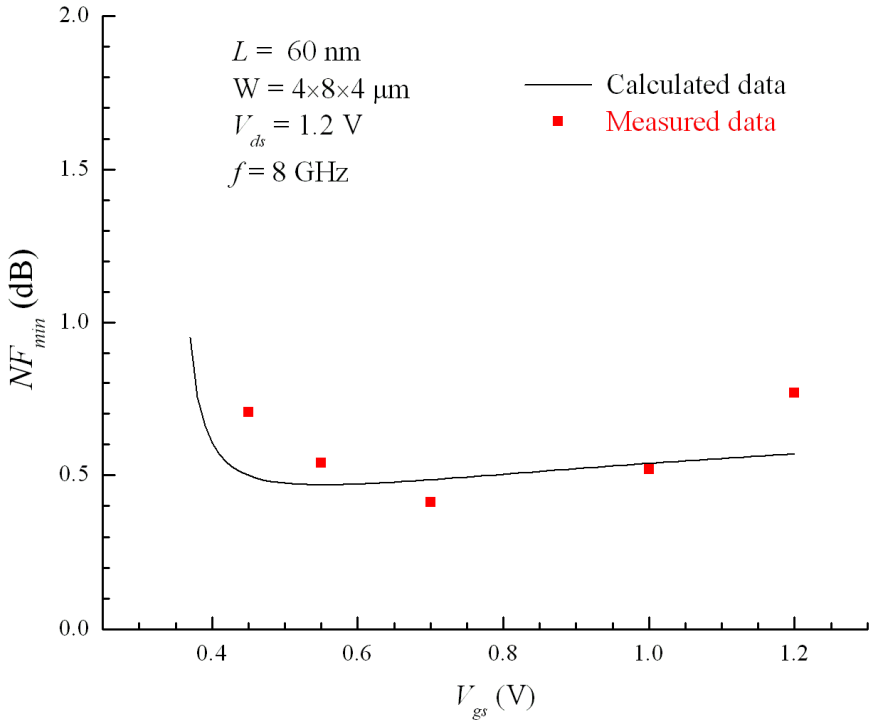
Chapter 4:

IMPACT OF SCALING ON CHANNEL THERMAL NOISE

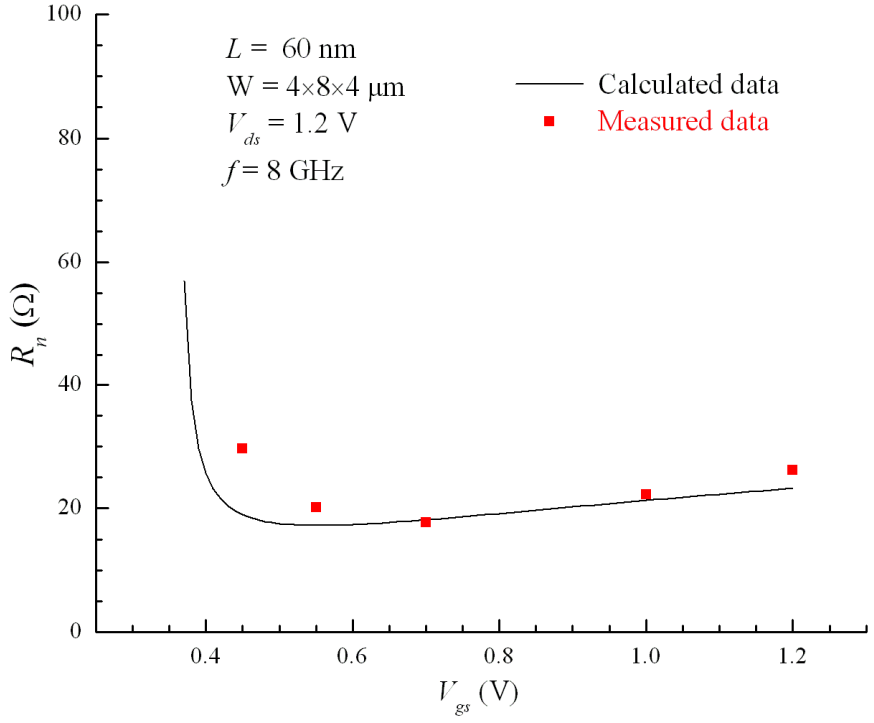
4.1 NOISE MODEL CALIBRATION AND VERIFICATION

This chapter started with the calibration and verification of the noise model. The transconductance at each bias condition is calculated based on the dc model. Same parameter values are then applied to the physics-based noise models to calculate the channel thermal noise. Analytical expressions for noise parameters are used to calculate the noise parameters and demonstrate the noise trend down to 17 nm technology node.

The model parameters described in Chapter 2 are calibrated using experimental results from devices in 60 nm technology node. Fig. 4.1 shows the results for the minimum noise figure (NF_{min} in dB) and the equivalent noise resistance (R_n in Ω) for devices with W/L = 4×8×4/60 (μm/nm) measured at f = 8 GHz as a function of V_{gs} at V_{ds} = 1.2 V. In this figure, lines represent the calculated data and symbols are for the measured data. Fig. 4.1 verifies and confirms the equitability of the dc and noise models proposed in this thesis.



(a)



(b)

Figure 4.1: Calculated (lines) and measured (symbols) (a) NF_{min} and (b) R_n for an n-type MOSFET with L = 60 nm and W = 4×8×4 µm biased at V_{ds} = 1.2V.

Although our model at high V_{gs} region does not match that well with the data, this is mainly due to not including the parasitic effect R_s and R_d. In real devices, there will be degradation in the transconductance at high V_{gs} region due to R_s and R_d. In our simple model, the parasitic effect is not included, but it can still capture the trend and level of noise performance. Here we just want to provide a simple compact model that can capture the general trend such that we can learn the noise insight when transistor scales down.

4.2 NOISE BEHAVIOR IN FUTURE DEVICES

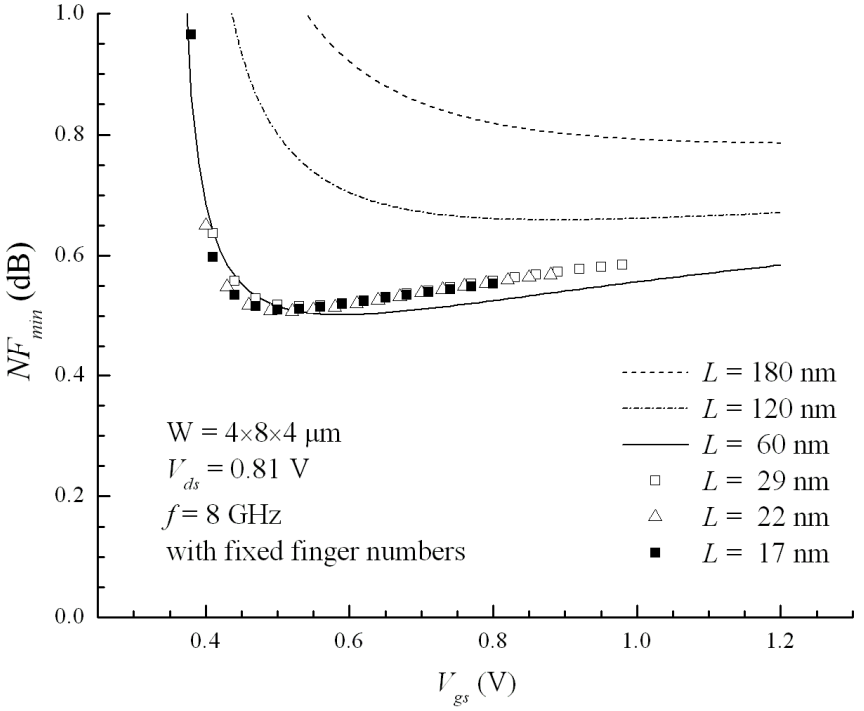
To predict the noise performance of future devices with channel lengths smaller than 60 nm, we used the process parameters for the extended planar bulk devices in the RF and Analog Mixed-Signal CMOS Technology Requirements, ITRS Roadmap 2009 edition [49]. The devices used in the calculation have their channel width $W = 4\times8\times4$ μm and channel lengths L = 180 nm, 120 nm, 60 nm, 29 nm, 22 nm, and 17 nm, respectively. Table 4.1 shows the calculated threshold voltage (V_{th}), the extracted λ to model CLM effect and to match the targeted drive current $I_{d,sat}$ in ITRS roadmap [49] (values in the bracket), and the resulting saturated current $I_{d,sat}$ to make sure that the process parameters and the extracted λ are reasonable for the performance of future devices. We set up doping concentration for devices with different channel length based on the ITRS roadmap. Based on our dc model, the doping concentration results in a relatively stable threshold voltage.

Table 4.1 Projected MOSFET Performance Analog Mixed-Signal CMOS Technology to Calibrate λ

Year	Channel length (nm)	Projected Device Performance			
		Doping (cm^{-3})	λ	V_{th} (V)	$I_{d,sat}$ (μA/μm)
2009	29	$3.7 \cdot 10^{18}$	6.0	0.3702	1240 (1210)
2010	27	$4.0 \cdot 10^{18}$	5.8	0.3700	1242 (1200)
2011	24	$4.5 \cdot 10^{18}$	5.5	0.3695	1245 (1190)
2012	22	$5.0 \cdot 10^{18}$	3.7	0.3696	1341 (1300)
2013	20	$5.7 \cdot 10^{18}$	2.5	0.3697	1451 (1450)
2014	18	$6.6 \cdot 10^{18}$	2.0	0.3698	1541 (1580)
2015	17	$7.5 \cdot 10^{18}$	1.2	0.3699	1682 (1680)

Fig. 4.2 shows the calculated noise parameters for the devices with the process parameters in 60 nm technology node (lines) and in future technology nodes (symbols) based on the ITRS roadmap 2009 and Table 4.1 without the CLM effect. To be consistent between technology nodes, we plot the noise parameters as a function of V_{gs} biased at the same drain to source voltage V_{ds} = 0.81 V for all different lengths, which is the maximum power supply voltage for the 17 nm technology node in ITRS roadmap.

It is shown in Fig. 4.2 that for devices with the same 60 nm process parameters, the NF_{min} of the shorter channel devices drops as we expected, but R_n becomes higher in high V_{gs} regions when the device length reduces. This is because of the faster drop in g_m in the high V_{gs} regions in short channel devices as seen in Fig. 4.3.



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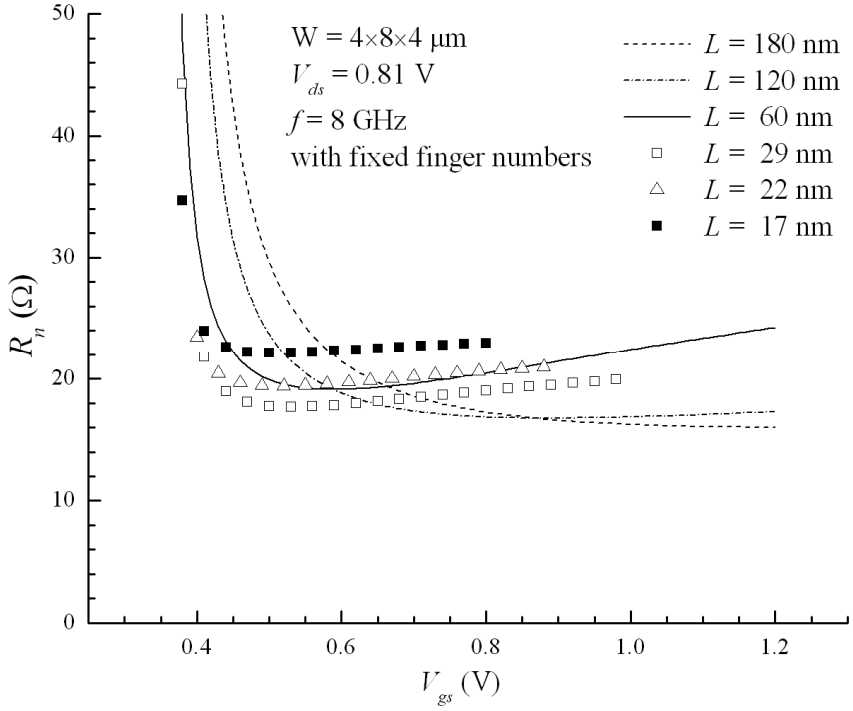


(b)

Figure 4.2: Calculated (a) NF_{min} and (b) R_n for n-type MOSFETs with process parameters in 60 nm technology node (lines) and in future technology nodes (symbols) without the CLM effect.

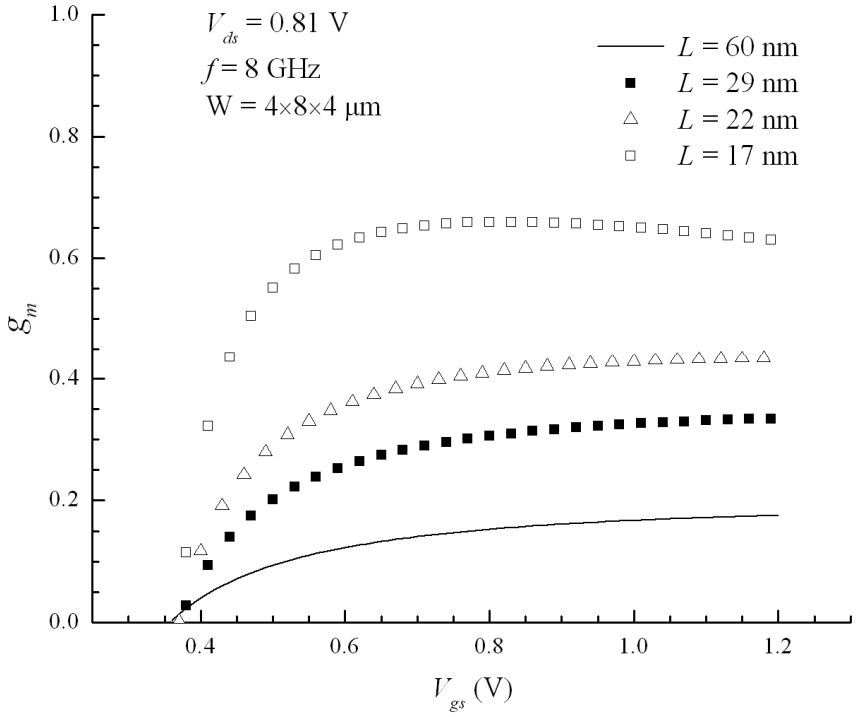
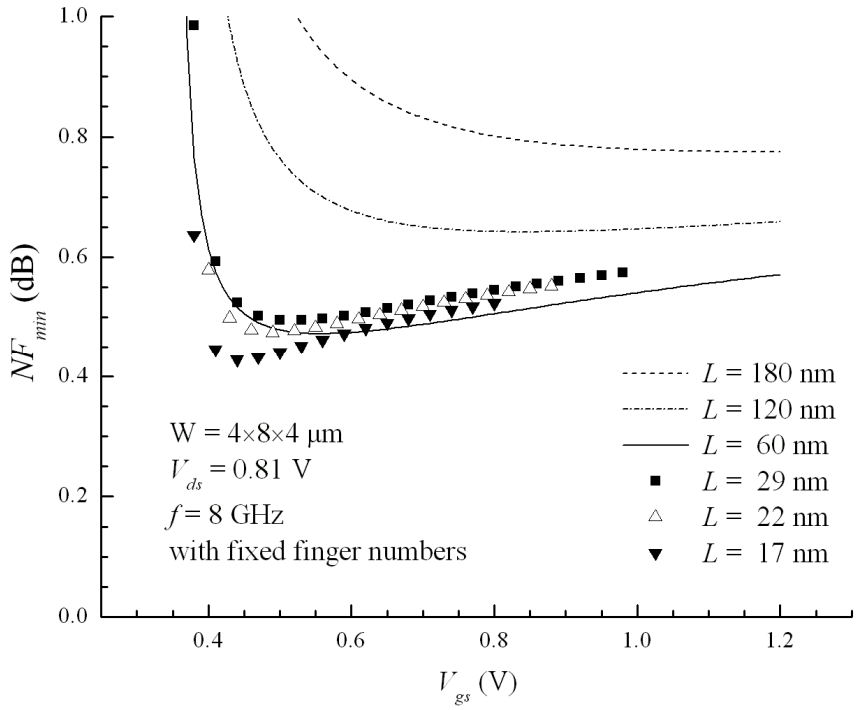
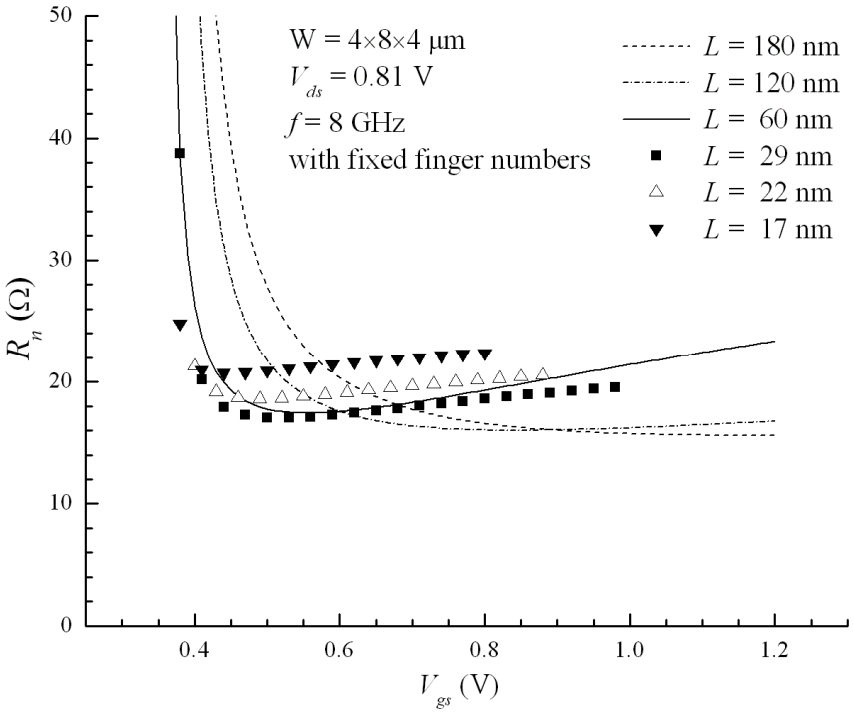


Figure 4.3: Simulated g_m for n-type MOSFETs with process parameters in 60 nm technology node (lines) and in future technology nodes (symbols) including the CLM effect.

In Fig. 4.3, we found that the g_m for n-type MOSFETs will decreases for shorter channel MOSFETs at the high V_{gs} region. On the other hand, for future devices with different process parameters, R_n actually becomes higher after 29 nm technology node. According to our model, the increased noise parameters starting from 29 nm technology node are mainly due to the enhanced gate resistance. As technology develops with channel length reduced, the increased gate resistance becomes comparable with the channel thermal noise in the R_n equation and thus cannot be neglected. It prevents the improvement in the noise behavior of future technology nodes. More device fingers are required to reduce the effective gate resistance and continuously enjoy the benefits of advanced technology nodes.



(a)



(b)

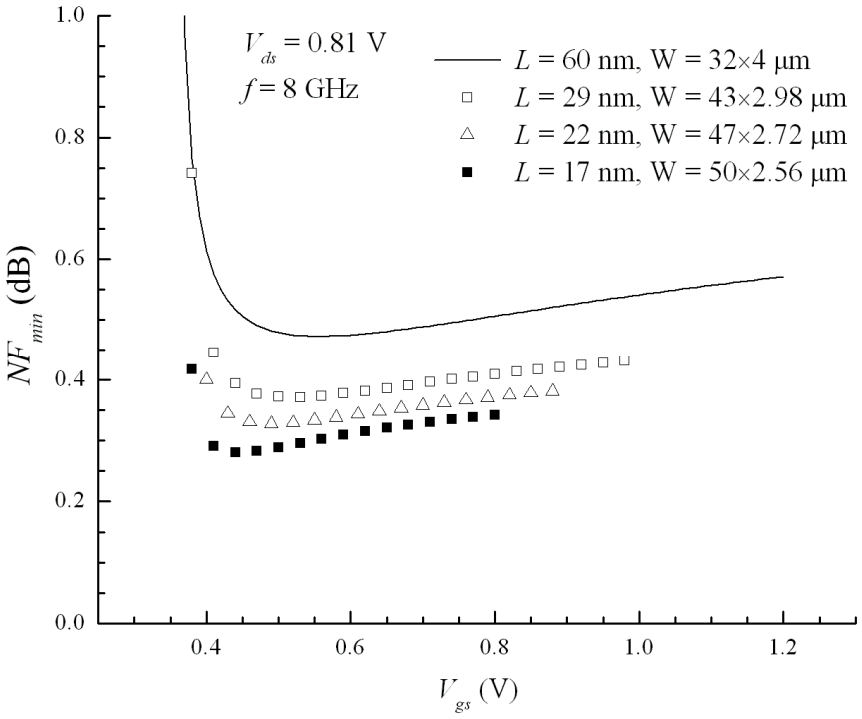
Figure 4.4: Calculated (a) NF_{min} and (b) R_n for n-type MOSFETs with process parameters in 60 nm technology node (lines) and in future technology nodes (symbols) including the CLM effect.

Table 4.2 Updated Number of Fingers and Channel Width of MOSFETs

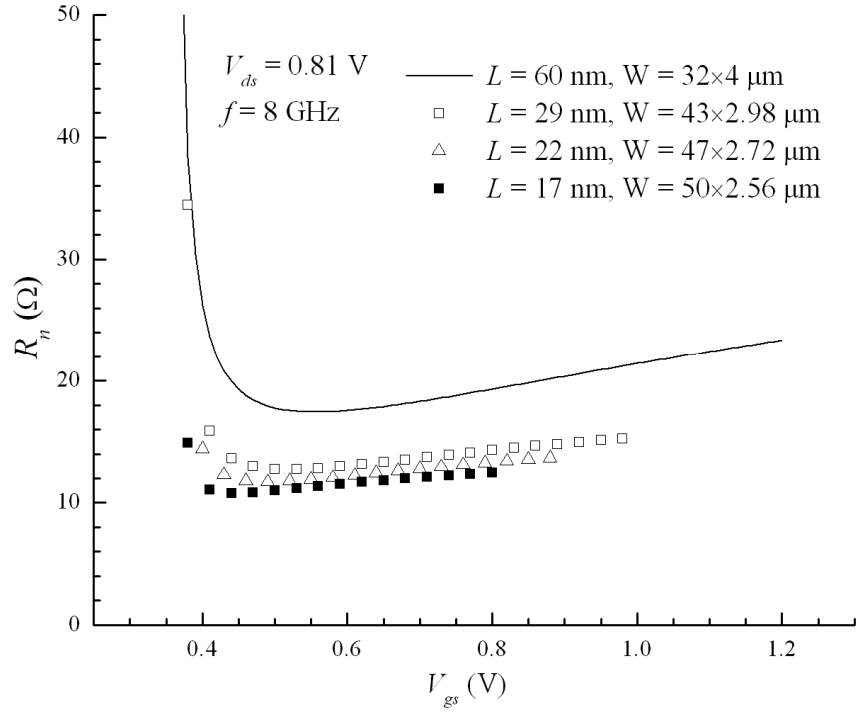
Year	Channel length (nm)	Number of fingers	Width (μm)	Minimum R_n (Ω)
2009	29	43	2.98	12.73
2010	27	44	2.91	12.55
2011	24	46	2.78	12.41
2012	22	47	2.72	11.74
2013	20	48	2.67	11.31
2014	18	49	2.61	11.18
2015	17	50	2.56	10.80

As we already know in [16], the CLM effect results in the enhanced S_{id} which cannot be neglected when the channel length is shorter than 0.18 μm. Fig. 4.4 shows the NF_{min} and R_n with the CLM effect using the λ values in Table 4.1 for n-type MOSFETs with the process parameters in 60 nm technology node (lines) and in future technology nodes (symbols).

By comparing the results in Fig. 4.2 and Fig. 4.4, we found that the noise parameters actually improve slightly. Although the CLM effect elevates the PSD of the channel thermal noise, the g_m of the transistor is enhanced a bit more than the noise. In order to keep the benefits of the noise improvement due to the enhanced g_m in future technology nodes, as indicated in Figs. 4.2 and 4.4, we need to reduce the gate resistance by increasing the number of fingers. Table 4.2 shows the finger number required for each



(a)



(b)

Figure 4.5: Calculated (a) NF_{min} and (b) R_n for n-type MOSFETs with process parameters in 60 nm technology node (lines) and in future technology nodes (symbols) with different finger numbers.

technology node and each finger width in order to keep the smallest R_n reduced from one technology to another.

Based on the finger numbers in Table 4.2, Fig. 4.5 shows the simulated NF_{min} and R_n for each technology node. After adjusting the number of fingers, NF_{min} and R_n retain their decreasing trend when technology enhances.

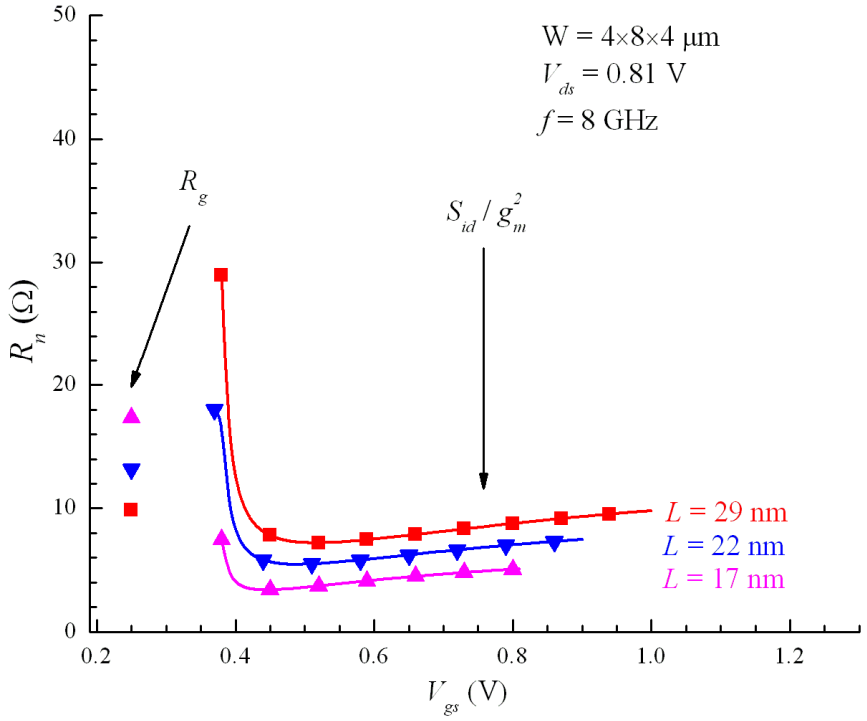


Figure 4.6: Decomposed R_n scaling trend – gate resistance R_g and S_{id}/g_m^2.

By decomposing the equivalent noise resistance in equation (3-24), we see there are two major terms in R_n – the gate resistance R_g and the ratio between the intrinsic thermal noise S_{id} and the g_m. From the following illustration, it is shown in Fig. 4.6 that the S_{id}/g_m^2 is decreasing, which is favourable. It means we can still enjoy benefit of technology enhancement. On the other hand, because of the increment of the gate

resistance, we need to increase the number of fingers in order to reduce the gate resistance when utilizing short channel devices.

4.3 SCALING IMPACT ON NOISE BEHAVIOR

Until now, we defined the equivalent noise resistance so as to catch the noise behavior of devices. Among all the different devices with different dimension sizes, it is still hard for people to compare the performance for different transistors. By observing the analytical expression of equivalent thermal noise resistance, a new parameter called "equivalent noise sheet resistance" is defined for the first time by excluding the geometry information of devices. The analytical expression for this new parameter is defined by

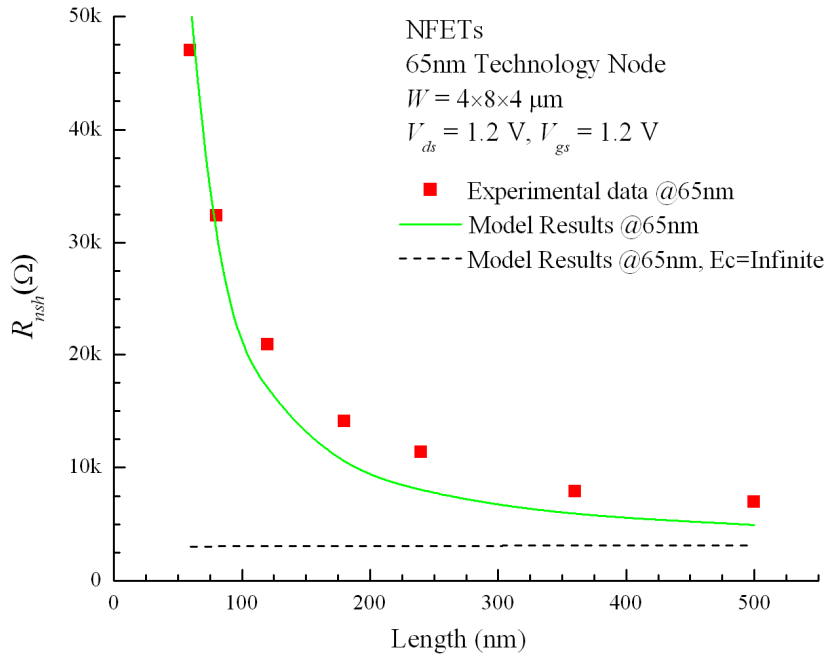
$$R_{nsh} = \frac{S_{id}}{g_m^2} \cdot (\frac{W}{L}) . \tag{4-1}$$

By multiplying the aspect ratio of the device, this "equivalent noise sheet resistance" does not depend on the device geometry. It is a process parameter which is only related to technology parameters, such as mobility, critical field along channel, and silicon dioxide thickness. By using this term, people can study the noise performance of devices from different technologies, and with different dimensions. This term can not only provide IC designers to evaluate the technology, but also help process engineers when they improve the process conditions.

Fig. 4.7 shows the experimental data at 65nm technology nodes along with the model predictions. As the channel length reduces, the equivalent noise sheet resistance increases, and this trend can be captured by our model. By analyzing the data and adding another curve with infinite critical field, we found this increment in R_{nsh} is due to the

infinite E_c. In long channel devices, the effective carrier mobility is about constant. For short channel devices, the effective mobility is degraded due to the transverse field [59]. Because of the equivalent noise sheet resistance is related to technology mobility, the impact of the critical field elevates the level of noise sheet resistance. When setting E_c to be infinite, we see that the equivalent noise sheet resistance reduces as device channel length reduces.

In Fig. 4.8 and Fig. 4.9, equivalent noise sheet resistances, R_{nsh}, are plotted as a function of gate lengths at different critical fields and mobilities for NFETs and PFETs. We found that by increasing the mobility alone, the equivalent noise sheet resistance is enhanced in the short-channel devices, but reduced in longer-channel devices. This is because the critical field effect changes the CLM enhanced noise power spectral density and E_c degraded noise power spectral density separately in the total channel thermal PSD. On the other hand, for devices with the same mobility, once E_c is increased, the equivalent noise sheet resistance is reduced dramatically for both NFETs and PFETs. This confirms the idea in Fig 4.7 that the lateral field effect is the key factor which stops the R_{nsh} improvement in short-channel devices. In order to improve noise performance, a device with channel engineering to have a higher E_c should be selected. It also shows that by increasing the intrinsic mobility and critical field together will improve the noise performance in future technology nodes. Moreover, the equivalent noise sheet resistance is approximately proportional to the oxide thickness. Therefore, reducing the t_{ox} will be another efficient way to reduce the equivalent noise sheet resistance and enhance the noise performance.



(a)

Figure 4.7: Measured (symbols) and calculated (lines) R_{nsh} for NFETs.

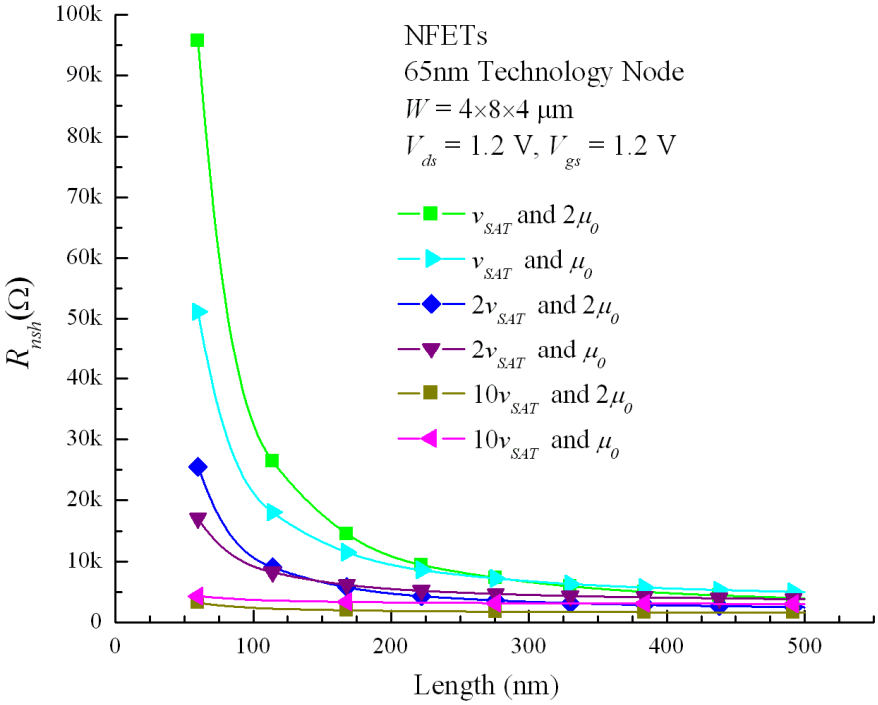
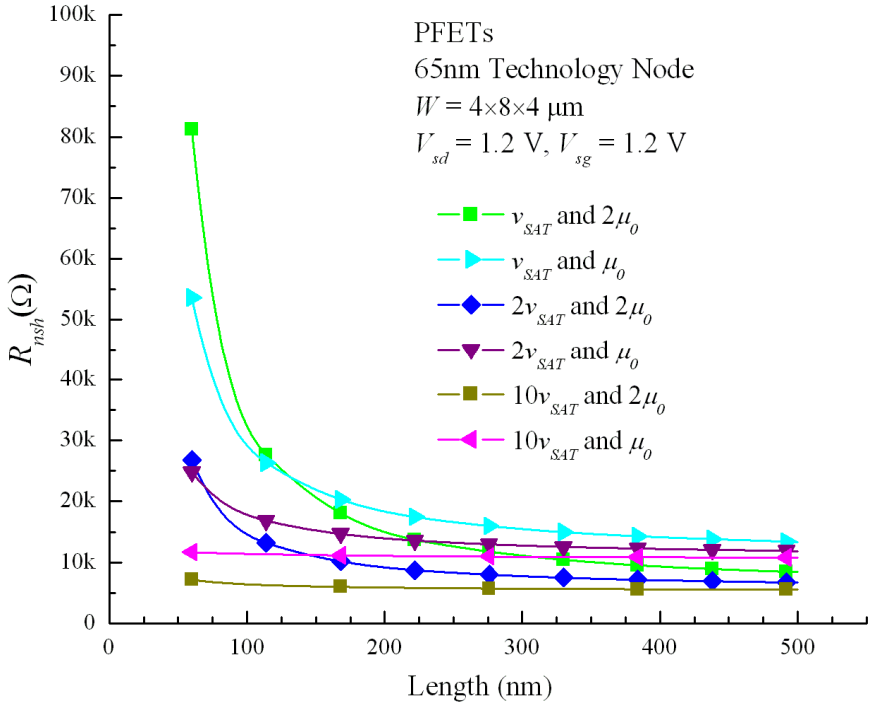


Figure 4.8: Simulated equivalent noise sheet resistance R_{nsh} as a function of gate lengths at different E_c and mobilities for NFETs.



(b)

Figure 4.9: Simulated equivalent noise sheet resistance R_{nsh} as a function of gate lengths at different E_c and mobilities for PFETs.

Chapter 5:

CONCLUSIONS AND RECOMMENDATIONS

5.1 CONCLUSIONS

Device noise, is one of the key factors which limit the technology advancement. In order to predict the performances for future devices, three main topics are accomplished in this thesis. First, the noise model for deep sub-100nm MOSFETs is proposed and developed, which includes the non-ideal effects in short-channel MOSFETs. Enhanced channel thermal noise due to non-ideal effects is considered and modeled, by including short-channel effect, channel length modulation effect, velocity saturation effect, mobility variation effect and hot carrier effect. By taking them into consideration, a good fitting between the model simulated result and the experimental data is presented in this thesis.

For noise behavior projection, the proposed model is first implemented to simulate devices' noise performance at 60nm. By comparing with experimental data, the model parameters such as λ in channel length modulation effect is fitted to capture the noise level of selected device, which confirms the equitability of proposed model. To predict noise performance of future devices with channel lengths shorter than 60nm, process parameters for extended planar bulk devices in RF and Analog Mixed-Signal CMOS Technology Requirements in ITRS Roadmap 2009 are used as model parameters. It is found that the noise parameters such as the minimum noise figure and the equivalent noise resistance will actually increase because of the increment in the gate resistance. The intrinsic part in equivalent noise resistance, which is the ratio between the thermal noise

S_{id} and the g_m, is still decreasing. This means the signal power increases faster than the device noise. However, due to the increment of the gate resistance, increasing number of fingers of the transistor is necessary to keep the improvement of noise parameters.

The newly introduced parameter, namely equivalent noise sheet resistance measures the scaling impact on noise in MOS transistors. By processing the experimental data in 65nm technology nodes, this equivalent noise sheet resistance increases. It means that the process parameters of devices degrade the noise performance. This increment trend is due to the critical longitudinal field along the channel. In order to reduce this equivalent noise sheet resistance, process engineers need to concern about how to enhance the critical field, or reduce the oxide thickness while still maintaining the leakage current.

5.2 RECOMMENDATIONS

Based on the research results obtained from this thesis, the following are the recommendations for future research.

First, since our model is a simple dc compact model, it misses the parasitic effect on the noise prediction. Therefore, parasitic effect including R_s and R_d, should be considered.

Second, since devices are going into nano-meter scale, the quantum effects will become significant for future devices and cannot be neglected. People should be concerned about how to include these effects into the device models.

Finally, accurate noise measurement and characterization become more critical in future devices. People should pay more attention to the noise data extraction techniques

and the measurement accuracy, in a way such that the noise characterization for nano-meter MOSFETs can be accurately modeled in future research.

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